A NEW DEEP REACTIVE ION ETCHING PROCESS BY DUAL SIDEWALL PROTECTION LAYER

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ABSTRACT

This paper describes a new deep reactive ion etching (D-RIE) process which drastically improves the aspect ratio of the etched trench. The conventional D-RIE process obtains the high aspect ratio trench etching with the protection layer, such as a polymeric layer. The etching anisotropy is limited in this process because this protection layer prevents not only lateral etching, but also vertical etching. In contrast, the new process we developed intensively prevents lateral etching with a dual protection layer consists of a polymeric layer and a SiO_2 layer on the trench sidewall. Therefore the etching anisotropy and the aspect ratio can be improved. Furthermore, this process can only be performed by switching the introducing gas into the etching chamber.

INTRODUCTION

The D-RIE process is a dry etching technique fabricating a high aspect ratio trench prescribed by a mask pattern on the silicon wafer. This is one of the most important techniques in the MEMS field. For example, a comb-structured resonator driven by electrostatic force can be fabricated by D-RIE. In this case, the capacitance between the comb-structured electrodes is proportional to the aspect ratio of the trench between the electrodes. Therefore the device performance can be improved if the aspect ratio becomes higher. Recently, this etching technique has been improved by using the Advanced Silicon Etching (ASE) process[1-3]. This process repeats a protection layer deposition cycle and an etching cycle alternately. Because the protection layer deposition is free from etching plasma, this sequential process has higher etching anisotropy compared to the simultaneous etching and protection layer deposition technique[4] used before.

However, the aspect ratio is limited even in this process. Experimental results using this process in the inductively coupled plasma (ICP) etcher report that the highest aspect ratio is typically in the range of 20 to 30 [5,6]. Moreover, in the case we examined for this process, the highest aspect ratio was below 25.

The purpose of this paper is to clarify the limitation factor of the highest aspect ratio in the conventional D-RIE process and to develop a new D-RIE process solving this factor.

LIMITATION FACTOR OF THE ASPECT RATIO

In this section we clarify the factor limiting the highest aspect ratio of the etched trench in the conventional process (the ASE process). The ASE process advances as shown in Figure 1.

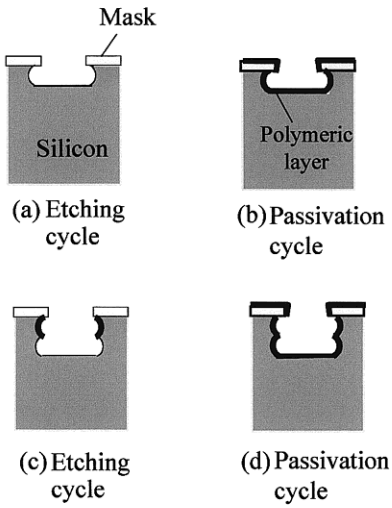


Figure1 The ASE process

This process repeats the etching cycle using SF_6 gas (steps a and c) and the passivation cycle using C_4F_8 gas (steps b and d) until the trench reaches the desired depth. During the etching cycle, the silicon is etched by fluorine plasma. During the passivation cycle, a Teflon-like polymeric layer is deposited inside the trench as the protection layer. At the beginning of each etching cycle, the polymeric layer on the bottom is removed faster than that on the sidewall because of the etching anisotropy of the RIE. After that, the silicon etching proceeds until each etching cycle finishes. On the other hand, lateral etching is prevented while the sidewall polymeric layer remains.

Figure 2 shows the experiment result of the silicon etching we obtained by the normal ASE process with the ICP etcher. This graph shows the dependence of vertical etching rate, lateral etching rate, and the aspect ratio of the etched trench on the etching time. In this case, a SiO_2 layer was used as a mask material, and the mask aperture size was 0.8 μ m. This result shows that constant lateral etching occurs while the vertical etching rate decreases as the etching time goes. Therefore the anisotropy of the etching is reduced and the aspect ratio is saturated below 25. The vertical etching rate reduction is inevitable because the density of fluorine radicals which reaches the trench bottom decreases as the trench becomes deeper. However, lateral etching is a result of incomplete sidewall protection. In other words, the polymeric layer on the sidewall is removed before each etching cycle finishes.

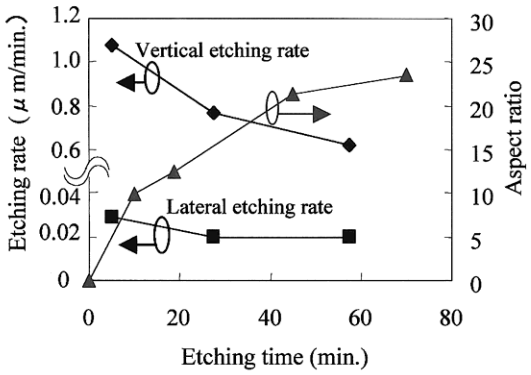


Figure2 Etching time dependence of the etch rate, the aspect ratio obtained by the normal ASE process

Therefore we examined the silicon etching of the ASE process under modified conditions. In this case, the passivation cycle time was increased in order to increase the deposition of the polymeric layer on the sidewall. The result is shown in Figure 3. In this case, not only lateral etching but also vertical etching was prevented. The vertical etching is considered to be prevented by a thick deposition of the polymeric layer on the bottom

because the deposition also occurs on the bottom in the ASE process.

From these results, the limitation factor of the highest aspect ratio is considered to be an isotropic deposition of the polymeric protection layer in the ASE process.

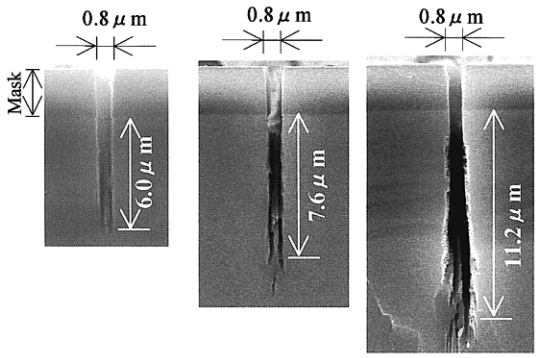


Figure3 The trench profile obtained by the ASE process under polymeric layer deposition increased condition

CONCEPT OF THE NEW D-RIE PROCESS

In order to solve the above-mentioned limiting factor, we have developed a new D-RIE process. The new process named "Dual sidewall protection layer process" is shown in Figure 4.

This process repeats the ASE process (steps a and c) and a secondary protection layer formation process (steps b and d) alternately until the trench reaches the desired depth. The ASE process of this process is the same as shown in Figure 1. The duration of each ASE process is prescribed so as to repeat the etching cycle and the passivation cycle more than two times, and the plasma condition of each ASE process is prescribed independently. During the secondary protection layer formation process, a protection layer which has much higher erosion resistance than the polymeric layer is formed inside the etched trench. At the beginning of each ASE process, the secondary protection layer formed on the bottom is removed faster than that on the sidewall because of the etching anisotropy of the ASE process. After that, silicon etching proceeds until each ASE process finishes. While the silicon etching proceeds, the secondary protection layer still remains on the sidewall, and the polymeric layer is deposited on and removed from this layer repeatedly during the ASE process.

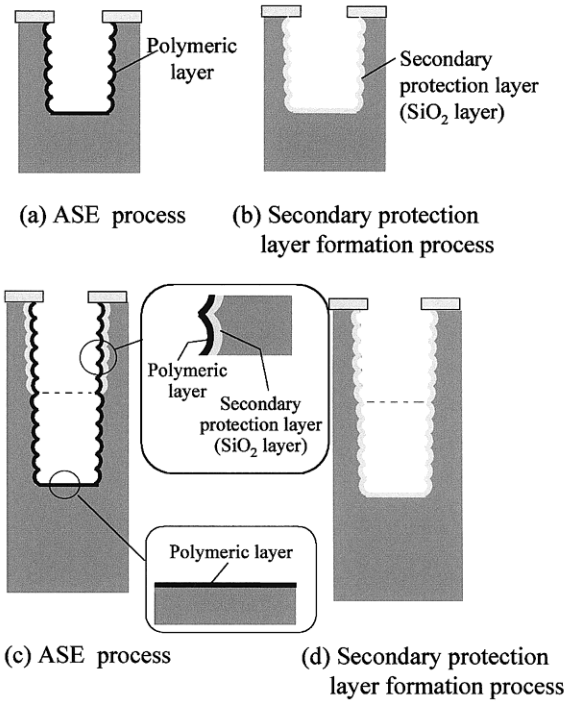


Figure4 The new process (Dual sidewall protection layer process)

Thus, a dual protection layer consisting of the polymeric layer and the secondary protection

layer is formed on the sidewall while the silicon etching proceeds. If the polymeric layer is removed in the etching cycle, the secondary protection layer can still remain on the sidewall. Therefore if the duration of each ASE process is prescribed shorter than the lifetime of the secondary protection layer on the sidewall, the dual protection layer can prevent the lateral etching completely. On the other hand, the secondary protection layer does not exist on the bottom except at the beginning of each ASE process and prevention of vertical etching can therefore be minimized. Thus, this process can improve the etching anisotropy by forming an anisotropic protection layer.

In our new process concept, the material of the secondary protection layer is important. We adopted a SiO_2 layer formed on the silicon surface by O_2 plasma irradiation for the following two reasons.

One reason is because the SiO_2 layer has higher erosion resistance against the fluorine plasma than the polymeric layer. Consequently, if the SiO_2 layer is formed inside the trench with sufficient thickness, the lifetime of this layer can be longer than the duration of the subsequent ASE process. Moreover, since the polymeric layer can be removed by the irradiation, the SiO_2 layer can be formed even if the polymeric layer remains. The second reason is because the O_2 plasma irradiation technique forms the SiO_2 layer much easier than thermal oxidation or chemical vapor deposition. This technique can form the SiO_2 layer on the silicon surface at room temperature. Furthermore, if the O_2 gas is introduced into the etching chamber, a whole new process can be performed only by switching the introducing gas into the etching chamber.

EXPERIMENTAL RESULTS

At first, we examined the SiO_2 layer formation process on a silicon bare wafer by O_2 plasma irradiation. Before and after the irradiation, the surface of the wafer was analyzed with XPS and Ellipsometry.

Figure 5 shows the result of the XPS. A left peak is derived from the silicon-oxygen bonding of the SiO_2 layer, while a right peak is derived from the silicon-silicon bonding of the silicon wafer. The silicon-oxygen bonding peak of the wafer before the irradiation is derived from the natural oxidation layer. After 30 seconds of O_2 plasma irradiation, this peak is increased. From this result, the SiO_2 layer formation on the silicon surface by O_2 plasma irradiation is confirmed.

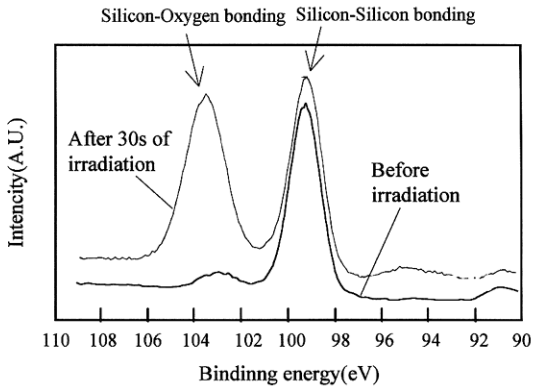


Figure 5 XPS measurement on silicon surface before and after O_2 plasma irradiation

Figure 6 shows a dependence of the SiO_2 layer thickness obtained by the Ellipsometry on the irradiation time. The condition of the O_2 plasma irradiation is same as that shown in Figure 5. This graph shows that the thickness is saturated at 2nm after more than 2 minutes of irradiation. This saturation is caused by a lack of thermal diffusion for oxygen atoms because the O_2 plasma is irradiated to the wafer at room temperature.

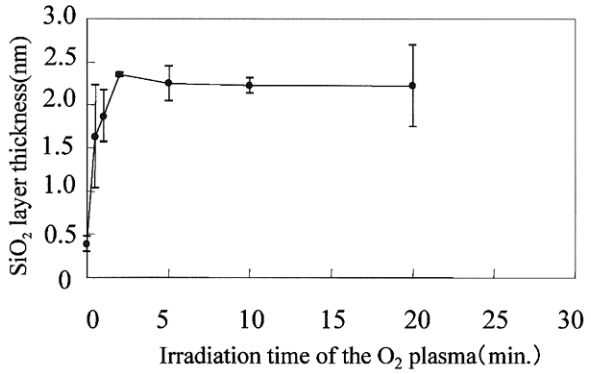
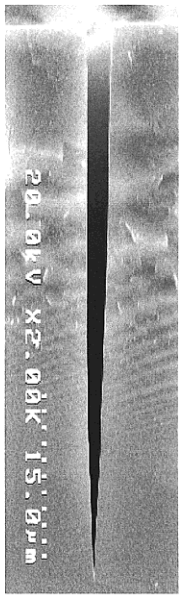
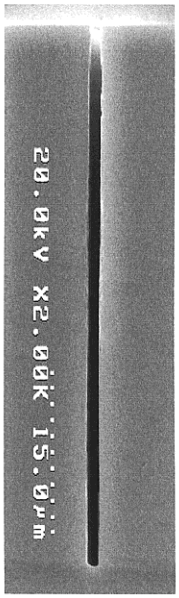


Figure 6 Irradiation time dependence of the SiO_2 layer thickness

According to the detailed experimental results, if a 2nm-thick SiO_2 layer is formed on the trench sidewall, the lifetime of this layer during the ASE process is estimated to be 10 minutes. Therefore, if the duration of each ASE process is prescribed at several minutes in our new process, the SiO_2 layer can remain during each ASE process. However, since the most of the incident oxygen ions are parallel to the trench sidewall, the SiO_2 layer formation rate on the sidewall is slower than that on the bare wafer. Therefore, the duration of the O_2 plasma irradiation process has to be sufficiently long in the new process.

Second, we examined the new process experimentally. The process was prescribed to repeat the ASE process and the O_2 plasma irradiation process alternately in several minute intervals. The plasma condition of each ASE process and O_2 plasma irradiation process were prescribed independently. The total etching time for the ASE process was 70 minutes. In this experiment, a SiO_2 mask was used and the mask aperture size was 0.8 μ m. The etching result obtained by the new process is shown in Table 1.

Table1 Etching results obtained by the conventional process(the normal ASE process) and the new process (The mask aperture size is 0.8 μ m)

	The conventional process	The new process
Trench profile		
Trench depth (μ m)	51.2	50.6
Trench width (μ m)	2.21	1.10
Aspect ratio	23	46

The result obtained by the conventional process (the normal ASE process) is also shown in Table 1 as the reference. In the conventional process,

the trench width is widened up to 2.21 μ m when the trench depth is 51.2 μ m. On the other hand, in the new process, the trench width is 1.10 μ m when the trench depth is 50.6 μ m. The difference between them means the lateral etching is almost completely prevented by the dual protection layer in the new process. Therefore the aspect ratio can be improved up to 46. Furthermore, no extraordinary etching such as black silicon is found in the new process. In an optimized condition, the highest aspect ratio can be further improved.

CONCLUSION

In this paper, we have clarified the limitation factor of the highest aspect ratio of the etched trench in D-RIE. The factor is the isotropic formation of the protection layer in the conventional process. We have therefore developed the new D-RIE process, which forms the protection layer anisotropically, in order to solve the factor. In this process, the dual protection layer consists of the polymeric layer and the SiO_2 layer is formed on the trench sidewall while the silicon etching proceeds. On the other hand, only the polymeric layer is deposited on the trench bottom while the silicon etching proceeds. Lateral etching is almost completely prevented and the aspect ratio of the etched trench is improved drastically by the new process. Furthermore, this process can be performed only by switching the introducing gas into the etching chamber. This process can improve the fabrication technique of high aspect ratio microstructures for MEMS devices.

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