BALL SEMICONDUCTOR TECHNOLOGY AND ITS APPLICATION TO MEMS

Nobuo Takeda
Ball Semiconductor Limited

ABSTRACT

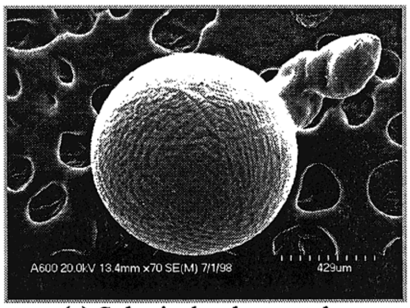
This paper discribes Ball semiconductor technology that realizes integrated circuits and other devices on 1-milimeter sphere. Single crystallization, no-contact processing, spherical liothograpy, 3D VLSI design and VLSI by clustering are five key enabling technologies of the Ball semiconductor. Three major product categories of the Ball, integrated circuits, RF applications and MEMS (Micro Electro Mechanical System), are discribed here. Especially electro-statically levotated 3-axis accelerometer is mentioned as an application of Ball semiconductor technology to MEMS.

INTRODUCTION

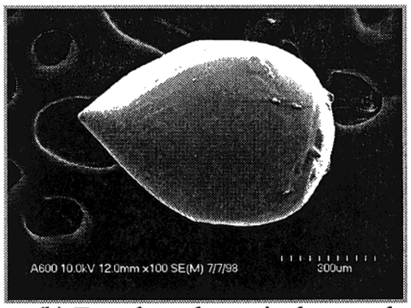
Today's semiconductor industry focuses on making integrated circuits on flat-surface wafers, with chips becoming ever more complex, wafers becoming ever larger, and the manufacturing process increasing dramatically in complexity and cost with each new generation. The investment to establish a new factory reaches \$1billion and the investment to establish a factory for the manufacturing of 1G DRAM may account for \$10billion in the future. In other words, today's semiconductor industry is approaching an economical limit in addition to the physical limits and the technological limits in the case of the deep sub-micron semiconductor devices.

Instead of today's semiconductor industry, we are challenging to overcome the economical limit using a brand-new concept. Our idea is to make semiconductor integrated circuits and other devices on 1-millimeter sphere [1], which has about 3 times larger surface area than 1-millimeter square chips. Our internal goal is to reduce the manufacturing cost down to one-tenth of the conventional semiconductor and to shorten the production lead time less than a week. We call this technology Ball™ semiconductor. Using Ball semiconductor technology, we are able to create unique MEMS (Micro Electro Mechanical System) devices with three-dimensional structure. Some of our fabrication technology itself is applicable to the fabrication of conventional MEMS devices as well.

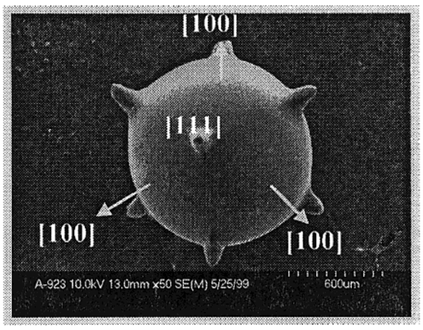
In this paper, the five key enabling technologies [2-4] to realize the integrated circuits on a sphere are presented and several ball products are introduced.



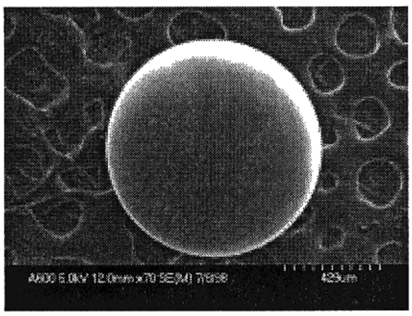
(a) Spherical poly crystal



(b) Tear drop shape single crystal



(c) Honed single crystal



(d) Single crystal sphere after polishing

Figure 1: Various shapes of spherical crystal

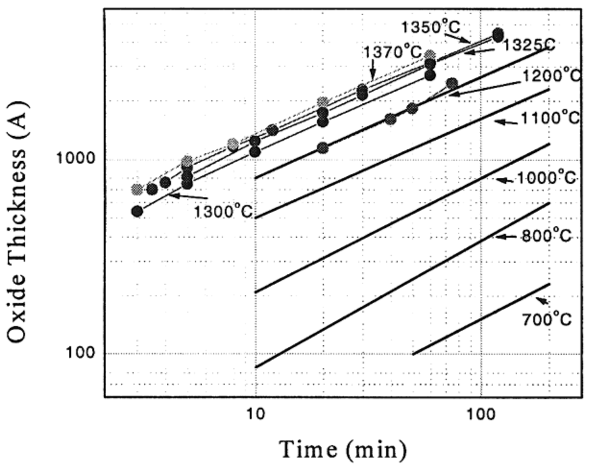
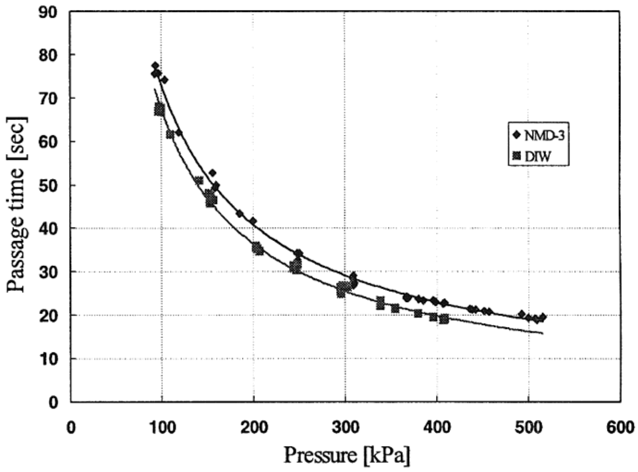
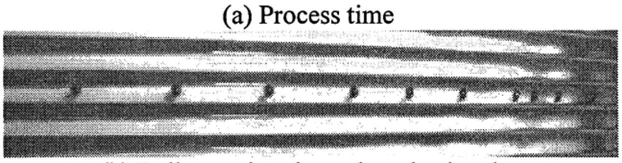


Figure 2: No-contact high temperature
Dry oxidation



(a) Process time



(b) Balls running through a plastic tube
Figure 3: Photo-resist developer system

KEY ENABLING TECHNOLOGIES

The basic concept of Ball production line is manufacturing the Ball in a continuous, enclosed tube process like a chemical plant, except for the exposure process and the bumping process. The smallness and the roundness of the spherical feature make this unique process concept available. The Ball devices with three dimensional structure requires unique design technology. We have identified the following five fields as the key enabling technologies of Ball semiconductor.

Single crystallization

The first and foremost step in making a Ball™ integrated circuit is the fabrication of single crystal spheres. Poly-crystal granules are sorted by weight and/or size to get appropriate raw materials for making 1-milimeter single crystal spheres. The granules are preheated and melted by a high-energy plasma source, Inductively Coupled Plasma (ICP). The melted granules are then dropped through a solidification tube, which is about 7 meters in height. During the free fall, the granules are solidified. The crystal shape, as shown in figure 1, depends on the heating and cooling conditions. Figure 1 (a) shows a spherical poly crystal and figure 1 (b) shows a tear drop shape single crystal. Figure 1 (c) is the current best shape of the spherical single crystal and 8 horns are an evidence of the single crystal. The crystal orientation of the horns is the [111] direction. The formed horns are attributed to the volume expansion from the liquid phase to the solid phase and the difference of the solidification speed in crystal orientation. The [111] direction has the slowest solidification speed, so that the excess liquid is maintained in [111] direction until the end of the solidification with forming the horns.

After the single crystallization, the horned crystal is lapped to make the perfectly spherical crystal and then polished to make mirror-like finish with no surface deformations (Figure 1 (d)). The lapping accuracy is 1.0mm +/- 0.07um, and the polishing accuracy is about 1.0mm +/- 2um, which is a little bit worse than that of lapping.

No-contact processing

Integrated circuit fabrication involves deposition and etching of various types of films on the ball. These typical semiconductor fabrication steps are done in clean pipes or tubes instead of a clean room. Such processing requires that the balls do not hit the walls of the pipes, or each other, to prevent damage and contamination. To meet this requirement, we have developed two types of the process equipment. One is for the gas phase processes and the other is for the liquid processes.

In the prototype gas phase system, a ball is floating inside the tube in atmospheric pressure. The inner diameter of the tube is about 2-milimeters. The carrier gas of the precursor suspends the ball itself. We have already built oxidation systems, diffusion systems, a poly Si CVD system, oxide CVD system, metal CVD systems for Al, Cu and TiN [5]. As an example of the gas phase system, figure 2 ilustrates a relationship between the oxide thickness and the oxidation time of the high temperature oxidation up to 1370C. The solid line indicates the data of the oxidation results in the conventional wafer processing and the plots are our results on the Ball. Both of them follow the Deal-Grove's Law. Ball's small size and floating feature enables the

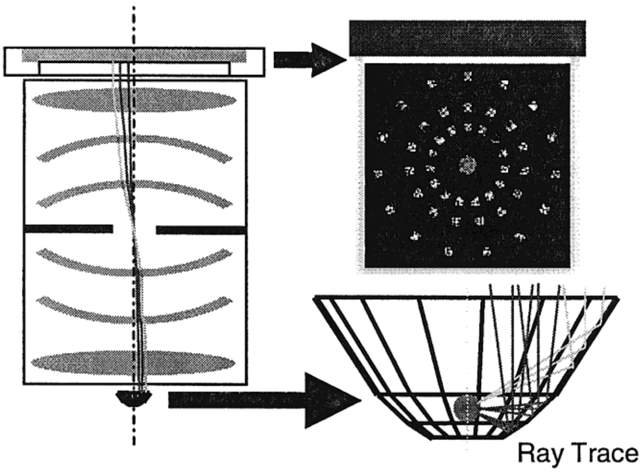
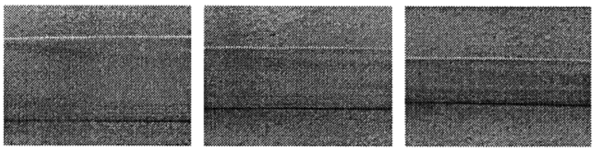


Figure 4: Multi-faceted mirror lithography system



(a) 3um (b) 2um (c) 1.5um

Figure 5: photo-resist line
Light source: g-line
Resist: TOK OFPR-800,
Reduction: 1/5

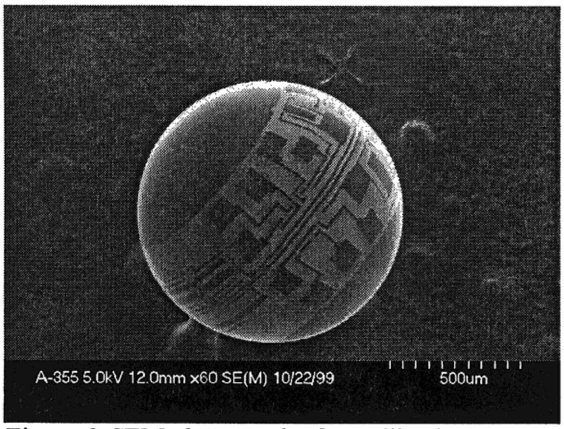


Figure 6: SEM photograph of metallization patterns

oxidation process to be performed at such a high temperature.

In the liquid system, balls are flowing with the liquid chemical(s) along the inside wall of the plastic tube, which is wrapped like a coil followed by a DI water rinse system. We have been developing wet etching systems, developing systems, plating systems and so forth. In the case of the liquid system, the processing time can be controlled by the tube length and by the pressure. For example, figure 3 (a) shows a relationship between the processing time and the pressure of the chemical in the photo-resist developer system. Figure 3 (b) is a picture of the balls running through the plastic tube with the chemical.

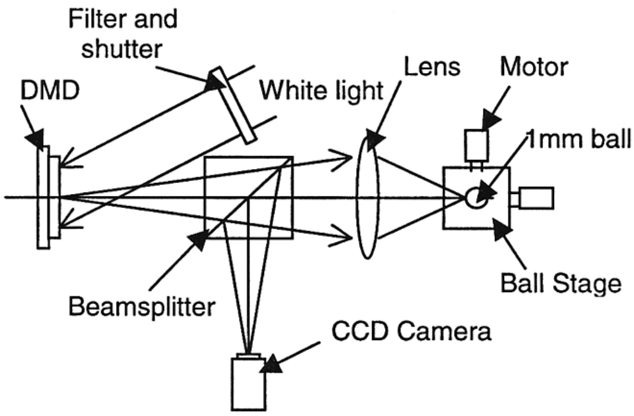
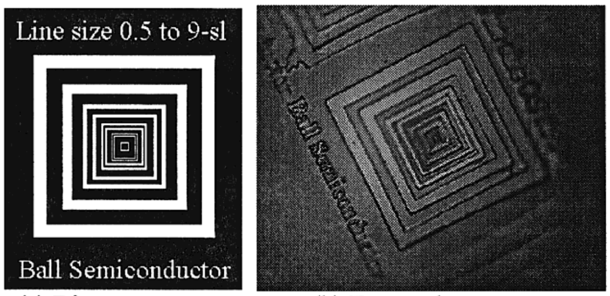


Figure 7: Mask-less lithography system



(a) Bit map pattern (b) Exposed pattern

Figure 8: Exposed pattern by Mask-less lithography

Spherical lithography

One of the high hurdles in Ball Semiconductor technology is spherical lithography. We have developed a lithography system including a multi-faceted mirror, spherical alignment and 2D mask generation to expose about 60% of the entire surface of a sphere in one exposure shot. An optical system focuses the images of 45 sub-fields in a flat mask through the 45 small flat mirrors onto the ball as shown in figure 4. Each mirror size, position and angle are well designed and fabricated to have enough focus depth, enough resolution and proper stitching characteristics on the sphere. The estimated resolution is 1.75um. Figure 5 (a), (b) and (c) shows photo-resist lines of 3um, 2um and 1.5um in width, respectively. Figure 6 is a SEM picture of a D-type Flip Flop metal pattern, which is mapped around the equator of the sphere in one shot.

As a second generation of the exposure system, we recently developed so-called mask-less lithography system as illustrated in figure 7. This system includes two important concepts. One is the Digital Micro-mirror Device (DMD) [6], which works as a pattern generator instead of a quartz mask, and the other is the original micro lens system which has a spherical focal plane rather than a flat focal plane.
The DMD consists of an 800x600 micro-mirror array. Each micro-mirror is 16um x 16um square in size and the

array places each micro-mirror on a 17um pitch, leaving a gap of less than 1um between mirrors. Each micro-mirror can be individually addressed for two tilting positions, +10 or –10 degrees, so this device can be used as a pattern generator which is driven by computer directly. In addition, the electrical alignment of the patterns becomes possible without using the mechanical alignment method.

The original micro lens system has a reduction ratio of 10:1. The Depth of Focus (DOF) is almost 10um when the resolution is 1.5um. The Numeral Aperture (N.A.) of the lens is 0.2, so the spatial frequency, which is lower than 50l/mm in the object space, will pass the lens. As the lens is same as a low pass filter, the 1um gaps between micro-mirrors do not affect the image on the ball. The shutter is a red filter. The red light is for the purpose of focusing and aligning ball position after the shutter (red filter) is off. The pattern on the DMD and the pattern on the ball is observable on the CCD monitor.

Figure 8 (a) and (b) shows the designed bit map pattern and the exposed resist pattern respectively. The bit map pattern is successfully exposed on the surface using the DMD. Six micro lens systems with DMD will cover almost 100% of entire surface of a sphere.

In general, it takes about a month and huge cost to make quartz masks. On the other hand, the mask-less lithography system could reduce R&D cycle time and cost dramatically. The flexibility of pattern designing and mapping has much benefit produce small quantities and many varieties of devices such like MEMS as well.

3D VLSI design

Designing circuits on a sphere is another unique aspect of Ball Semiconductor technology. There are two main issues in 3D design over conventional 2D design. The first is the closed surface topology with the inability to look at the entire design surface as a whole. The second is that there is no perpendicular grid system, which can cover the entire surface of the sphere. So we need a unique display system with a specifically ruled grid system.

Currently we have developed a 3D layout design tool, ABLE (Advanced Ball Layout Editor). ABLE was created to have high flexibility featured in (1) changing its viewpoint all the way around the sphere and (2) moving its relative coordinate in any desired direction. We can draw the shortest path between two specific points, which is characterized by a great circle, as well as parallel lines as shown in figure 9.
Recently, ABLE has been connected to the mask-less lithography system. We are improving the tool by adding the functions of design rule check, electrical simulation capability and so forth.

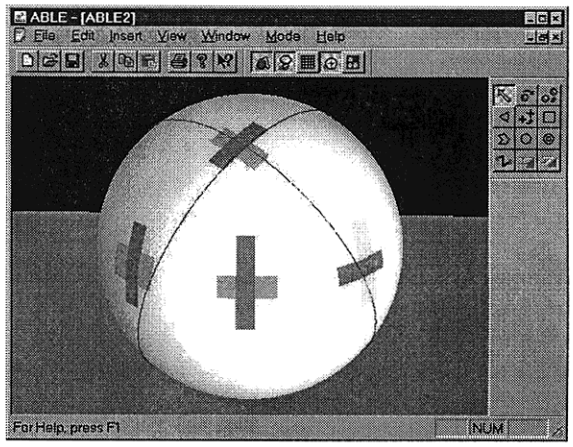


Figure 9: 3D layout design tool ABLE

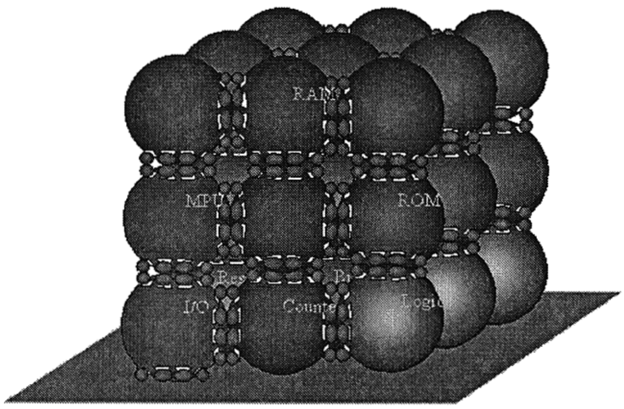
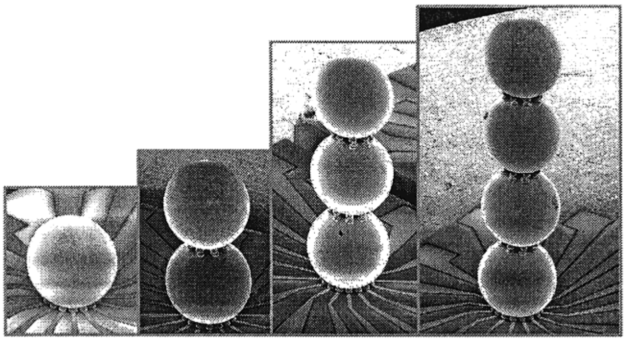


Figure 10: Image of clustering system

VLSI by clustering

In today's semiconductor industry, there is a trend to integrate as many functions as possible in one chip. For example, digital circuits and analog circuits, or logic circuits and DRAM are embedded in one chip, though the process becomes more complex and the device structure might be compromised. It is symbolized as "system on chip".

Our approach toward the large scale integration is to cluster the Balls together like a molecule. Figure 10 schematically illustrates the concept of clustering. Each ball may have a specific function separately like logic circuit, DRAM, ROM, I/O circuit, analog amplifier, high voltage device and so forth, which are designed and processed for the specific structures. Furthermore, opt-electrical devices such as Light Emitting Diode, sensors, MEMS are possibly clustered. We call this technology as "mixed technology". Each ball could be a hardware-macro, which is related with a software library. We are developing clustering software including the library and the partitioning technology of the large scale circuit.



(a) 1ball (b) 2balls (c) 3balls (d) 4balls
Figure 11: Clustering by micro gold bump

Figures 11 (a) to (d) are SEM pictures of the clustering Balls using the micro ball bump technology [7]. The material of the bump is gold and its size is about 80 um in diameter. The size and the position of the bumps are designed to match the requirement of the number of the pins. This bump technology involves a unique surface mount technology since it deals with an electrical interface between balls and the substrate as well.

BALL PRODUCTS

Our ultimate goal for the product is the integrated circuit on the sphere. However we are exploring ball unique products utilizing the smallness, the roundness and other features of the Ball. We have identified the following three fields for our product.

IC Ball

The integrated circuit technology is a fundamental for whatever product we will aim at. The characterization testing of MOS diode, P/N junction diode and MOS transistor on the spherical surface has been done to prove the fabrication processes. Recently the first 5um NMOS E/E mode inverter on the spherical surface was developed. Figure 12 is a picture of the inverter and figure 13 shows an inverting function of the circuit using a logic state analysis of input signal, output signal and power supply of the inverter.

The next target for the development will be CMOS circuit and memories. The minimum feature size of the devices will become smaller and smaller for the time being as the conventional chip technology has been doing during the past 40 years or more.

RF Ball

Because of the three dimensional shape of the ball, a coil on the 1-milimeter ball surface is expectable to have several times larger value of inductance than that on a 1-milimeter square chip surface. So, another candidate of Ball unique product is RF applications such as RF ID tag and telemetry.

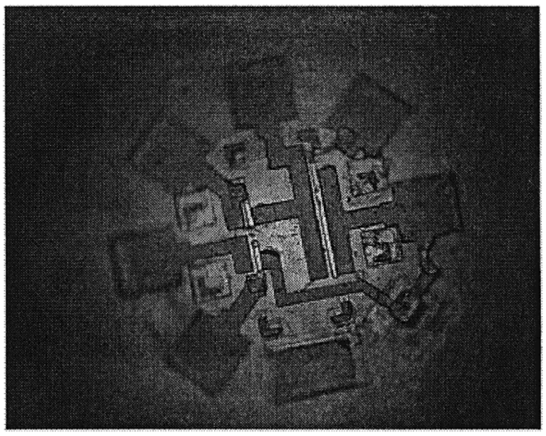


Figure 12: 5um NMOS inverter on the sphere

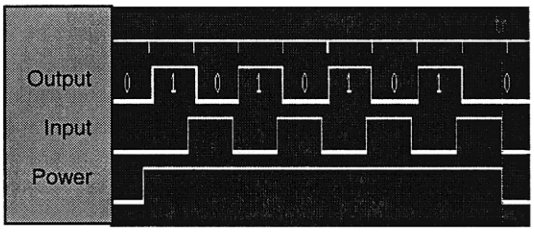


Figure 13: Logic state analysis of an inverter on the sphere

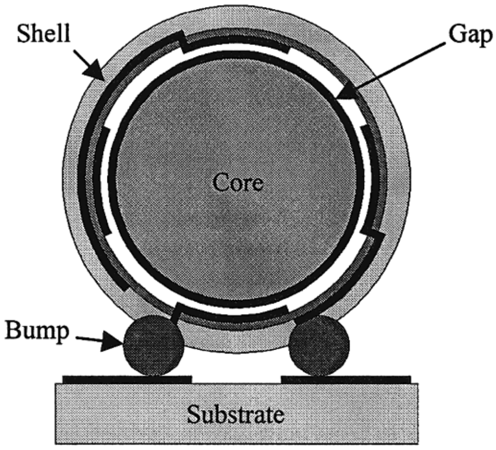


Figure 14: Cross section of 3D accelerometer

MEMS Ball

Benefited by highly symmetrical 3D structure, closed topology of the ball, and surface process capability, the MEMS is one of the most interesting applications of the Ball technology. We are currently developing an electro-statically levitated 3-axis accelerometer using the surface micro-machining technology on the ball [8,9]. The accelerometer consists of an outer shell and an inner core as shown in figure 14. There is a narrow and precise gap between the shell and the core. Electrodes for the electrostatic actuation and the capacitive sensing are placed at the inner surface of the shell. The position of

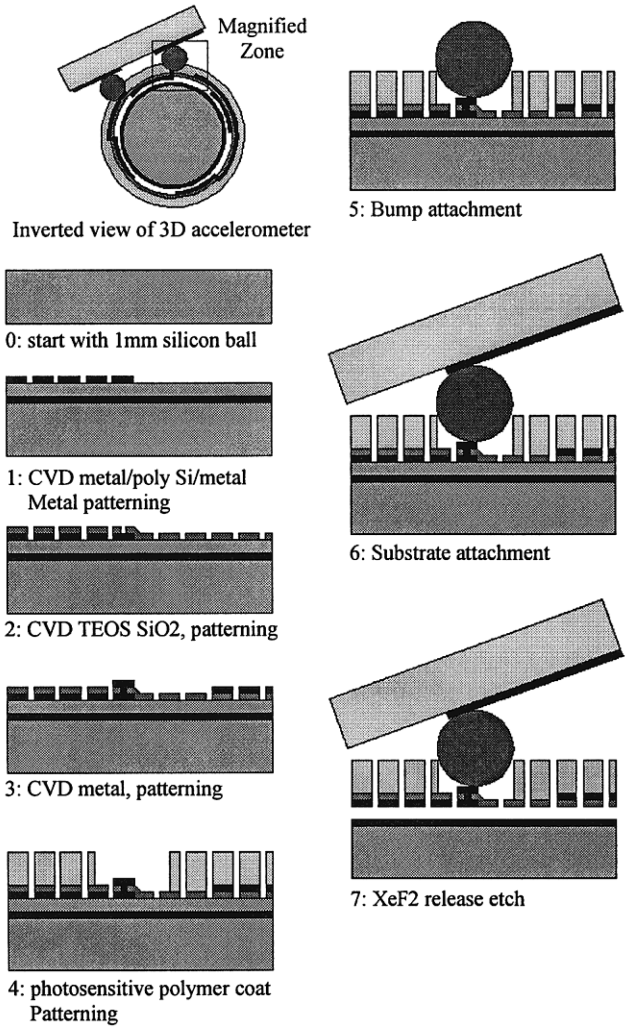


Figure 15: Process flow of 3D accelerometer

the core is controlled by a closed-loop system to keep in the center and a feedback intensity tells the acceleration. The mass of the 1milimeter core is relatively large compared with the typical 2D surface micro-machined sensors. A conceptual process flow for the accelerometer is illustrated in figure 15. A key process is a sacrificial layer etching using xenon difluoride (XeF2), which generates the gap. A beauty of the XeF2 etching is its extremely high selectivity between the Silicon and other materials. This etching process is performed at the final step of the flow to avoid the damage of the shell from excessive stress of the bump and mount.

Other inertia sensors, such as clinometer and gyroscope, may be realized by utilizing a similar structure. In the case of clinometer, the inner core moves freely so that capacitance change is measured according to the device tilting. In the case of gyroscope, the inner core will be electro-statically levitated and rotated. This principle of the gyroscope is well known to have the highest sensitivity among various gyroscopes [10].

CONCLUSION

We have developed spherical single crystallization system, gas phase and liquid chemical process equipment using tubes and pipes, two different types of spherical lithography systems, 3D layout tool, clustering technology and so forth. We have demonstrated the characteristics of 5um NMOS inverter as an evidence of the process establishment. These research and development activities have just begun and our efforts will be continued to reduce the fabrication cost and the cycle time of semiconductor devices. We are exploring unique products not only for the integrated circuit but also for RF, sensor and MEMS fields so as to open up new markets utilizing the smallness, the roundness and the 3D features of the Ball.

ACKNOWLEDGMENT

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