FABRICATION OF A THREE-AXIS ACCELEROMETER INTEGRATED WITH COMMERCIAL 0.8μm-CMOS CIRCUITS

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ABSTRACT

In the present study, a fabrication technology of bulk-micromachined three-axis accelerometer integrated with commercial CMOS circuits has been investigated for low cost realization and improvement of device performance. The key technologies in the developed fabrication technology are wafer thickness control, backside polishing with chemical spin etching and anisotropic etching with PVD SiO_2 mask. The signal processing circuits were fabricated with a commercial 0.8μm-CMOS technology, and all the micromachining processes were performed to complete CMOS wafers. Characteristics of the devices and reliability for the repetitive vibration load were evaluated. As a result, basic performance of the accelerometers with this technology was confirmed.

INTRODUCTION

Silicon micromachined sensors are well known for their ability to integrate peripheral circuitsß in the same die. It is necessary for such smart sensors to form the integrated circuit part with low-cost technology, because total cost of devices should be reduced. So, utilization of commercial (i.e. standard) CMOS technology is necessary to produce smart sensors in a reasonable cost. Post-CMOS micromachining becomes much important for the purpose. However, some problems have been remained in post-CMOS bulk-micromachining as follows. (1): Accommodation to variable wafer thickness of commercial CMOS, (2): Existence of unnecessary layers on the initial backside of CMOS wafers, (3): Difficulty to form mirror face on the backside for following anisotropic etching process and glass bonding, (4): Development of proper masking material for post-CMOS anisotropic etching. Anisotropic etching is necessary to form 3D-structures in low-cost, because it does not need expensive apparatuses.

Due to the above problems, there have been many limitations to fabricate smart sensors with commercial CMOS technologies.

In this study, a fabrication technology of bulk-micromachined three-axis accelerometers integrated with a commercial CMOS technology has been investigated for low cost realization and improvement of device performance. The above problems are solved in the developed fabrication technology. All the micromachining processes were performed to complete CMOS wafers fabricated with a commercial CMOS technology. So, smart sensors can be fabricated from most of commercial CMOS wafers using the developed fabrication technology in a reasonable fabrication cost.

In the article, the post-CMOS fabrication technology established for a three-axis accelerometer is presented. The integrated circuitry in the device was fabricated with a commercial 0.8μm-CMOS technology. The technology can be applied for advanced deep sub-micron CMOS technologies because of its versatility. Detail of the fabrication technology, principle and characteristics of fabricated devices, and reliability of the sensor devices with this fabrication technology are mentioned and discussed in the later sections.

DEVICE CONFIGURATION

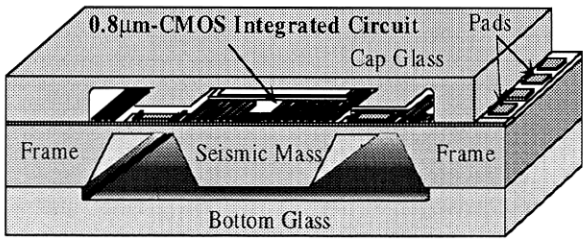

Figure 1: Cut-away simplified drawing of the 0.8μm-CMOS integrated three-axis accelerometer.

In this study, two kinds of accelerometer were fabricated. The sizes of the devices are 3×3 mm^2 and 6×6 mm^2, respectively. Fig. 1 shows cut-away simplified drawing of the 0.8μm-CMOS integrated three-axis accelerometer. The device has a three-layer structure formed by SW-3 glass, silicon and SW-3

glass. The cap glass is bonded on the surface of silicon structure to seal the accelerometer. It makes it possible to use plastic package for low-cost packaging of the accelerometer. On the silicon surface, CMOS integrated signal processing circuits are integrated with a commercial 0.8μm-CMOS technology on the surface of the seismic mass. For detection of acceleration, p-MOSFETs are used as stress sensitive elements in this accelerometer [1]. It is based on piezoresistive effect of p-type inversion layer in p-MOSFETs [2]. Since p-MOSFETs are standard elements in standard CMOS circuits, it is one of a useful way for CMOS integrated sensors to use them as sensing elements.

Fig. 2 shows the configuration of the new-type strain detection circuit with stress sensitive p-MOS inputs formed on thin beam structures.

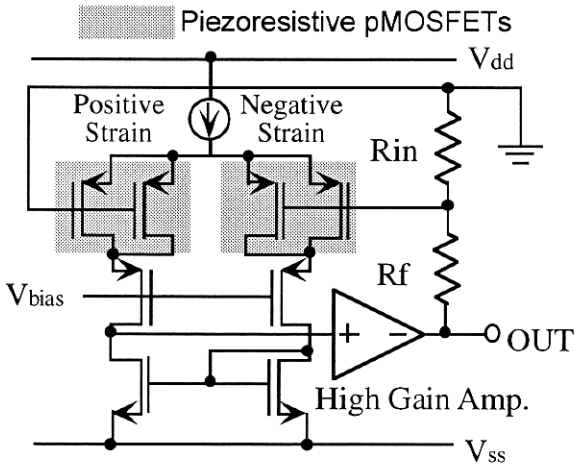

Figure 2: Configuration of the new detection circuit with negative feedback technique.

The detection circuit detects deflection of the beams like Whetstone bridges. The applied stress causes mobility imbalance in the input pair of the differential amplifier. As the result, input referred offset voltage is shifted, and it is amplified by the total voltage gain of the feedback amplifier (-Rf/Rin). As compared to our previous detection circuit [1], total gain of the amplifier is more stable due to the negative feedback effect. In this study, the voltage gain was set to 100.

Fig. 3 shows the beam structure of the three-axis accelerometer with four suspension beams. Piezo-resistive p-MOSFETs are formed on the edges of each beam shown by the dark markers. So, four sets of the detection circuits shown in Fig. 2 are integrated in the accelerometer. Since the folded beams can be formed in longer length and balanced structure, higher sensitivity can be obtained without any horizontal rotation mode in X-Y plane.

Three-axis components of acceleration are calculated from the signals of the four detection circuits. The principle is similar to our previous device [3], but circuit configuration and device structure is much improved in this study. Three components of acceleration can be detected by addition and subtraction of output signals from the four detection circuits as expressed in the following expressions.

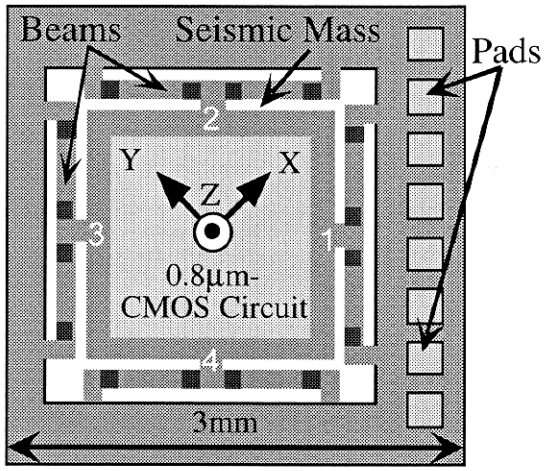

Figure 3: Top view of the three-axis accelerometer with integrated 0.8μm-CMOS signal conditioning circuit.

$$Voutx = (V_1+V_2) - (V_3+V_4) \quad (1)$$

$$Vouty = (V_2+V_3) - (V_1+V_4) \quad (2)$$

$$Voutz = V_1+V_2+V_3+V_4 \quad (3)$$

V_1, V_2, V_3 and V_4 are the output voltage of the detection circuits formed on the beams 1 ~ 4, respectively. With this detection principle, each component of acceleration can be extracted without cross-axis sensitivity.

In the previous CMOS integrated three-axis accelerometer reported by us, the design rule of the CMOS circuit was 5 μm, and some fabrication steps in CMOS fabrication were modified for micromachining [1]. If the configuration is same, the part of signal processing circuits can be formed approximately in 1/36 area with 0.8μm-CMOS technology. This means that, larger chip area can be used for formation of seismic mass as compared to the device with larger design rule. This results in improvement of sensitivity, if the total die size is equal. From the economical point of view, small-sized circuit in accelerometers has an advantage on fabrication cost. Considering the fact explained above, integrated accelerometer with same sensitivity could be formed in a smaller die size. This is directly concerned with the device fabrication cost. Thus, reduction of CMOS design rule is quite effective for improvement of cost-performance ratio.

For the benefit of advanced CMOS technologies, fabrication technology, which makes it possible to use advanced CMOS technology was developed.

DEVELOPED FABRICATION PROCESS

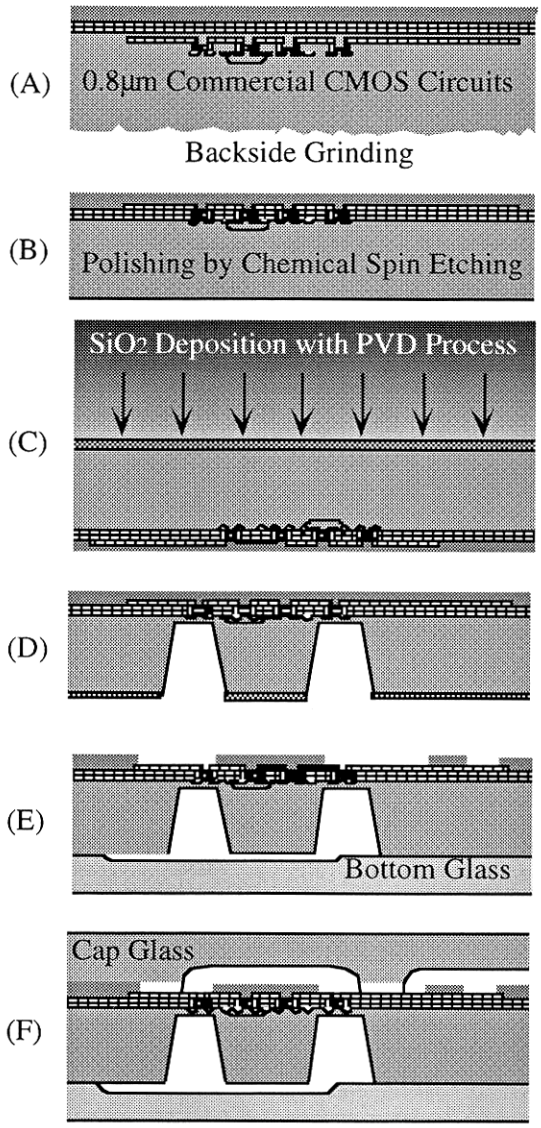

Figure 4: Fabrication process flow developed in this study.

The outline of the fabrication process devoloped is shown in Fig. 4. In this process, a commercial 0.8μm-CMOS technology was used to form signal-processing circuit. However, most of the CMOS fabrication technology is also available in the fabrication process, because it does not depend on the thickness of wafers and condition of the wafer backside.

(A): Firstly, thickness of complete 0.8μm-CMOS wafer was roughly controlled by grinding backside of wafer.

(B): Then, the backside was etched and polished by chemical spin etching process [4], [5]. These wafer thinning and backside polish processes are used normally in standard LSIs for IC card applications. Fig. 5 shows the look of the chemical spin etching process at SEZ Japan Inc. [4]. The backside of the CMOS wafers can be etched and polished at the same time. So, the defective layer due to the backside grinding process is removed perfectly. In this case, the backside was etched by 100 μm by the process, and wafer thickness was controlled to 300 μm.

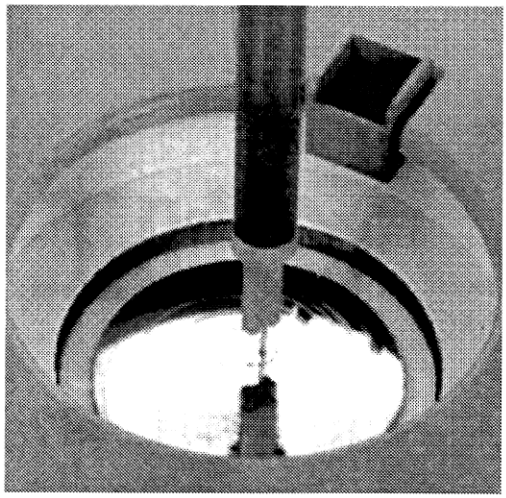

Figure 5: Chemical spin etching process [4].

Fig. 6 (a) and (b) show AFM images of the backside of CMOS wafers after the backside grinding, and the chemical spin etching process, respectively. The roughness of the backside surface was much reduced after the spin etching process as shown in Fig. 6 (b). The RMS value of the spin-etched surface was 0.88 nm. It is enough small to bond an anodic bonding glass with to the backside. Furthermore, as the surface of the backside becomes smoother, roughness of the surface etched by anisotropic etching also becomes smoother.

(C): On the polished backside, PVD SiO_2 layer was formed as the masking layer for followin bulk-etching process with TMAH solution. As a result of our experiments, PVD SiO_2 layer was a good masking material for post-CMOS anisotropic etching [6]. PVD SiO_2 layer was formed on the backside without any electrical damages in 0.8μm-CMOS devices.

(D): The PVD SiO_2 masking layer was patterned by photo-lithography process using a backside lithography system, and etched in BHF solution. After that, silicon substrate was etched in 90 °C-TMAH solution to form 10-μm thick structure for beam formation.

(E): SW3 glass (Asahi Techno Glass Co.) was etched to form 10-μm depth air gaps for mass. Special groove patterns connecting all the chips were formed at the same time to make the pressure in the structures be equal to outside pressure. The grooves have a function to avoid fracturing of devices due to the pressure change at the release process. On the other hand, PVD SiO_2 masking layer on the backside of CMOS wafers was removed. The CMOS wafers and patterned SW3 glass were bonded with anodic bonding at 380 °C. Then, the seismic mass and the beam structures were

released from peripheral rib with RIE etching. Because of the special grooves on the glass, there is no fracture risk due to the pressure difference between the device inside and the RIE chamber.

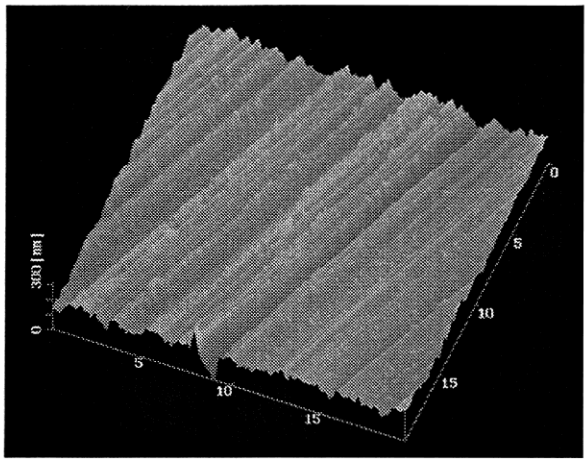

Fig. 6 (a)

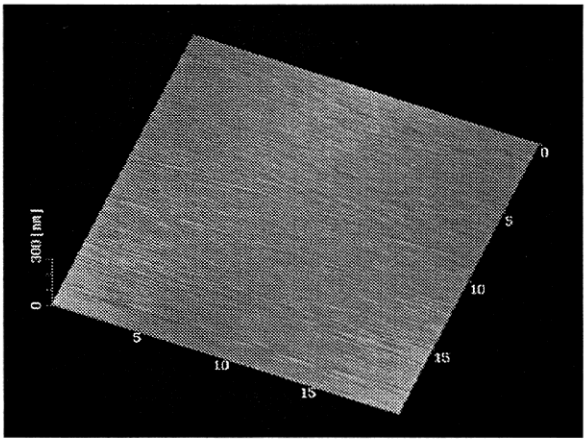

Fig. 6 (b)

Figure 6: AFM images of the backside of CMOS wafers; (a): before the spin etching process, (b): after the spin etching process.

(F): A glass cap for device sealing is bonded to the top Al layer of the CMOS circuit. As the glass is bonded to the top metal layer, electrical through pass between the bonding pad and circuits are formed with lower level of metal layer. After bonding the cap glass, the accelerometers are diced and packaged.

The die size of the fabricated accelerometers were 3×3 mm^2 and 6×6 mm^2. Fig. 7 (a) and (b) shows the photographs of a fabricated three-axis accelerometer with 3×3 mm^2 die area. The p-MOSFET sensing elements and Al wires are seen on the surface of the 50 μm-width beams. The size of piezoresistive p-MOSFETs was designed to have relatively large area (100 μm/30 μm of W/L) in order to reduce 1/f noise from the sensing elements. A detection circuit corresponding to Fig. 2 is seen on the mass near a connecting point of the beam. At this stage, cap glass is not bonded on CMOS surface. The best way to bond the cap glass has been investigated. There are some available ways to bond the cap glass, however it is necessary to prevent any electrical or physical damages in the integrated CMOS circuits.

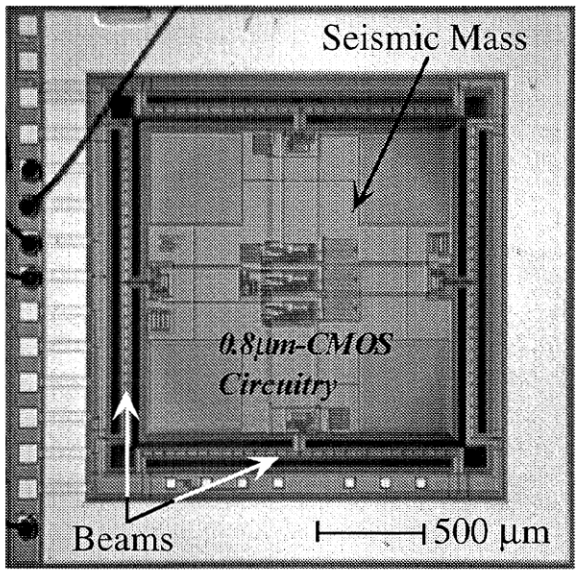

Fig.7 (a)

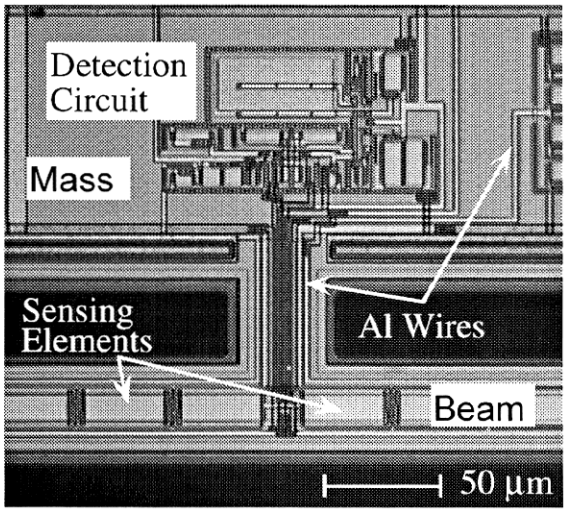

Fig. 7 (b)

Figure 7: Chip photograph of fabricated three-axis accelerometer (3×3 mm^2); (a): Top view of the accelerometer, (b): Expanded photograph around a beam structure.

This fabrication technology can be applied to most of commercial CMOS technologies, because it does not depend on the backside condition and thickness of wafer after CMOS fabrication. Using the wafer thickness control and the polish technique mentioned above, functional smart sensors with sophisticated

CMOS processing circuit would be realized in a reasonable total fabrication cost.

CHARACTERISTICS OF DEVICES FORMED WITH THE DEVEOPED TECHNOLOGY

Basic Performance

The fabricated device has been evaluated with a feedback controlled vibration generator system. Fig. 8 shows the output signal of each-axis detection circuit for Z-axis acceleration input. This is the characteristic of accelerometer with 3×3 mm^2 die size. The amplified Z-axis sensitivity of it was about 12.5 mv/G. On the other hand, Z-axis sensitivity was 167.5 mv/G for 6×6 mm^2 accelerometer. Lager size accelerometer has higher sensitivity for the same fabrication technology.

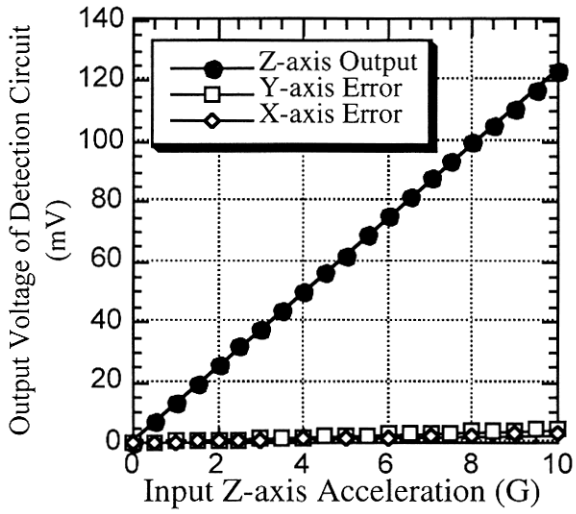

Figure 8: Output signal of each-axis detection circuit for Z-axis acceleration input.

With the signal operation expressed in Eqs. 1–3, X and Y-axis detection output for Z-axis acceleration input was canceled to around 1.3 % of Z-axis detection output. As the principal axis sensitivity for X and Y-axis of the accelerometer was about 25 % of Z-axis sensitivity, maximum cross-axis sensitivity of X and Y-axis output was around 5% for Z-axis acceleration.

The minimum resolution (i.e. noise level) of acceleration was determined by the ratio between the circuit noise at the output and the sensitivity of the device for unit acceleration. The calculated minimum resolution of the 6×6 mm^2 accelerometer was about 2.0 mG_{rms} for Z-axis acceleration, and 10.8 mG_{rms} for X and Y-axis acceleration. On the other hand, minimum resolution of 3×3 mm^2 accelerometer was about 26.8 mG_{rms} for Z-axis acceleration, and 119.0 mG_{rms} for X and Y-axis acceleration. Since the output noise from each detection circuit was almost same among all the accelerometers, minimum resolution of each accelerometer depends only on the stress level generated by unit acceleration on the piezoresistive p-MOSFETs. Therefore, an accelerometer with larger device area has improved minimum resolution because of its larger sensitivity.

Temperature Characteristics

Temperature characteristics of the accelerometer were evaluated with a feedback temperature control system. Temperature dependence of offset and sensitivity of the fabricated accelerometer are shown in Fig. 9. These are measured characteristics of the accelerometer with 6×6 mm^2 die area.

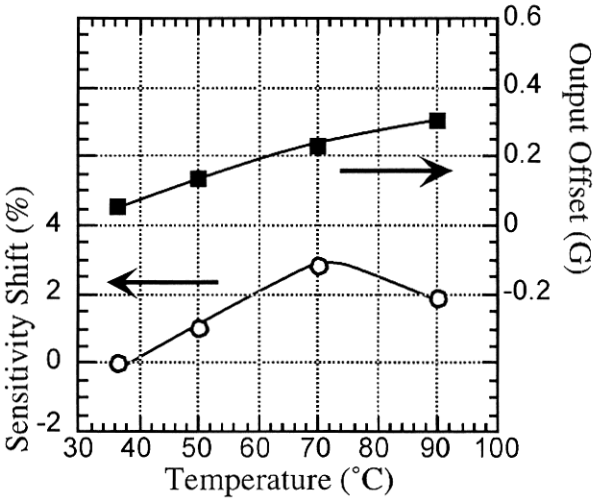

Figure 9: Temperature characteristics of output offset voltage and acceleration sensitivity.

Sensitivity shift in a temperature range from room temperature to 90 °C was within 3 % of the room temperature sensitivity. The offset shift at the output in the temperature range was below 0.3 G in acceleration equivalent value for Z-axis input. On the other hand, the offset shift will be larger in the accelerometer with 3×3 mm^2 die size, because sensitivity of the device is smaller than that of 6×6 mm^2 accelerometer. Smaller sensitivity results in larger offset drift, when the voltage drift is referred as an acceleration equivalent value. This is similar with the case of the minimum resolution.

Reliability Test with Repetitive Load

Reliability of the beam structure formed with this technology has been investigated with repetitive vibration load to the accelerometer. Fig. 10 shows the relationship between the load cycles and device characteristic shift. As the repetitive vibration load, 20 MPa stress was applied to sensing piezoresistive p-MOSFETs formed on the edges of the beam structures.

Significant changes in sensitivity and offset were not observed after applying 6×10^7 time repetitive load.

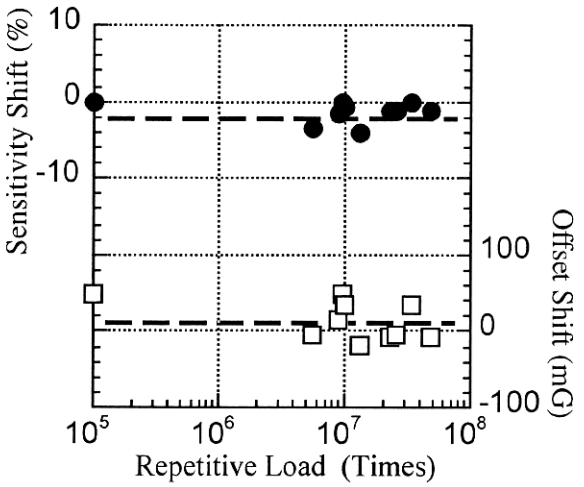

Figure 10: Sensitivity and Offset shift of the accelerometer for Repetitive Load of 20 MPa stress in the beam structures.

Table 1: Summary of characteristics of accelerometers formed with the developed fabrication technology.

Die Size	**6×6 mm^2**	**3×3 mm^2**
Minimum Resolution Z-Axis	2.0 mG_{rms}	26.8 mG_{rms}
Minimum Resolution X, Y-Axis	10.8 mG_{rms}	119.0 mG_{rms}
Cros-Axis Sensitivity	~ 5 %	~ 5 %
Signal Bandwidth	> 100 Hz	> 240 Hz

The characteristics of the fabricated three-axis accelerometers are summarized in Table 1. Comparing with our previous device fabricated with modified 5μm-CMOS technology [1], the accelerometer with commercial 0.8μm-CMOS showed about 20 times better performance on minimum resolution for the same die area. In advanced CMOS technologies, gate oxide thickness is scaled down according to their design rules. Assuming the same surface state density in MOSFETs, 1/f noise is inversely proportional to the thickness of the gate oxide. So, noise from MOSFET can be reduced using advanced CMOS technology. Furthermore, thanks to narrower width of metal lines, width of beam structures can be narrowed. Thus, sensitive structure can be formed easier with advanced CMOS technologies. These are the major reasons why the performance of accelerometer with advanced CMOS is much improved.

CONCLUSIONS

In this paper, a fabrication technology of bulk-micromachined three-axis accelerometers integrated with commercial CMOS technology has been investigated for low cost realization and improvement of device performance. One of the key technologies to use commercial CMOS for such devices was thickness control with backside chemical spin etching. In the fabricated devices, integrated circuits were formed with a commercial 0.8-μm CMOS technology, and all the micromachining processes were performed after the CMOS fabrication steps. As a result of evaluation, the three-axis accelerometer fabricated with this technology showed improved performances as compared to integrated accelerometer with a larger CMOS design rule.

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