A SUBSTRATE-INDEPENDENT WAFER TRANSFER TECHNIQUE FOR SURFACE-MICROMACHINED DEVICES

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ABSTRACT

We report on a new wafer transfer technique that can remove and transfer surface-micromachined layers to application-specific substrates. This process, however, is not limited to only MEMS devices and can be applicable to other semiconductor devices. Successful transfer of a 1 cm x 1 cm MEMS chip with electrostatically actuated curled cantilever switches to a transparent quartz substrate has been demonstrated. Pull-in voltage for transferred devices is 31 V compared with 23 V for devices on standard silicon substrates.

Keywords: Wafer transfer, epitaxial liftoff, micromachining, fabrication

INTRODUCTION

Silicon has become the dominant semiconductor material in MEMS due to its excellent mechanical and thermal properties and compatibility with integrated circuit (IC) processes. However, an increasing number of applications demand MEMS devices fabricated on substrates other than silicon. For instance, high power devices require substrates with high thermal conductivity such as diamond or silicon carbide; optically transparent substrates comparable to quartz or sapphire are highly desirable in optical MEMS; lastly, RF and microwave applications necessitate semi-insulating substrates such as sapphire or semi-insulating GaAs. One approach is to fabricate MEMS devices monolithically on the desired substrate. However this technique is not usually compatible with standard processes nor is it cost effective for commercial applications.

Recently, there has been great interest in the integration of MEMS structures on dissimilar substrates. Batch transfer of bulk-micromachined structures have been demonstrated using dissolved wafer [1], flip-chip bonding [2-4], photoresist and photoresist-assisted bonding [5] techniques. However most have reported success in transferring only localized MEMS devices. Unlike previously reported techniques, our proposal involves the transferring of entire surface-micromachined layers onto various substrates. Additionally, our process works at room temperature and requires no heating during the actual bonding. This feature removes many problems caused by thermal expansion mismatches between differing materials. Our bonding process is independent of crystal orientation. Hence, in theory any target substrate can be bonded to device layers regardless of its chemistry or physical attribute, giving rise to a truly universal wafer transfer process.

FABRICATION DESIGN

Surface-Micromachining Process

Our wafer transfer process involves two phases. The first phase entails the fabrication of the MEMS cantilever switches by a standard surface micromachined process (multi-user MEMS Processes or MUMPs) at CRONOS. Figure 1 illustrates the corresponding layers of a surface-micromachined MUMPs process. A standard phosphorous-doped (100) silicon wafer is used as the

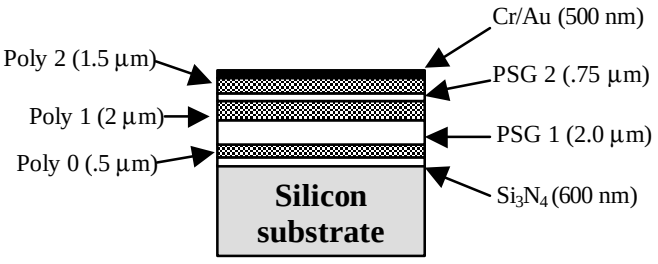

Figure 1: MUMPs process layers

host substrate. LPCVD nitride is then grown at a thickness of 600 nm to provide electrical isolation between the substrate and MEMS devices. The structural and sacrificial layers are comprised of polysilicon and polysilicate glass, respectively. Evaporation of 500-nm-thick chromium/gold provides the stress mismatch between the polysilicon and chromium for curling. MEMS cantilevers are finally shipped in 1 cm x 1cm die. Detailed designs and device characteristics of curled cantilever switches were reported in [6].

For RF applications, the thin nitride layer used to electrically isolate the conductive silicon substrate is not adequate to prevent parasitic losses and charge capacitance between the cantilever devices and substrate. To overcome this limitation, the substrate is removed and replaced by a insulating substrate.

Wafer Transfer Process

The actual wafer transfer is performed in house and involves the removal of the original silicon substrate, and then the reattachment of the device membrane onto a desired target chip. The process steps, from silicon removal to device release, are described in Fig. 2. Before any substrate removal, the MEMS chips are thoroughly cleaned and plasma enhanced chemical vapor deposition (PECVD) oxide is deposited over the top surface. A 1-μm-thick oxide will serve as a passivation layer over the devices to prevent any physical damage in subsequent processes. Following oxide deposition, Apiezon black wax is used to bond the chip onto a carrier wafer.

Apiezon black wax has proven to be reliable in previously reported epitaxial-liftoff procedure and thus we find no need to modify previous processes [7]. Besides providing strong adhesion, black wax imparts the necessary tensile stress onto the thin film to prevent the layers from inherently contracting during substrate removal.

After attaching the MUMPs chip onto a carrying wafer, the silicon substrate is selectively removed by a combination of lapping and XeF_2 etching, leaving behind a multilayered, chip-sized membrane of MEMS structures. A target wafer is placed over a clean membrane and is attached with adhesive. Pressure is applied over the chip to ensure maximal contact and the entire chip is left overnight to allow any solvent to evaporate from the interface. After a target substrate is securely bonded to the layers, black wax is removed in Opticlear (a less toxic organic solvent equivalent to TCE in removing wax) and the chip is released in 49% hydrofluoric acid (HF) for approximately five minutes. Silicon dioxide layers are selectively removed in the process. To reduce the risk of attack by HF upon the interface layer, photoresist is applied around the edges of the chip. We have shown that photoresist can withstand HF without peeling for at least 5 minutes. This provides sufficient protection to prevent any damage to the interface or membrane.

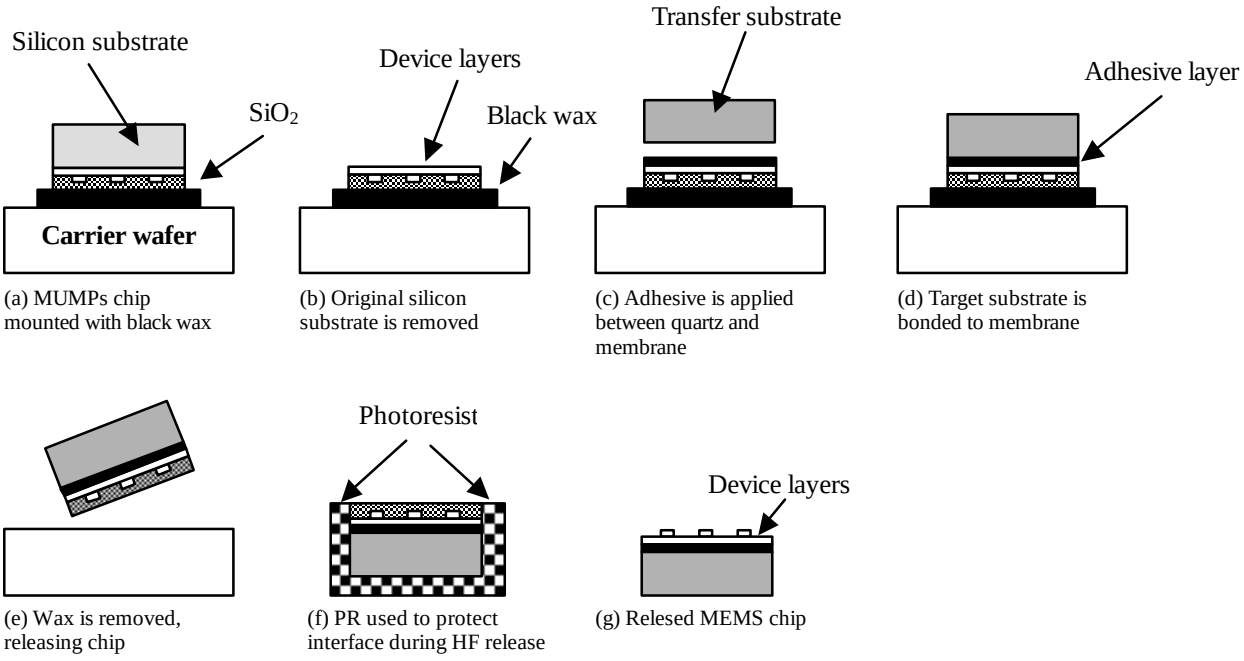

Figure 2: Wafer transfer processing steps

Residue

XeF_2 enchant is used for its high selectivity to silicon. However, we find that a by-product of XeF_2 etch is a residue over the entire membrane. These particulates have a size on the order of 1 μm. Residue density is observed to be greater at the corners of the chip than at the center; since XeF_2 is isotropic, the corners and sides are exposed to the gas for a longer time. The residue can have a detrimental effect on bonding between wafer and membrane. It can prevent close physical contact between device layers and target substrate. The residue can be removed with a thorough rinse in acetone followed by a 1 H_2SO_4: 1 H_2O_2 (piranha) clean. This clean removes most of the particulates and polymer. Figure 3 shows a membrane before and after an acetone-piranha clean. Even with an aggressive clean, the residue leaves an optical imprint on the membrane. We have determined that these optical fringes are a result of the difference in nitride thickness of the surrounding areas and the areas underneath the residue. Figure 3 also shows an inset of magnified fringes. During XeF_2 etch, areas under these particulates are shielded from the fluorine gas and remain thicker than surrounding areas. Judging from the color variation, we have approximated the discrepancy to be minor. We believe this minute variation in thickness will not obstruct our bonding process.

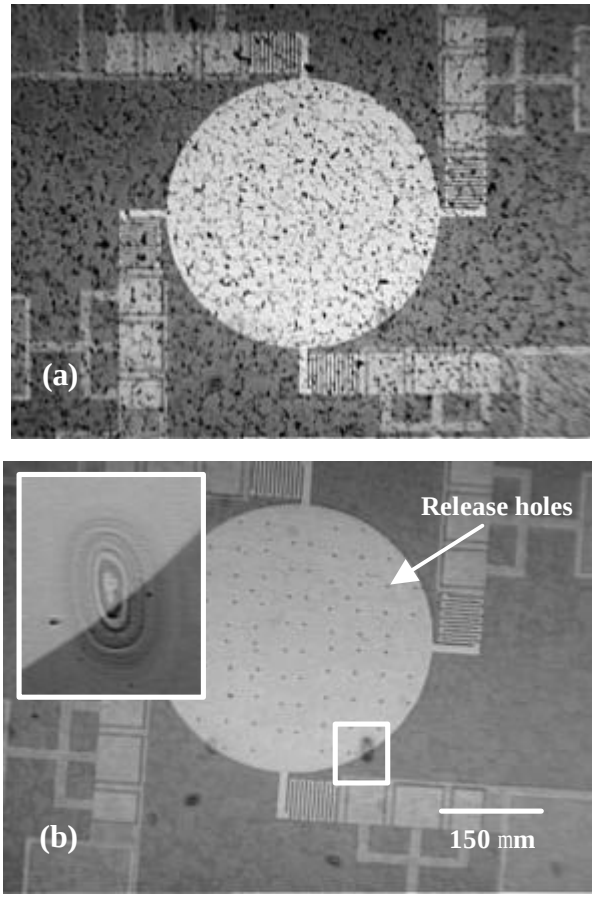

Figure 3: Before (a) and after (b) membrane cleaning

Bonding Techniques

Various options exist on how to bond a target substrate onto a thin membrane. Previous studies have reported using Van der Waals' forces in which the target substrate and epilayers are bonded in de-ionized water. As the water evaporates, Van der Waals' forces form between the new substrate and epitaxial layers [8]. Although this technique is simple and straightforward, the bonding is often too week for MEMS devices. Anodic bonding has also been mentioned and investigated as a viable bonding technique notably between silicon and glass [9]. Unfortunately the heat generated from anodic bonding is not desirable. One major challenge to our process is the membrane's sensitivity to temperature change. Due to the mismatch between the wax and membrane's thermal expansion coefficient, any slight temperature change can aggravate existing fractures as well as generate additional fractures within the membrane. This limitation dictates the use of room temperature bonding and eliminates the use of any form of epoxy resin that requires heating to fully polymerize the resin. In the process of finding a suitable bonding technique, we have accumulated and tested a list of various bonding techniques. While other forms of epoxies that can be cured at room temperature exist, many are prone to be attacked by HF.

Another bonding technique that is similar to Van der Waals' bonding is HF bonding [10]. Like Van der Waals' bonding HF bonding requires close contact between membrane and target wafer and can occur at room temperature. However, HF bonding takes the process one step further by making use of diluted HF between the membrane and wafer to chemically react with both surfaces to create silicon-oxide-silicon bonds. Given that the bond relies upon silicon oxide, the edges were covered with photoresist before release to prevent HF from attacking the interface. To further increase bonding strength, a layer of PECVD oxide can be deposited over the target wafer for use as an additional glue layer. HF bonding involves covalent bonds rather than relying upon weaker Van der Waals' forces. One major drawback with both methods is the need for an absolute particle-free surface on both membrane and wafer. We have found that sub-micron particles can prevent a complete bond.

After testing several bonding methods, we found that the reliability and durability of Norland Optic's UV epoxy has proven successful for our purpose. Although UV epoxy may be difficult to use with opaque substrate materials, its success in bonding membranes with glass, quartz, and sapphire substrate is proven. The transparence of these substrates greatly enhances the ease of curing the epoxy resin with UV exposure. Since UV curing is done at room temperature, we can avoid many problems associated with heat. UV epoxy provides an additional advantage of fast curing. Upon curing, UV epoxy can tolerate harsh solvents that are used in the release of the wax as well as HF acid during device release. Figure 4 shows a released device after transferred to a quartz substrate with UV epoxy.

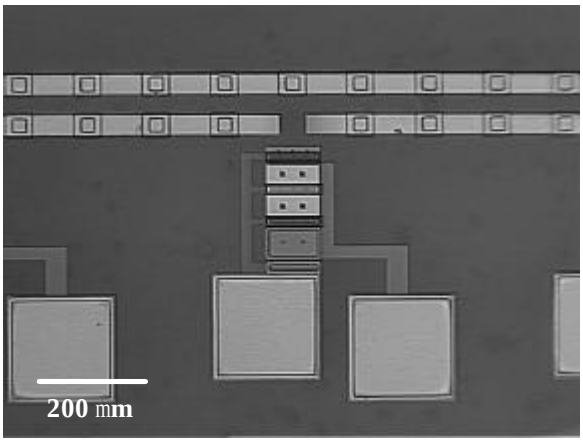

Figure 4: Optical microscope picture of a cantilever switch after HF release

Cracks

One major concern is the possibility of creating fractures within the membrane throughout the process. The nitride layer is inherently stressed during foundry processes. Subsequent in-house fabrication imposes additional stress to the layers. Cracks were seen throughout several processing steps. We have isolated several sources and determine possible solutions.

Cracks are inherently dependent upon MEMS design layout. Contact pads for ground connection are commonly used to electrically connect devices above the nitride layer to the silicon substrate. However, we observe that cracks can originate from these openings. In addition, these fissures tend to congregate at sharp corners. One obvious solution is omitting ground connections.

To reduce etching time and XeF_2 etchants, mechanical polishing was done on the silicon substrate to reduce its thickness. This too can impose additional strain on the membrane. Any scratches found on the reduced silicon substrate after lapping can translate to cracks upon substrate removal in XeF_2 etch.

MEASUREMENT

Electrical and mechanical measurements were performed to characterize the transferred devices. Comparisons were made between performances of transferred and controlled MEMS devices. Key features include frequency response and pull-in voltage. Normalized frequency response of cantilever devices on quartz and silicon are shown in Fig. 5. The graph does not show a resonant peak for both devices. Because of the small gap between the beam and ground plane, the cantilever can be modeled as an infinite plane. Frequency response is limited by squeeze film damping and resonant peak is not observed. Additional analysis on damping effects will be performed in the near future. The pull-in voltage of the transferred devices (31 V) is higher than that of the untransferred device (23 V).

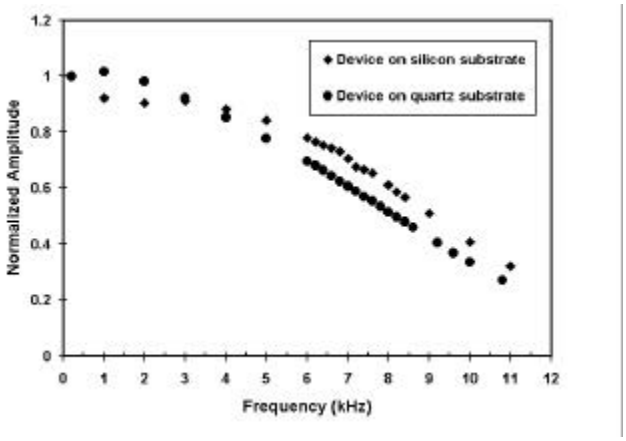

Figure 5: Frequency response of transferred switches

FUTURE CONSIDERATION

We will perform more extensive testing of the transferred devices to understand their electrical, mechanical, and thermal properties. We will continue to improve the etching and bonding processes that are compatible with the MEMS releasing process. We will also investigate MEMS design rules and their impact on wafer transfer processes.

CONCLUSION

We have successfully demonstrated a transfer of an entire MEMS device layer from a standard doped silicon substrate to a quartz substrate. Our bonding process is performed at room temperature and can be applied to different substrates. Electrical and mechanical performances of transferred devices were compared with those from devices on the original silicon substrate.

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REFERENCES

[1] T.E. Bell and K.D. Wise, "A dissolved wafer process using a porous silicon sacrificial layer and a lightly-doped bulk silicon etch-stop," *Proceedings MEMS '98*, Heidelberg, Germany, 25-29 Jan. 1998, pp.251-6.

[2] C.G. Keller, and R.T. Howe, "Hexsil Tweezers for Teleoperated Micro-Assembly," *Pro.s 1997 MEMS Workshop*, pp. 72-77, 1997

[3] A. Singh, D.A. Horsley, M. Cohn, A. Pisano, R.T. Howe, "Batch Transfer of Microstructures Using Flip-Chip Solder Bonding," *IEEE Journal of Microelectromechanical Systems*, pp. 27-33, 1999

[4] K.F. Harsh, W. Zhang, V.M. Bright, and Y.C. Lee, "Flip-Chip Assembly for Si-Based RF MEMS," Proc. MEMS '99, Orlando, Florida USA, Jan 1999, pp. 273-278.

[5] T. Akiyama, U. Staufer, and N. Rooij, "Wafer- and Piece-Wise Si Tip Transfer Technologies for Applications in Scanning Probe Microscopy," *IEEE Journal of Microelectromechanical Systems*, pp. 65-70, 1999

[6] R.T. Chen, H. Nguyen, and M.C. Wu, "A low voltage micromachined optical switch by stress induced bending," *Proc. 1999 MEMS Conference*, pp. 424-428, Orlando, Florida, U.S.A. Jan. 1999.

[7] A. Ersen, I. Schnitzer, E. Yablonovitch, and T. Gmitter, "Direct bonding of GaAs films on silicon circuits by epitaxial liftoff," *Solid-State Electronics*, vol.36, pp.1731-9, 1993.

[8] P. Demeester, I. Pollentier, P. De Dobbelaere, C. Brys, and P. Van Daele, "Epitaxial Lift-off and Its Applications," *Semiconductor Science Technology*, vol. 8, pp. 1124-1135, 1993

[9] W. H. Ko, J. T. Suminto, G. J. Yeh, "Micromachining and Micro-packaging for Transducers," *Elsevier Science Publishers*, 1985

[10] H, Nakanishi, T. Nishimoto, R. Nakamura, A. Yotsumoto, and S. Shoji, "Studies on SiO/sub 2/-SiO/sub 2/ bonding with hydrofluoric acid-room temperature and low stress bonding technique for MEMS," *Proc. 1998 MEMS Conference*, pp. 609-614, Heidelberg, Germany, 25-29 Jan. 1998.