IN SITU CHARACTERIZATION OF CMOS POST-PROCESS MICROMACHINING

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ABSTRACT

We have developed and demonstrated a new methodology for *in situ* monitoring and characterization of CMOS post-process micromachining utilizing integrated circuits and micromachine test-structures. In our demonstration, the circuits provide automated readout of N-well resistors surrounding each of the 140 test pit structures at up to 14,000 samples per second per device during the post-process silicon etch, and thus also provide etch progress and end point determination without extra analytical equipment. Pit sizes, surrounding layers, and topology are examined with this technique.

INTRODUCTION

Many MEMS devices utilize specialized processes and equipment and so require the MEMS designer to have access to a fabrication facility. This causes the process design to be tightly coupled to the design of the entire device. In contrast, integrated circuit processes have seen widespread use due to foundry services and looser coupling between circuit design and process design. To provide such capabilities to MEMS designers, CMOS post-processing was developed[1] to allow those without a fab to do micromachining with a single maskless post-processing step on standard foundry CMOS, thus requiring very little extra equipment. This method relies on the ability to stack the contact, via, and overglass cut layers (figure I) to yield exposed silicon when the chip returns from the foundry, which can then be sacrificially etched by Si etchants such as xenon difluoride (XeF_2)[2], tetramethylammonium hydroxide (TMAH), and ethylenediamine-pyrocatechol (EDP)[3] with the oxide acting as the mask and structural layer. This technique has been used to create a wide variety of devices including accelerometers[4], microwave power sensors[3], higher-Q spiral inductors[5], heart-cell transducers[6], thermal sensors[7], and thermally isolated circuits[8]. Although this method does not work in submicron processes that use tungsten plugs in the vias, it is still useful in the older, less expensive processes.

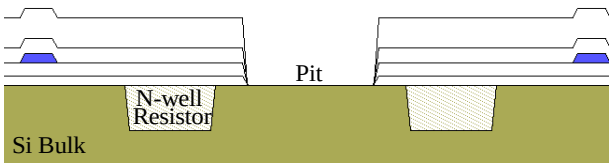

Figure I: *Cross-section of the basic pit cell in figure III showing the N-well resistor used to detect etch progression. The cross-sections in this paper were made with L-Edit 7.3 in the Tanner MEMS-Pro 1.5 suite.[12]*

One problem with this approach is that it violates the design rules in such CMOS processes, so the results are not guaranteed. J. Marshall *et al* [9] at the National Institute of Standards and Technology (NIST) did work to develop a set of design rules for this method in the Orbit 2μm process available through the MOSIS Service[10]. At the time that this characterization was taking place, the process technicians at Orbit were discovering that the vias and overglass cuts were not clearing, so they performed overetches and overexposures until they did clear, not realizing that these were actually micromachining pits that violated the design rules. Because of the success of these runs, NIST published their design rules. However, the circuit designers that used the Orbit process began to complain that their pads and vias were being overetched, so Orbit stopped performing the extra steps that ensured the pits cleared. With the process now changed, the design rules were no longer valid. A further problem was that the processing of the pits was not longer consistent, so another attempt at making design rules was not made.[11]

The primary issue in properly fabricating the pits is that the resulting abrupt topography can prevent proper development of the photoresist that ends up in them during subsequent processing steps, leaving SiO_2 and Al residue in the corners of the pits (figure II), which can moderate etching or even prevent it when the pit is filled. The minimum size of pit that will not be plugged depends on several factors, including local topography, the surrounding layers, and orientation. It varies from run to run due to changes in die placement on the wafer and process variations. To quantify the effects of these factors, a set of 140 test pits was designed, along with a readout circuit to ease measurement. Tea *et al* [3] previ-

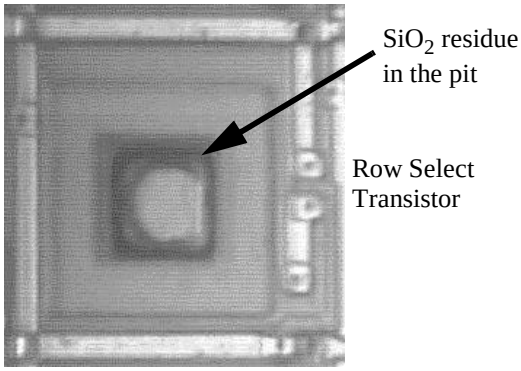

Figure II: *Photomicrograph of a square pit surrounded by poly1 showing the problematic pit residue.*

ously described the use of n-diffusion resistors to determine completion of the XeF_2 Si etch. We have extended this technique by utilizing the CMOS circuit capability to monitor the etch at many more etch fronts throughout the post-process, and to provide characterization of the preceding CMOS fabrication process.

PIT DESIGN

The basic pit cell (figure III) consists of a pit surrounded by an N-well resistor that is progressively destroyed as the etch progresses. The resistance is nominally 14.4kΩ, but as the etch front moves out from the pit and gradually destroys the resistor, the resistance will increase until the resistor has been totally destroyed.

The right-hand half of the array varies the size of the pit from 5µm to 30µm in 5µm increments along each row. Up each column, the stack of layers surrounding the pit varies from just the oxide films (figure I) to various combinations of the dielectrics and poly1, poly2, metal1, and metal2 (figure IV) in order to find out how increasing the thickness of the region surrounding the pit at various points in the process affects the resulting amount of exposed silicon.

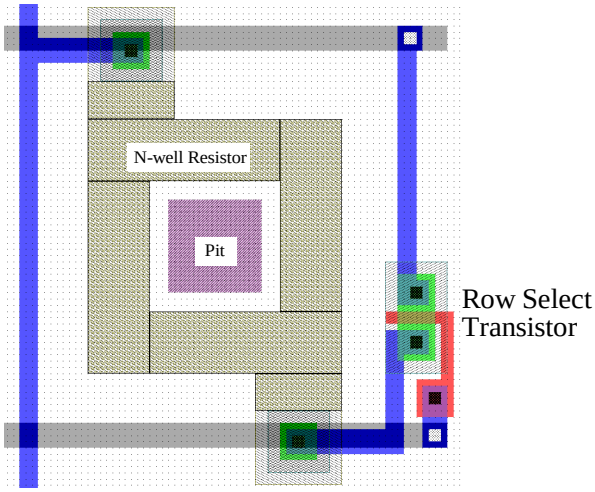

Figure III:*Layout of a the basic CMOS pit cell showing a 15x15µm pit surrounded by the N-well resistor, the row select transistor, and the access wiring.*

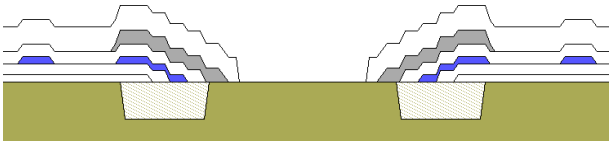

Figure V: *This pit is surrounded by metals 1 and 2, yielding increased topology, and utilizes a gradual pit cut to ease the processing requirements. This approach is often used in dicing streets.*

In an attempt to make the pits more manufacturable, the left-hand half of the array provides a slope to the edge of the pits by adjusting the hole size on each layer such that the overglass cut is 15µm across and holes in underlying layers are progressively larger (figure V, VI). Thus, the topographical changes are more gradual and the film being removed is always on a nominally flat region, factors which were expected to increase the minimum size hole that can be patterned. This approach is often used in dicing streets. Across each row the differential hole

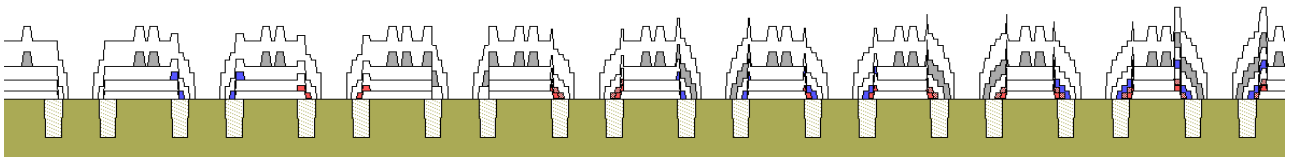

Figure IV: *Cross-section through a column of 15x15µm pits showing the variation in layers surrounding the pit.*

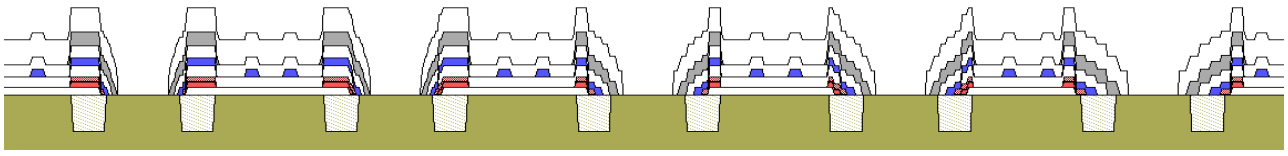

Figure VI: *Cross-section through part of a row of pits showing the variation in the slope to the pit as in figure V. These pits are surrounded by both polysilicon and both metallization layers.*

size from layer to layer is increased from 2µm to 8µm in 2µm steps. Within each column the stack of layers surrounding the pit is adjusted similarly to the right-hand half of the array.

CIRCUIT DESIGN

Since the post-processing is performed on fully functional CMOS circuits and allows electrical feedthoughs, it was realized that on chip circuits could be put to work automatically measuring the test pits. This capability greatly reduces the amount of work necessary to examine the 140 pits and facilitates the use of this structure in monitoring run to run variations, just as one would automatically monitor electrical device variations. The readout circuitry requires five electrical feedthroughs on the etch chamber: Vdd, GND, Clock, Reset-, and Output. The clock signal is first converted to a non-overlapping two phase clock, as the circuit utilizes the pseudo-static logic style of flip-flops. The core of the circuit consists of two circular pointers, the first of which drives each column in turn, while the second drives each successive row as the column pointer passes from the last to first column (figure VII). Each column pointer cell has a digital buffer that acts as a current source driving the N-well resistors in the column. The row pointer cells then control n-channel pass transistors connected to each resistor of the row so that the current from the column driver only flows through the resistor in the current selected row. The source of all the pass transistors are connected so that there is a single output from the array. In this manner, each element of the 14x10 array is driven in succession, yielding an output current that is dependent on the resistance of the N-well resistor surrounding the pit. As the etch front progresses through the resistor, the resistance increases until the element is open-circuited, resulting in zero output current.

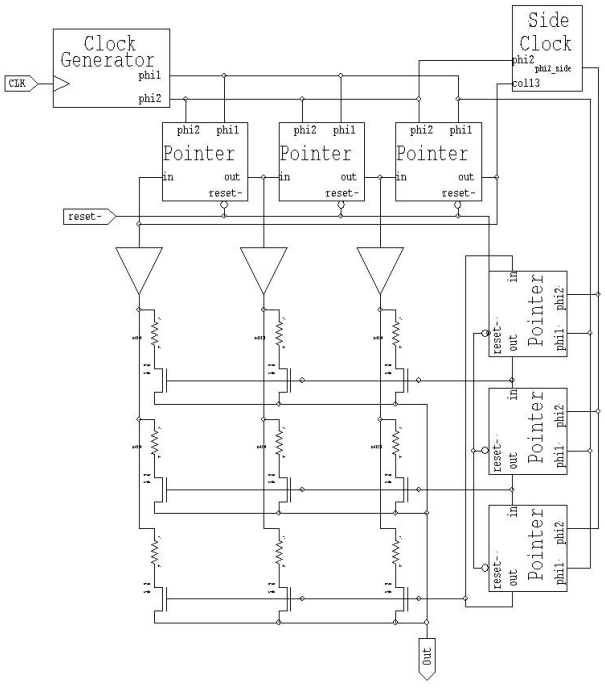

Figure VII: *Circuit schematic for a partial 3x3 pit array. The circuit contains two circular pointers that repetitively scan the entire array according to the clock. Each pit in the array is surrounded by an N-well resistor that is destroyed during etching. The circuit outputs a current proportional to the resistance of the selected pit's resistor and operates between 30 Hz and 2 MHz, but typical operation would be from 100Hz to 1kHz.*

MEASUREMENTS

The system has been fabricated through the MOSIS Service in the Orbit 2µm CMOS process (figure VIII), which has two polysilicon layers and two metal layers. The die was epoxied to a ceramic package, wirebonded, and inserted into a breadboard that provided connections to the electrical feedthroughs on the XeF_2 etching chamber. Since many such chambers include an acrylic viewing port to allow visual inspection of the etch progress, this window had to be rendered opaque to eliminate photogenerated carriers.

With a 50% duty cycle clock, the circuit can operate between 30Hz and 2MHz. XeF_2 is a fast etchant at up to 15µm/min[2], so to watch the etch progress through a 10µm resistor, we would want 1-10 scans of the array per second. Thus, the circuit would typically operate between 100Hz and 1kHz. The circuit can also be operated at lower clock rates as long as the clock low time is kept below 17ms; otherwise, some of the nodes in the pseudo-static logic circuit will discharge too far.

A computer with a data acquisition card and LabVIEW[13] generates the input signals for the circuit and measures the voltage dropped across a 470Ω resistor,

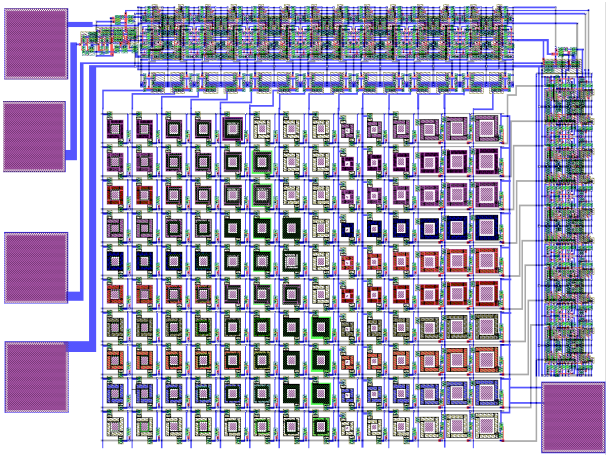

Figure VIII: *Layout of the full circuit and pit array for the Orbit 2µm process. Only five connections are necessary: GND, Vdd, Reset-, Clock, and Out.*

allowing easy correlation between the pit currently being measured and its output. The LabVIEW Virtual Instrument we created (figure IX) shows the circuit output in a strip chart mode and on an intensity chart where the *y* axis is the element of the array, the *x* axis is time, and the color of the point corresponds to the output value. The latter chart provides a clear, succinct picture of the status of the etch for each pit and thus can also be used as an end-point determination. A second Virtual Instrument reads the data files generated by the first Virtual Instrument, reformats the data into the 14x10 array, and generates an animated intensity graph, allowing one to see the progress of the etch across the array, quickly see how the variations in the parameters affect the etch time, and filter out crosstalk between pits.

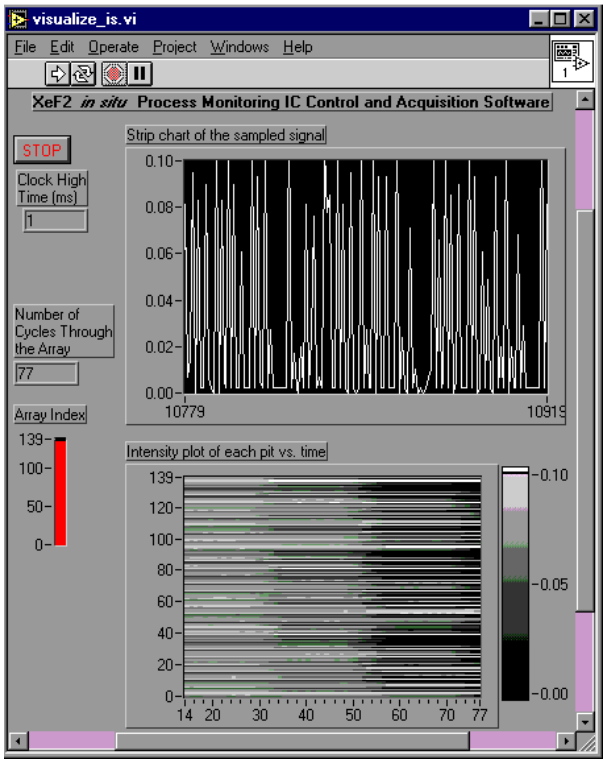

Figure IX: *Screen capture of the LabVIEW Virtual Instrument that generates the clock and reset signals to drive the circuit and reads the resulting output as the array is scanned. The top chart is a strip chart representation of the data coming directly out of the circuit for one entire scan of the array. The bottom chart is an intensity chart where the data from the top chart has been demultiplexed into individual pits such that the* y *axis represents the pit number, the* x *axis represents the number of the cycle through the array, and intensity is the relative value at the output. This capture was taken towards the end of the etch when a good number of pits have been etched through, giving a zero output. The bottom chart shows the pit signals gradually fading out, allowing rapid visualization of the large amount of data present being gathered.*

A photomicrograph of the fabricated circuit after etching (figure X) clearly shows the difference in etch progression among the various elements of the array. Figure XI shows the output waveforms for the first row of the array at several times during the etch. The first cycle is before the etch has started, showing small variations in the output current due to process-induced differences in the N-well resistance. The later cycles show the output changing as the resistors are etched, until after 230 cycles most of them are removed. Figure XII shows the waveforms

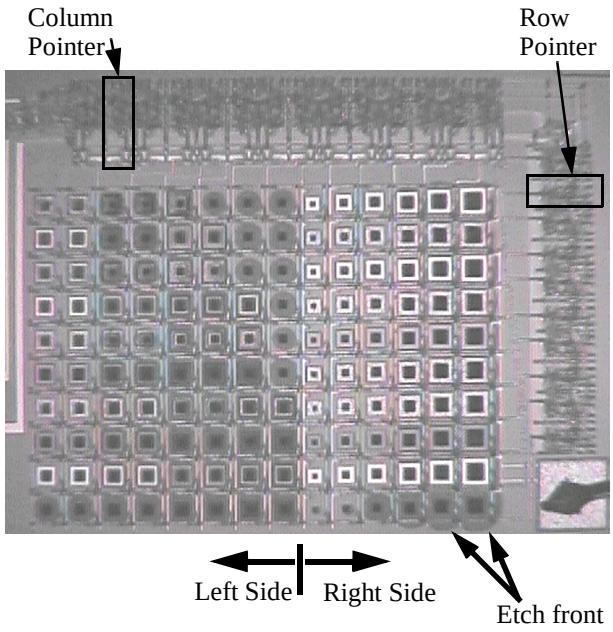

Figure X: *Photomicrograph of the circuit after the post-process XeF_2 etch. Note the different amounts of undercut for each type of pit.*

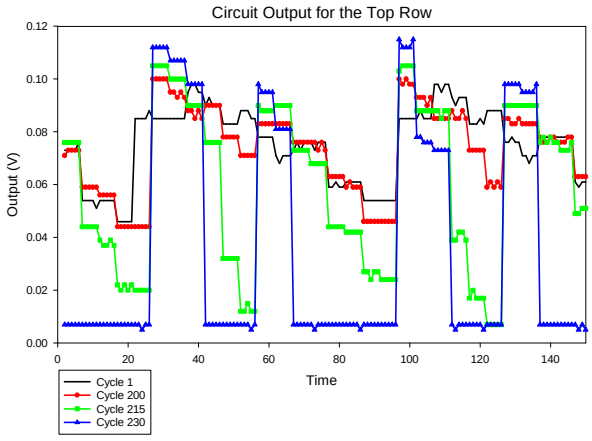

Figure XI: *Output waveforms for the first row of the test pit array at several times during the etch. Cycle 1 is before the etch, showing small variations due to the process-variation-induced differences in the N well resistance. The later cycles show the output changing as the resistors are etched, until at cycle 230 most of them*

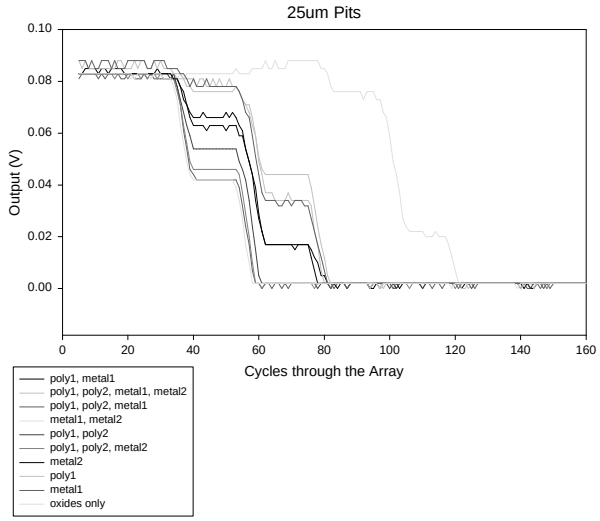

Figure XII: *Demultiplexed data for the column of 25µm pits with one curve per pit, showing that the pits etch at different times.*

from each of the 25µm pits, yielding different etch times. The steps in the waveforms are due to the pulsed nature of the etch[2]. Unfortunately, there are some aspects of the data that can not currently be explained, preventing a conclusive set of results for the various pits from being presented.

CONCLUSION

We have demonstrated a new methodology for *in situ* monitoring and characterization of the foundry CMOS used for post-process CMOS micromachining and the post-process etching itself. The on chip circuits allow a large number of structures to be measured automatically as the etch is proceeding and provide end point determination. This technique allows design guidelines to be developed as to the smallest pit that will be open for a given set of layers surrounding the pit. In addition, new styles of pits that reduce the abrupt topologies have been tested.

ACKNOWLEDGMENTS

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