METAL FILM PROTECTION OF CMOS WAFERS AGAINST KOH

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ABSTRACT

This paper reports a new protection for the front side of fully processed CMOS wafers against KOH etching solutions. The protection is based on thin TiW and Au films and is fully CMOS compatible. No mechanical fixture is required during the anisotropic etching step. Therefore, the new method is excellently suited for batch micromachining. Up to 100% of all chips on 6 inch wafers were fully operational after 4 hours KOH etching. The membrane yield after KOH etching was 100% and nearly 90% after the not yet optimized removal of the protection films. Thus, this protection fulfills the requirements of inexpensive and reliable sensor production.

INTRODUCTION

Protection of the front of fully processed CMOS wafers has been a constant concern with KOH etching. KOH heavily attacks the aluminum metallizations during micromachining of microsensors based on CMOS thin film membranes. The most widely used method to protect the front of fully processed wafers employs mechanical fixtures. Such fixtures, made from stainless steel or Teflon, allow the back of the wafer to be in contact with the KOH while protecting the wafer front [1]. Reliable etching of processed CMOS wafers is possible with this method. However, these fixtures prevent batch processing which raises production costs. Recently, protection schemes based on thin films were reported [2, 3]. These approaches are not compatible with gold bumping used in membrane-based sensor production [4]. Thin Au films deposited on the front of silicon wafers were reported as cathode for galvanic cell formation in contactless electrochemical etching [5]. However, only experiments with TMAH were successful, where no protection of the wafer is required because TMAH can be tuned not to attack aluminum. Attempts with gold films as protection against KOH failed [6].

For the first time, this paper reports on yield issues of thin metal films as protection against KOH. Two aspects of the yield can be distinguished. First, the metal film has to protect the front of fully CMOS processed wafers during the whole etching time with high yield. Second, high yield of the fragile membranes must not be hindered by the stresses introduced by the metal protection film. Further, the metal film must be easily removable without affecting the membrane yield. Both aspects are treated in this paper.

PROTECTION SCHEME

The new protection scheme is based on the bumping service commercially offered by EM Microelectronic-Marin SA (EM), Marin, Switzerland [7]. The bumping process is usually intended for the fabrication of electrical connections of IC chips in tape automated bonding. It starts after the regular CMOS process (Figure 1) with the sputtering of a TiW diffusion barrier and an Au plating seed layer onto the whole wafer. After that, photolithography with a thick photoresist is performed, defining size and position of the bumps. The gold bumps are formed by electroplating using the thick resist layer as plating mold and the Au plating seed layer as electrical contact. After the removal of the resist (Figure 2), the standard bumping process finishes with the back etching of the TiW and Au plating seed layers. In the previous art [4], KOH etching is done at this time with a mechanical etching fixture. In our new approach, the KOH etching step is performed before the diffusion barrier and the seed layer are removed. Thus, the diffusion barrier and the plating seed layers serve as a protection during the KOH etching and are removed afterwards (Figure 3).

EXPERIMENTAL

As protection coatings the diffusion barrier and the Au plating seed layers have to fulfill further tasks. The Au plating seed layer should be pinholefree in order to prevent the KOH from reaching the wafer surface. Because Au layers only adhere weakly on silicon wafers, the diffusion barrier layer must guarantee a good adhesion between the wafer front and

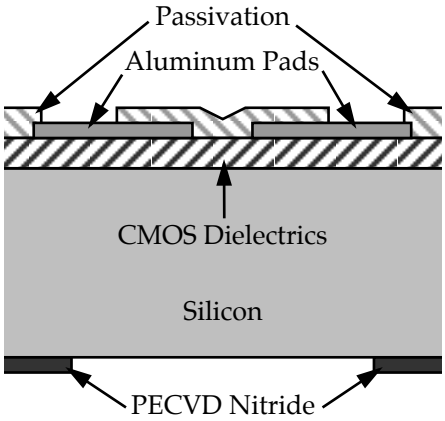

Figure 1: Schematic view of a wafer section after the complete CMOS process. Additionally, a silicon nitride layer serving as a KOH etch mask is deposited and structured on the wafer back.

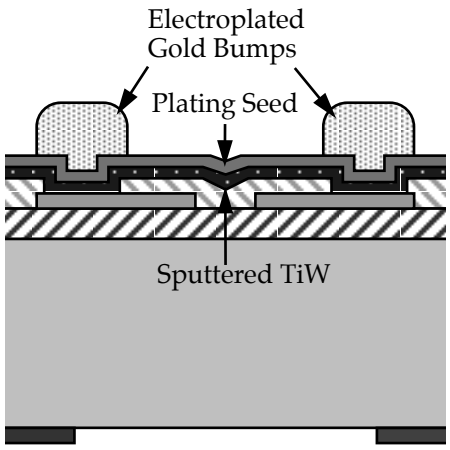

Figure 2: Schematic view of a wafer section after the bumping process. The gold bumps are formed by electroplating using a thick resist layer as plating mold.

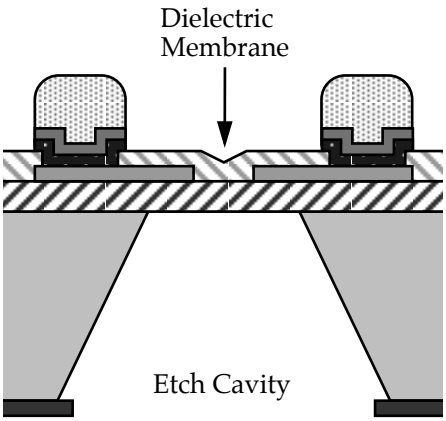

Figure 3: Schematic view of a wafer section after a 4 hour KOH etch at 95°C. A membrane consisting of the CMOS dielectrics has been released. The diffusion barrier and the plating seed layer are removed in the same way as with the standard bumping process.

the plating seed layer. Furthermore, it should be resistant against KOH in case KOH penetrates the Au layer via a pinhole.

We investigated the effect of the diffusion barrier and plating seed layers on the process yield. First, we analyzed different diffusion barrier metals in terms of etch rate in KOH, stress, adhesion, and yield after KOH etching. In particular, we concentrated on Ti, TiW, TiW:N (nitride rich TiW), and TiN diffusion barriers readily available at EM. The thicknesses of these diffusion barriers were between 0.1 and 0.3 μm. To guarantee a clean surface and a good adhesion, the deposition of the diffusion barriers were preceded by a cleaning step and a dehydration bake. The cleaning was performed in the organic solvent PRS3000 from J. T. Baker for 20 minutes at 80°C and for 20 minutes at room temperature in an ultrasonic bath. Afterwards, the wafers were dehydrated using a 400°C bake in nitrogen. Second, we optimized the plating seed layer in terms of deposition method, thermal treatment, and thickness. To assess the efficiency of the different protection schemes, we deposited the appropriate layers on fully processed six inch wafers which were immersed in a 27 weight-% KOH solution at a temperature of 95°C.

RESULTS

A first test for possible diffusion layers is their etch rate in KOH. In Table 1, the etch rates in 95°C KOH as well as the stress of Ti, TiW, TiW:N, and TiN films are summarized. The etch rates were determined for 95°C KOH. The thicknesses were measured before and after KOH immersion via resistivity measurements. For the stress measurements the layers were deposited on silicon oxide and the stress was measured with the wafer curvature method. Two TiW layers deposited by two different sputtering systems, which will be called A and B in the following, were investigated. The TiW:N layer was obtained by annealing the TiW

Diffusion barrier	Etch rate (nm/h)	Stress (MPa)
Ti	804	not measured
$TiW_{System\ A}$	40	-306
$TiW{:}N_{System\ A}$	27	-383
$TiW_{System\ B}$	17	-950
TiN	12	-868

Table 1: Etch rate and stress of different diffusion barriers. The etch rates were determined for 95°C KOH via resistivity measurements. The stress was measured with the wafer curvature method.

layer deposited by the sputter system A at 400°C in a nitrogen atmosphere. During this annealing step, free Ti-atoms in the TiW layer react with the ambient nitrogen to form TiN. Accordingly, the color of the TiW layer changed from silver to light brown typical for TiN layers. The etching rates for TiW, TiW:N, and TiN are all in the range of tens of nanometer per hour. The etching rate of the Ti film is nearly 1 μm/h which is too high for a single diffusion barrier. However, Ti layers were used as an additional adhesion layer in layer sandwiches because of their good step coverage.

In Table 2, the adhesion values of TiW films deposited by the sputtering systems A and B and a TiN film deposited by a sputtering system C on silicon, silicon oxynitride, and aluminum are summarized. The values were determined by a scratch test under progressive loading [8]. The forces leading to a complete delamination of the diffusion barrier on silicon and aluminum and to a rupture of the diffusion barrier on silicon oxynitride are given in the Table.

	Adhesion (N) on		
Diffusion barrier	Si	SiON	Al
$TiW_{System\ A}$	5.10	7.82	3.05
$TiW_{System\ B}$	7.70	7.15	5.56
TiN	19.73	15.53	10.40

Table 2: Results of a scratch test under progressive loading. The force at which a full delamination or rupture occurs is a measure of the film adhesion on the substrate.

TiN films show the best adhesion on all three substrate materials. Because TiN films also exhibited the lowest etch rates in KOH, they are the most prominent candidates as diffusion barrier.

Table 3 shows the surface integrity results after KOH etching for the different diffusion barriers. Since the combination of diffusion barrier and plating seed is decisive, we analyzed the diffusion barrier in combination with a seed layer consisting of a 0.1 μm thick sputtered Au layer and a 0.7 μm thick electroplated Au layer. The layers were deposited on processed 6" wafers and immersed in KOH for 2 hours. Afterwards, the wafer surface integrity was inspected optically. Wafers with a poor surface integrity showed delayering of large surface areas readily visible with the eye. Those with a fair surface integrity showed delayering visible with the eye and those with a good surface integrity showed small defects only visible with a microscope.

The best results were obtained with the TiW diffusion barrier layers deposited by the two different

Diffusion barrier layer	Surface integrity
$TiN_{0.1\mu m}$	fair
$Ti_{0.03\mu m}TiN_{0.1\ \mu m}$	poor
$TiN_{0.1\ \mu m}Ti_{0.1\ \mu m}TiN_{0.1\ \mu m}$	fair
$TiW_{0.3\ \mu m,\ System\ A}$	good
$TiW{:}N_{0.3\ \mu m,\ System\ A}$	good
$Ti_{0.02\mu m}TiW_{0.3\mu m,\ System\ A}$	poor
$TiW_{0.3\mu m,\ System\ B}$	good
$TiW{:}N_{0.3\mu m,\ System\ B}$	poor

Table 3: Surface integrity for different diffusion barrier layers after two hours in 95°C KOH. The TiW layers were deposited by two different sputtering systems A and B.

sputtering systems and the TiW:N layer deposited with sputter system A. Additional Ti layers were deposited to increase step coverage and adhesion. However, the resulting surface integrity was deteriorated by adding a Ti layer, probably due to the high etch rate of Ti in KOH leading to a fast delayering. The TiW:N layer from system B obtained by sputtering in an argon-nitrogen environment does not lead to satisfactory results. The thickness of the TiN layers was restricted to 0.1 μm due to a recommendation of the sputter equipment supplier to avoid possible particle formation. Due to the low etch rate and the good adhesion of TiN layers, future work will concentrate on depositing thicker TiN layers.

Two deposition methods of Au plating seed layers were analyzed: (a) a single sputtered Au layer and (b) a Au layer sandwich consisting of a 0.1 μm sputtered Au layer with an electroplated Au layer on top of the sputtered layer over the whole wafer surface. This gold layer sandwich can also serve as a plating seed layer. For the same total gold thickness of 0.5 μm we found a much better protection using the sandwich of sputtered and electroplated gold layers. No change in resistivity was measured after an one hour immersion in KOH at 95°C indicating negligible etch rates of Au layers for the two deposition methods. Thus, we suppose that electroplating yields denser films. After a 300°C anneal of one hour, the protection quality of both plating seed layers decreased drastically. High temperature steps cause an increased Au grain size, thus forming small channels through which the KOH can reach the wafer surface.

We tested the protection efficiency of the diffusion barrier and Au layer sandwich for different thicknesses of the electroplated gold layer. The appropriate layers were deposited on fully processed CMOS wafers with a chip size of 5.65 by 4.35 mm^2.

These wafers were immersed in KOH at 95°C for 4 hours which is sufficient to release membranes on 600 μm thick 6" wafers. Subsequently, the chips not attacked by the KOH were counted and the resulting chip yield was calculated. Chips even with only one defect small compared to the chip size were rated defect.

Of course, the chip yield depends on the chip size and will generally increase with smaller chip sizes. But it is the only realistic industrial yield test accounting for every defect on a chip. An other measure of the protection efficiency would be the surface integrity yield. However, it is very difficult to measure and generally gives to optimistic values. E.g., the chip yield for 0.7 μm electroplated Au on the diffusion barrier deposited with system B (see Figure 4) of approximately 85% corresponds to a surface integrity yield of approximately 99%.

Figure 4 shows the chip yield as a function of the plated Au thickness for the three different diffusion barriers showing good results in Table 3. A 0.1 μm sputtered gold film was used as plating seed for the Au layer electroplated over the whole wafer surface.

Generally, the chip yield increases with increasing electroplated Au thickness. Furthermore, the chip yield depends on the sputter equipment used for the diffusion barrier deposition. The best results were achieved with the TiW layer deposited by the sputter system A. The difference in chip yield between the sputter systems A and B is due to particle formation. Figure 5 shows a SEM image of a

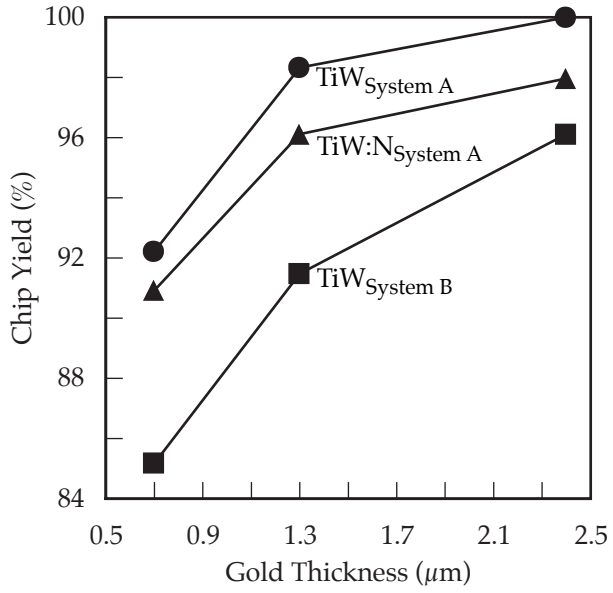

Figure 4: Chip yield as a function of plated gold thickness for three 0.3 μm thick diffusion barrier layers.

particle leading to a delayering of the diffusion barrier and plating seed deposited by system B. Two reasons explain the higher particle density in the layers deposited by sputter system B. First, system B is installed in a class 100 clean room, whereas system A is installed in a class 1 clean room. Second, TiW sputter processes are known for their particle susceptibility due to a flaking off of Ti dendrites from the sputter target [9]. System A uses a sputter sideways technique which is optimally suited for this kind of application since the flakes are generally falling down between sputter target and wafer. System B uses a sputter downwards technique eventually leading to Ti flakes falling onto the wafer. The difference between the TiW and TiW:N layer deposited by sputter system A cannot be explained since the incorporation of nitrogen atoms into the TiW layer reduced the etch rate and was expected to improve the adhesion according to Tables 1 and 2 and, thus, the chip yield.

A beneficial side effect of the protection with electroplated layers is the possibility to plate around the wafer edge. This way, the wafer edge is protected and not attacked during KOH etching. We found a better edge protection with thicker Au layers. For a plated Au thickness of 2.4 μm and a TiW layer deposited by system A without annealing, the wafer edge was nearly 100% intact after 4 hours KOH etching.

We tried to further improve the protection efficiency by etching at a lower temperature. The chip yield results for the TiW:N layer deposited by system A are shown in Figure 6. The chip yield decreased for the lower etch temperature. In the case of the 0.7 μm electroplated Au layer etched at

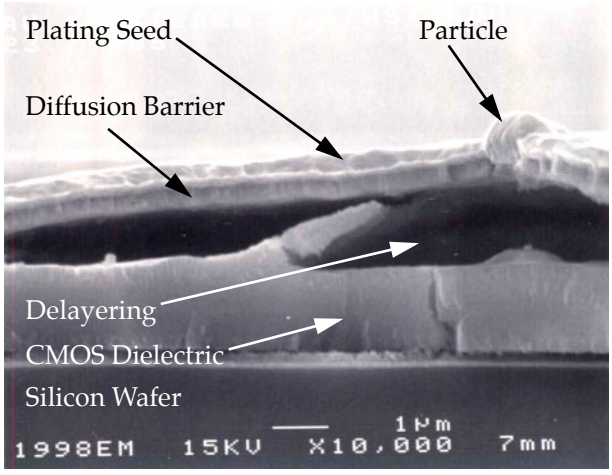

Figure 5: Delayering of the diffusion barrier and the plating seed layer due to a particle. The particle causes an irregular sputter result which promotes the penetration of KOH onto the wafer front.

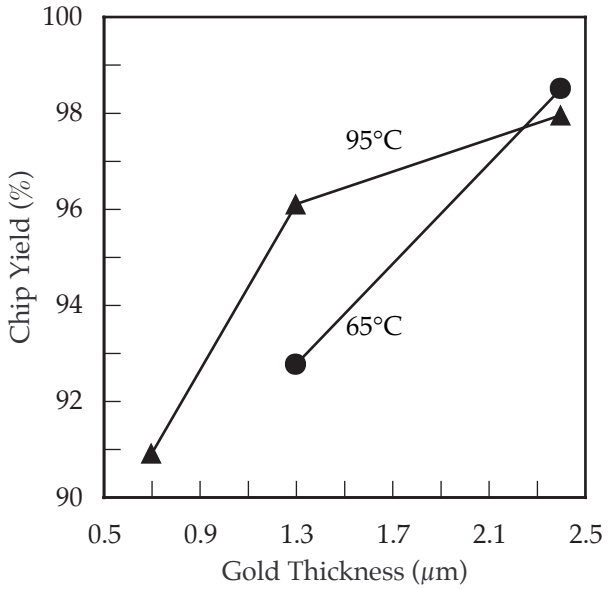

Figure 6: Chip yield as a function of plated gold thickness for the same TiW:N layer of System A. The KOH etching temperatures were 65°C and 95°C.

65°C, the protection layers delayered from whole chips, which points to a reduced adhesion, and prevented an thorough yield analysis. What can be said is that the yield in this case was considerably lower than the 91% found for the same protection layers etched at 95°C.

Finally, membranes consisting of the CMOS dielectrics were released by KOH etching with the wafer front protected by a 1.2 μm electroplated Au layer as shown in Figure 7. We found a membrane yield of exactly 100% for over 1500 membranes with sizes ranging from 350 by 550 μm^2 to 875 by 1550 μm^2. The protection layer consisted of a sandwich of 0.3 μm TiW:N with a stress of -383 MPa, 0.1 μm sputtered gold with a stress of 134 MPa and 1.2 μm electroplated Au with a stress of 39 MPa. The layer sandwich introduced an additional average compressive stress of -34 MPa on the membrane. The protection layers were back etched using the spray etcher/rinser used in the standard bumping process. After the removal of the layers, the membrane yield was 89.3%. The reason for this reduced yield is the overall compressive stress in the CMOS dielectric layers leading to fragile buckled membranes. Some of the membranes were destroyed by the liquid jets in the spray etcher/rinser hitting the buckled membranes. This is indicated by the fact, that the destroyed membranes were mainly found along the wafer perimeter. In the spray etcher/rinser, the wafers are located closely together. Consequently, the membranes in the middle of the wafers are geometrically shielded by the other wafers from the liquid jets. An intact membrane is shown in Figure 8. The micrograph was taken using Nomarsky photography. The membrane is buckled due to the compressive stresses in the CMOS dielectrics. In future work, a passivation will be used which compensates the compressive stress in the dielectrics to obtain flat and more stable membranes [10]. Furthermore, the pressure of the etching liquid jet will be reduced. These two measures will lead to a higher membrane yield after the removal of the protection layers.

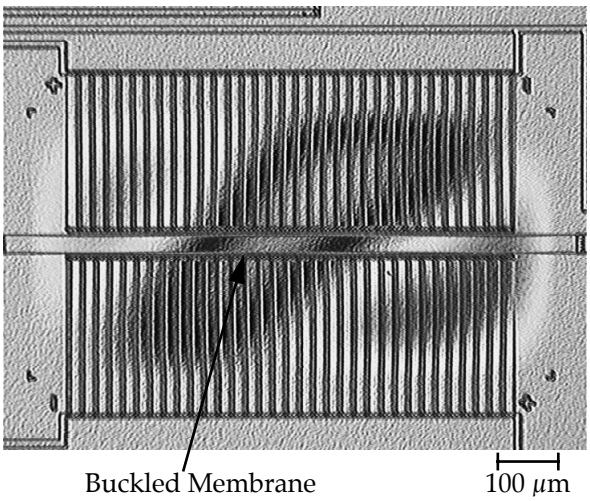

Figure 7: Micrograph taken with Nomarsky photography after the KOH etch with diffusion barrier and plating seed layers not removed. The buckled membrane as well as the rough gold structure are clearly visible. The membrane size is 1050 by 550 μm^2.

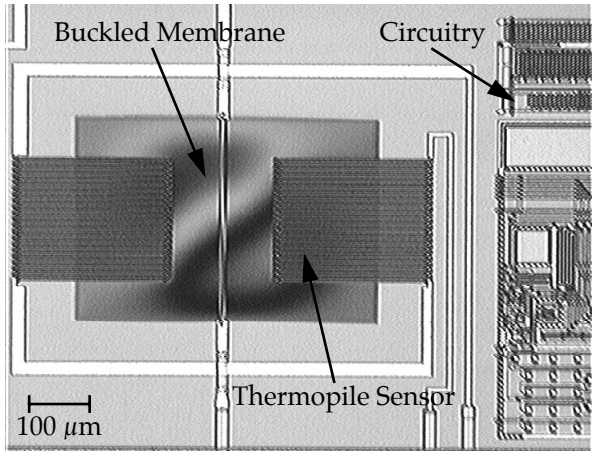

Figure 8: Micrograph taken with Nomarsky photography after the removal of the protection layer. The membrane is still intact although it is buckled. The membrane size is 350 by 550 μm^2. The circuitry does not show any defects.

Conclusion and Outlook

We presented a fabrication technology for batch bulk micromachining of 6" wafers. The technology is based on a commercially offered gold bumping process. Chip and membrane yields of up to 100% were achieved. Future work will concentrate on the use of TiN as a diffusion barrier and on improving the membrane yield during the etch back of the protection layers. Furthermore, the protection process has to be combined with the fabrication of gold bumps.

Acknowledgments

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