ELECTRICAL ISOLATION PROCESS FOR MOLDED, HIGH-ASPECT-RATIO POLYSILICON MICROSTRUCTURES

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ABSTRACT

A new process for fabricating molded, thin-film microstructures with electrical and mechanical interconnects is presented. A two step molding process is used to create a composite structure of undoped polysilicon, silicon nitride, and doped polysilicon. The doped poly is used to create regions of conductivity within a nonconducting structure. Thus it is possible to create high-aspect-ratio, monolithic electro-mechanical microstructures which are transferable from a reusable mold. These microstructures are more resistant to thermal changes and misalignment errors compared to microstructures transferred in segments. A suspended electrostatic microactuator was successfully fabricated using this process. High-aspect-ratio structures, 100 μm and 75 μm tall, were fabricated with 7 μm wide capcitive gaps. Experimental verification of the isolation showed an acceptable 10 nA current leakage at ±25 V and 150 nA leakage at ±50 V.

INTRODUCTION

Molded, thin film structures involve the chemical vapor deposition of thin films, typically 3-5 μm thick, onto a mold created by deep reactive ion etching (DRIE) of a network of trenches in silicon [1]. There are three key advantages to this microfabrication process. The first advantage is the generation of high-aspect-ratio structures from the deposition of a thin film. The second advantage is the use of several materials to form a composite structure and the third is the combination of high-aspect-ratio beams with surface features. In addition, the silicon mold is reusable resulting in an economical high-aspect-ratio fabrication technology.

Molded polysilicon structures have been utilized in the fabrication of microgrippers [1], microactuators for disk drives [2], and microgyroscopes [3]. Electrical isolation for these applications has been achieved by mechanical discontinuity, either by breaking flexures after the transfer of the polysilicon structure from the mold [2] or by using the mold itself to provide anchors for different parts of the structure [3]. Using mechanical discontinuity to provide electrical isolation has several drawbacks. Fabrication of several discontinuous components presents problems during the transfer step where misalignments can result. Alternatively, breaking flexures after the transfer of a monolithic structure is not compatible with volume manufacturing. Using the silicon mold to provide isolation by anchoring discrete parts of a device negates the economical advantage of a reusable mold.

The electrical isolation approach presented in this paper was developed specifically for monolithic micro- and milli-structures that are transferable out of a reusable mold. An example of a released and transferred device is shown in Figure 1. This suspended electrostatic microactuator was constructed from a combination of undoped polysilicon (4 μm), low-stress nitride (2000 Å), and doped polysilicon (3.8 μm). Electrical isolation between doped regions in this composite structure was achieved by a combination of nitride and undoped polysilicon, providing dual protection against current leakage.

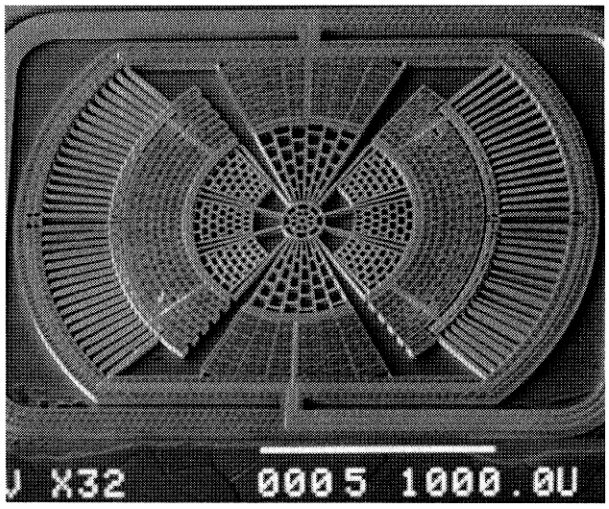


Figure 1: Suspended electrostatic microactuator, molded from a combination of undoped poly, nitride, and doped poly to provide electrical isolation.

FABRICATION PROCESS

Approach

There are two methods to achieve isolation in monolithic structures: (1) create isolation within a conductive structure or (2) create regions of conductivity within a nonconducting structure. The former is commonly used

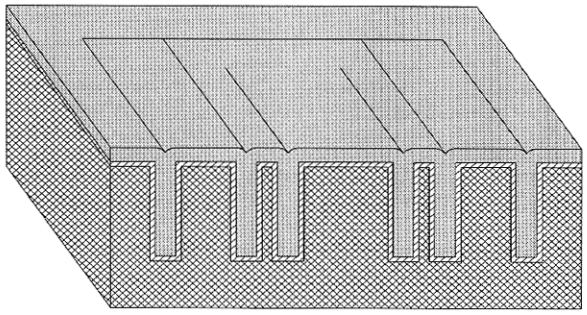
in the silicon-on-insulator (SOI) microfabrication technology. In SOI, nitride is used to backfill trenches, isolating regions of doped single crystal silicon. The nitride is then etched back [5]. This approach presents a few challenges when implemented in a molded thin film process. The primary challenge involves the etch which defines the isolation trench. In SOI, that trench is etched in single crystal silicon. In molded structures, this etch involves removing polysilicon that has backfilled the original trenches in the mold. Thus the etch front proceeds down a trench which is lined with a sacrificial film. Any stringers or residual polysilicon left behind in the isolation trench will cause a short across the isolation trench.

By defining regions of conductivity within a nonconducting structure, the importance of the etch is eliminated. Residual nonconducting stringers will not affect overall conductivity. Another advantage is that the conductive film used to define regions of conductivity is deposited last and can be used for interconnects on the surface of the molded structure. In addition, because the high-aspect-ratio beams and interconnects are created from a single film deposition, there is no need to define contacts.

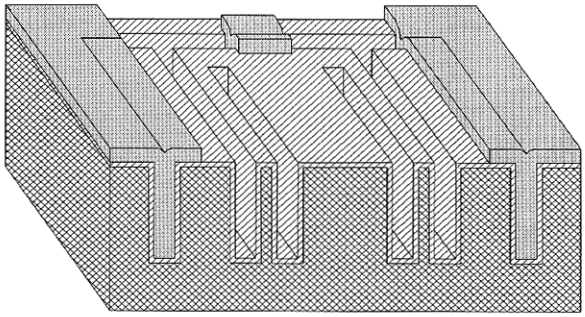
Detailed Process Flow

The process flow for the isolated, molded polysilicon structure is presented in Figure 2. The details of the process are provided below:

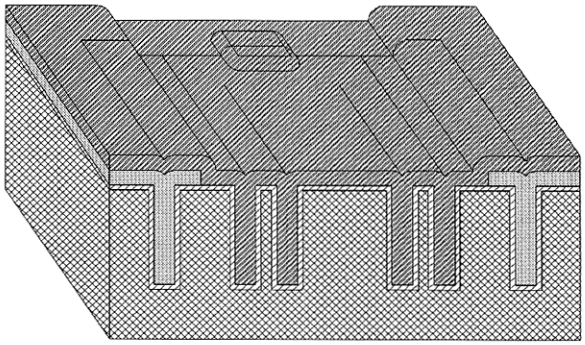
The process begins with the fabrication of a reusable silicon mold. This is accomplished with an inductively-coupled plasma (ICP) DRIE to achieve high-aspect-ratio trenches. Because of the etch lag phenomenon in the ICP process that results in a higher etch rate for wider trenches, all trenches within the mold are of uniform 8 μm width, with a corresponding etch rate of 2.3 μm/min. Two types of molds were fabricated: 75 μm and 100 μm deep. The SF_6/C_4F_8 ICP process utilized resulted in a 25:1 etch aspect ratio which dictated the minimum distance between trenches: 4 μm for a 100 μm deep trench. After the etch, the molds were oxidized and stripped in HF to remove "grass" from the bottom of the trenches as well as to reduce the scalloping effect on the sidewalls resulting from the ICP process.



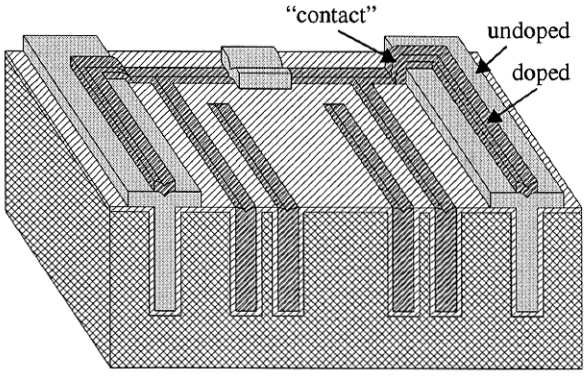
(a) A silicon mold is defined with a network of trenches. Sacrificial oxide is deposited followed by the deposition of undoped, structural polysilicon.



(b)In regions where conductivity is desired, undoped polysilicon is etched away. The sacrificial oxide is used as an etch stop.



(c) A 2000 Å thick low stress nitride is deposited, followed by a deposition of in-situ doped polysilicon.



(d) Surface features are patterned: Doped polysilicon with nitride etch stop, then undoped polysilicon with sacrificial oxide etch stop.

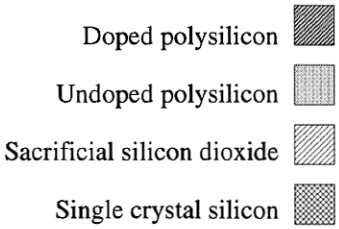


Figure 2: Primary process steps in a molded, polysilicon microstructure with "built-in" isolation.

Once the mold is completed, low stress nitride is deposited to protect it during release. A conformal, sacrificial film is then deposited. Silicon dioxide can be deposited conformally using TEOS or LTO with N_2O at elevated temperatures [3]. Since neither were available to the authors, sequential oxidation of polysilicon films were used. Low temperature (900°C) oxidation of 0.25 μm thick undoped polysilicon films produce extremely conformal 0.5 μm thick layers of oxide [1]. This process can be repeated as necessary to achieve the desired sacrificial film thickness. The thinner is the sacrificial layer, the smaller is the gap between a pair of electrostatic plates. However, the thinner is the sacrificial layer, the more difficult it is to pull the structures out of the mold. A sacrificial film of 2.5 μm was used in this work.

After the deposition of the sacrificial layer, the first structural layer is deposited. A 4 μm thick film of undoped polysilicon is deposited at 580°C with a deposition rate of 45 Å/min. Although the trenches are 5.25 μm wide after the smoothing oxide growth and removal and the sacrificial oxide deposition, more than half that amount needs to be deposited. An additional 25% is added to ensure that intersections of trenches get completely filled and another 20% is added to increase surface flatness, resulting in a 4 μm thickness requirement. The film is annealed for 1 hour at 1000°C. The measured film stress is 47.3 MPa tensile. The resulting cross section is shown in Figure 2a. Up to this point, the process is identical to the hexsil process introduced in [6]. All subsequent steps are incorporated to enable electrical isolation.

Once the structural polysilicon is deposited, lithography is possible as the surface is relatively flat. The conductive areas are then defined and the undoped polysilicon in those regions is removed with a DRIE step (Figure 2b). The etch stop for this step is the sacrificial oxide lining the mold. The selectivity of oxide to silicon in this process is 100:1. This polysilicon etch involves identical etch chemistry and duration to the etch used to define the silicon mold. Our experiments show that although there are 3 significant differences between the two etches, the etch rate appears to be identical. The differences are: (1) removal of polysilicon instead of single crystal silicon, (2) approximately 80% less area is exposed during the poly etch, and (3) aspect ratio of the trenches in the poly etch is 50% higher as the trenches are narrower due to the sacrificial film on the side walls. In addition, it is unclear what role the oxide on the sidewalls plays in this etch step. An SEM of etched trenches is shown in Figure 3. Note the footing that occurs on the surface poly film and that this is *not* a critical step. Any residual undoped polysilicon, such as stringers along sidewalls and films at the bottom of trenches, will not degrade the performance of the device appreciably.

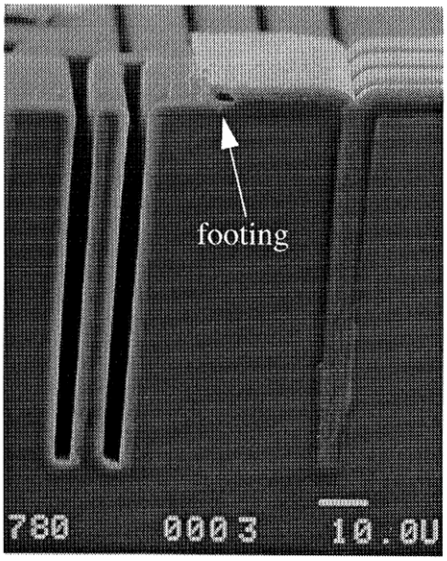


Figure 3: SEM of a cross section after the second DRIE step. This etch undercuts the photoresist mask (not shown) and erodes the surface poly.

After the DRIE step, a 2000 Å film of low stress nitride is deposited. This film is used as a dopant barrier between the undoped polysilicon and the doped film to be deposited. With this film, isolation is achieved with a combination of undoped polysilicon and nitride. Immediately following the nitride deposition, the conductive film is deposited. First a 0.5 μm thick doped polysilicon film is deposited at 605°C with in-situ phosphorus doping (20 Å/min dep rate). Then, 3.3 μm thick undoped poly is deposited at 580°C. This 2 film stack is then annealed for 1 hour at 1000°C to activate and redistribute the dopants. The resulting stress state of the film was measured to be 26.6 MPa tensile. This stress is lower than the undoped polysilicon alone because doped poly is compressive. Stress gradient is not an issue because the film stack is symmetric about the trench centerline. The measured sheet resistance of this 3.8 μm thick film is 6.8 Ω/sq. The corresponding cross section is shown in Figure 2c.

Next, the doped polysilicon film is patterned and etched to form electrical interconnects. The etch utilizes a Cl_2 and HBr chemistry which is very selective to the underlying nitride. Note that the doped poly lines patterned on the face of the wafers are continuous with the doped poly which backfills the trenches to create high-aspect-ratio beams. Thus, no contacts need to be defined in this process. Next, the nitride is removed with a blanket SF_6 etch. The undoped polysilicon is then patterned and etched to define mechanical structures that combine high-aspect-ratio beams with surface features (Figure 2d). An example of where such a combination is

utilized is the T-bar design of torsion beams for microgimbals [4].

Finally, the structure is released in HF and transferred out of the mold onto a target die using a flip-chip process (Figure 4). A section of a rotary microactuator, highlighting the isolation structure, is shown in Figure 5. In both Figure 4 and Figure 5, the horizontal beam that makes the structure mechanically continuous yet electrically discontinuous is visible.

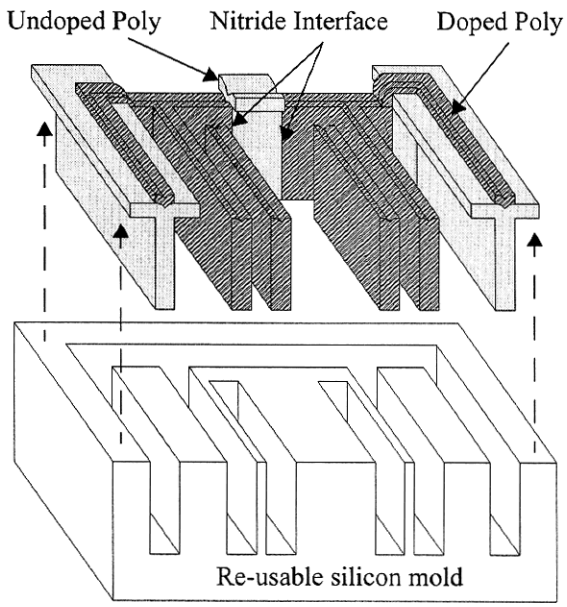


Figure 4: Final step in process flow: microstructure is transferred out of a reusable mold and onto a target substrate (not shown).

Process Challenges

Three primary challenges were overcome in the development of this process. The first was the prevention of the migration of dopants from the sacrificial film into the structural undoped polysilicon. In prior molded polysilicon processes, thin (2000 Å) layers PSG and LTO were deposited after the thermal oxide was grown as the sacrificial layer. The dopants from the PSG increase the HF etch rate and thus reduce release time. However, in this process which involves an anneal step for each of the poly film deposited, the LTO was insufficient in blocking dopant migration. Dopants from the PSG migrated into the undoped polysilicon and made the walls of the undoped polysilicon beams conductive effectively shorting out devices. This problem was overcome by avoiding the introduction of any dopants into the process until the last polysilicon deposition.

The second challenge was the prevention of footing that occurred in the surface poly during the DRIE etch to defined the conductive regions. To avoid the footing,

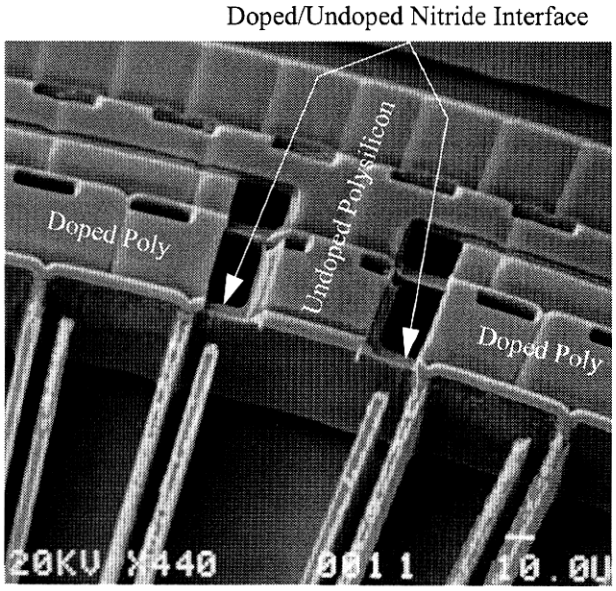


Figure 5: Close-up of the isolation structure in the molded polysilicon process.

prior to the DRIE step the surface polysilicon was etched isotropically (using SF_6), undercutting the photoresist. Then the resist is stripped and the lithography step is repeated using the same exact mask. This avoids the exposure of the surface film to the DRIE chemistry.

The third challenge was the improvement of surface topography. When polysilicon is deposited conformally onto a mold, a small dent results on the surface along the centerline of all trenches (this can be seen schematically in Figure 2a-c). This is a significant effect when the trenches are underfilled. When doped polysilicon is deposited on top of that surface, this conformal and conductive film fills the dent. The doped polysilicon etch which follows does not remove the doped film completely, leaving behind stringers on top of all trenches. These stringers create a network of conductive lines that short out the device. It is therefore critical to ensure that the structural, undoped polysilicon fills the trenches completely.

APPLICATION AND RESULTS

The molded polysilicon process with electrical and mechanical interconnects was utilized in the fabrication of a suspended, electrostatic microactuator for disk drive applications [4]. An SEM of this multi-degree-of-freedom structure is shown in Figure 6. The integration of the suspension and the microactuator has several advantages including a compact design which is simpler to assemble into the disk drive arm and a lowered sensitivity to thermal effects. The suspension is constructed from a honeycomb-like frame made from a network of undoped polysilicon beams. The torsion

beams of the suspension combine a vertical beam and a horizontal (surface) film to produce a cross sectional geometry that is soft in torsion yet stiff in bending. Doped poly interconnects traverse the suspension from the bond pads to the actuation quadrants and center shuttle (ground) of the microactuator. The doped poly is therefore limited to the capacitive plate areas and surface interconnects.

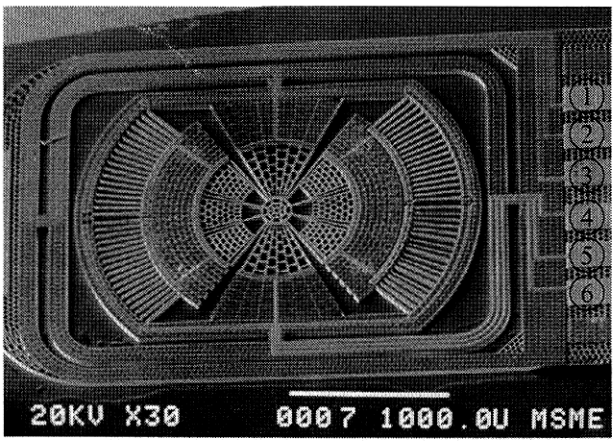


Figure 6: Gimballed rotary microactuator for magnetic disk drive application (released and transferred). The 6 labelled contact pads on the right control the microactuator. Pads no. 1, 3, 4, and 6 contact each of the actuation quadrants while pads no. 2 and 5 connect to the center shuttle (ground).

The electrical isolation was experimentally verified before the device release and transfer. This is possible due to the 2.5 μm thick thermal oxide that lines the mold and electrically isolates the structure from the substrate and neighboring structures. In the structure shown in Figure 6, bond pads 1, 3, 4, and 6 connect to each of the four quadrants of the electrostatic microactuator. These are required to be isolated from each other. Two different types of isolation structures were tested. Schematics of these two mechanically-continuous beams and their corresponding I-V curves are shown in Figure 7.

Figure 7 shows that the isolation is good in the operating range of the microactuator (± 25 V), with current leakages of no more than 10 nA, resulting in a maximum power dissipation of 0.25 μW which is acceptable for electrostatic actuation. Beyond the 25 V range, the isolation begins to break down. In both isolation structures, the breakdown is more pronounced in the taller structures. It is likely that the nitride layer failed well below its breakdown voltage. Low-stress, silicon-rich nitride is known to have pinholes. In this process, we attempted to circumvent the pinhole problem by depositing the nitride in two CVD steps to stop the growth of pinholes at the interface. Since pinhole distribution is statistical in nature, it is likely that the leakage is greater when the area of interface is larger.

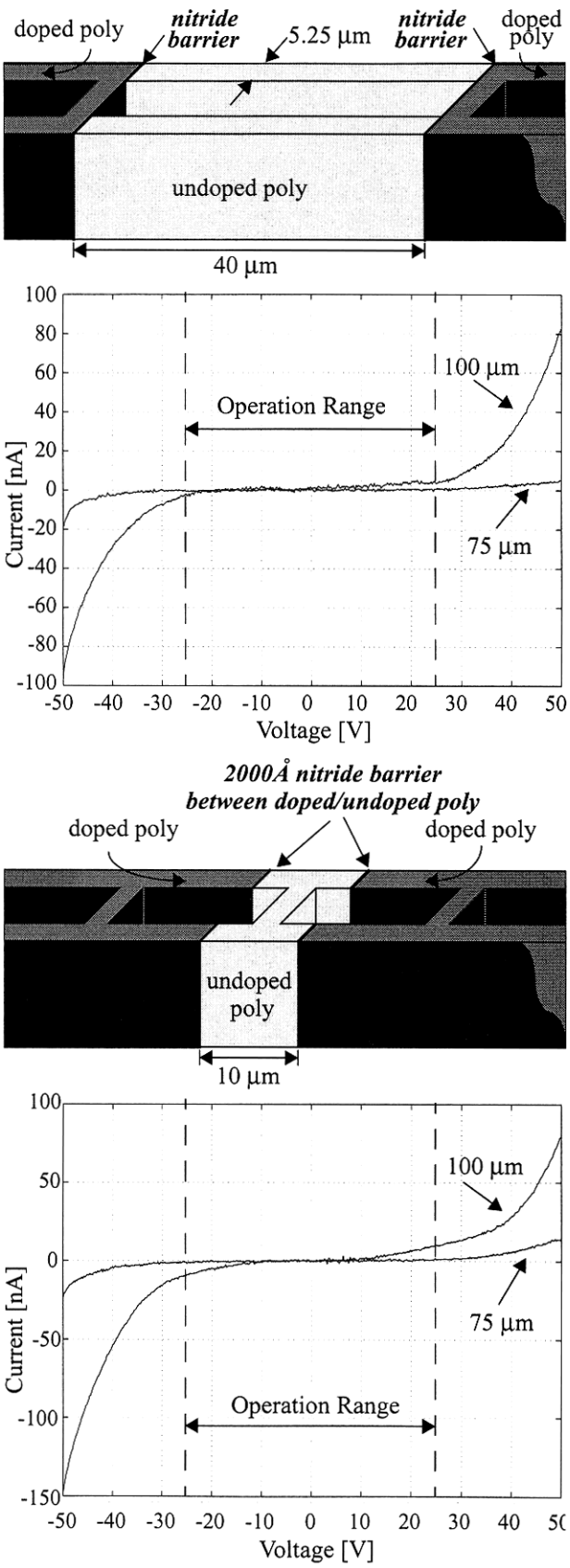


Figure 7: I-V curves across two types of isolation structures: 40 μm and 12 μm long undoped beams. The two curves indicate the two structure heights tested. The dashed lines indicate the designed operation range of the microactuator.

The data presented in Figure 7 supports this hypothesis by showing higher leakage currents for the 100 μm tall structure for both isolation geometries. In addition, it is possible that the nitride layer is slightly nonconformal resulting in films which are thinner at the bottom of the 100 μm trench than at the bottom of the 75 μm trench. Thinner films can exacerbate the leakage problem. In addition to pinholes, surface effects can also contribute to the increased current leakage at higher potentials. Charges trapped on the surface of the nitride are mobile and can potentially cause a short in the presence of stringers.

In addition to isolation, it is important to characterize conductivity paths. In Figure 6, two pads (no. 2 and 5) connect to the center shuttle. Either one can provide ground to the structure. This conductivity path involves two very long surface interconnects that are joined by the center shuttle which is constructed from high-aspect-ratio beams. The resistance of this entire path was measured to be 6.5±0.3 kΩ for the 75 μm tall structure and 7.0±0.4 kΩ for the 100 μm tall structure. Based on the sheet resistance values, the 800 square surface interconnects provide 5.4 kΩ of resistance.

CONCLUSIONS

We have demonstrated a new, high-aspect-ratio fabrication technology with "built-in" isolation and integrated interconnects. Composite microstructures consisting of undoped polysilicon, silicon nitride, and doped polysilicon were utilized in creating regions of conductivity within an insulating structure. Isolation was achieved with a nitride barrier. We have characterized the electrical isolation and verified the technology's applicability for electrostatic devices in the ±25 V operating range. In addition, we have demonstrated paths of conductivity which include doped polysilicon interconnects and high-aspect-ratio beams. Reduced interconnect resistance is possible with an additional metal layer, or by creating silicides on top of the existing doped poly interconnects. It was observed that leakage current increases with the aspect ratio of the structure.

This molding technology can be significantly improved by utilizing an LPCVD oxide film instead of nitride for the isolation. This is possible using poly silicon germanium (poly-SiGe) technology [7]. With a poly germanium (poly-Ge) sacrificial layer, the release is done in hydrogen peroxide leaving the silicon dioxide unattacked. The resulting structure is therefore a composite of undoped poly-SiGe, oxide, and doped poly-SiGe. This process is currently under development at BSAC.

ACKNOWLEDGMENTS

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