Characterization of Silicon Isotropic Etch by Inductively Coupled Plasma Etch in Post-CMOS Processing

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ABSTRACT

In this paper, a novel post-CMOS micromachining technique using inductively coupled plasma (ICP) etching is described, the processing space is explored and characterized. Unlike most ICP processes using photoresist as a mask, we demonstrated that aluminum can be used in this type of system. Also, we demonstrated in this hybrid process that vertical and lateral etching can be specified separately. This bulk micromachining process gives more freedom for designing CMOS-MEMS structures, and enhances the reliability and yield of post-CMOS micromachining. The design rules are furthermore extracted from the characterization of the process.

INTRODUCTION

A promising path for low-cost monolithic integration of circuits with MEMS is to fabricate microstructures directly out of the interconnect layers in conventional CMOS processes[1,2]. Such a process utilizes only maskless post-CMOS fabrication steps. The top metal layer in the CMOS process is used as an etch mask during Reactive Ion Etch (RIE) to release microstructures as illustrated in Fig. 1(a). The basic post-CMOS micromachining process flow is shown in Fig. 1. After an anisotropic etch step shown in Fig. 1(b) by CHF_3/O_2 RIE, the next releasing step is performed by SF_6/O_2 isotropic etch to undercut microstructures, as in Fig. 1(c)[1,3]. Composite mechanical structures can include polysilicon layers, metal layers and the inter-metal dielectric layers. The dry etch release steps avoid the sticking problem usually associated with the wet etch processing. About 5:1 high-aspect-ratio of beam and gap height to width is achieved in this process.

However, there are some major design considerations. Because of different residual stress in different layers of metal-dielectric composite beams, the structures are usually curled after release, especially for the devices like accelerometer and gyroscope, the structure most likely are curled down[4], as shown in Fig. 2. In severe cases, the proofmass may touch the silicon substrate, which inhibits its movement. Moreover, to reduce capacitive coupling from the substrate to the sensor, the separation between the sensor and substrate should be maximized.

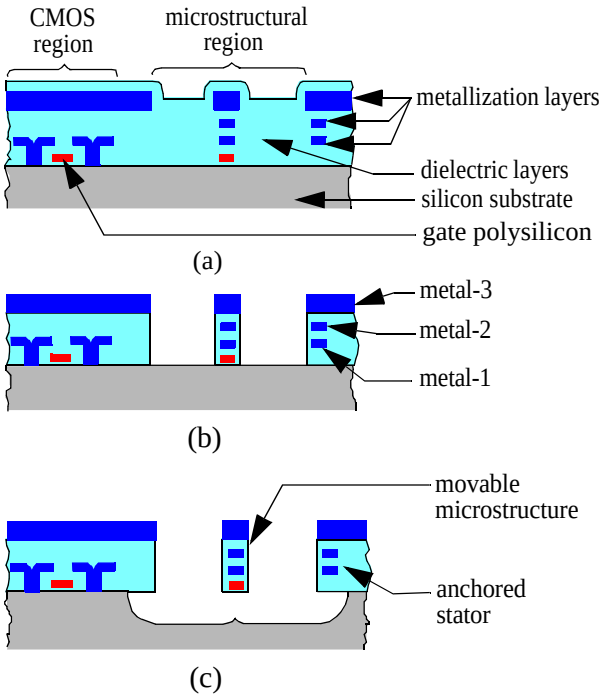


Figure 1. *Cross sections of device in each stage of the process flow.*
(a) Device from CMOS processing.
(b) After anisotropic isolation layers etch.
(c) After isotropic Si etch to release the mechanical structure.

Nevertheless the isotropic etch time to release microstructure from the substrate can not exceed a certain limit. First, because the second etch step in Fig. 1(c) is almost isotropic, circuitry must be put far away from the edge of the etch-resist mask to prevent being etched away during this step. But the extra spacing from sensor to circuitry will increase the parasitic capacitance to the input of the sensing circuitry. Second, it has been found that SF_6 can quickly etch Ti/W layers, which are present above and below each Al layer in many submicron CMOS processes as shown in Fig. 3. Long etch times can cause electrical contacts to be opened and mechanical structures to delaminate[3].

To overcome these shortcomings, a new fabrication technique is invented by introducing the ICP system to replace the previous microstructural release step with a silicon anisotropic etch, Fig. 4(a), followed by a silicon

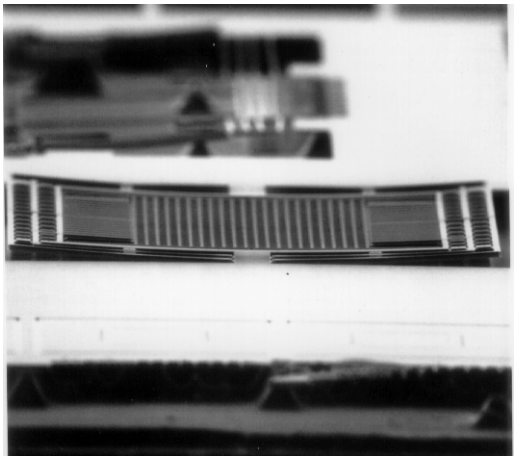


Figure 2. *Device curled down after released. This is an accelerometer from Gang Zhang's design at CMU mems group.*

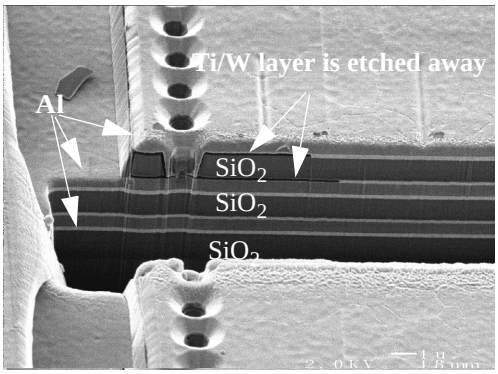


Figure 3. *Device shows Ti/W layer etched after Si isotropic etch by SF_6/O_2 plasma. The bright thin layers are Ti/W.*

isotropic etch, Fig. 4(b). The primary benefit is that the vertical etch and lateral etch are decoupled. Separation between the sensing element and substrate is guaranteed by the first anisotropic etch. The amount of lateral etch required is determined by the second isotropic etch and is set by design requirements.

PROCESS CHARACTERIZATION

Up to now, the SiO_2 anisotropic etch in Fig. 1(b) and the deep Si trench etch in Fig. 4(a) has been thoroughly examined[3,5], whereas, no database for using an ICP system to conduct silicon isotropic etching is available.

Screening experiments

The very first experiment is to verify that ICP system can be adopted into post-CMOS process. From the data collected, we find that Al from the CMOS foundry is a very good etch mask. We have not observed any decrement of Al layer thickness and critical dimension in this process within useful etch time. The robust etch is a big advantage of the ICP system over the common parallel-plate system, where the Al mask layers' dimension

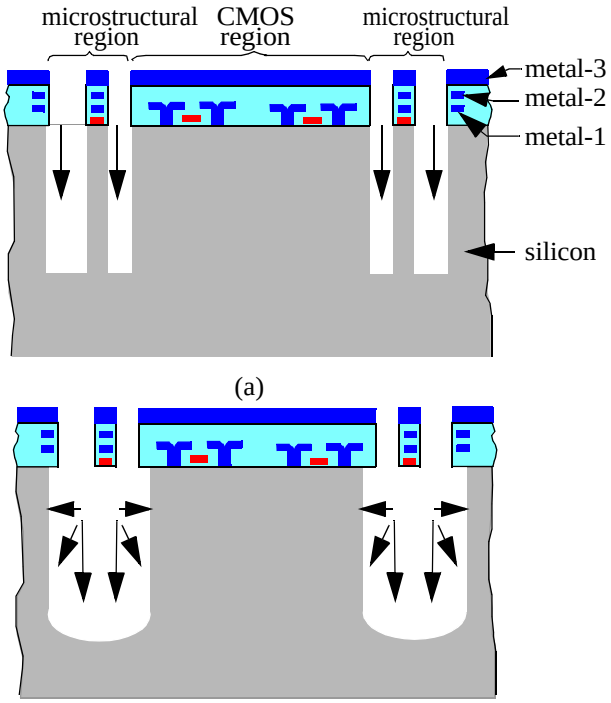


Figure 4. *Process flow of combining directional etch of silicon and isotropic etch of silicon to release thin film CMOS microstructures with minimum undercut.*
(a) Process of directional etch.
(b) Process of isotropic etch.

reduction can be significant[3].

The second observation is that there is no noticeable etching of Ti/W layers, that clad Al metallization in CMOS process. Preserving the Ti/W layers ensures that the mechanical structures do not delaminate and that electrical contacts between different metal layers survive after the release process. So the process yield is significantly increased and device reliability is assured.

Figure 5 shows lateral etch depth *vs.* time for 5 runs of $4mm^2$ dice from the Hewlett-Packard 0.5μm CMOS process under 50mT chamber pressure, 130sccm SF_6 flow, 12W platen power and 600W coil power process condition. Lateral etch rate at the edge of large open areas, is 4.0±0.8μm/min, which is relatively constant over the etch time investigated, 4 mins. The variation in etch rate comes from ramping up pressure to stabilize the plasma. With process times greater than 3min, the variation is reduced to 4.5±0.3μm/min.

Theory

It is well known that plasma systems have many processing variables, such as gas flow rate, pressure, RF power, electrode spacing, electrode temperature, total wafer area(loading) and previous processing steps. All these variables affect the etch result and their influence is non-

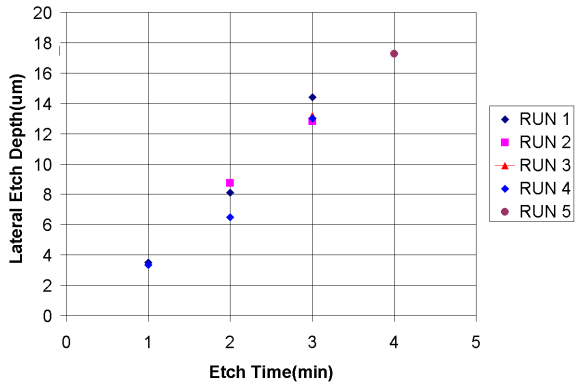


Figure 5. *Lateral etch depth(μm) as function of time(min) at the edge of large open regions.*

linear and correlated. The construction of a mathematical model which quantitatively represents the process responses as functions of the process variables is highly desirable, and permits the identification of the optimized settings to satisfy different requirements and precision process control.

In our experiment, we used Response Surface Methodology[6] to characterize this process. The benefit of this statistical technique is that the experimental strategy and data analysis are combined efficiently to generate a parametric model that represents the process response. After the response has been quantitatively modeled, graphical representation of the response surface can be generated in the parametric space. The trends in individual responses from changes in the processing factors can be predicted, and from multiple response surfaces of each processing factor, an acceptable range can be obtained. The effect of experimental error on the validity of a parametric model can be assessed using statistical analysis. First, the experimental error can be estimated by repeating experimental runs and calculating the standard deviation of the replicate differences. Also, the lack-of-model-fit can be estimated by performing extra trials to calculating the deviation between the model and the experimental data.

Response Surface Design

With an assumption that the response surface can be represented as a full quadratic model, three levels of the various factors are needed for a quadratic model. A full quadratic model for *n* factors contains a constant term, *n* linear terms, and *n(n-1)/2* interaction terms, and *n* quadratic terms and is expressed as in Eq. (1).

$$Y = b_0 + \sum_{i=1}^{n} b_i X_i + \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} b_{ij} X_i X_j + \sum_{i=1}^{n} b_{ii} X_i^2 \qquad (1)$$

where Y is the process response and the X_i are the process variables. The three levels of X_i should be equally spaced on same scale (e.g., linear, log, or square root).

Thus for 3 factors, 10 coefficients must be determined, since Eq. (1) can be simplified to:

$$Y = b_0 + b_1X_1 + b_2X_2 + b_3X_3 + b_{12}X_1X_2 + b_{13}X_1X_3 + b_{23}X_2X_3 + b_{11}X_1^2 + b_{22}X_2^2 + b_{33}X_3^2 \qquad (2)$$

Following common practice, we add 5 extra trials to estimate residual error. A large number of data points gives better error estimation and model fitting; however, this will lead more consumption of time and effort.

A Box-Behnken factorial experiment[6] has been applied to characterize the isotropic Si etch process in an Surface Technology Systems(STS) ICP system with 4" wafers including key mask features used in CMOS-MEMS structures. Effects are measured by varying three major processing parameters: process pressure, platen power and SF_6 flow. Under the assumption of a quadratic response model, 15 trials for 3-factor 3-level experiments with 12 points on each edge of the experimental space cube and 3 replicates at the center, as shown in Fig. 6, are required to determine the lateral etch response surface. The 3 levels of factors (platen power, pressure and SF_6 flow rate) are shown in Table 1. The total lateral etch time is 4 min. Compared to full-factorial design, which requires 27 runs, 12 runs are saved. The experiment covers the primary process space currently available for deep Si etching using ICP.

RESULTS

The measured data on different patterns, as in Fig. 7, from the factorial experiment are given in Fig. 8 and Fig. 9. These includes squares with 1:1 and 1:5 spacing, cantilever beams with 1:1, 1:5 and 1:10 spacing as in Fig. 8 and holes of 5 μm, 10 μm, 20 μm, 40 μm and 100 μm size as in Fig. 9. The etch rates on all patterns follow the same trend. For test patterns of holes with 1:1

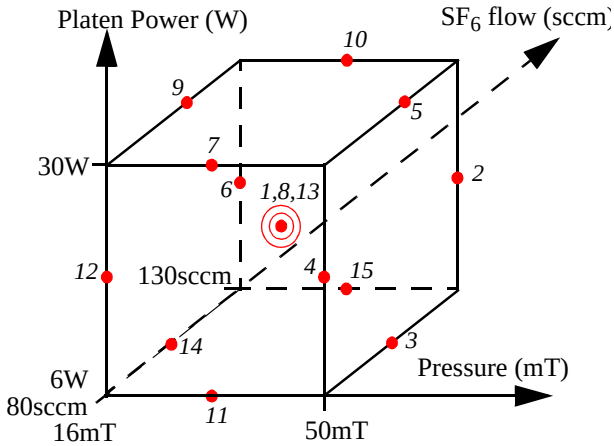


Figure 6. *The Box- Behnken 3-factor design of experiment. The run numbers are labeled beside solid dots which indicate the processing parameter set-up.*

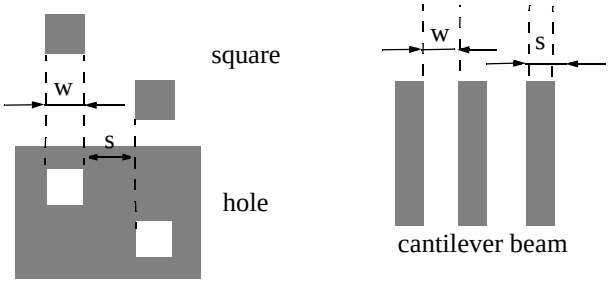


Figure 7. *Test patterns include squares, holes and cantilever beams. Their width (or size) over spacing ratio is equal to w:s. If the adjacent cantilever beams' width w are different instead of same for 10 contiguous ones, they are called quick cleave, with w:s=1.*

and 1:5 spacing, there is no significant difference between them, therefore, the etch rate of holes does not depend on hole spacing.

Table 1: 3 Levels of 3 Factors

Factor	low-level (-)	mid-level (0)	high-level (+)
X1=Pressure (mT)	16	33	50
X2= Platen Power (W)	6	18	30
X3=SF_6 flow (sccm)	80	105	130

Square patterns are chosen as the benchmark geometry in future processing tests, since the etch rate can be quantized by visuality inspecting the checkerboard. The etch rates on other features can be derived from the benchmark etch rate. Hole etching, which is the key point for release of plate, is much slower compared with that of squares. When the hole opening is small, e.g. 5μm, the etch rate is very insensitive to the system parameter variation. In this case, the geometry constraint plays a dominant role.

Response surface results from design of experiment are

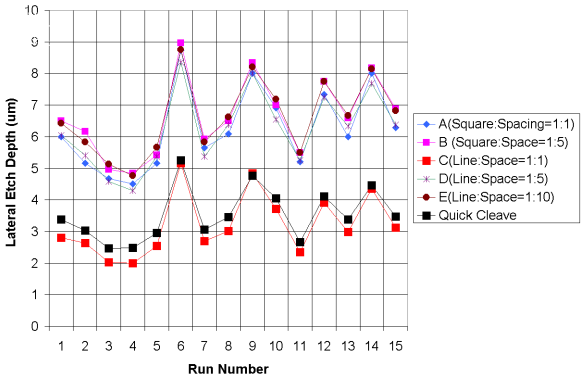


Figure 8. *Lateral etch depth(μm) of different patterns in statistical experimental runs.*

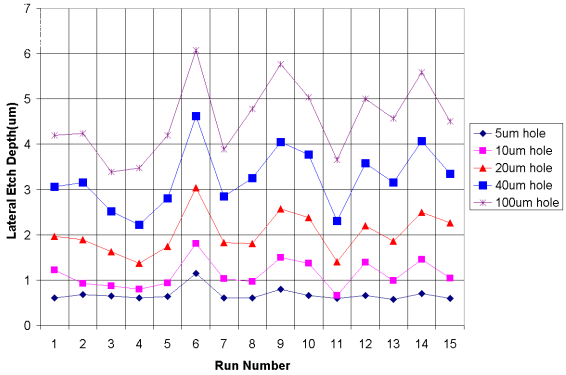


Figure 9. *Lateral etch depth (μm) on different size of holes (hole width:space=1:5) in statistical experimental runs.*

illustrated in Fig. 10. Pressure plays the most important role on lateral etch rate, followed by SF_6 flow and platen power. Etch rate is increased with decreasing chamber pressure and increasing of SF_6 flow; it is not significantly affected by platen power especially under high pressure. The relation of etch rate to pressure is totally different from the result obtained from a parallel-plate system. The fastest etch rate in run #6 is about 45% faster than that of run #2 which is similar to screening experiment conditions. The etch rate on the whole wafer test is slowed down due to the fact that the exposed silicon area is about 1655 times larger than a single $4mm^2$ dice.

The data generated by the response surface design is analyzed using Least Square Regression(LSR) analysis software from Minitab® which determines the model coefficients by minimizing the residual variances. The coefficients of Eq. (2) are enumerated in Table 2

Table 2: Coefficient of the Full Quadratic Model

Coeff. Term	Coeff. Value	Unit
b_o (Constant)	12.056	μm
b_1 (Pressure)	-3.142	μm/mT
b_2 (Platen Power)	0.392	μm/W
b_3 (SF_6 Flow)	1.104	μm/sccm
b_4 (Pressure^2)	0.847	$\mu m/mT^2$
b_5 (Platen power ^2)	0.014	$\mu m/W^2$
b_6 (SF_6 Flow^2)	-0.036	$\mu m/sccm^2$
b_7 (Pressure * Platen Power)	0.250	μm/(mT*W)
b_8 (Pressure * SF_6 Flow)	-0.367	μm/(mT*sccm)
b_9 (Platen Power * SF_6 Flow)	0.092	μm/(W*sccm)

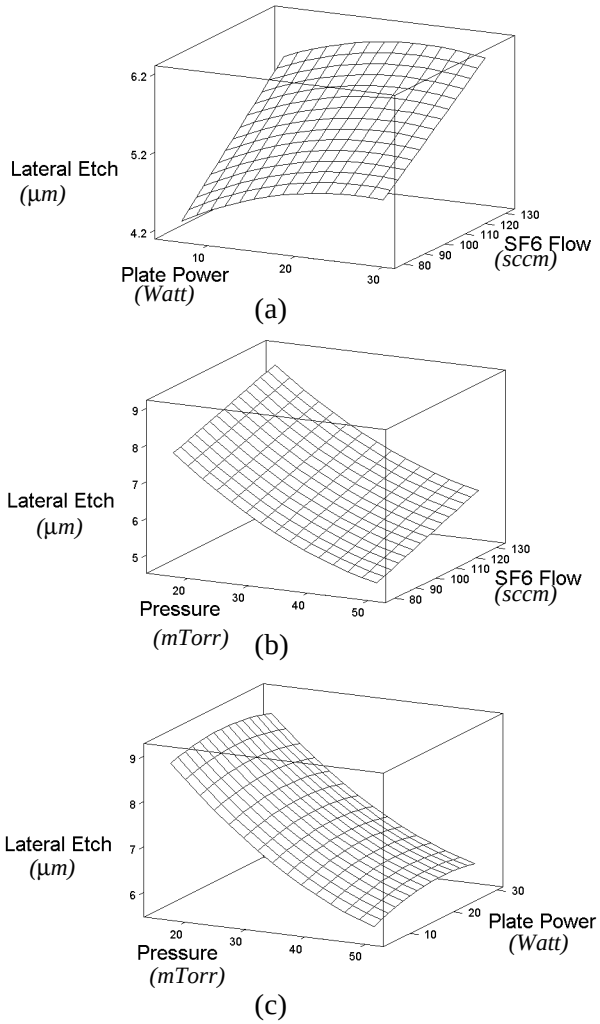


Figure 10. *Response surface on lateral etch of a square mask with width over spacing=1:5.*
(a) with fixed processing pressure, at 50mT.
(b) with fixed platten power, at 29W.
(c) with fixed SF_6 flow rate, at 130sccm.

The quality of the model can be determined by examining by the adjusted-R^2 number[6]. A perfect fit would have an adjusted-R^2 value of 100%. The adjusted-R^2 for the etch rate model is 99.3%. This value indicates that the parametric model represents this processing accurately.

The etch rate of different patterns in different runs of the factorial design normalized to the 1:5 square checkerboard pattern is in Fig. 11. The average ratio of etch rate of 1:1, 1:5, 1:10 line/space, quick cleave, and 100μm square hole to that of square pattern is 0.475, 0.936, 1.000, 0.529 and 0.695 respectively. From the data, it is obvious that long rectangular etch pits with width over space less than 5 etch similarly to squares. This means the geometric constraint to the etch is not dominant, and the patterns have similar efficiency of mass transportation in etch reactions. On the other hand, the 100μm etch holes may be considered as a big opening, but the geometric configuration limits the mass transportation, and slows down the etch rate.

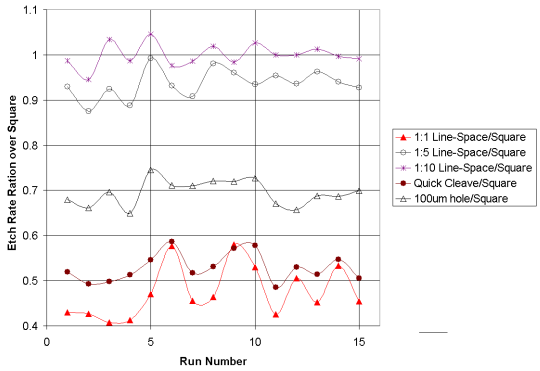


Figure 11. *The ratio of etch rate for different patterns normalized to that of the 1:5 square.*

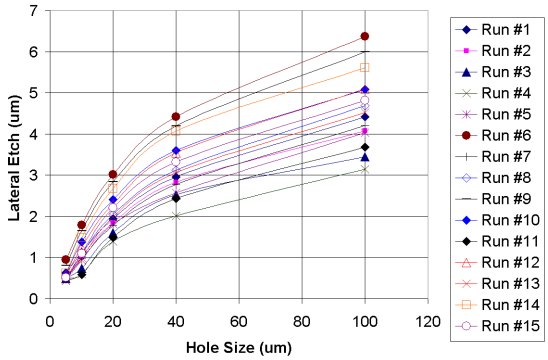


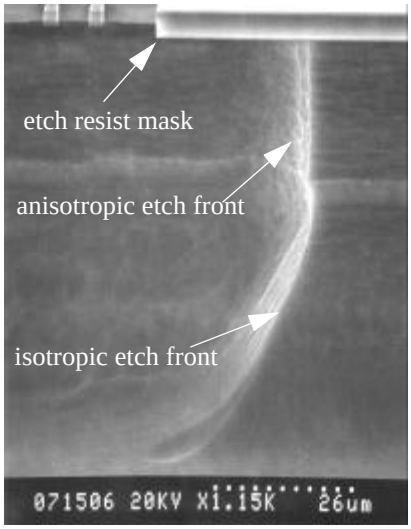
Figure 12. *Lateral etch depth (μm) vs. hole size on different size of holes in statistical experimental runs.*

As shown in Fig. 12, the etch rate on different hole size can be modeled as cubic relation when the hole size is less than 40μm, and as a linear relation when the hole size is between 40μm and 100μm. For example, for the condition in run #6, the etch rate (Y in μm) can be expressed to hole size (X in μm) as Eq. (3):

$$
\begin{aligned}
&5\mu m \le X < 40\mu m \\
&Y = 1.59\times10^{-5}X^3 - 3.00\times10^{-3}X^2 \\
&\quad + 0.205X + 2.81\times10^{-3} \\
&40\mu m \le X \le 100\mu m \\
&Y = 0.0327X + 3.10
\end{aligned}
\qquad (3)
$$

SEM pictures of the etch profiles in Fig. 13 show the decoupling of the lateral and vertical etch. Undercut of Ti/W layer is not observed. One demonstration etch is shown in Fig. 14, where the deep Si etch in the process has been exaggerated. After more than 100μm deep Si etching, the 2.1μm width, 5μm tall microstructures survive, and they suspend a plate about 50μm above the silicon substrate.

(a)



(b)

Figure 13. *SEM corresponding to post processing step shown in Fig. 4 (a) and (b) steps. (a) Sideview after silicon deep trench etch. (b) Sideview after silicon isotropic etch, the final release step. The Vertical anisotropic etch front comes from the vertical sidewall by anisotropic Si etch and is etched inward by isotropic Si etch.*

CONCLUSION

In this paper, we have demonstrated that the ICP Si isotropic etch process can be adopted to post-CMOS micromaching. Process constraints have been resolved, therefore improving the post-CMOS dry release process. By using a Box-Behnken factorial design of experiment, the quantitative parametric model to represent this process has been obtained. Design rules for releasing mechanical structures in this process are now able to be extracted from the analytical model of process.

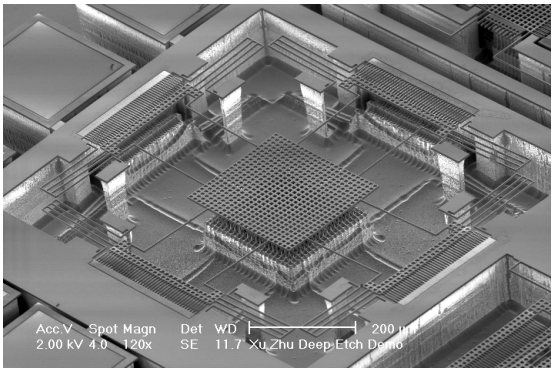


Figure 14. *Demonstration of deep silicon etch combined with silicon isotropic etch, the mechanical structure is suspended from silicon substrate by about 50μm.*

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