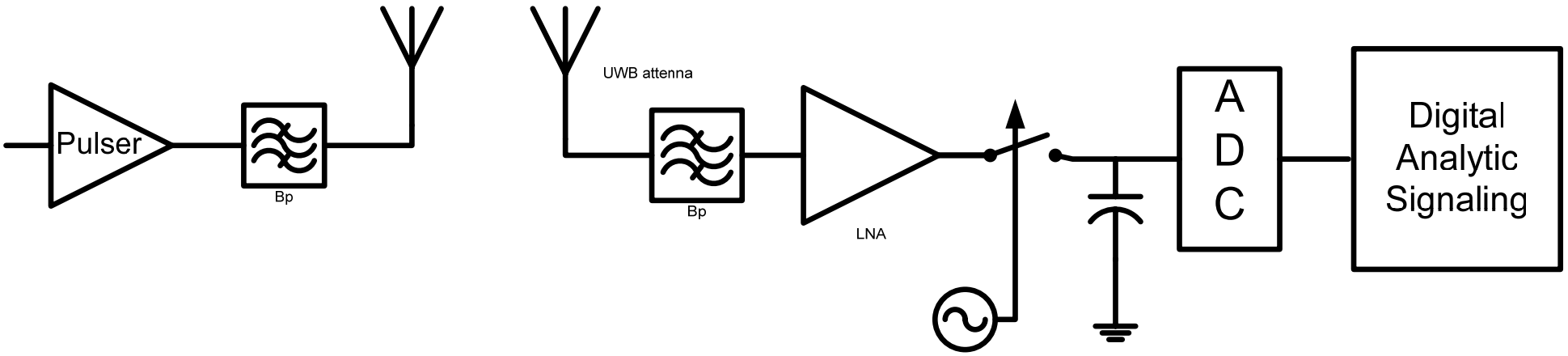
A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13µm CMOS

Mike Shuo-Wei Chen
Robert W. Brodersen

University of California, Berkeley

Background

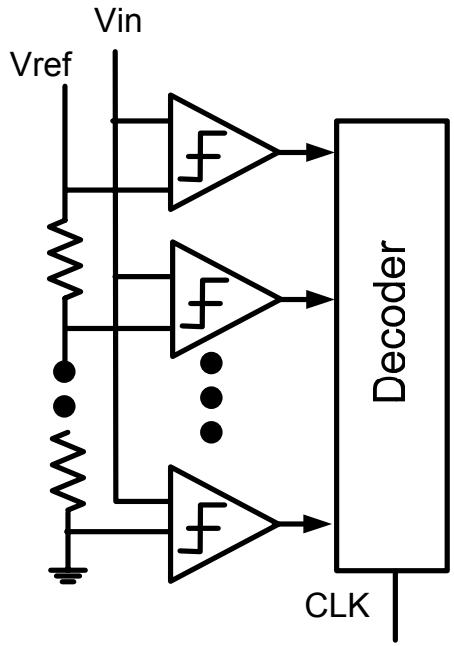
- Application
  - A sub-sampling UWB impulse radio architecture [Chen, ICASSP 2004]



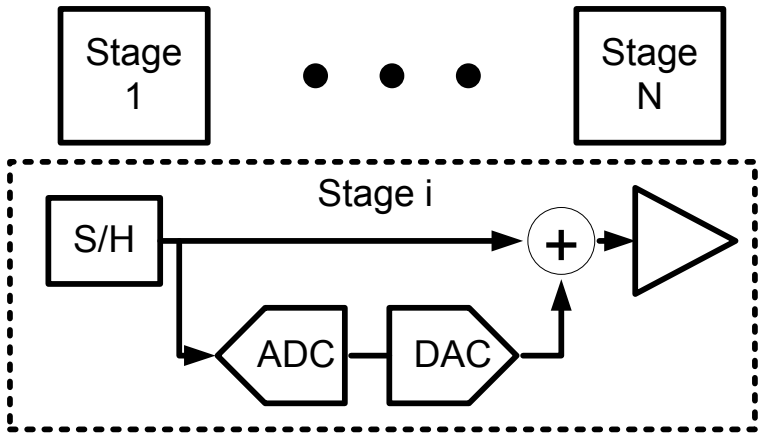
- Design Goal
  - Low power, high-speed (~GS/s), 6-bit ADC able to sub-sample an RF signal

Conventional ADC Architectures

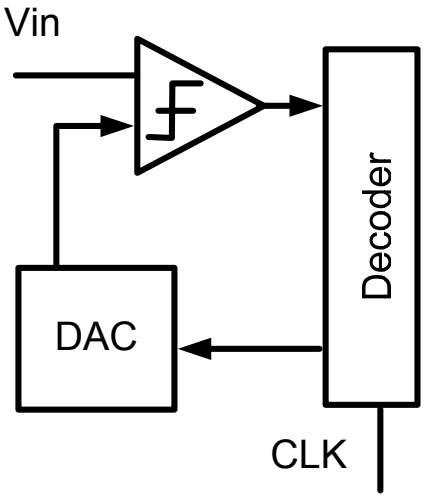
Flash



Pipeline

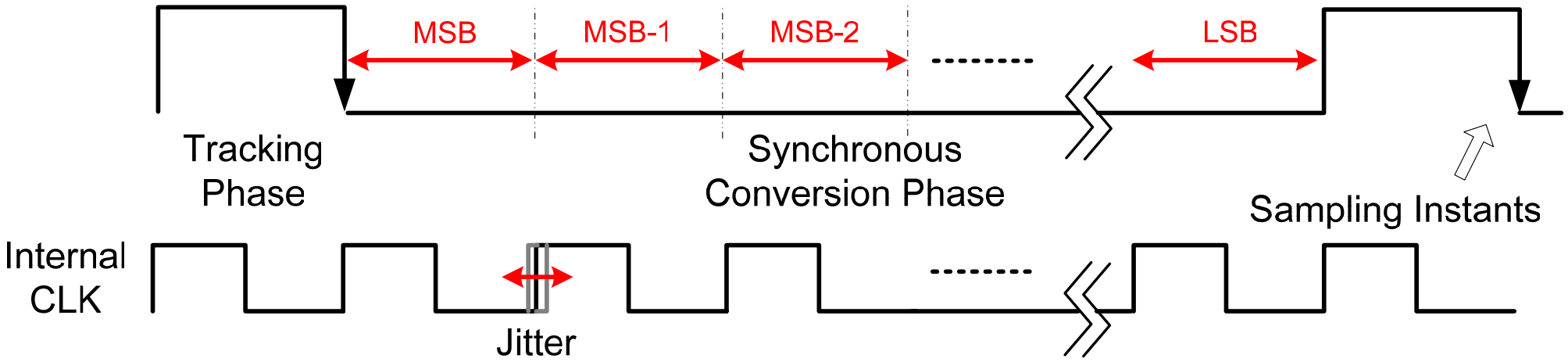


SAR



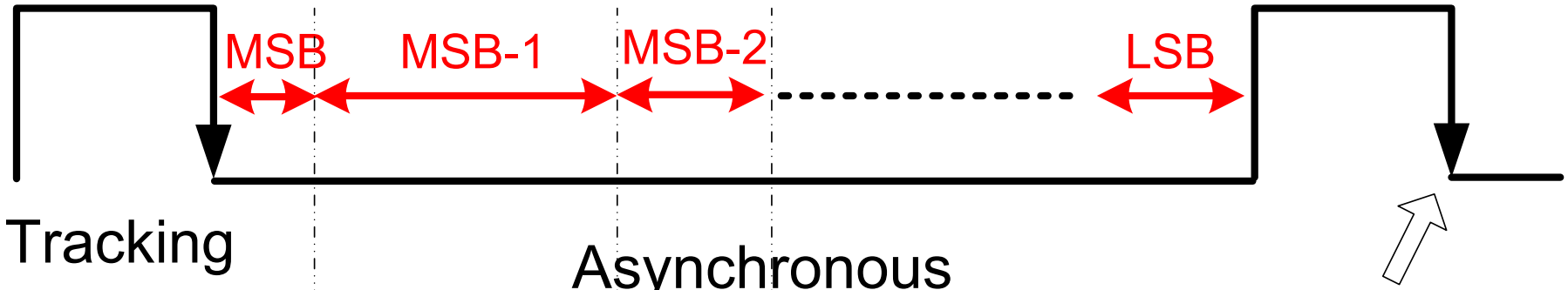
Power	2^N	>N	1
Speed	1	<1	1/N
PW/Speed	2^N	>N	N

Synchronous SA



- Power
  - No redundant comparison ✓
  - High-speed internal clock ✗
- Speed limitation
  - Worst-case cycle time ✗
  - Margin for clock jitter ✗

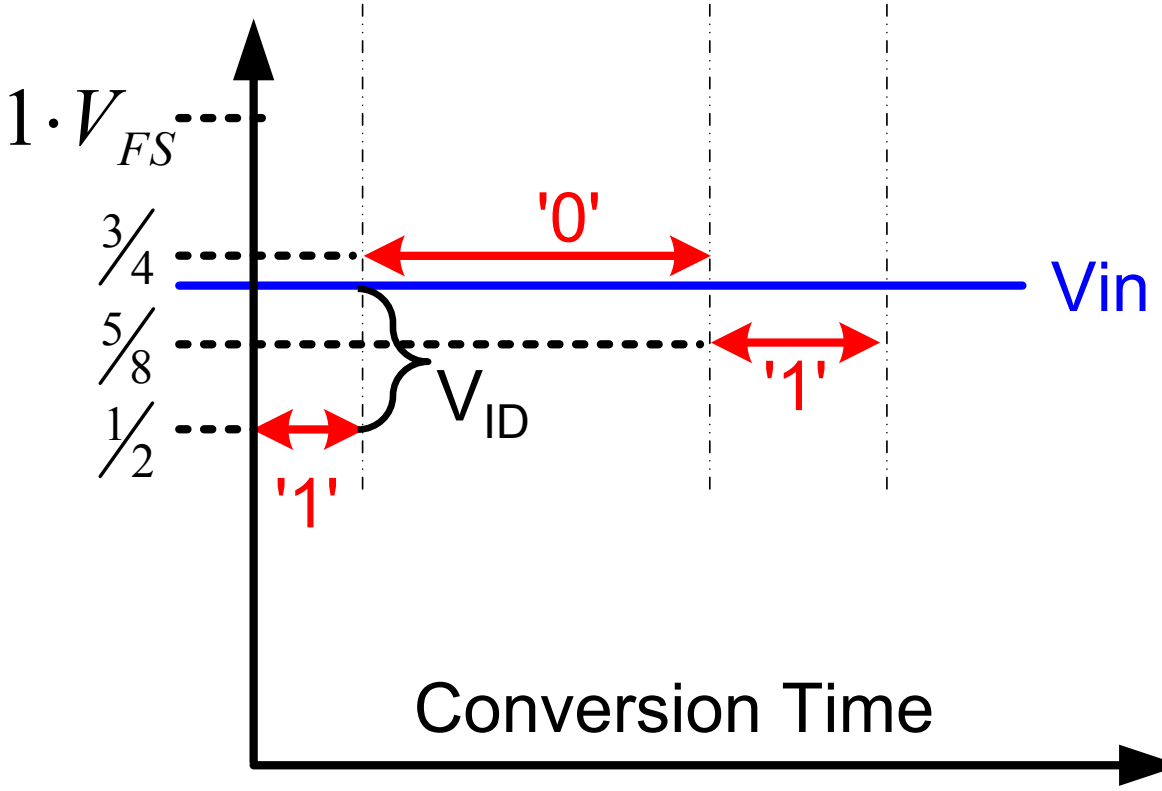
Asynchronous Processing



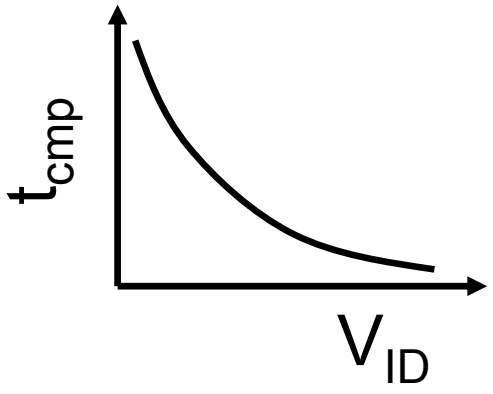
Tracking Phase

Asynchronous Conversion Phase

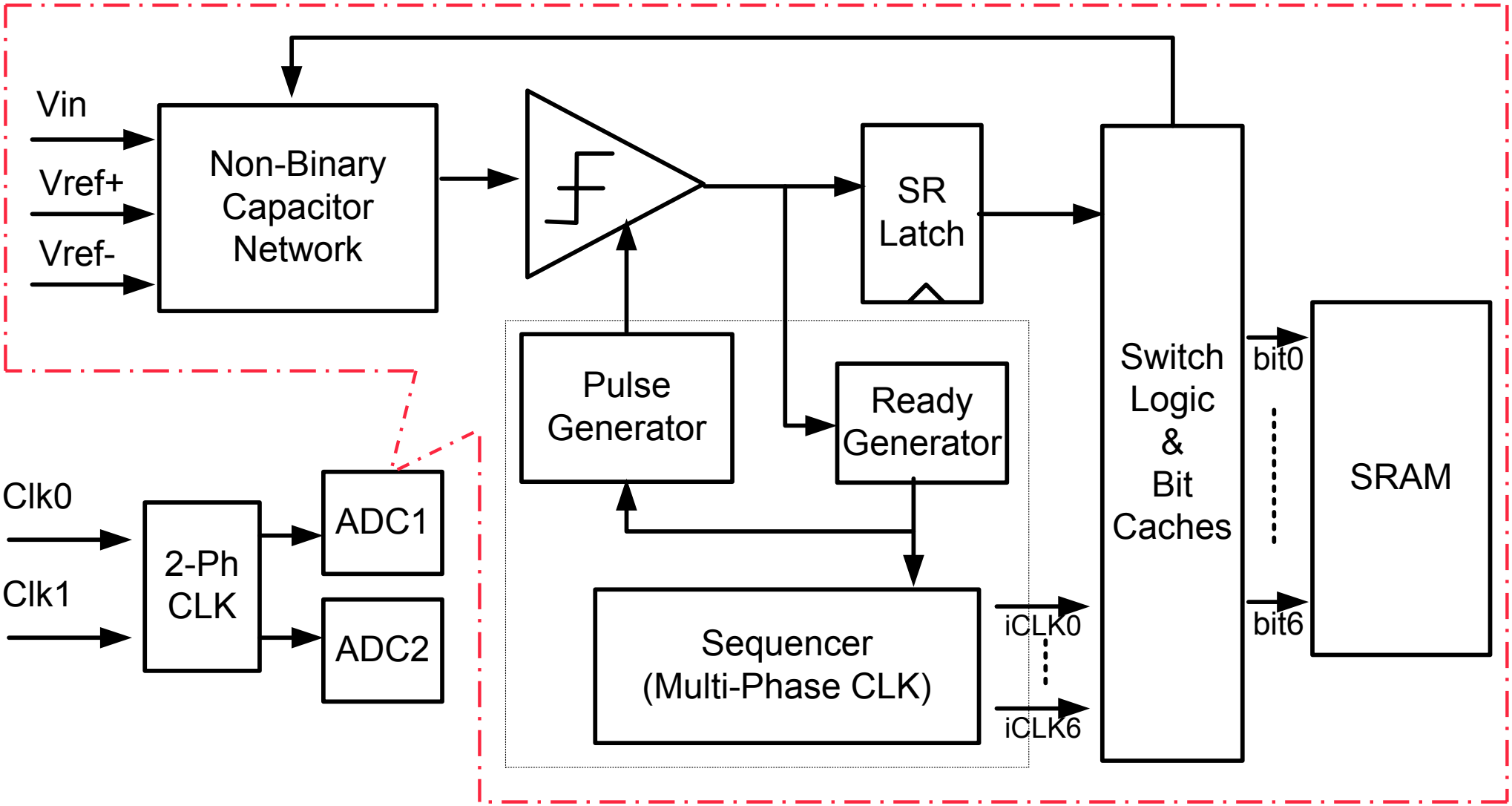
Sampling Instants



$$t_{cmp} \propto \frac{C}{g_m} \ln\left(\frac{V_{FS}}{V_{ID}}\right)$$

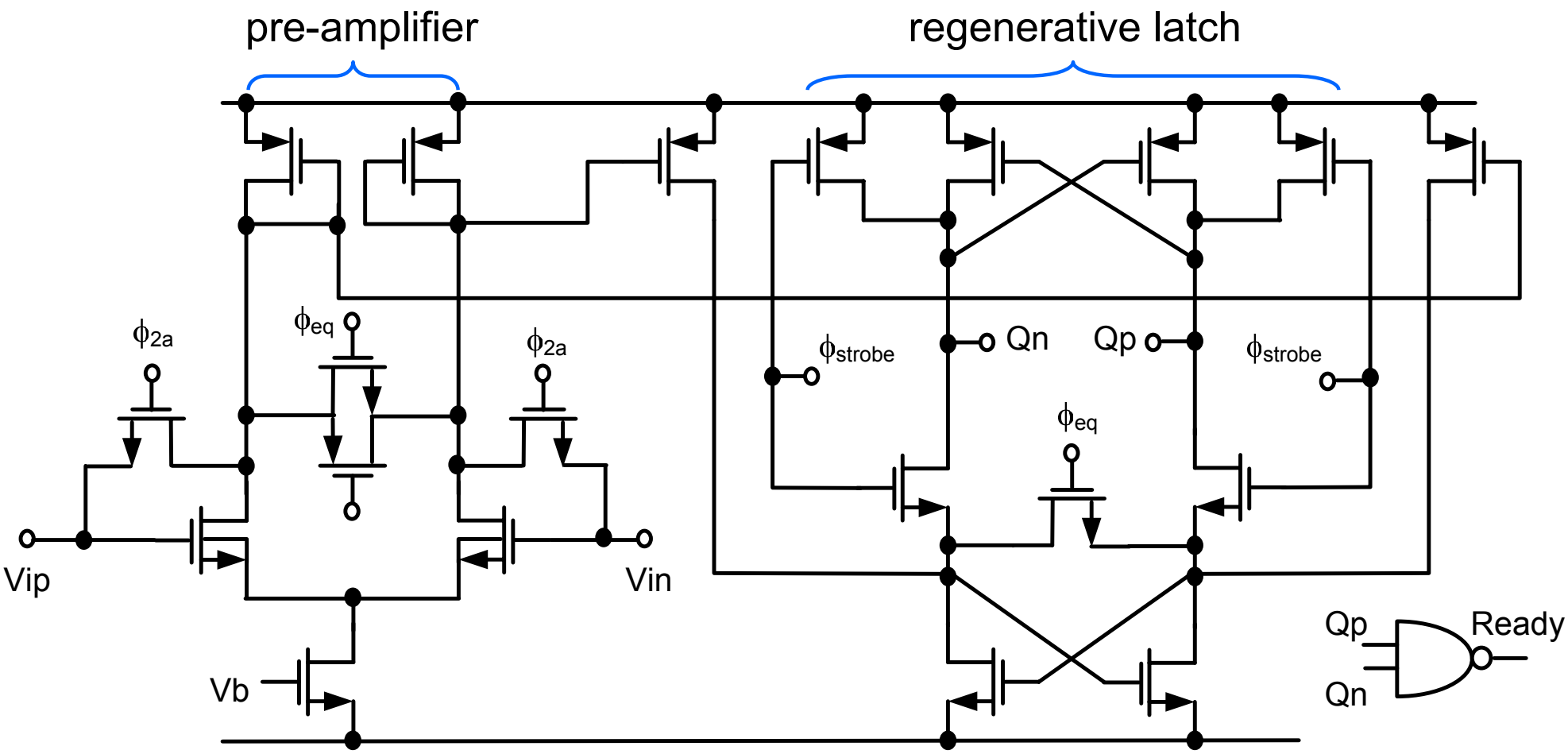


Time-interleaved 2X Async. ADC



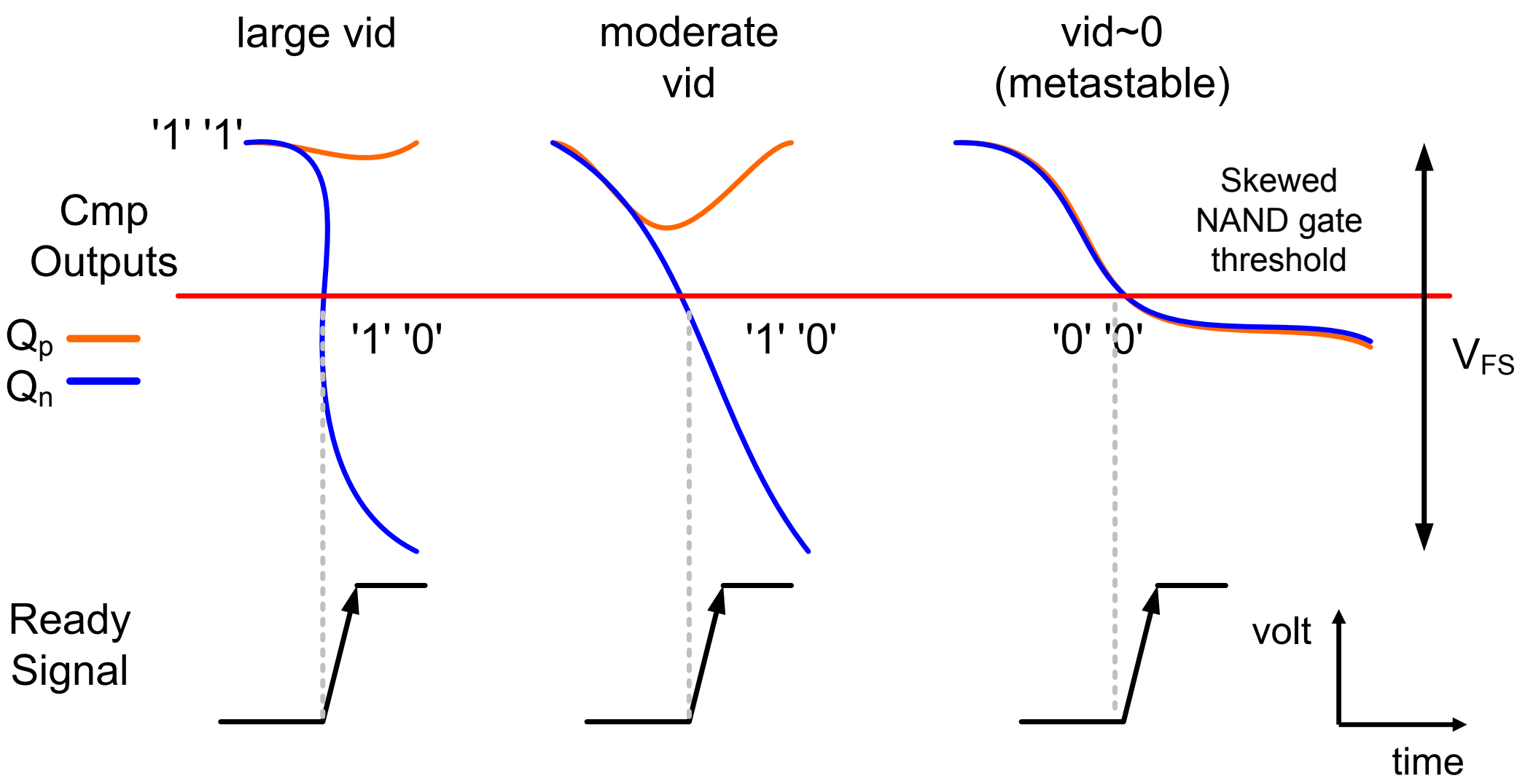
No clock higher than the sampling frequency

Dynamic Comparator



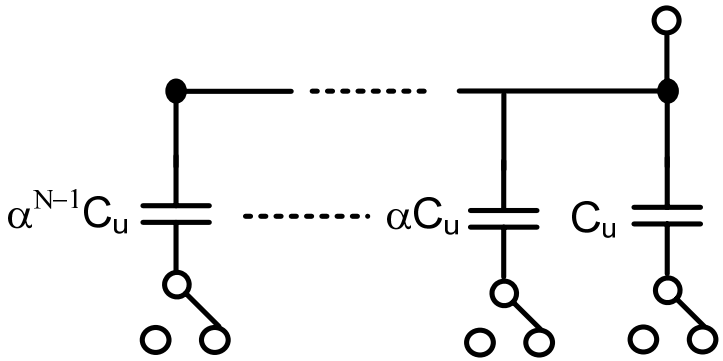
- Dynamic to save power and generate ready signal
- Reset switches for fast recovery
- Low charge kickback

Metastability Issue



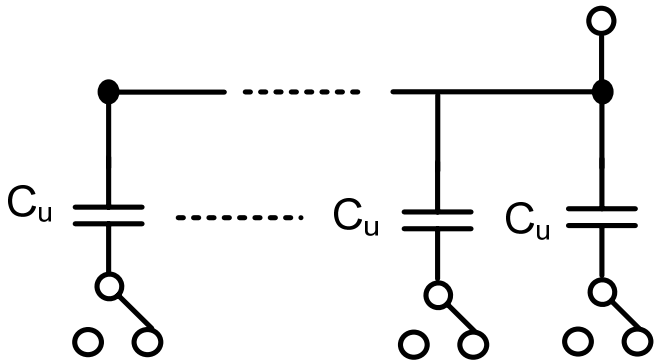
Non-Binary Radix Overview

- Redundant code allows settling errors [Kuttner, ISSCC 2002]
  - 7b code length used for 6b resolution (radix=1.81)
- Existing implementations ($C_{in} \sim 2^N \cdot C_u$)



Switch Logic

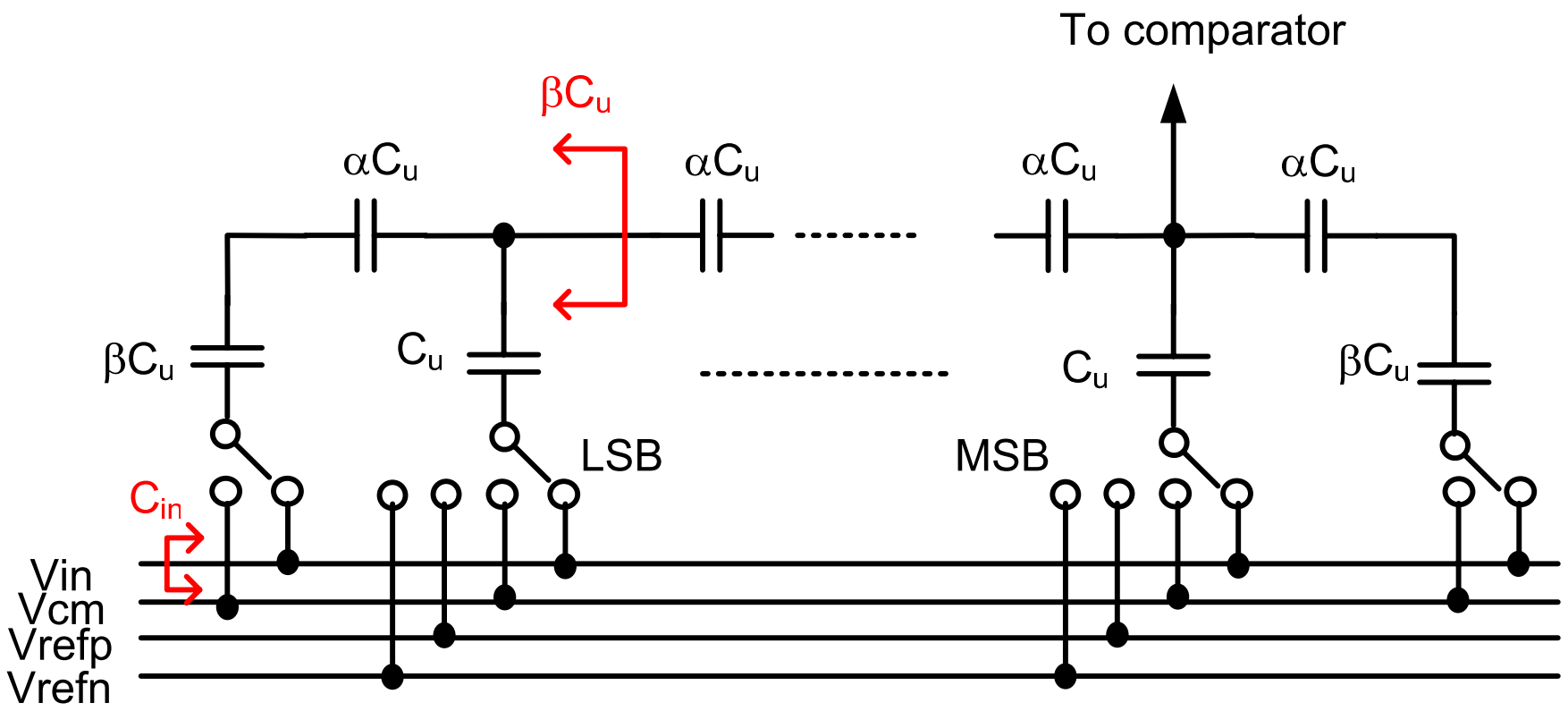
- Matching problem (α is non-integer)



Digital ROM

- Long propagation delay

Series Non-Binary Capacitive Ladder



- Non-binary radix
- Min C_{in}
- Relaxed matching

Design Equation :

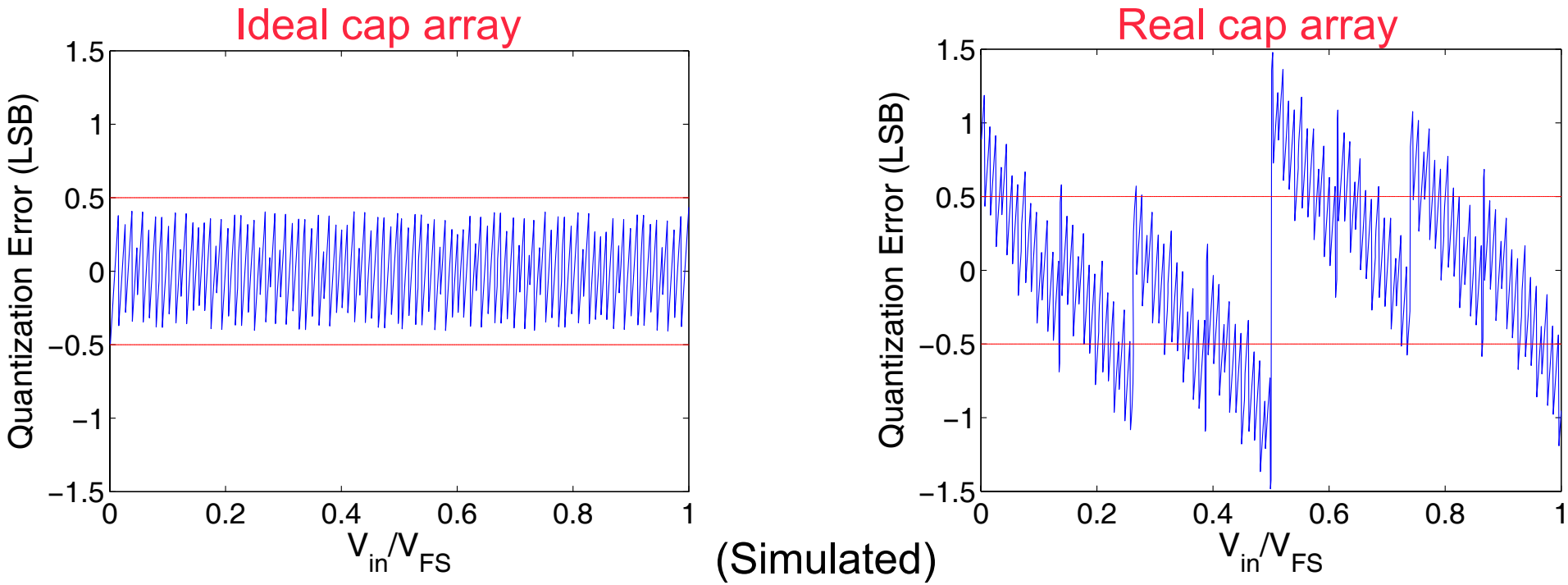
$$\begin{cases} \beta = 1 + \alpha \parallel \beta \\ radix = 1 + \dfrac{\beta}{\alpha} \end{cases}$$

Effective Input Capacitance :

$$C_{in} = [1 + 2 \cdot (\alpha \parallel \beta)] \cdot C_u$$

Compensating for Non-Idealities

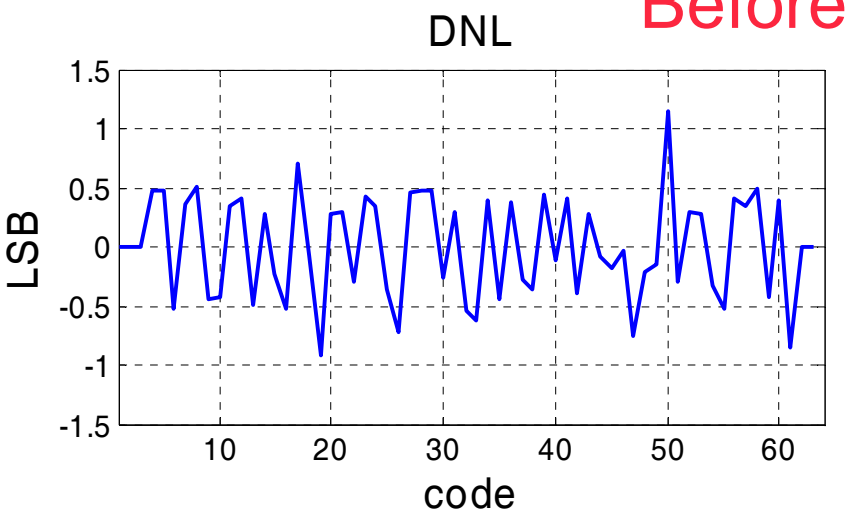
- Use minimum C_u and MOM-cap instead of MIM-cap
- Main problems: capacitor mismatch and parasitics
- Solutions:
  - ↑ α : systematic error
  - Digital calibration : random error

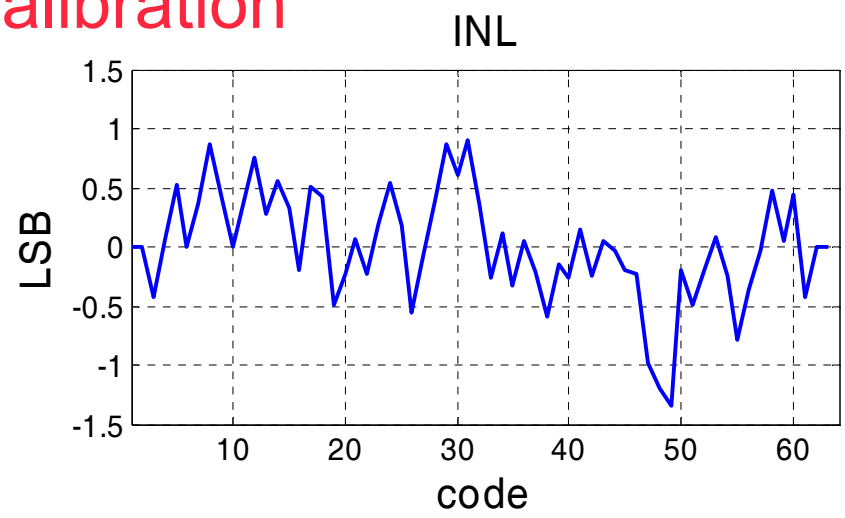


(Simulated)

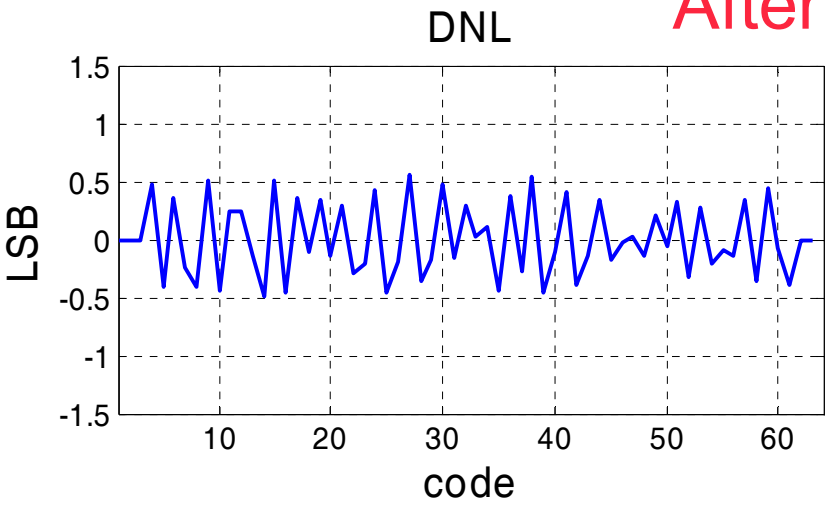
Measured DNL/INL

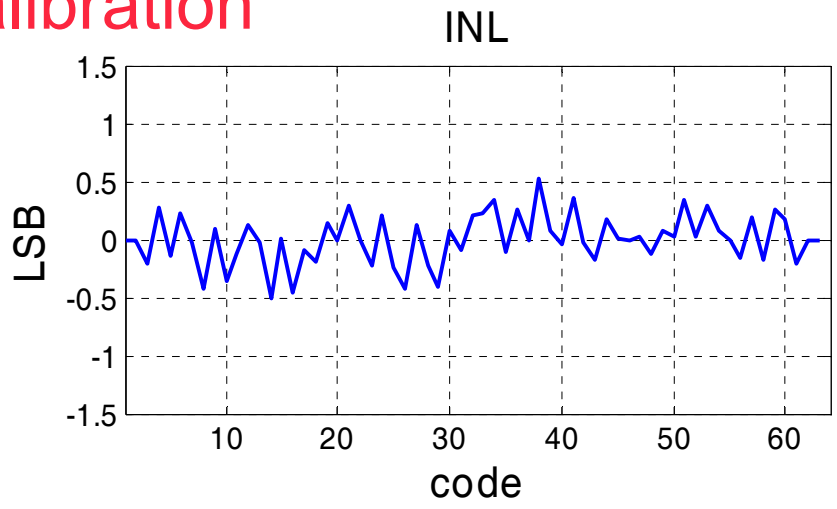
Before Calibration





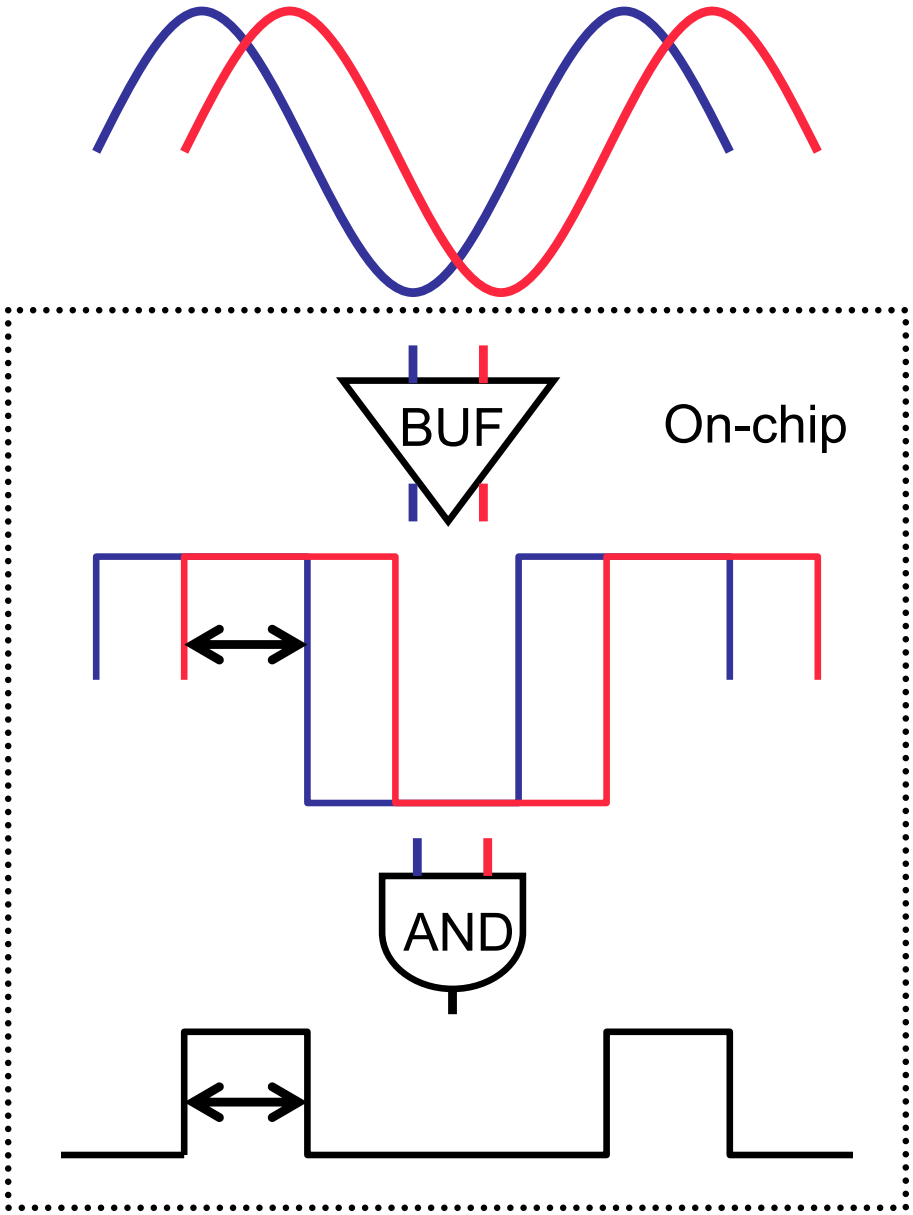
After Calibration





Sampling Clock

- Requirement
  - Variable duty-cycled clock for prototype
  - Low jitter requirement for sub-sampling
- Solutions
  - External sine waves
  - Careful layout
  - Big buffers

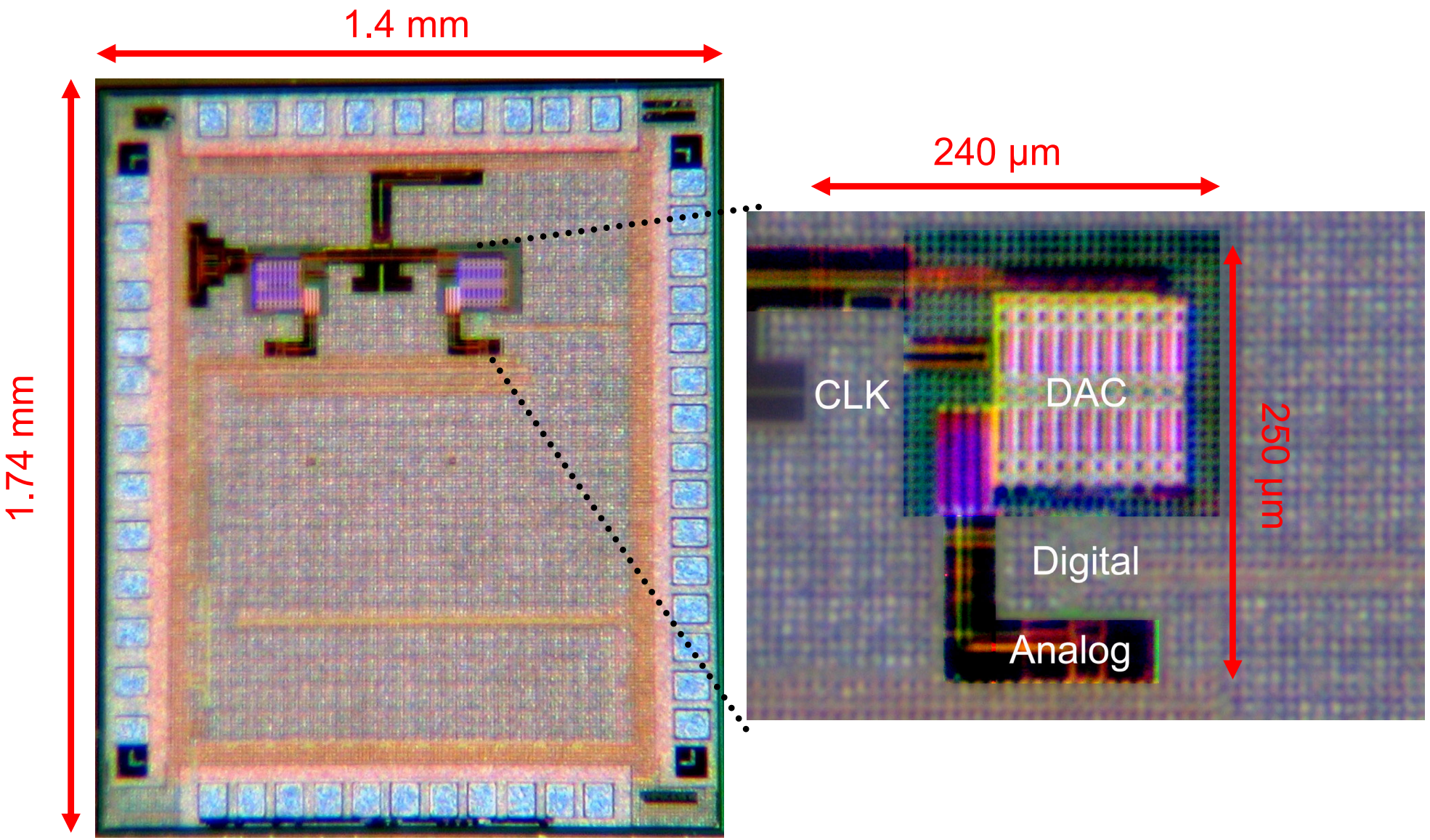


Enabling Techniques

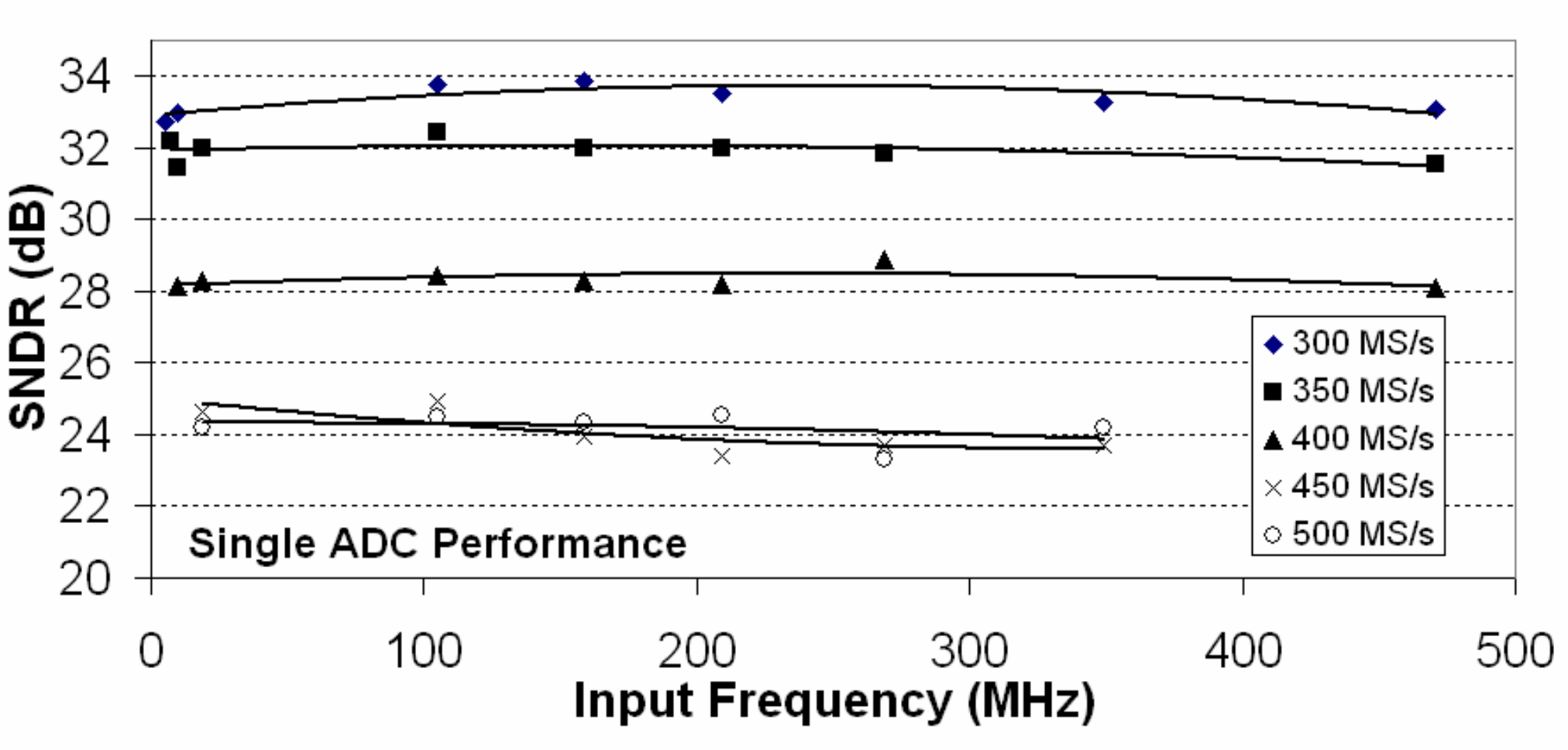
- Architecture to speed up SA algorithm ⇨ Asynchronous ADC architecture
- Critical circuit to enable async. conversion ⇨ Dynamic comparator
- Fast settling time
- High input BW

  } ⇨ Series capacitive ladder network
- Mitigate random error ⇨ Post-proc. calibration
- Minimize digital propagation delay ⇨ Dynamic logic

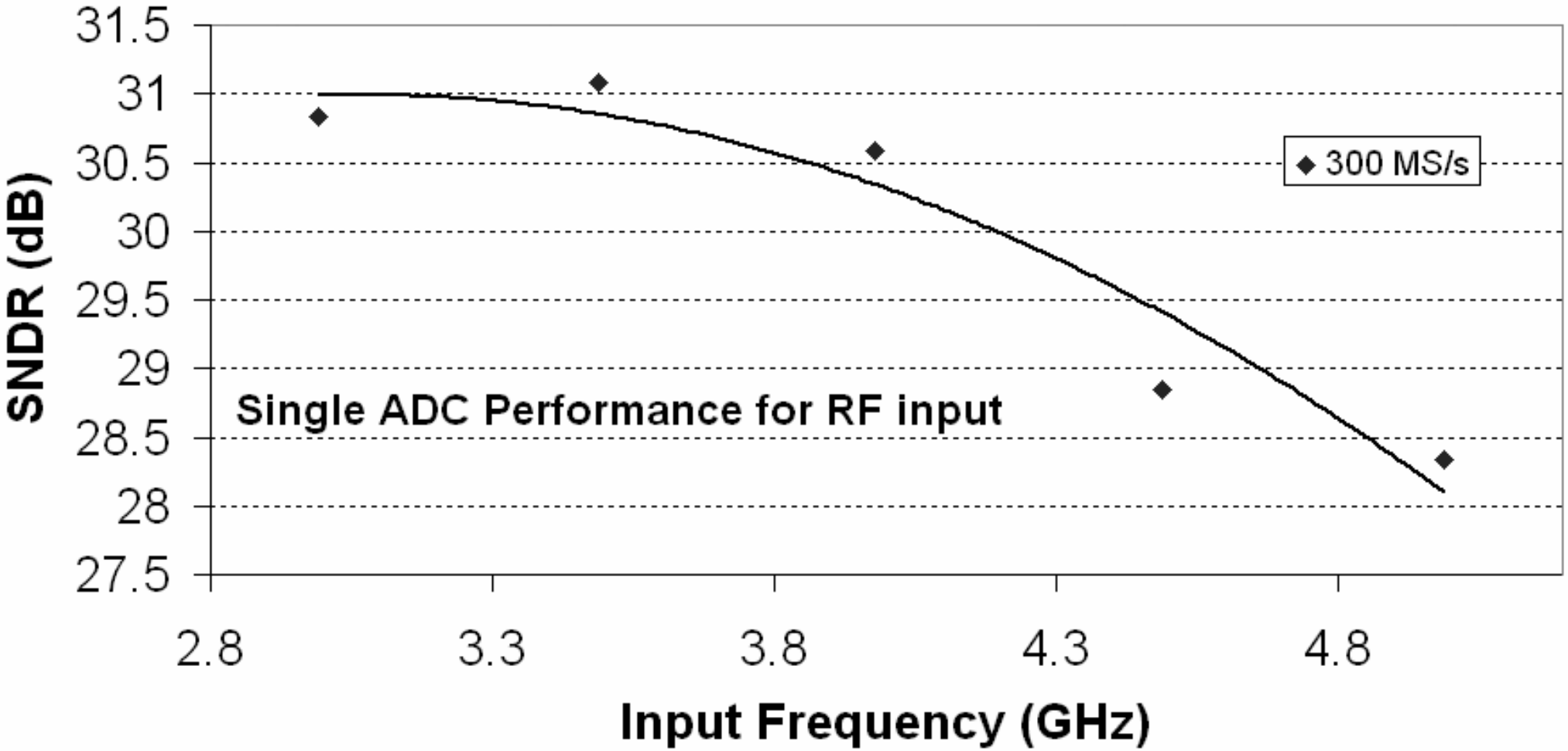
Die Micrograph



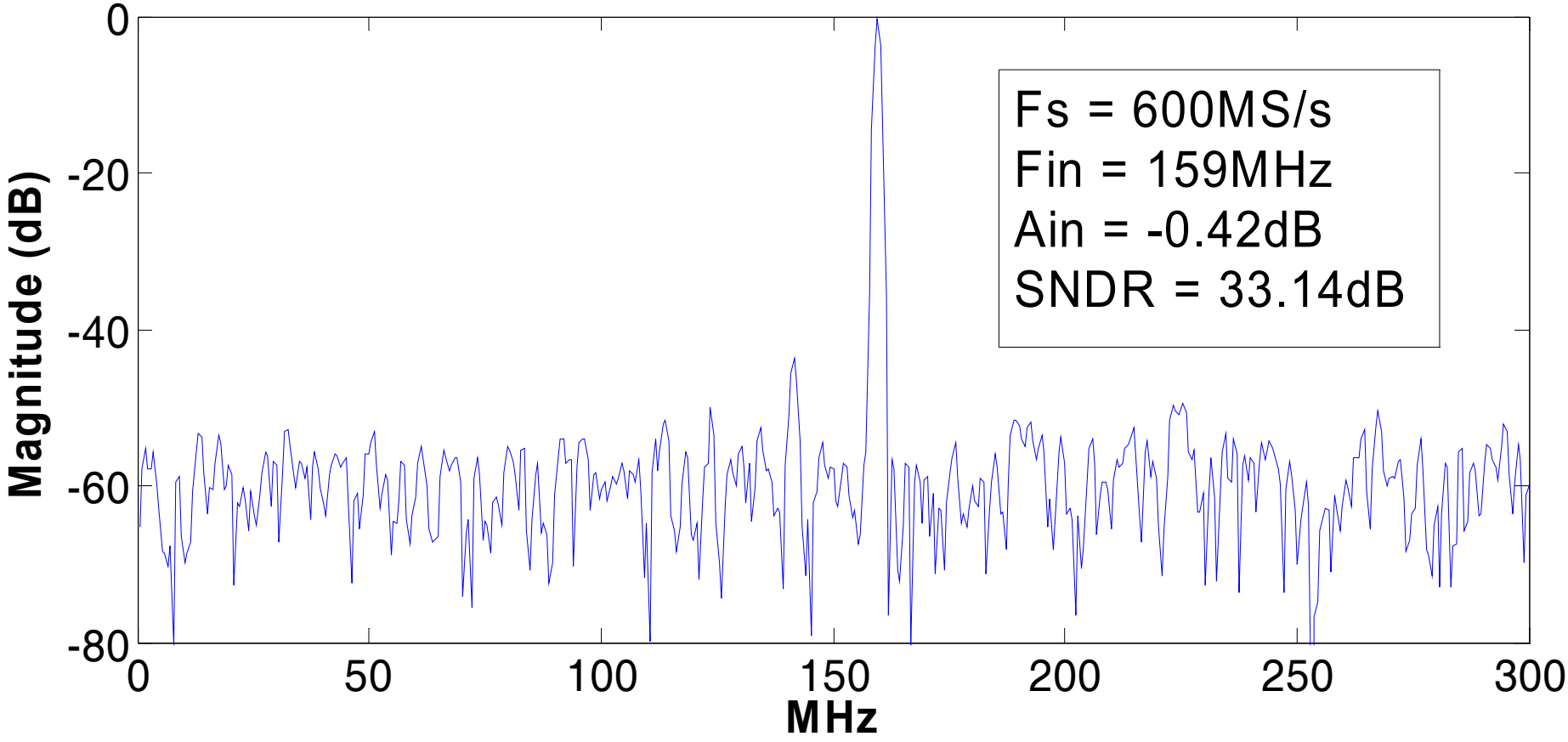
Single Async. ADC



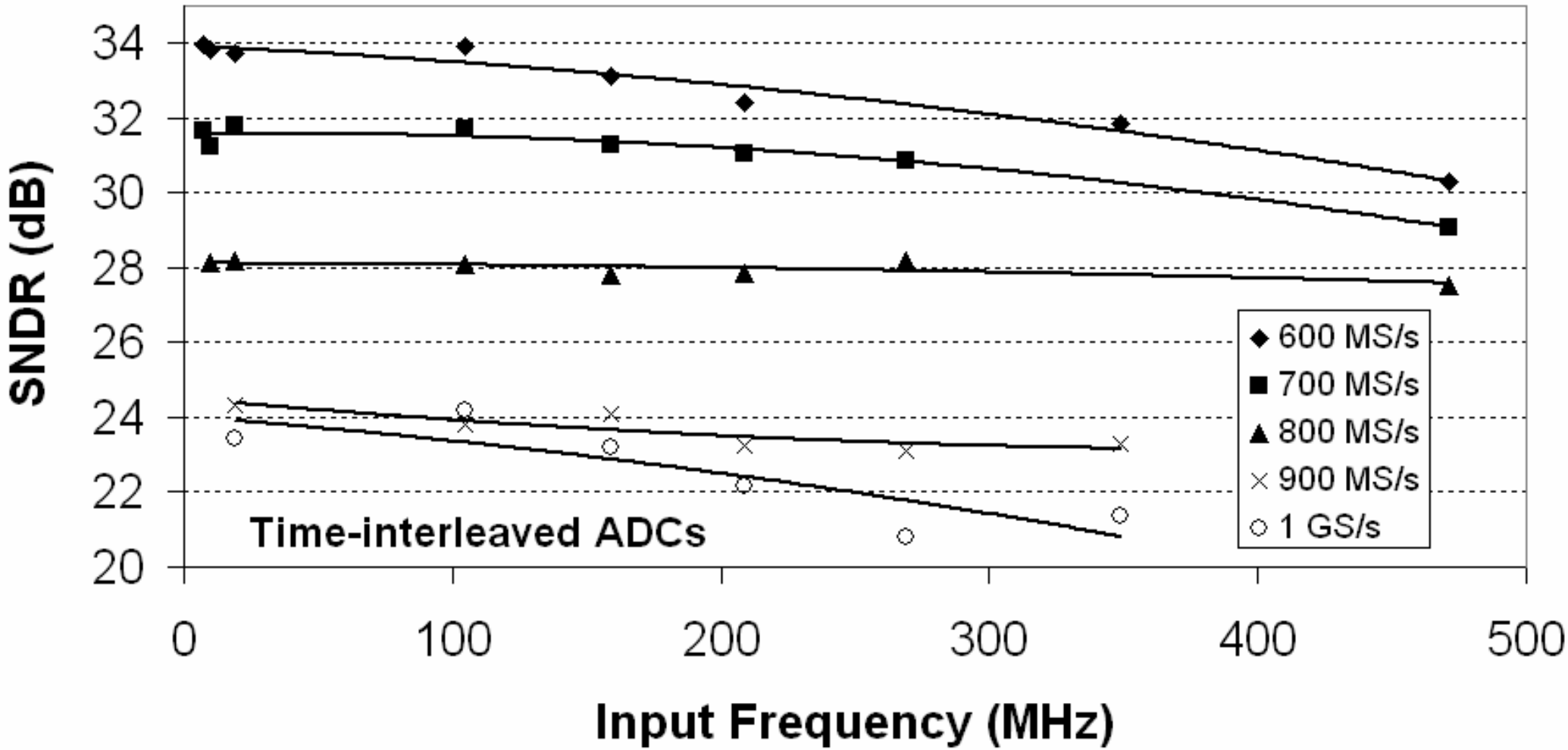
Single Async. ADC w/ RF Input



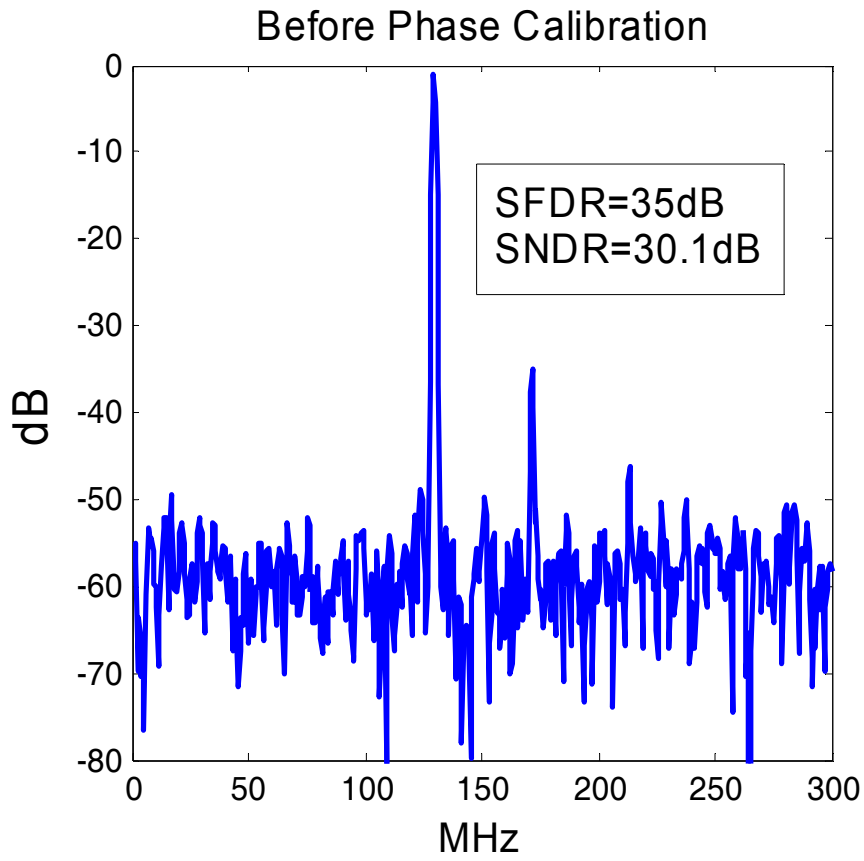
FFT Plot for Time-interleaved ADCs

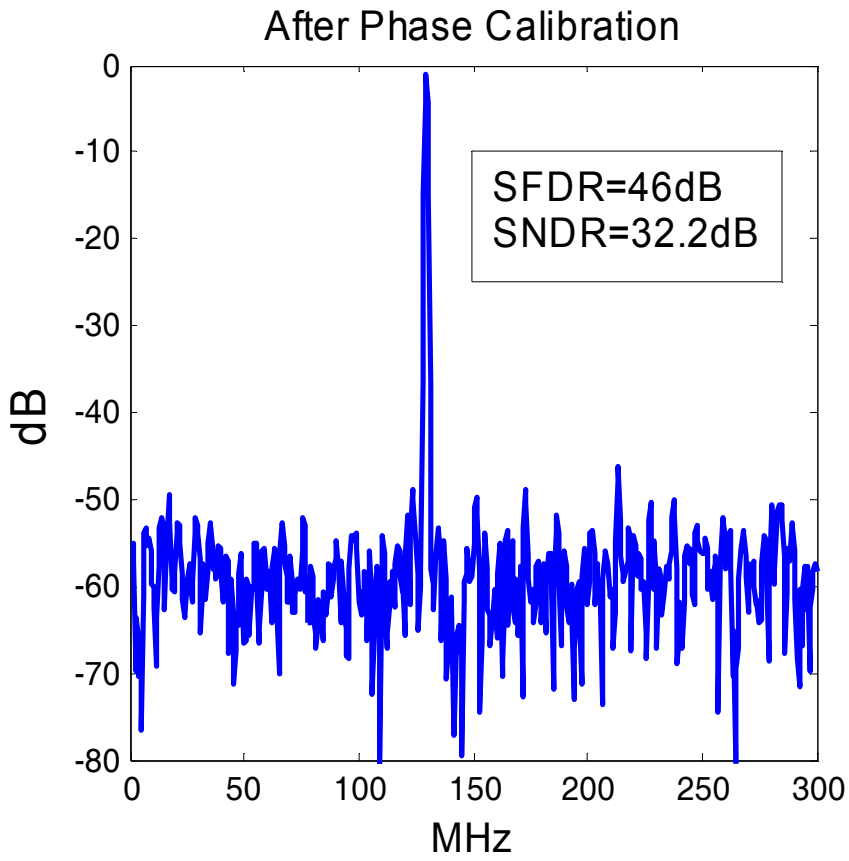


Time-interleaved Async. ADCs



Phase Calibration





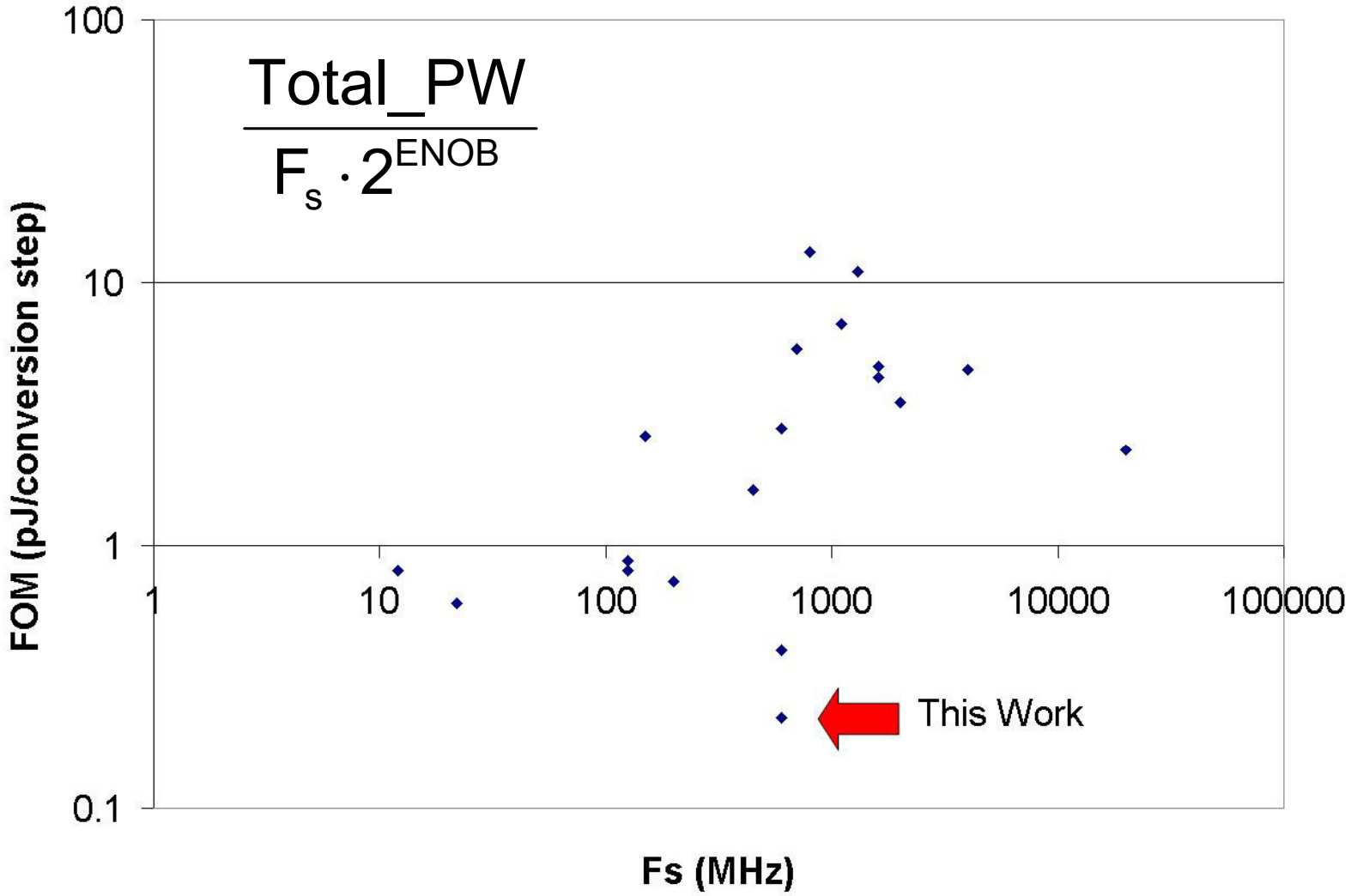
F_{in}=471 MHz, F_s=600 MS/s

Performance Summary

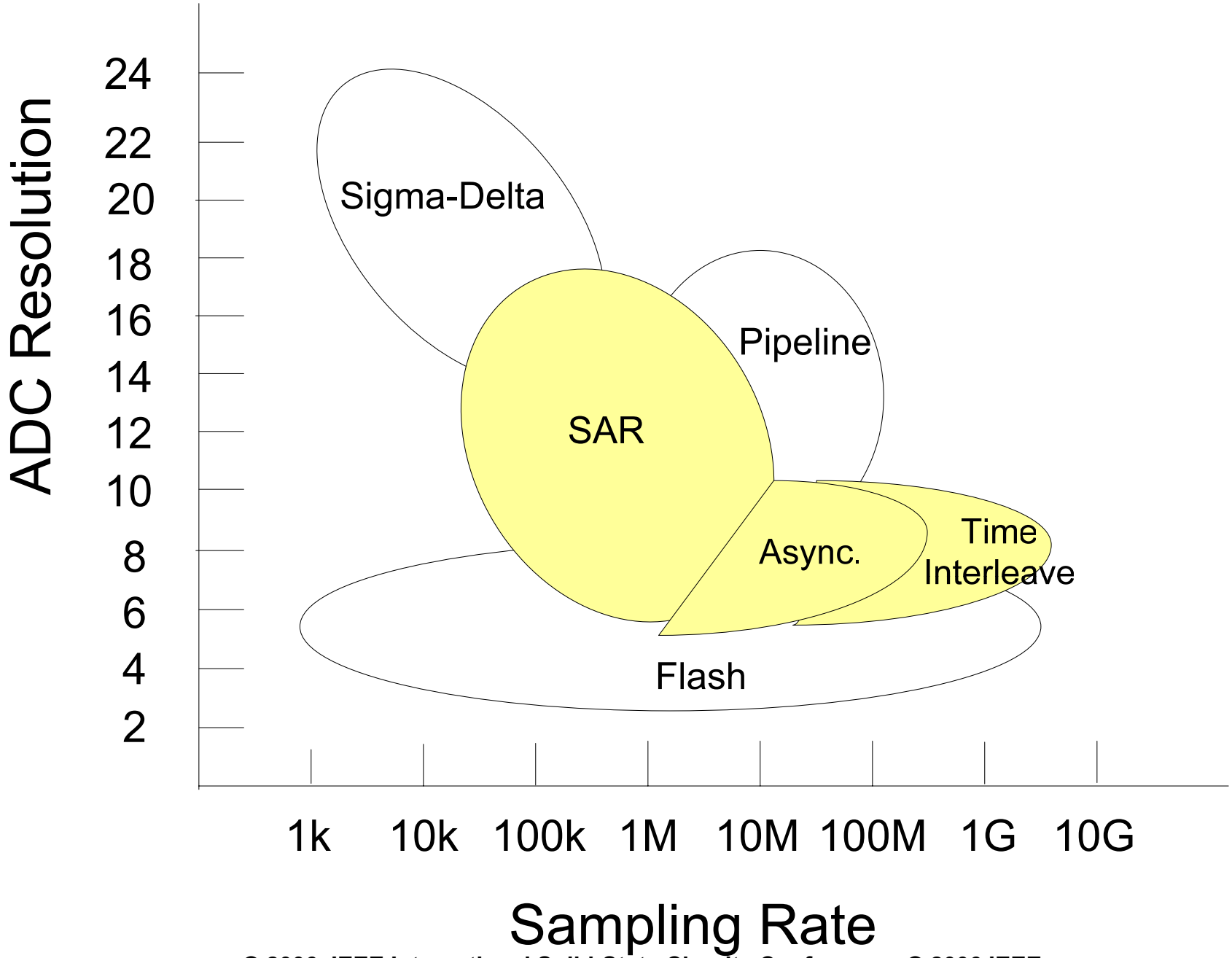
Technology		0.13-μm 6M CMOS	
Package		Chip-on-board	
Resolution		6 bits	
Sampling rate		300-500 MS/s for single ADC (600M-1GS/s for time-interleave)	
Supply voltage		1.2 V	
Input 3dB BW		> 4 GHz	
Peak SNDR		34 dB (f_s = 600MS/s for two ADCs)	
FOM		0.22 pJ/conversion step	
Power	Analog	1.2mW	Total (two ADCs): 5.3mW
	Digital	3.2mW	
	Clock	0.9mW	

Comparison

- High-speed (>10MS/s, 6-10b) ADCs from ISSCC (00'-05')



Future Role of SA



Conclusion

- In a given technology, SA architecture achieves the best power efficiency
- Series non-binary capacitive ladder enables the RF sub-sampling capability
- Asynchronous conversion and time interleaving push SA architecture into GS/s regime

Acknowledgements

- STMicroelectronics for chip fabrication
- ARO Award # 065861 for funding support
- Taiyo Yuden and Colby Instruments for donating parts