Outline of Seminar

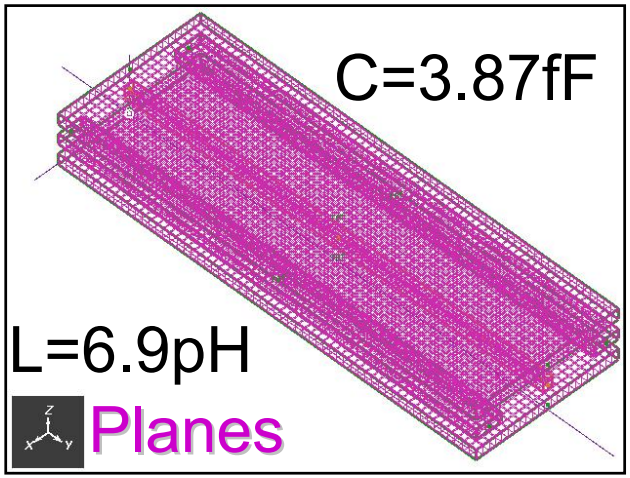
- Important concepts regarding RLC on-chip
- Difficulties and dangers of including full-chip extract
- Alternatively (or as well as) how to manage the magnetic field effects from a design perspective
  - Rules of thumb for designing robust interconnects
    - Post-layout "topology" checks for correctness
  - Waveforms illustrated in 6LM and 8LM, at 0.13μm
    - Very disturbing results for "poor" designs in worst-case
    - Avoiding worst-case behavior through length & exclusivity
- Impact of physical parameters on RLC noise/delay
- Effects of breaking reference wires.

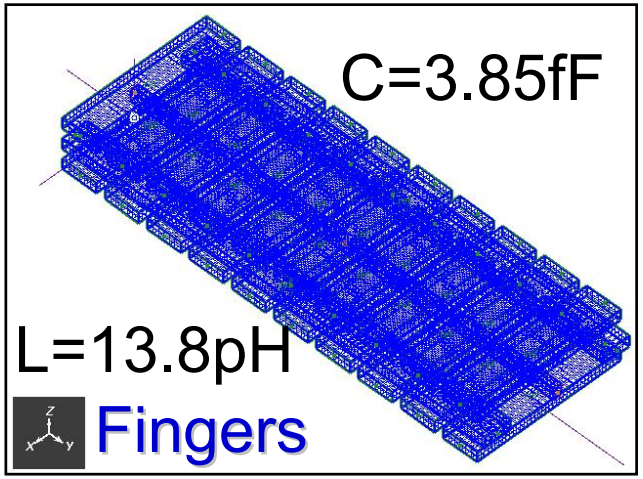
The Essence of Inductance

- Only has meaning in the context of a loop
  - A wire in and of itself has NO inductance
  - A loop must be broken into 2 open segments for ports
  - Loop inductance can be arbitrarily split across segments
- But… 3D extract of two open wires $\Rightarrow$ 2x2 matrix ?!
  - Assignment is arbitrary. Consistency achieved by referencing to infinity. Only matters that $L_{loop}=L_1+L_2-2M$
  - Can also assign a reference to remove arbitrarity
- Potential differences have limited meaning across die, unless references are $\approx$static through sufficient design

Myth: $\sqrt{LC}$ is a constant

- Tempting to compute capacitance, and infer the inductance "assuming" $v = c/\sqrt{\varepsilon_r} = 1/\sqrt{LC}$
- WRONG! It assumes two important properties:
  - Conductors are loss-less (no skin effect)
  - Waveguide is uniform (no orthogonal routes)
- Coupled systems have VERY complex modes



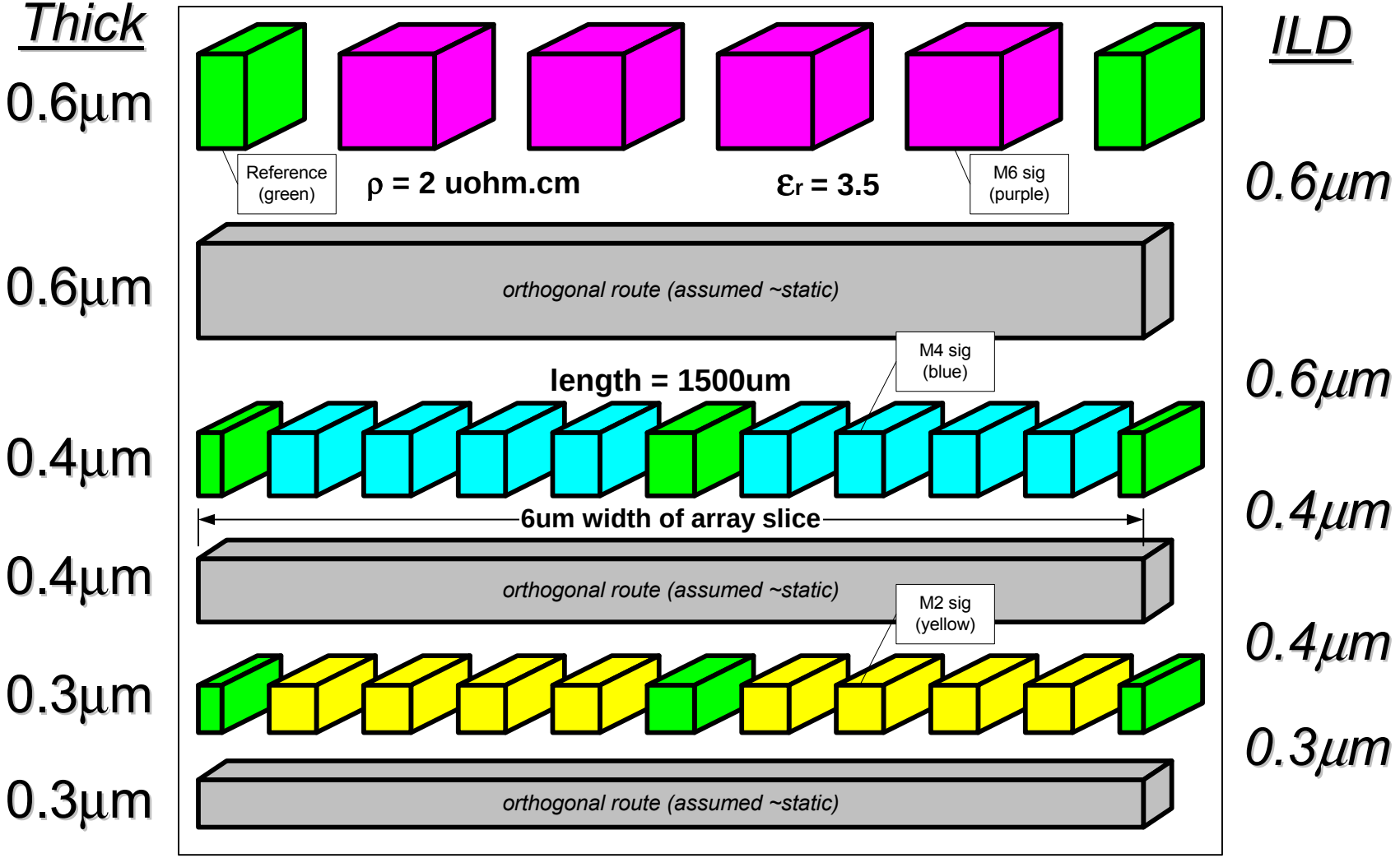


Importance of return path resistance

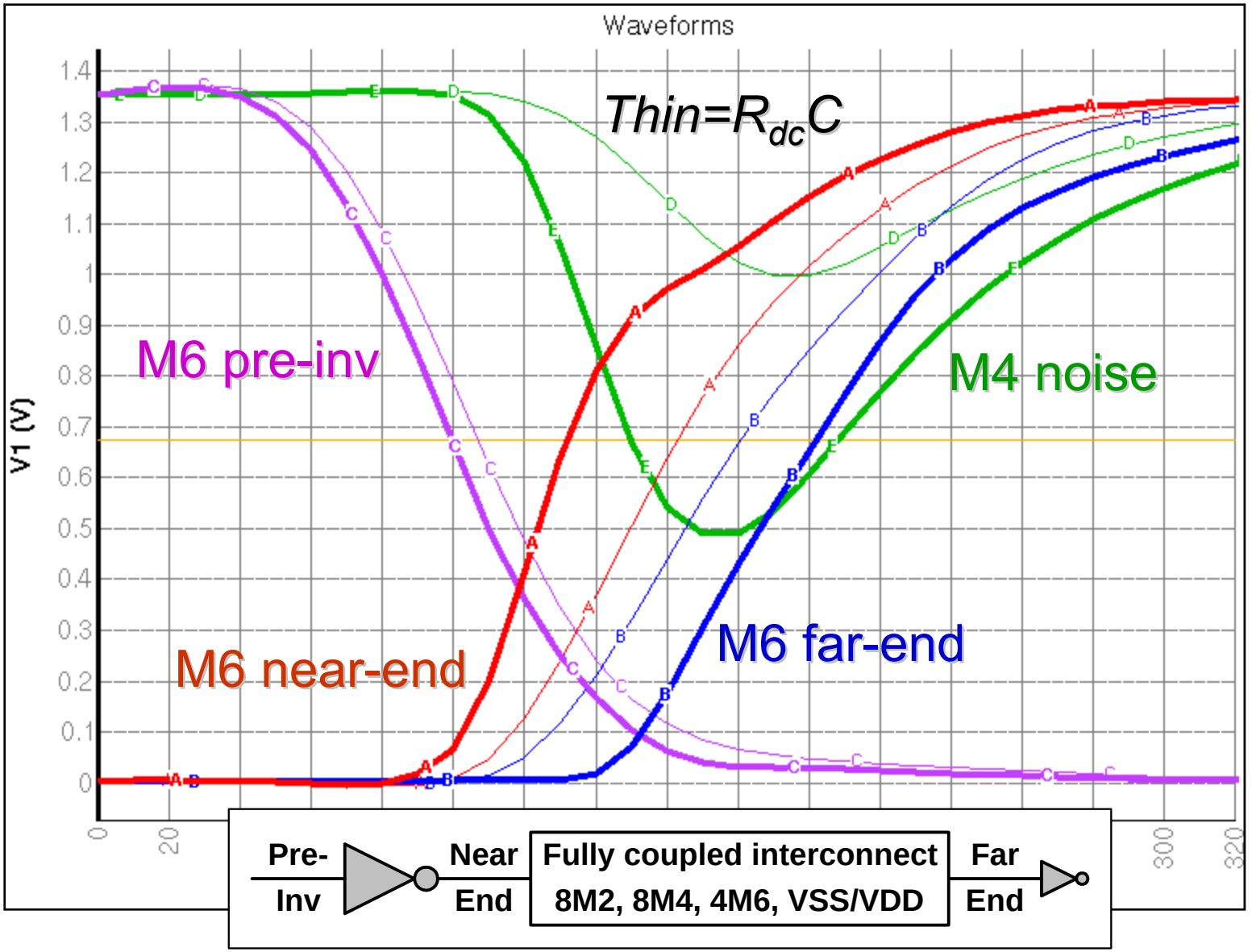
- Inductance has NO meaning without also considering the resistance of the return path
- Signal : Reference (SR) ratios are not sufficient
  - Return path resistance, which completes the inductive loop, MUST also be designed for
  - On-chip, return paths are SHARED across many signals
- How should signals & power be organized to achieve good signal integrity in the context of RLC?
  - Focus on coupled noise and $R_{dc}C$ delay correlation
  - Illustrated with a typical 0.13μm 6-8LM process

4:1 SR ratio with “poor” loop resistance

- Desire to have significant signal routing on all layers

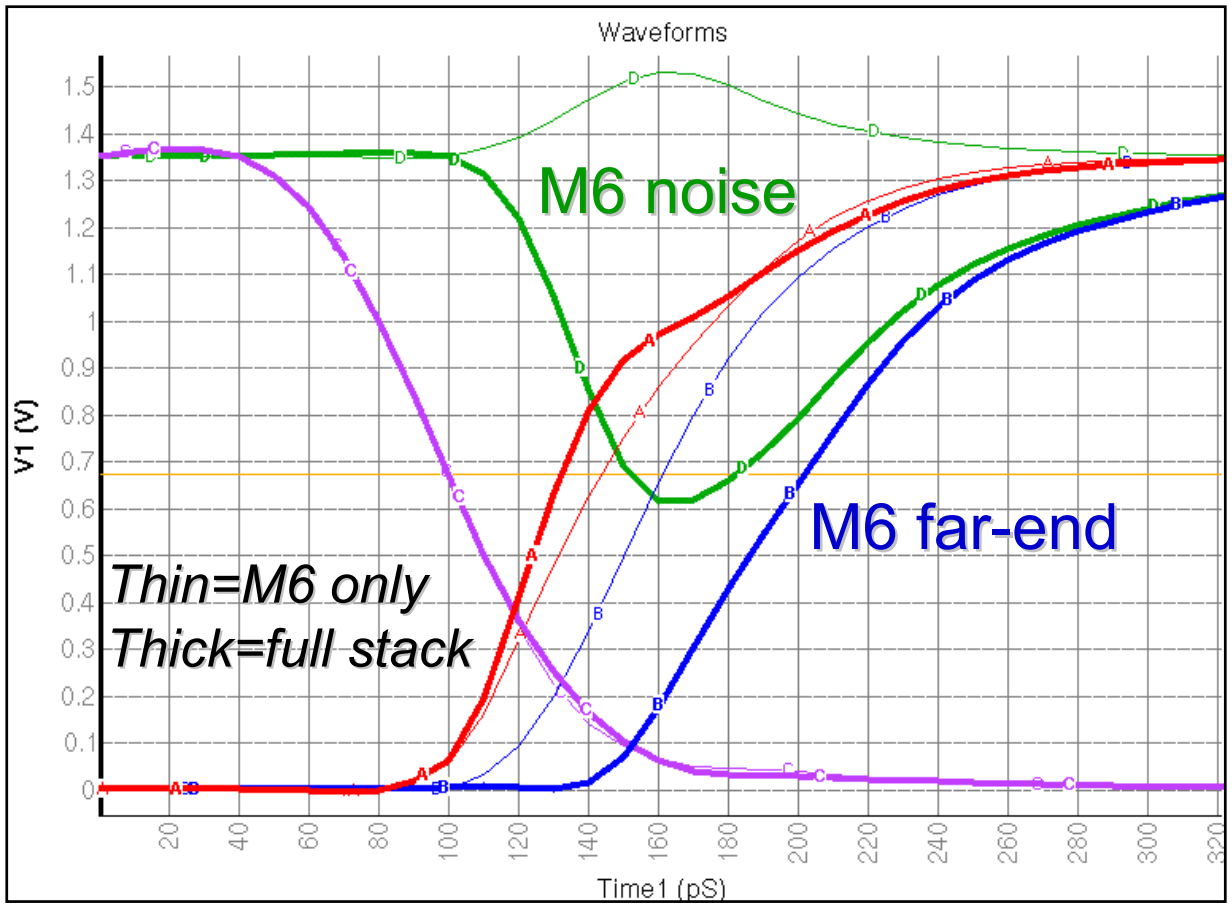


4:1 SR ratio with “poor” loop resistance



Important to extract across ALL layers

- MASSIVE error if M6 inductances extracted separately from stack



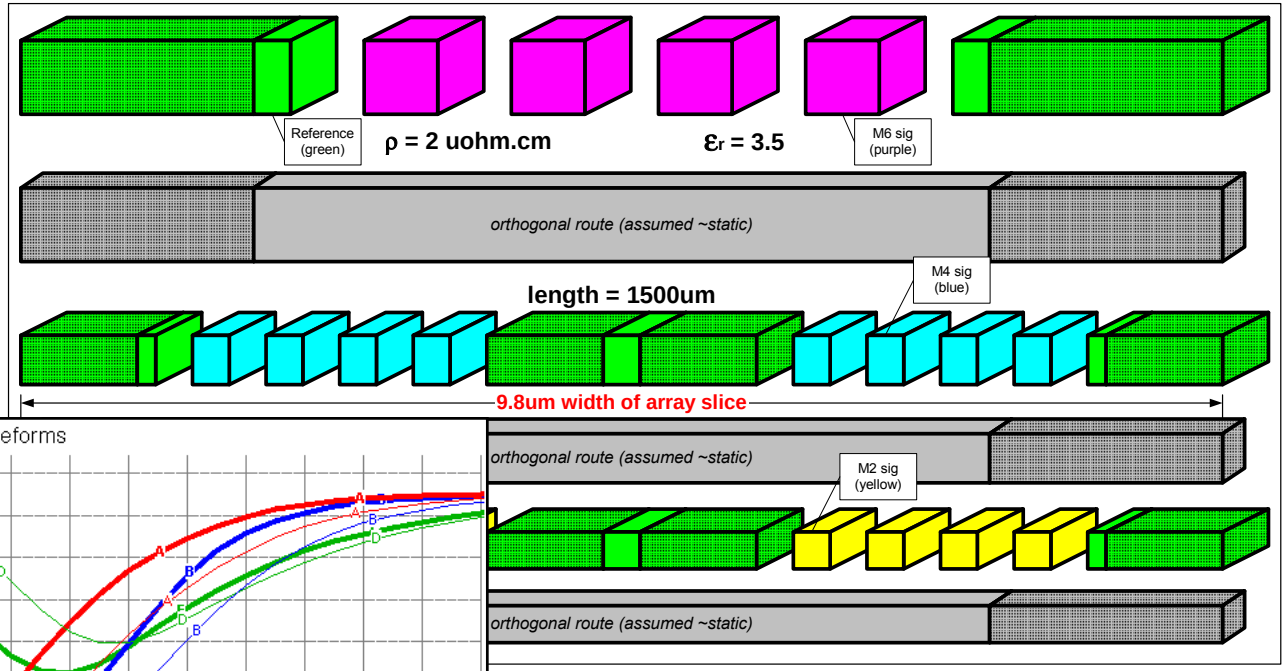
- Full w.c. loop resistance not evident due to ↑↓↑↓ nature of w.c. delay
  - Odd mode switching
  - Resistance of return path appears to be irrelevant

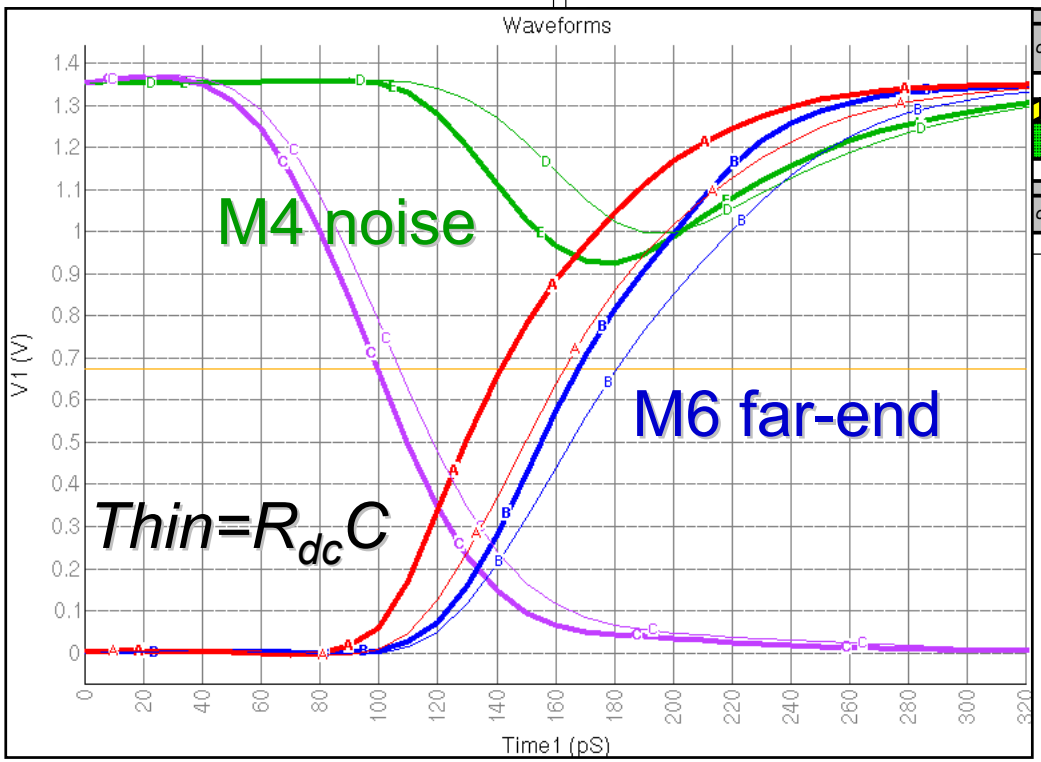
2X Rule for return resistance

- Provide at least as much metal cross-section for references as for ALL switching signals.
  - Compute overall supply area for a slice of the complete metal stack (given some regular structure).
  - Divide by the worst-case *net* switching activity across all influential signals.
  - Ensure that this number is ≥ lowest signal area.
    - Use conductances (not area) if different ρ on layers.
- Needs to be used *in addition* to SR ratios
- Thicker signal routing layers suffer more from the effects of return path resistance on delay.

4:1 SR ratio with “good” loop resistance

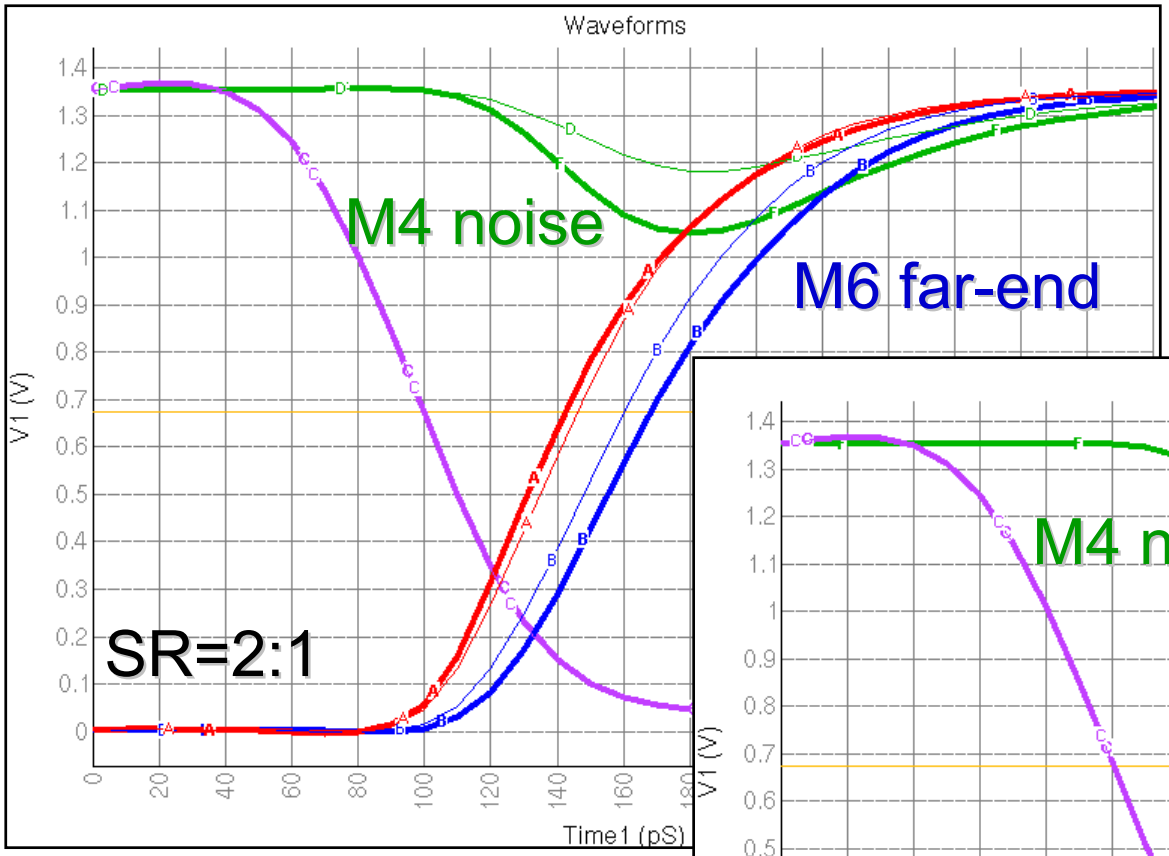
- Requires returns to be 7.4x wider than signals



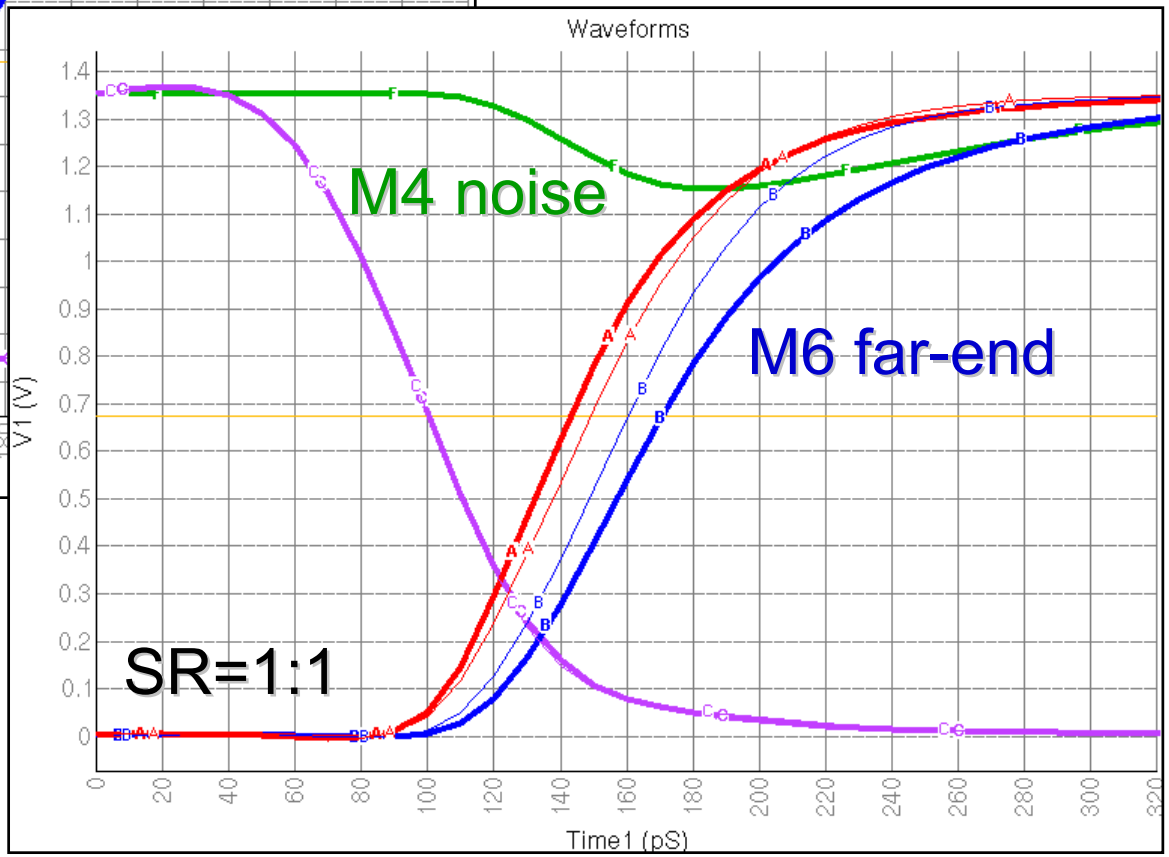


- Larger pitch (from 6µm to 9.8µm) ⇒ better off with a 2:1 or 1:1 SR ratio

Same pitch at 2:1 and 1:1 ratios



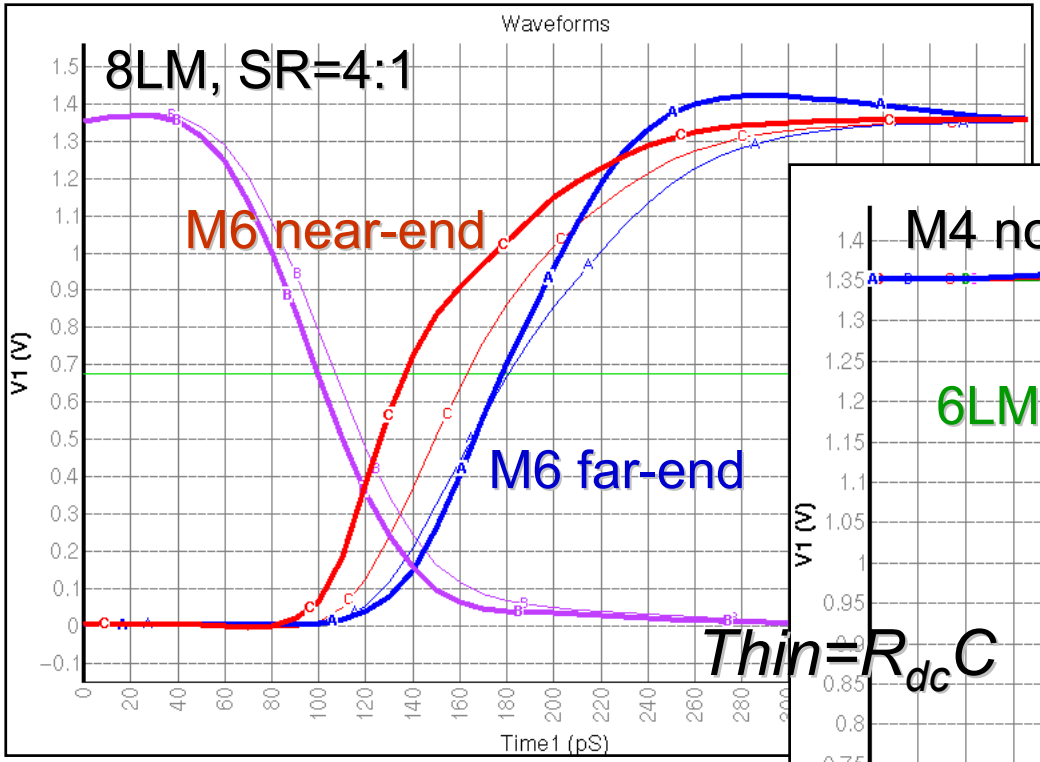
Thin=R_{dc}C response



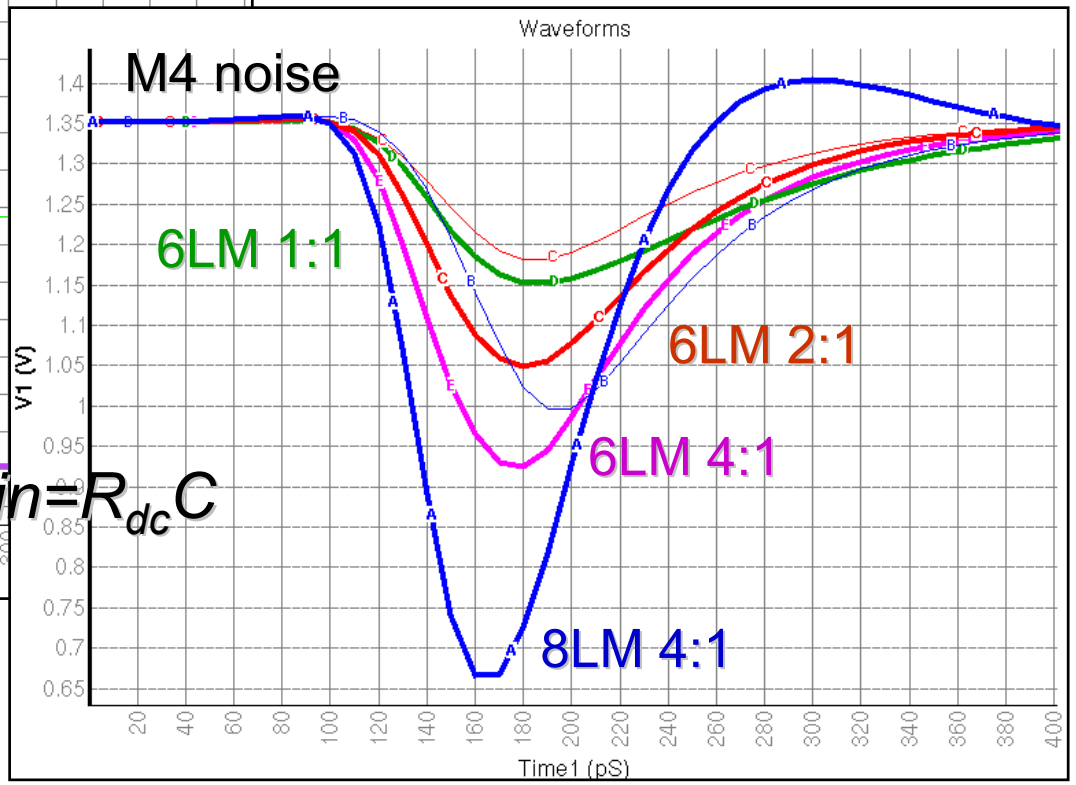
- RoT: Allow 4% per layer to “gate+IC” delay

Alternative: Thick upper level grid

- Maintains the narrow (6μm) pitch for signal layers
  - But… incur more inductive coupling between layers



2x rule requires grid thick-ness of 1.0μm (reasonable)



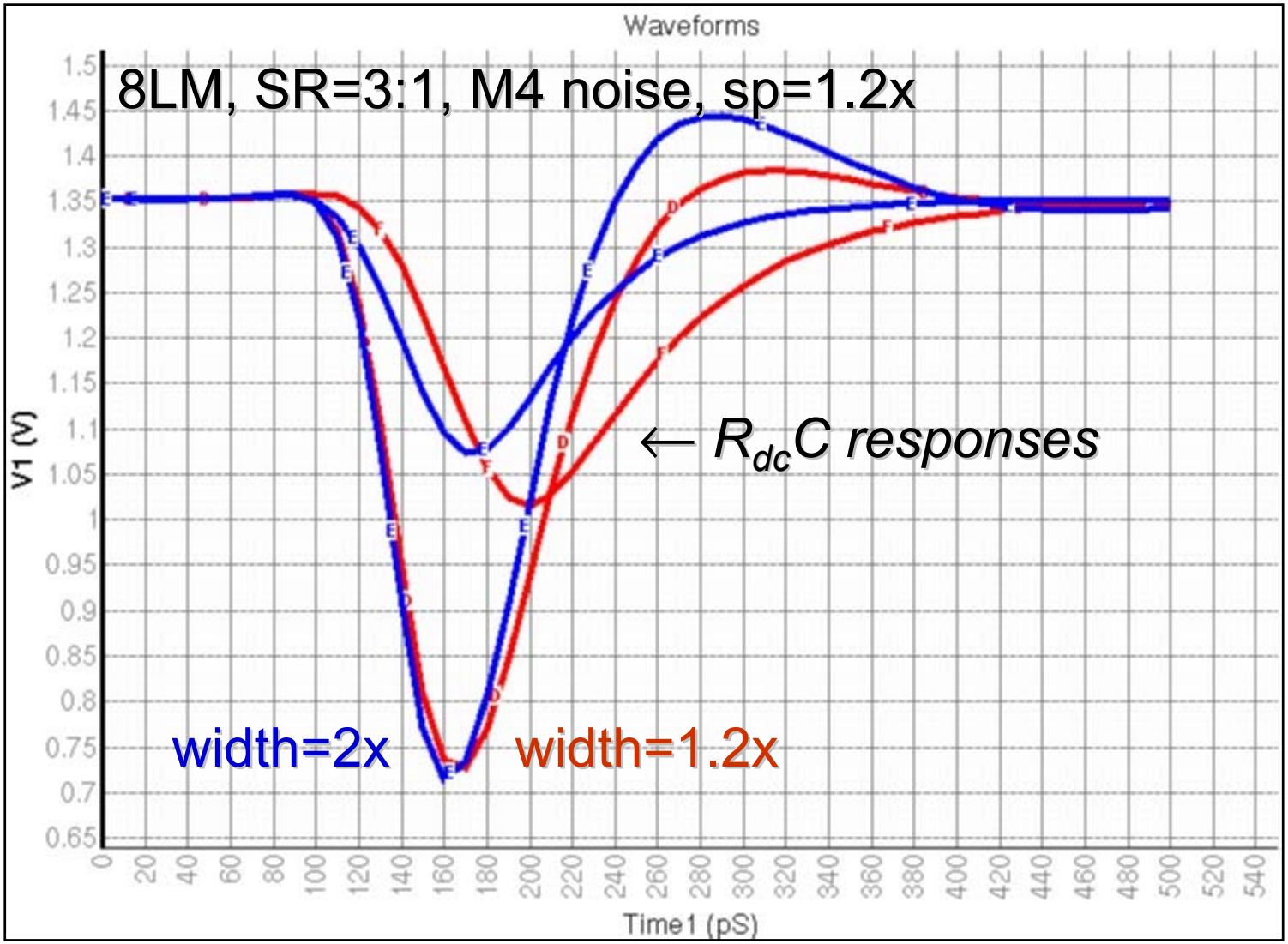
$Thin = R_{dc}C$

Reducing noise to acceptable limits

- Glitches can result in functional failures, reliability faults, and excessive cycle time.
- Under $R_{dc}C$ conditions, widening wires (for delay) would reduce coupling.
  - Of no noise benefit under RLC conditions: reduction in C_{coup} is offset by an increase in L_{coup}.
- Only effective solutions are to:
  - Improve SR ratio to 2:1
  - Increase spacing to neighbors
    - Reduction in C_{coup} is more than increase in L_{coup}
    - Must be cautious of increasing up/down C_{coup}
  - Employ techniques which incorporate exclusivity, etc.

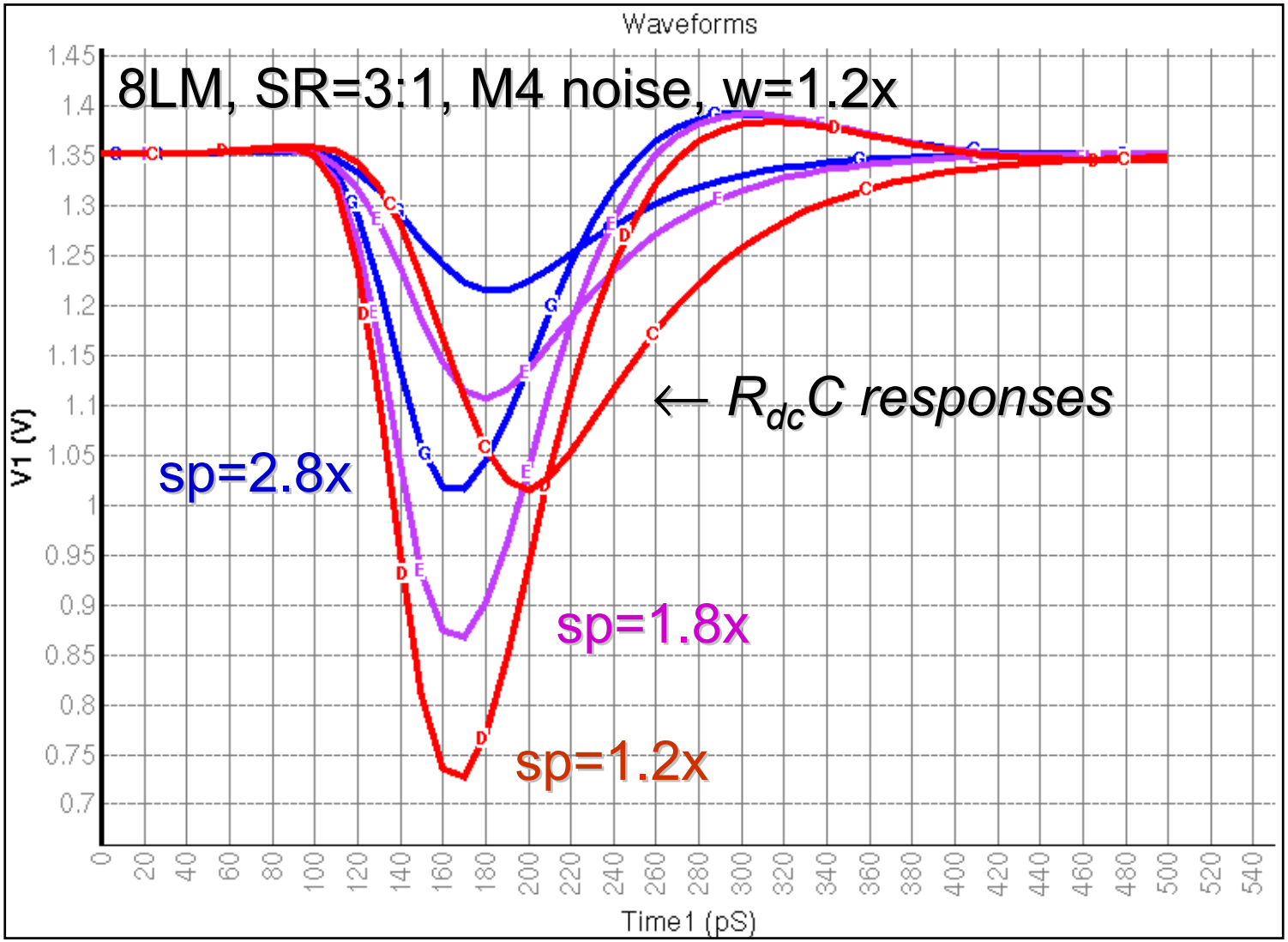
Impact of Width on noise

- RLC noise ≈unchanged, but $R_{dc}C$ indicates reduction



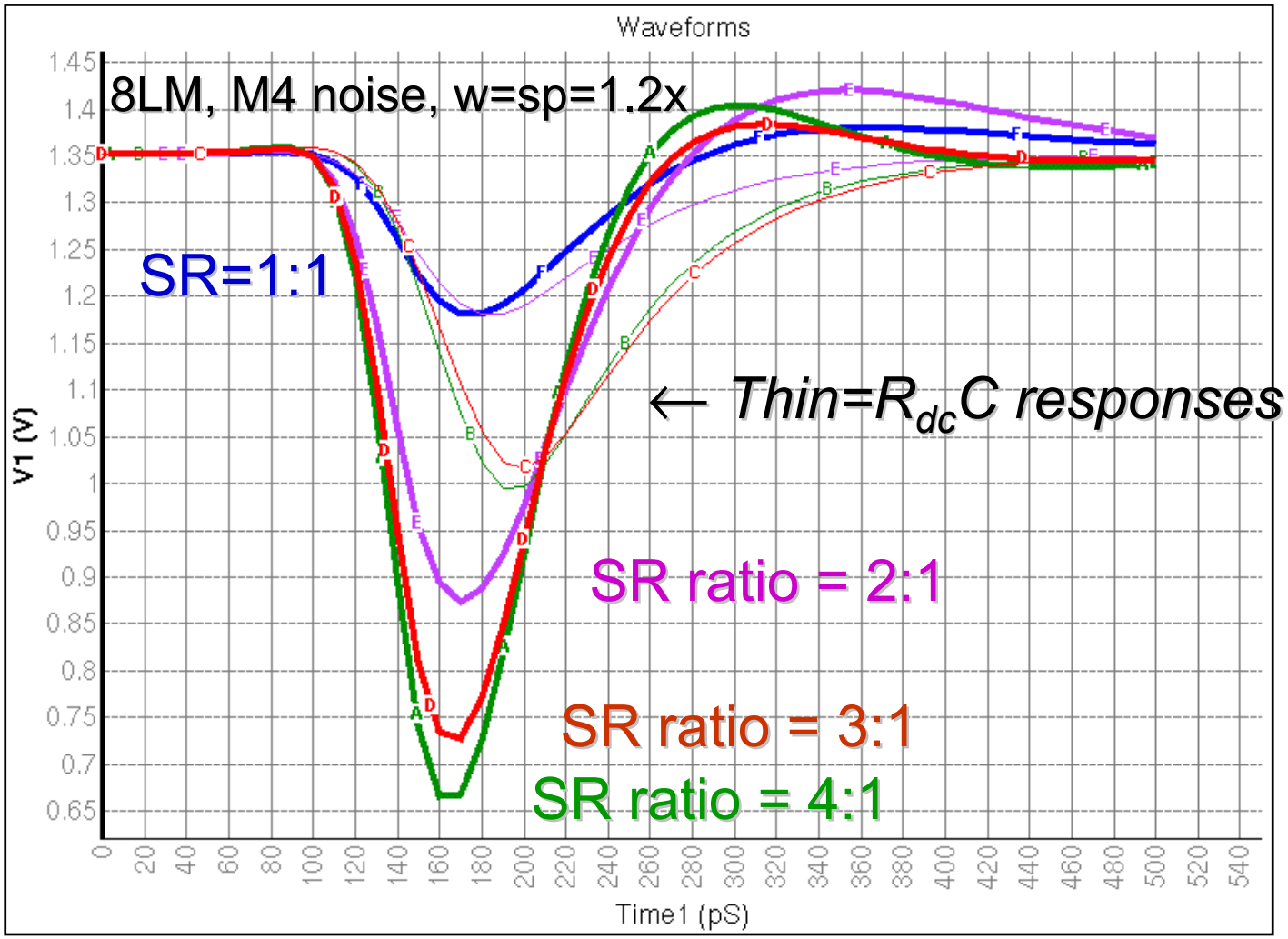
Impact of Spacing on noise

- RLC and $R_{dc}C$ noise levels reduced



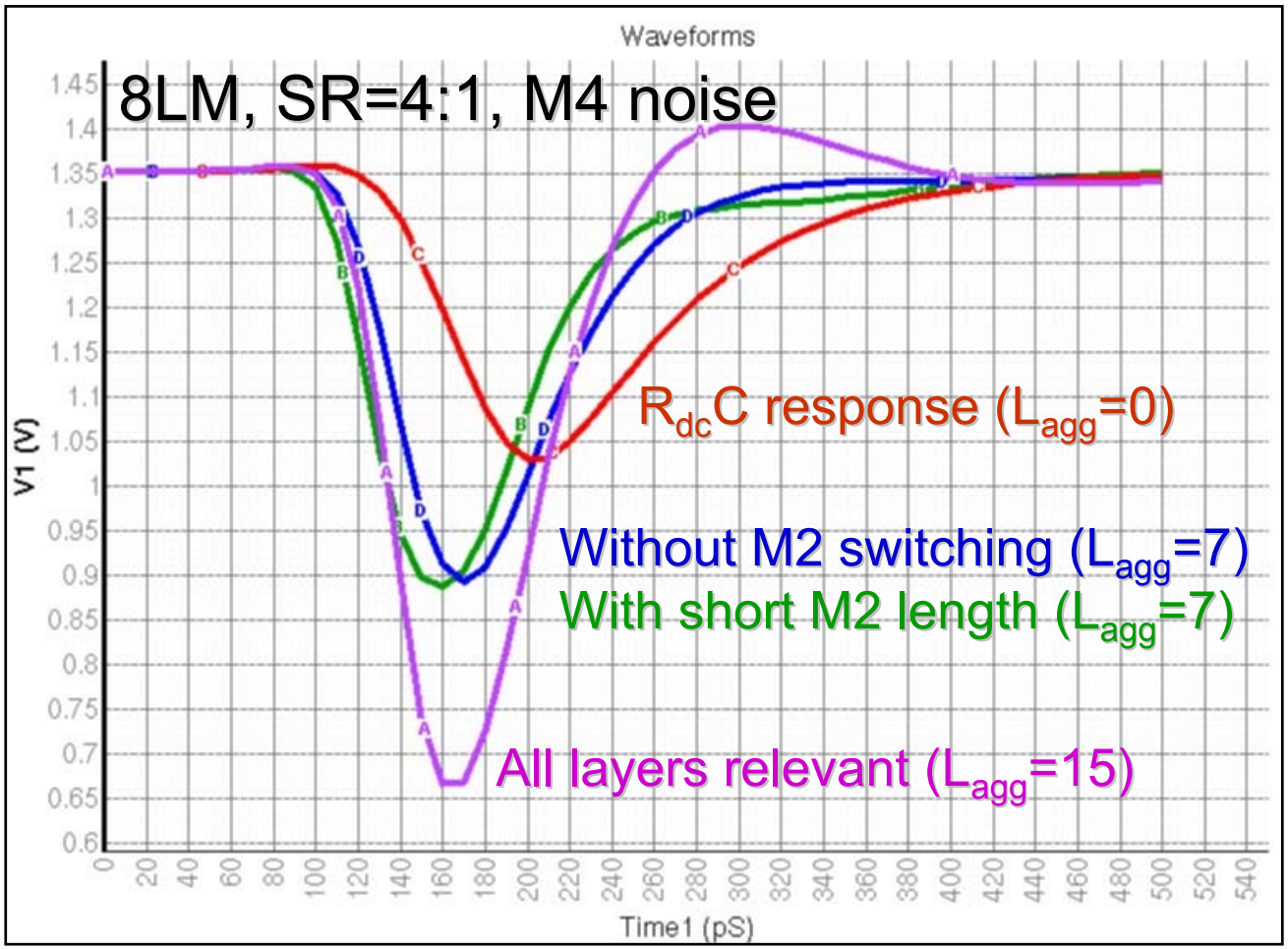
Impact of SR ratio on noise

- Noise increases sharply but plateaus at ≈3:1
  - RoT: allocate 4% of VDD per parallel layer to RC noise



Impact of Exclusivity and Length

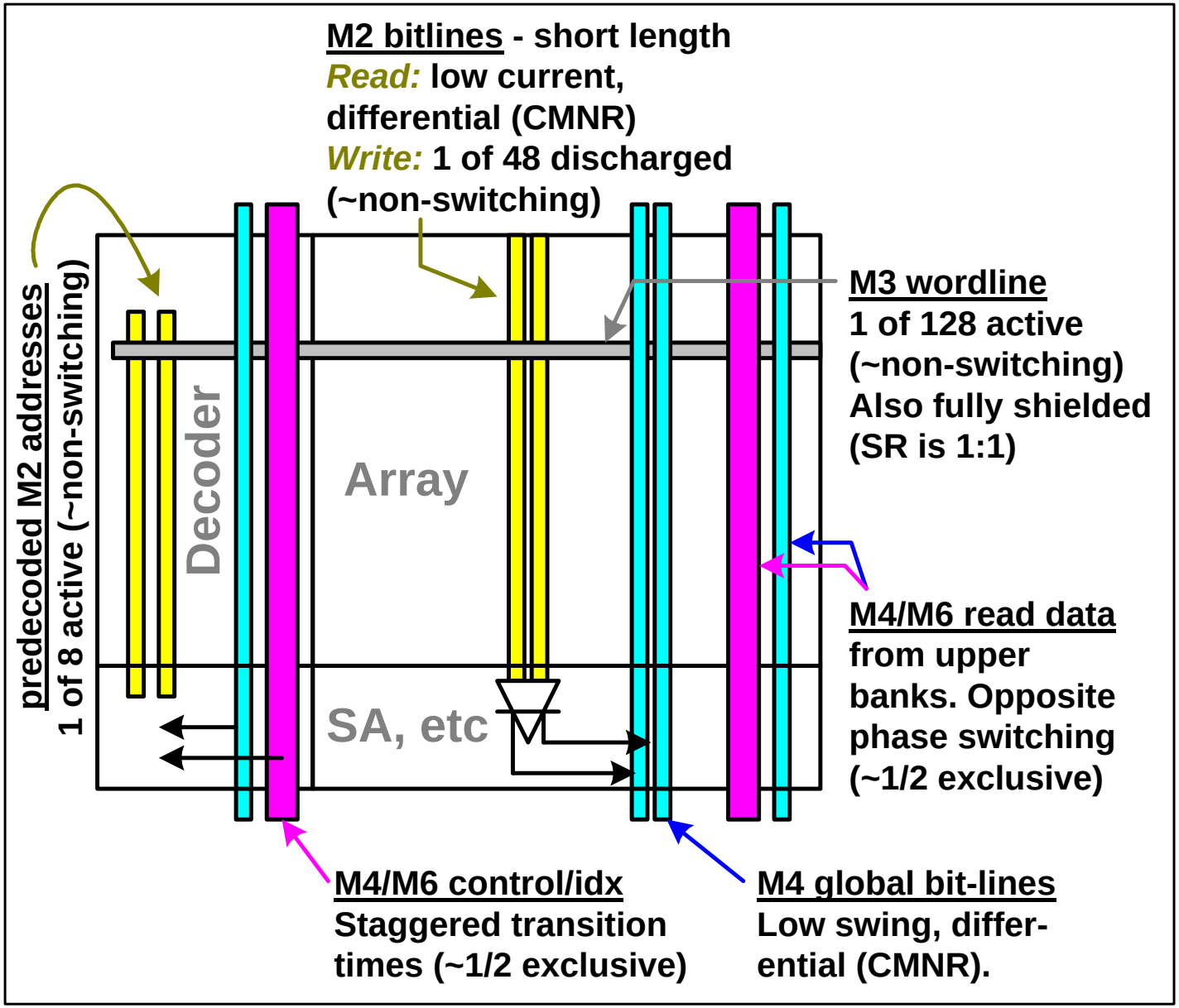
- Exclusivity and short lengths reduce the impact of inductive coupling to a victim node ≈<u>linearly</u>.



- >(3000*FS) ps between signals switching ⇒ exclusive.
- Ignore inductive coupling effect to and from nodes <(3000*FS) μm in length.

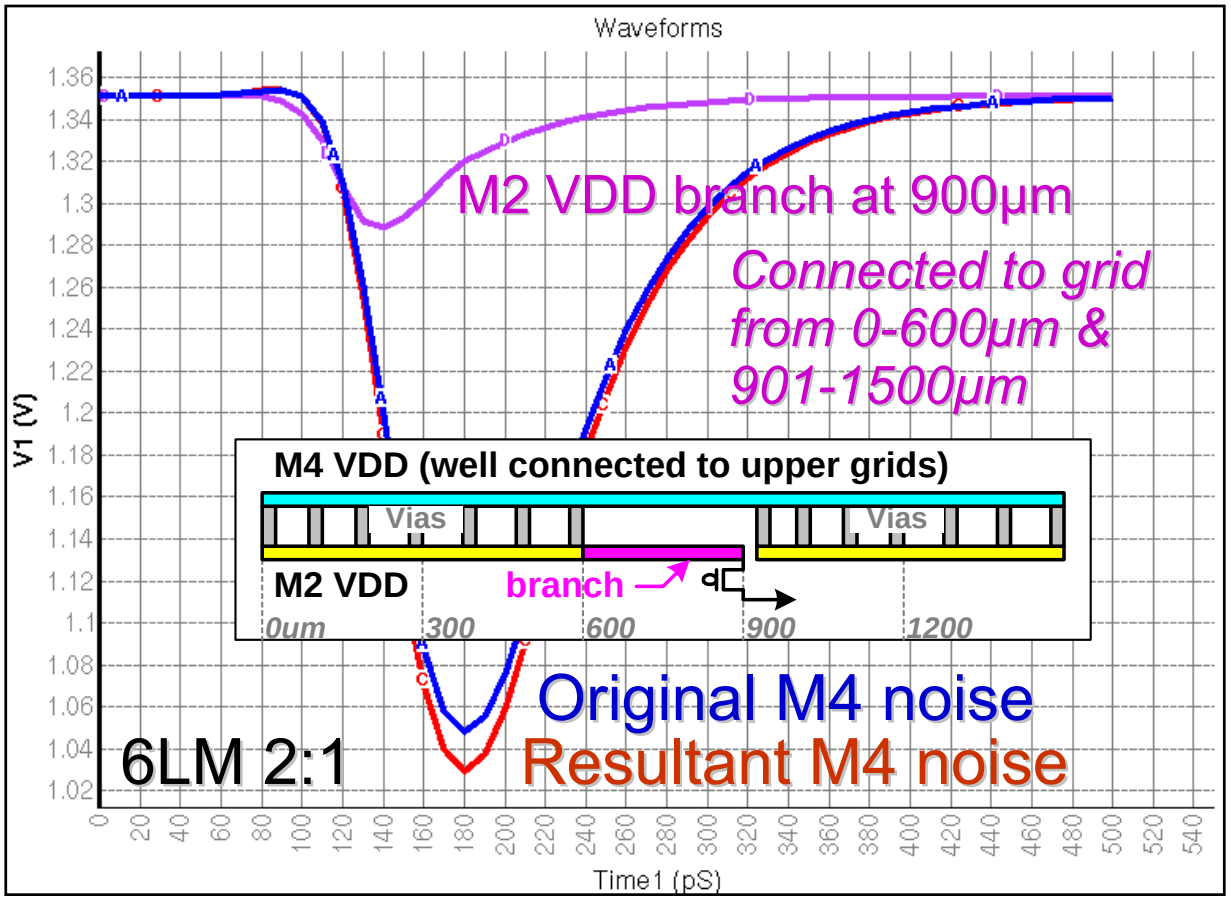
FS=feature size(μm)

Example: L2 Cache Bank for EV8



When good current loops go bad

- **WARNING**: Signal is only ½ of the loop. A partially connected reference results in a dangerous “wiggle”.



- “Wiggle” occurs on M2 VDD when 300µm midsec-tion left dangling
- M4 signal noise is also marginally increased due to wider field dispersion

Conclusions – Full Chip Extract

- Must perform extract/match across ALL layers in the stack to avoid erroneous results
- Must extract the loop resistances, not just the inductances
- Incorporation into timing/coupling/reliability tools
  - Increased run-time and memory requirements
  - Knowledge of switching activity on ALL layers required
- Reduction in risk, through improved analysis, must be traded off against increase in schedule.
- Ultimately, problems need to be fixed by topology

Conclusions – Managed Design

- Maintain the $R_{dc}C$ approach to timing & coupling.
- Analyze a range of structures/conditions that represent the bulk of the variations in routing
  - Develop general rules for global & local routes
  - Provide margins into timing & coupling limits:
    - Suggest +4% (of VDD) to coupling per switching layer
    - Suggest +4% to “gate+IC” delay per switching layer
  - Implement special DRC checks in the back-end to verify adherence to the rules
- Waivers for length, exclusivity, etc.
- Case-specific analyses for VERY critical nets

General guidelines

- SR ratio of 2:1 recommended
  - For high stacks, also use 1.5x minimum spacing
- Design X-section of references for ≤ 2x loop resistance
- Noise can be scaled ≈linearly from the worst case
- Do not break the major current-carrying return wires
- Shielded clocks also experience coupling from signals if not isolated vertically (≈ 5-10%) & vice versa
- In truth, everything influences everything else!
  - Buddhism: *The precept of Interdependence*
    - So do good things: as a person, and as a circuit designer