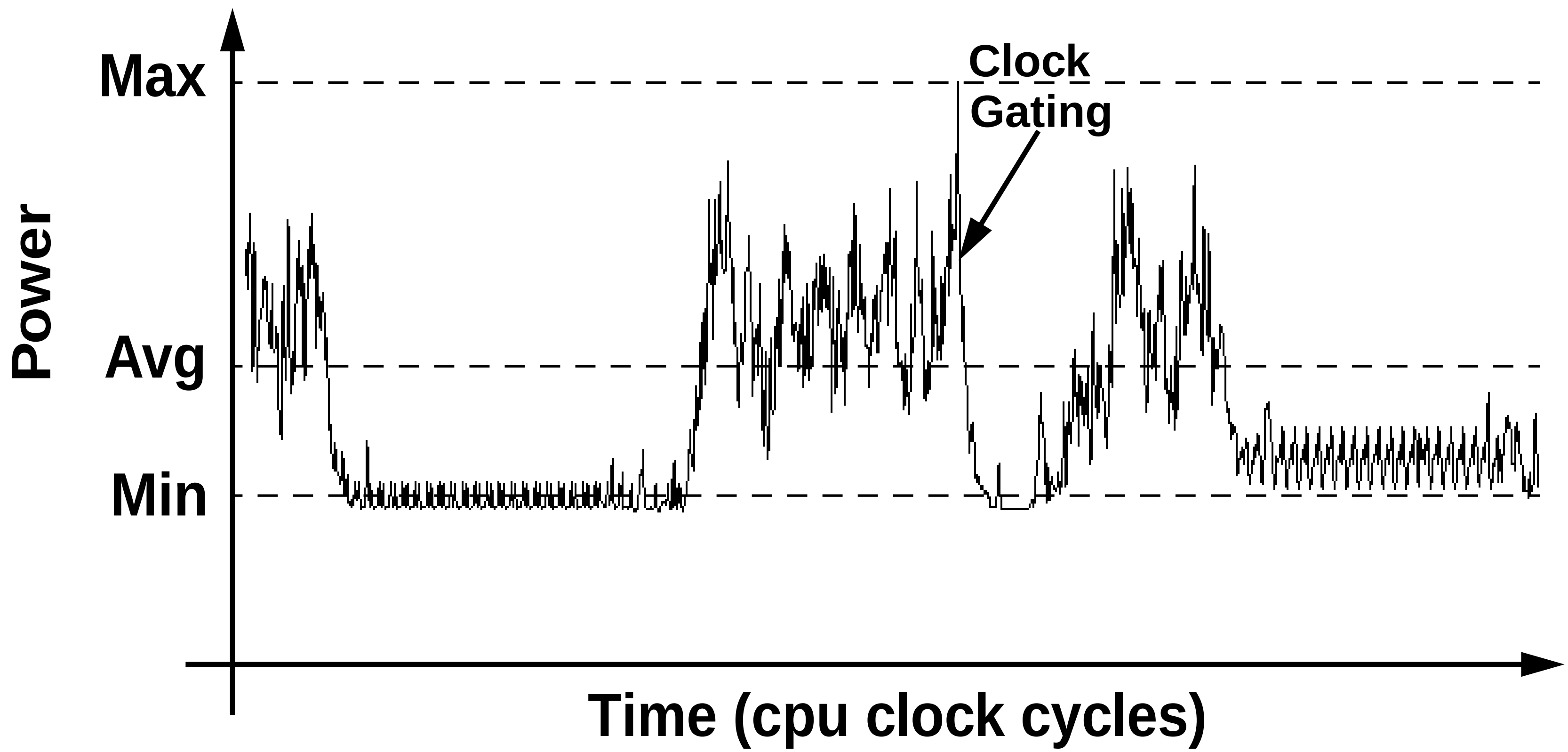
Major Electrical Interfaces

- Core Power Delivery
  - Physical and electrical view
  - Parasitic inductance estimation
  - Distribution issues, guidelines
- I/O Power Delivery and Signaling
  - Signal return current
- Summary

Microprocessor Design Constraints

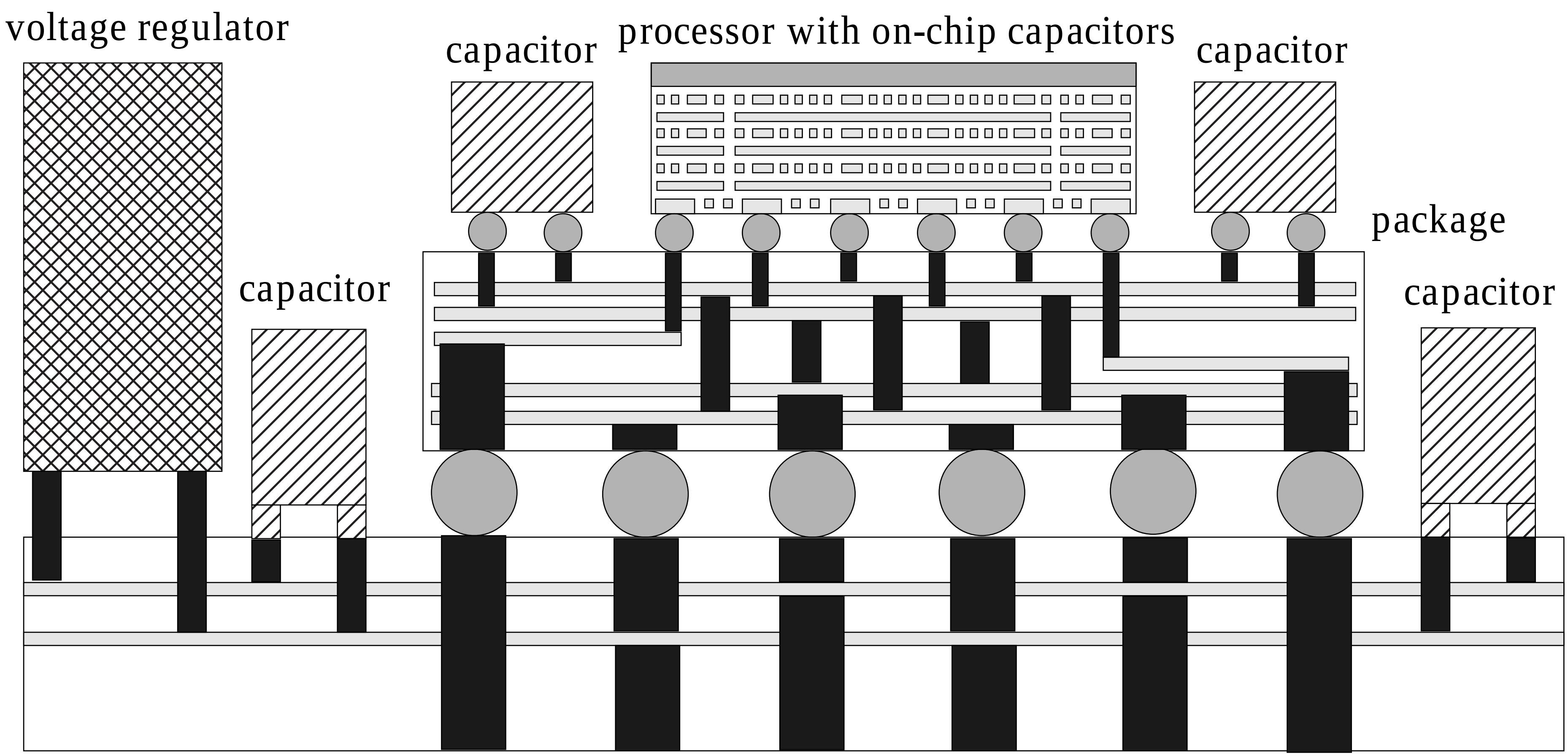
- Power supply impedance
  - $Z=(\Delta V_{SPEC})/(\Delta I_{ESTIMATE})$: Ex. 1.8-V x 5% / 10-A = 9-mΩ
  - Must deliver power over a broad frequency spectrum

Architectural Power Model To Estimate ΔI



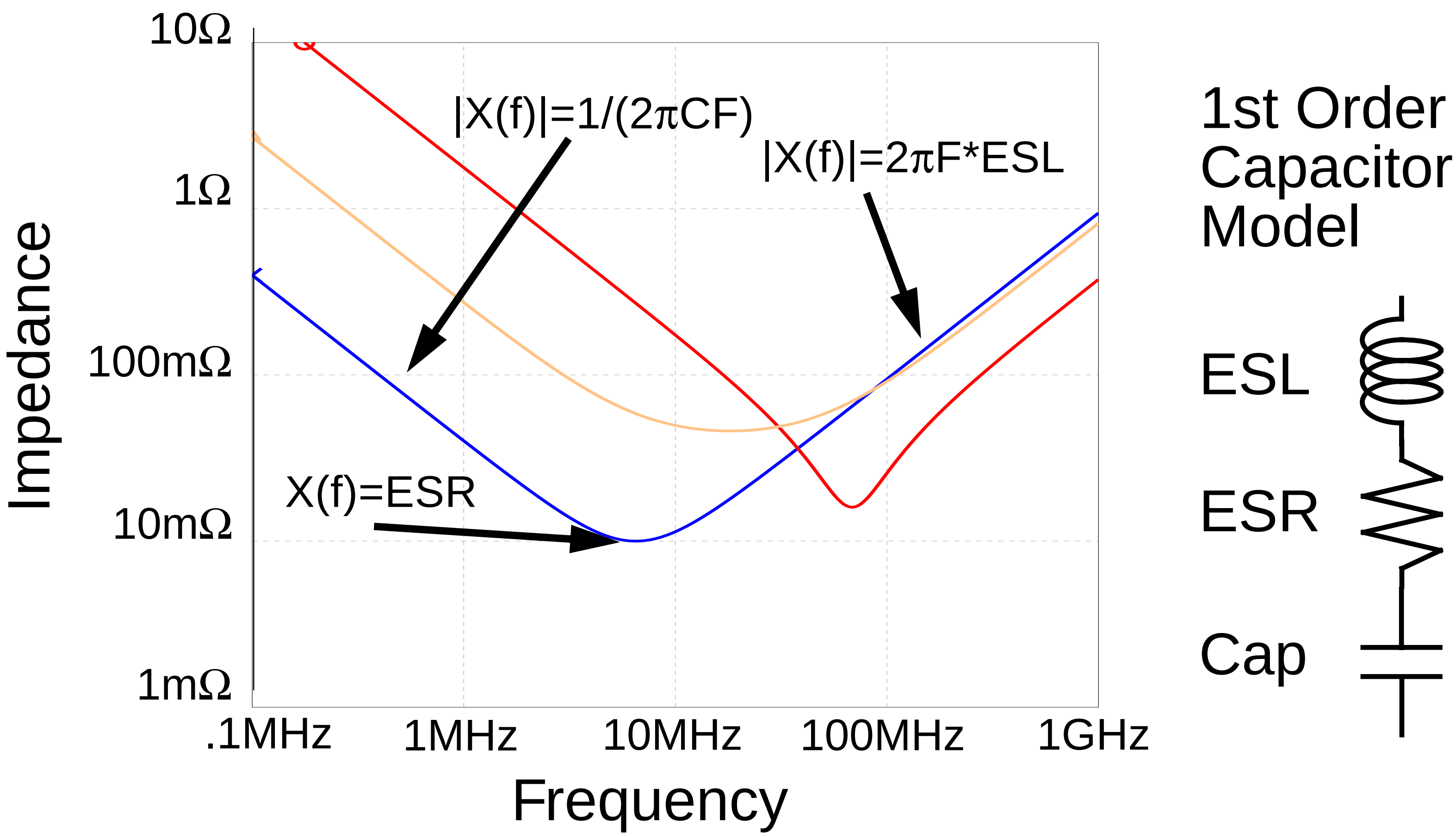
Microprocessor System

- Power perspective
  - Package types, attach strategy, board or MCM type, package/board layer assignments, decoupling capacitor requirements.



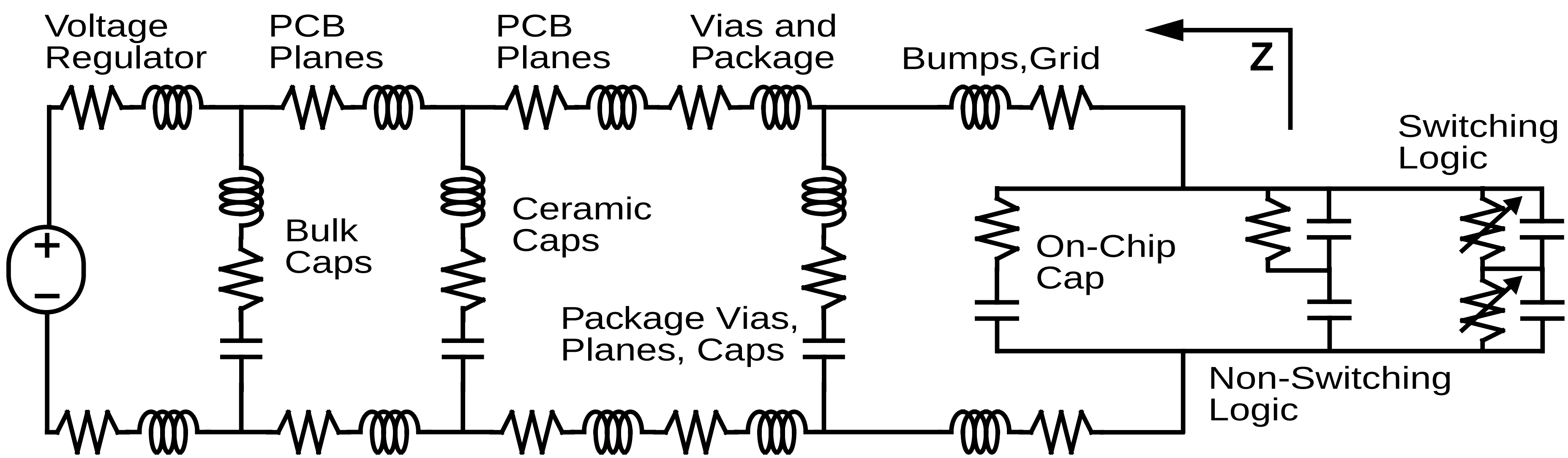
Decoupling Capacitor Modeling

- Wide range in performance and cost
  - Example: 3 different capacitors

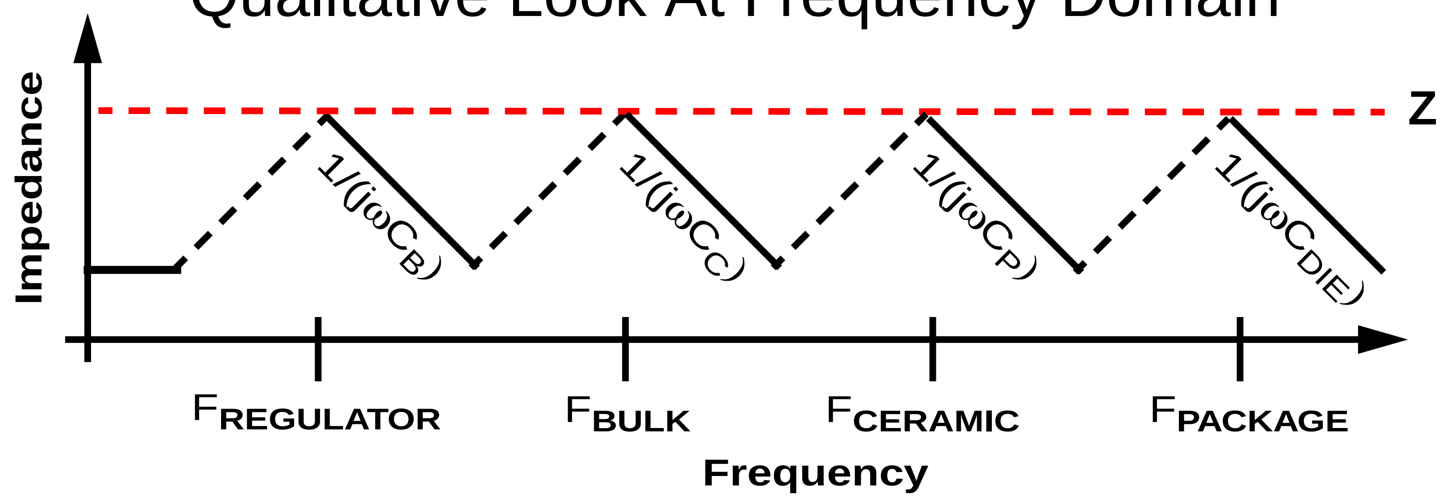


- Parasitics between banks must be included

Low Frequency Electrical View



Qualitative Look At Frequency Domain



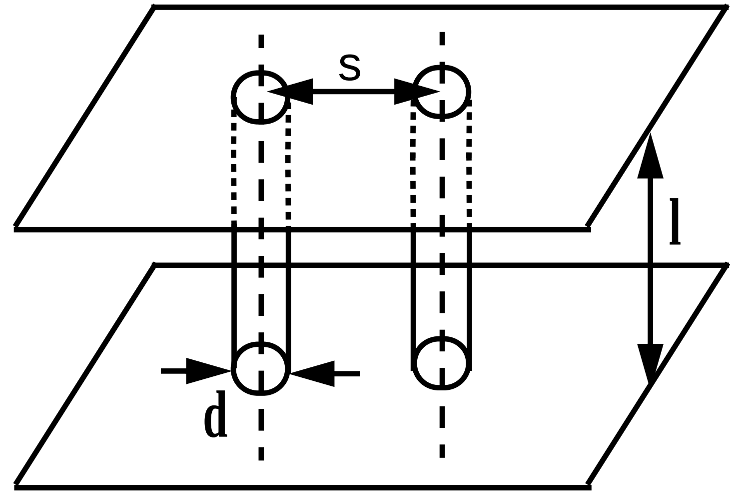
Inductance of Vias, Pins, Bumps

- Mutual inductance [1],[2]

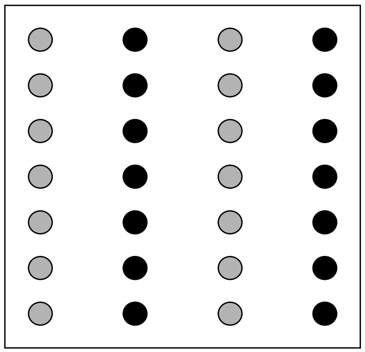
$$M = \frac{u_o}{2\pi} l \left(\ln\left(\frac{l}{s} + \sqrt{\left(1 + \frac{l^2}{s^2}\right)} \right) - \sqrt{\left(1 + \frac{s^2}{l^2}\right)} + \frac{s}{l} \right)$$

- Self inductance [1],[2]

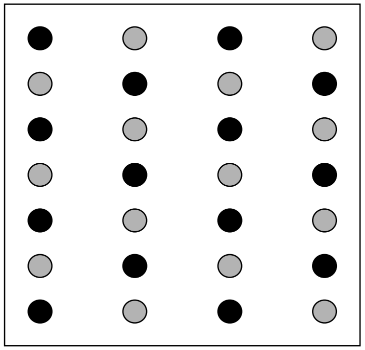
$$L = \frac{u_o}{2\pi} l \left(\ln\left(2\frac{l}{d} + \sqrt{\left(1 + \frac{4l^2}{d^2}\right)} \right) - \sqrt{\left(1 + \frac{0.25d^2}{l^2}\right)} + 0.5\frac{d}{l} + \frac{u_r}{4} \right)$$



- Loop inductance of arrays is pattern dependent [3]



POOR

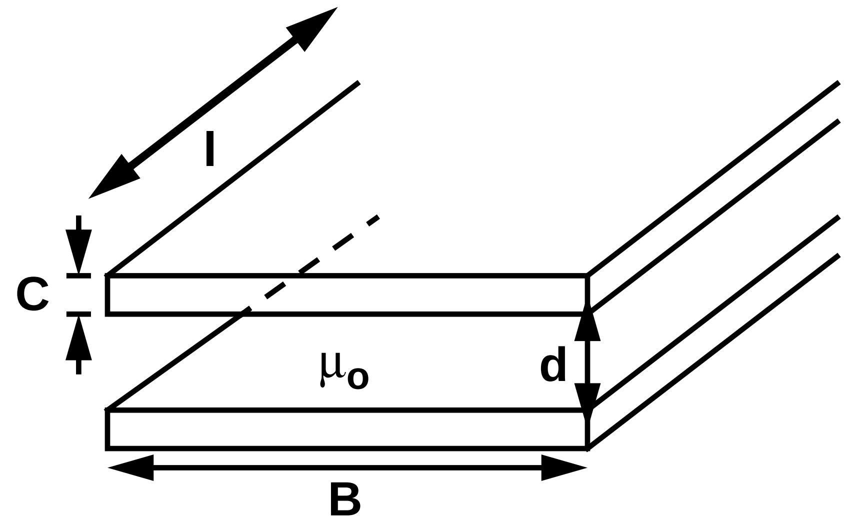


BETTER

Power Plane Inductance

- Planes are present in the package and on the board
- Loop inductance [2]:

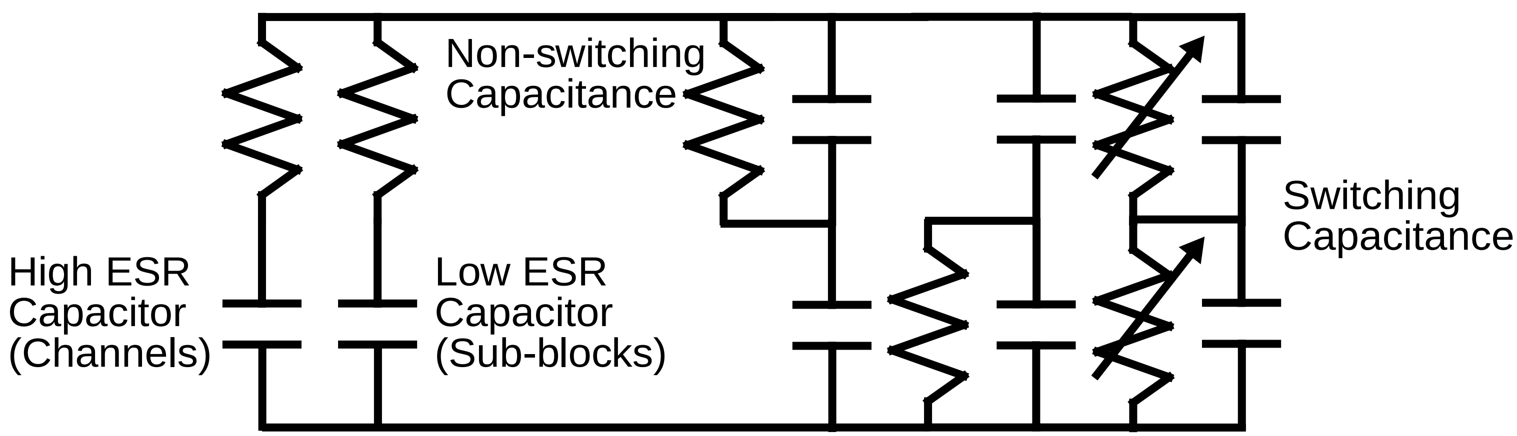
$$L = \frac{u_o}{\pi} l \left(\ln\left(\frac{d}{B + C} \right) + 1.5 \right)$$



- Most planes are actually perforated
- Decrease inductance for multiple pairs by 2n-1 dielectrics, where n is the number of power plane pairs, assuming V_{DD}-G_{ND}-V_{DD}-G_{ND} stack-up
- Thin spacing decreases inductance

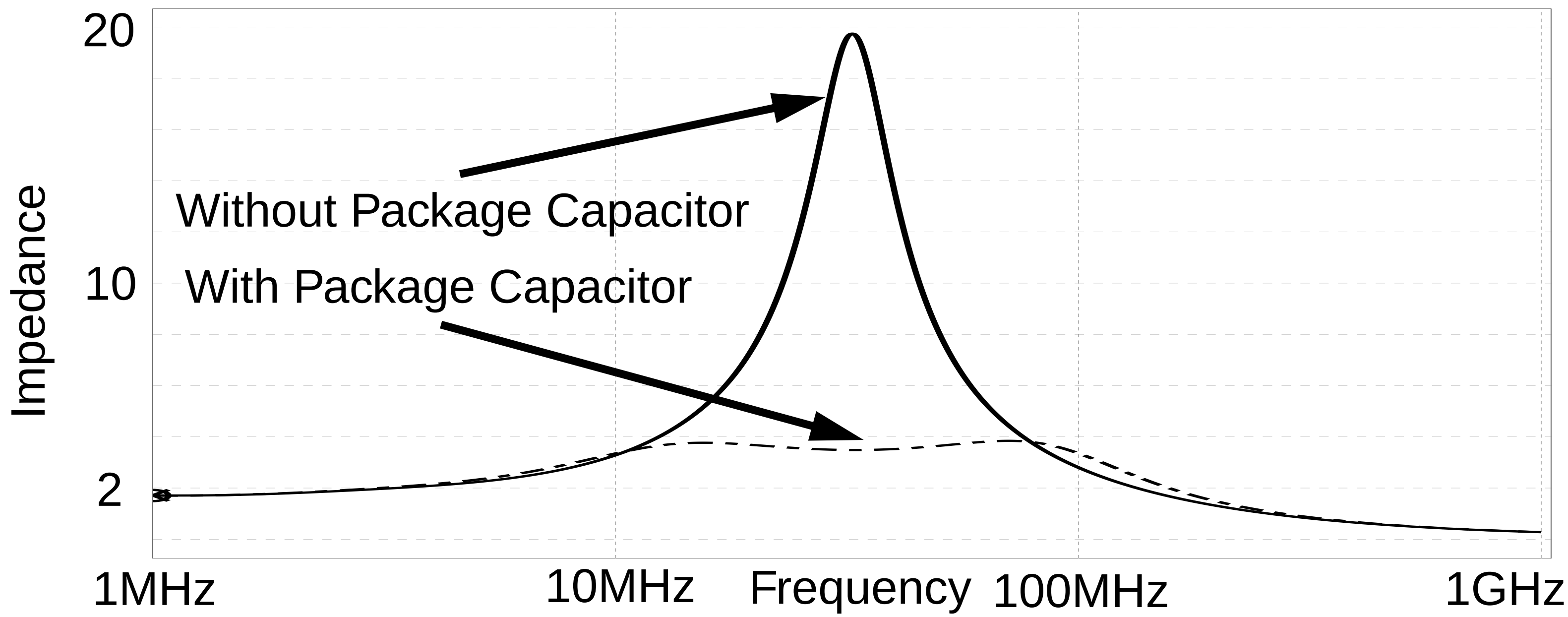
Low/Mid-Frequency Chip Model

- Estimate switching capacitance from thermal power
  - $C_{SWITCH}=P/(V^2f)$
- On-die decoupling capacitance is typically about 10x the switching capacitance (rule of thumb)
  - Yield issue (decoupling is ~15-20% of die area)
  - Scaling issue for process shrinks - leakage
- Equivalent series resistance (ESR)
  - Ratio of one type to the other is design-specific

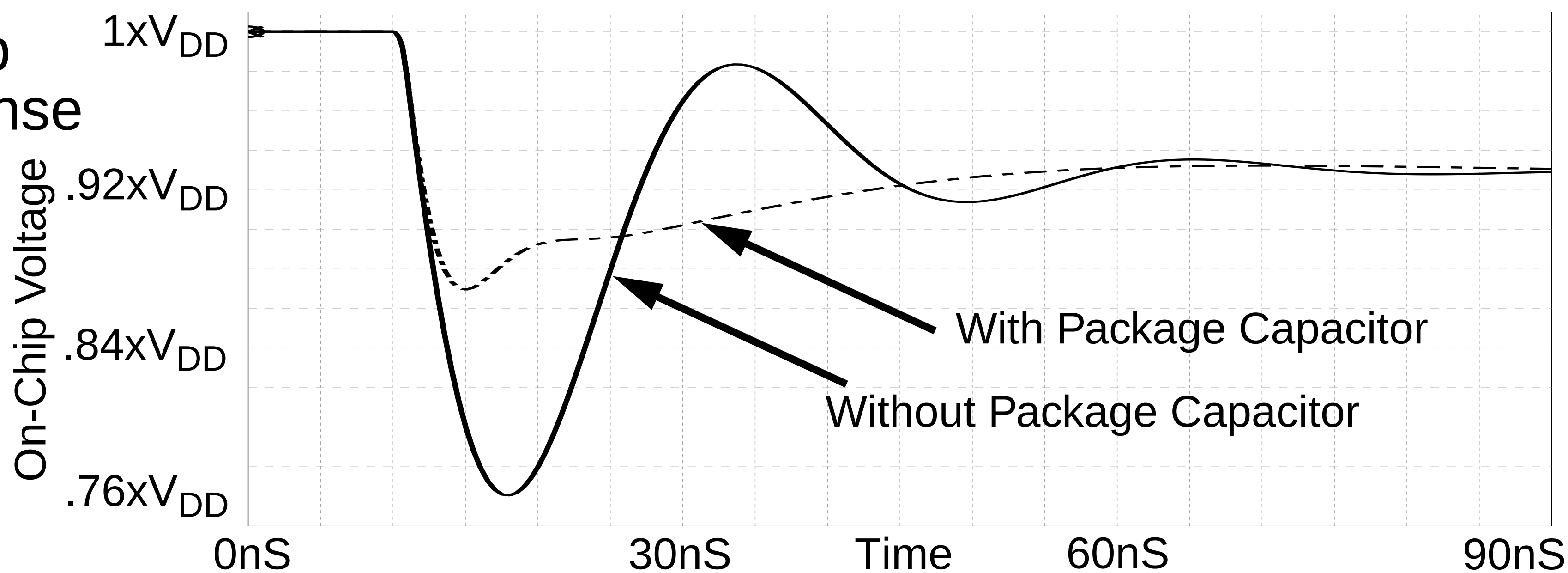


Decoupling Capacitor Design

Frequency Response

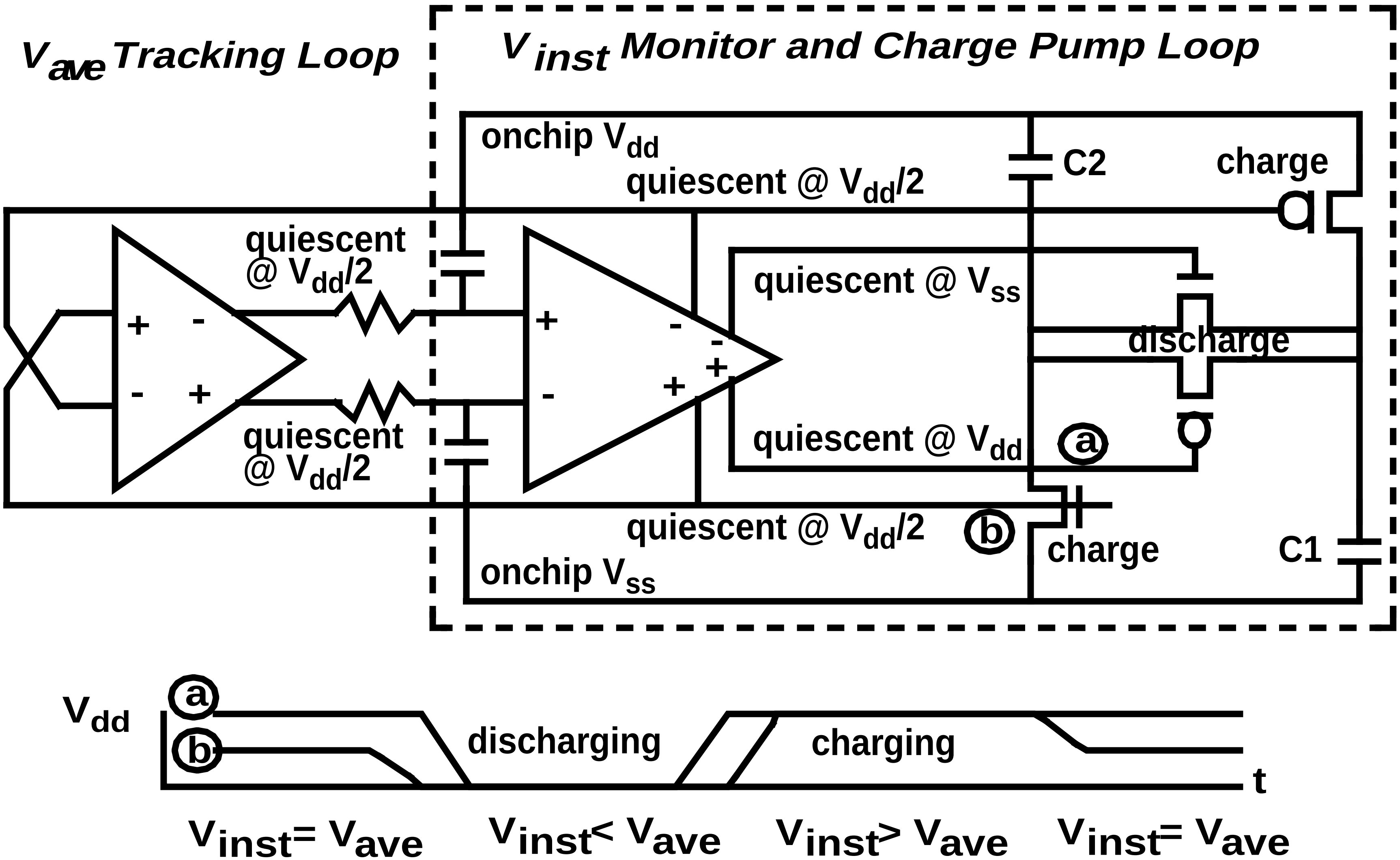


Step Response

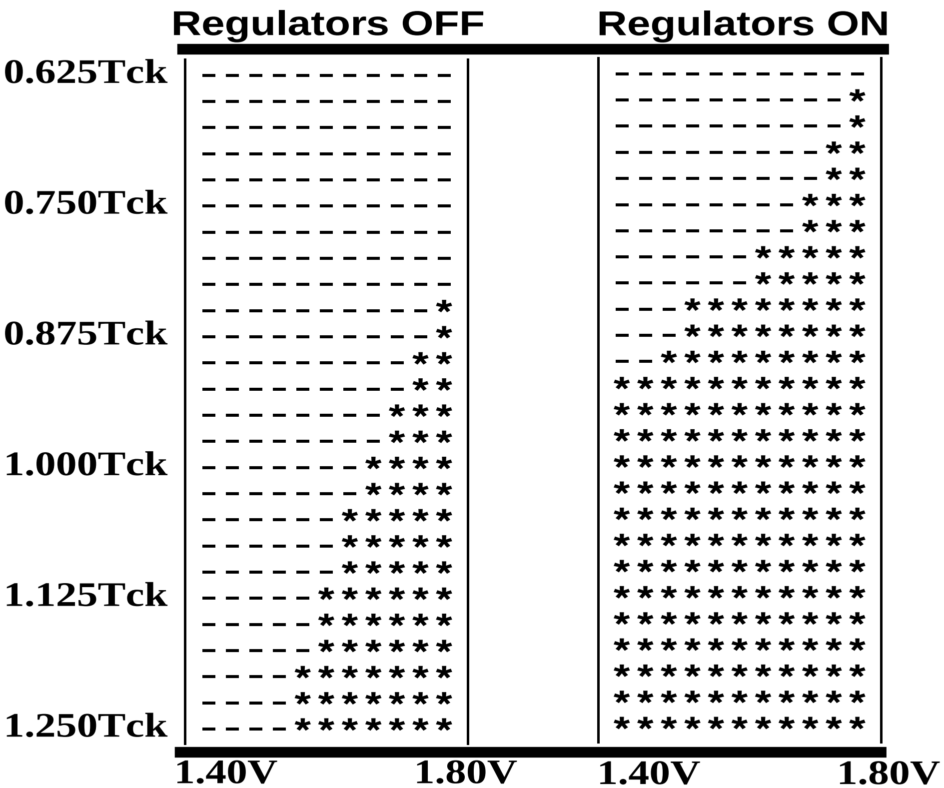


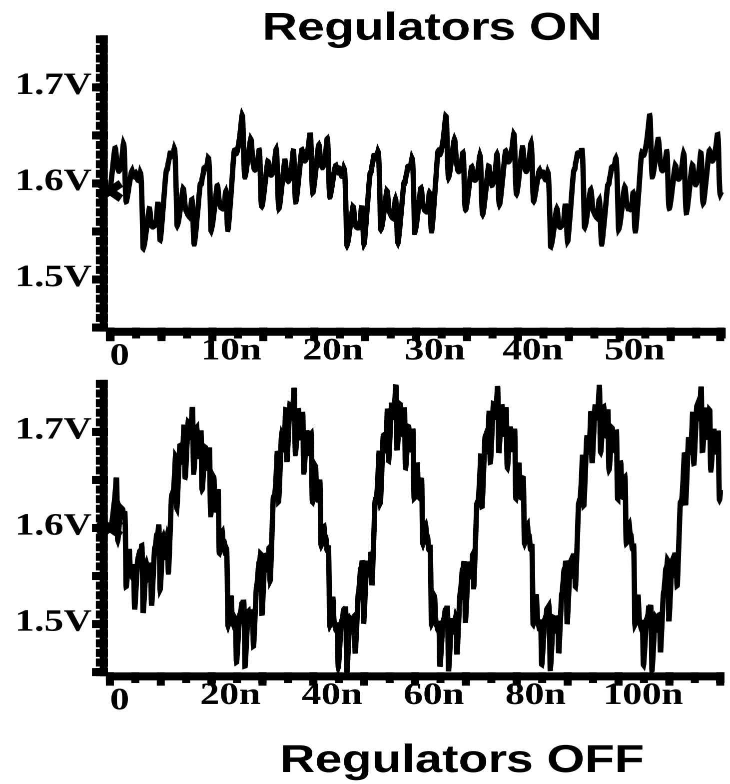
On-Die Voltage Regulator

- Detect, and actively compensate for voltage swings in the target frequency range [4]:



Results [4]

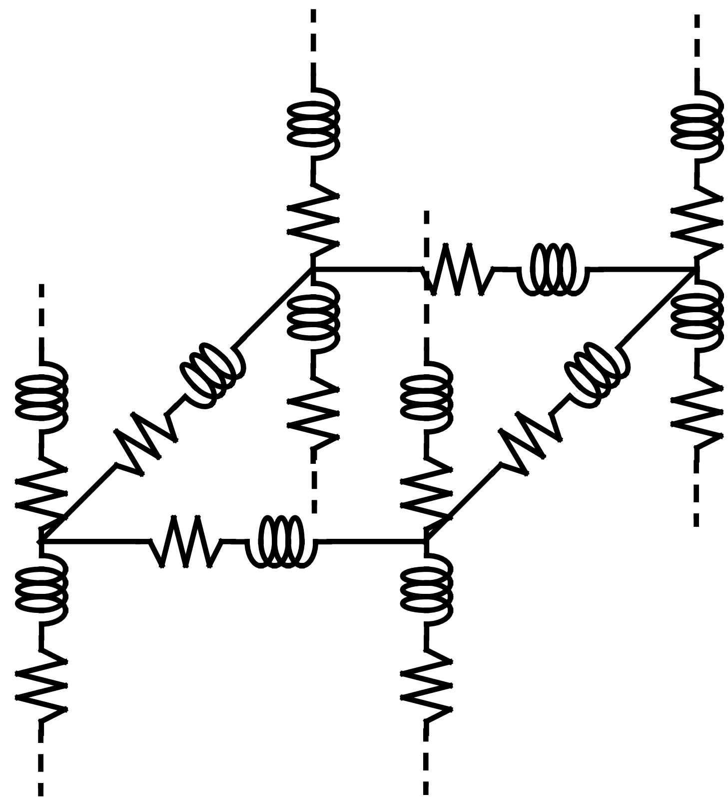




- See paper for more details

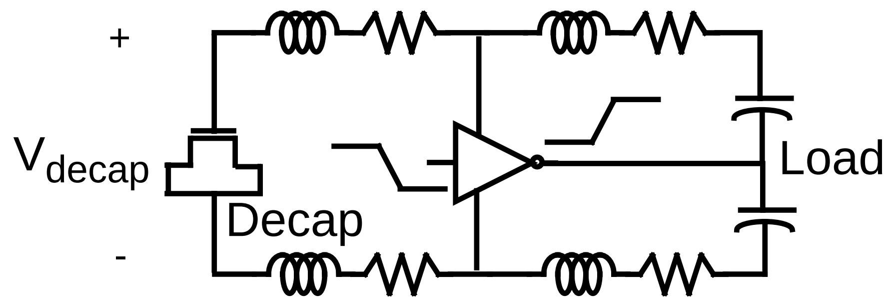
Higher Frequency Models

- Expand plane / via examples to derive a new model, with smaller 'lumps'
- Mid/high frequency
  - 3-D package/chip models
- Very high frequency
  - Small localized regions
  - 3-D chip model
  - Field solvers



On-Chip Decoupling

- MOS capacitors provide on-die decoupling
  - Effectiveness is proportional to capacitor time constant - a long channel length will not decouple a signal rise time - a small channel length reduces area efficiency
- Distance to capacitor series parasitics
  - Set a guideline based on simulations
  - Scaling issue for process shrinks as rise times and parasitics scale



- Maximize on-die decoupling capacitance subject to yield/area constraints

On-Chip Power Distribution Guidelines

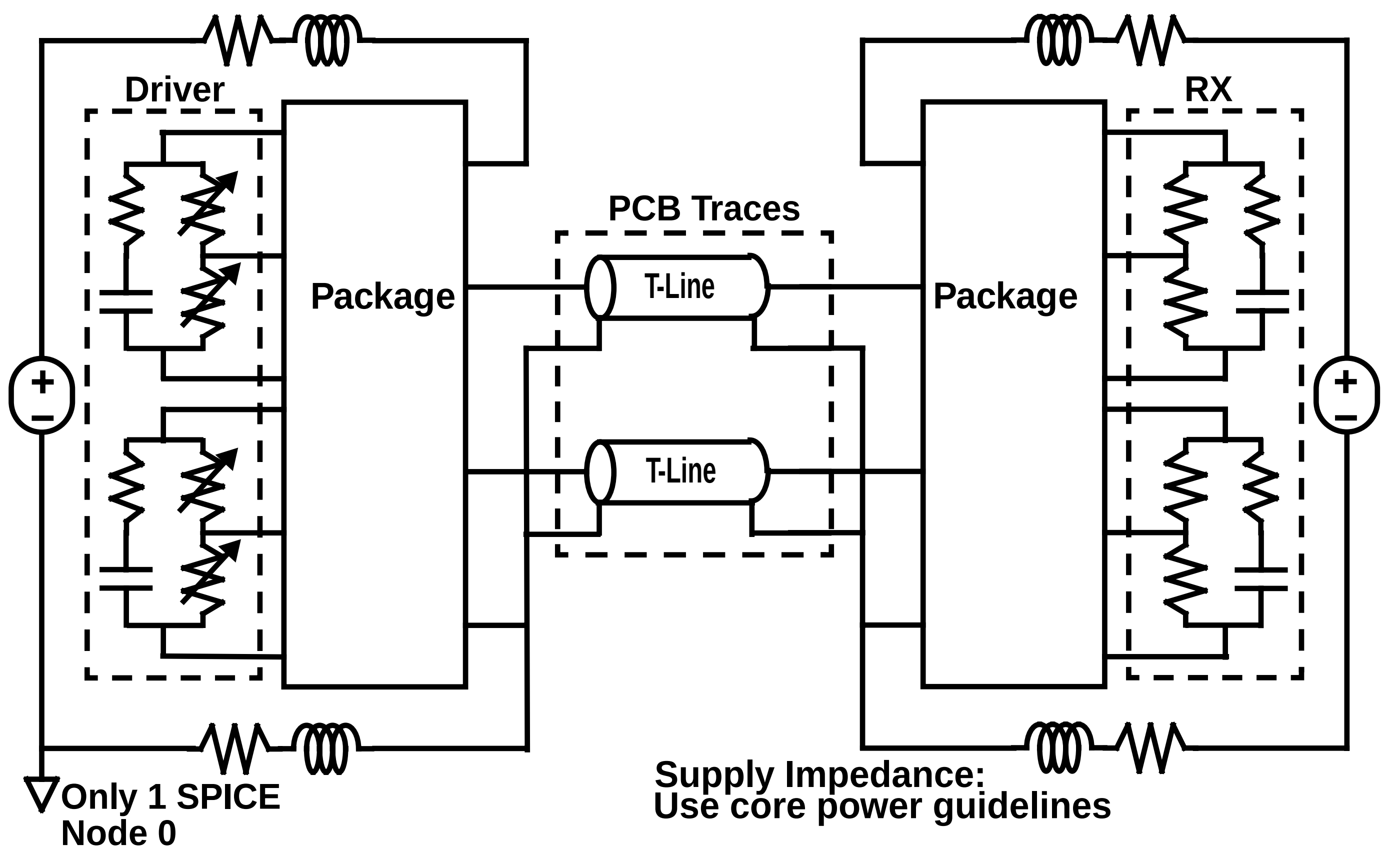
- Checkerboard bump pattern
  - Close to switching circuits
  - Watch for electromigration
- Dense power-grid
  - Alternate V_{DD}/V_{SS}
- Explore μarchitectural fix for clock-gating
  - Control ramp-rates of clock gating
- Circuit techniques are also effective
  - Lower the Q of the power supply network or reduce ΔI

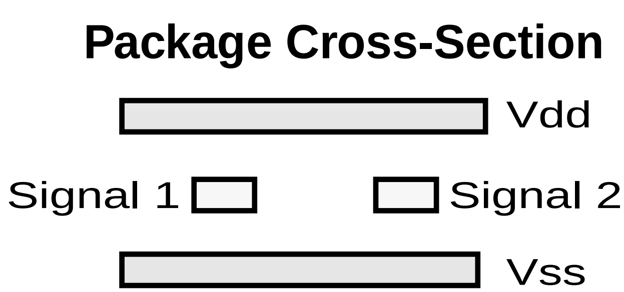
Off-Chip Power Delivery Guidelines

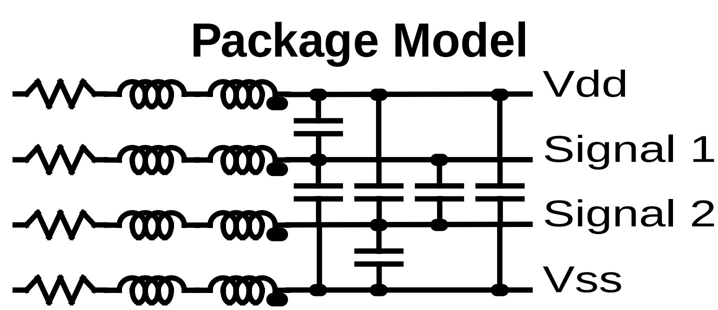
- Pay attention to the capacitor mounting and shorten the leads
- Place capacitors close to the chip
- Reduce spacing between planes
- Add more V_{DD}, V_{SS} planes in an alternating pattern
- Sockets, vias, bump arrays
  - Use checkerboard patterns where possible
  - Use as many parallel paths as possible, without eating up the entire plane with anti-pads

I/O Signaling

- Two separate paths to consider: power, signal return

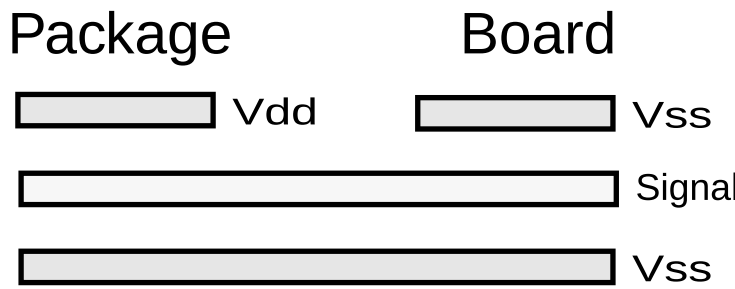


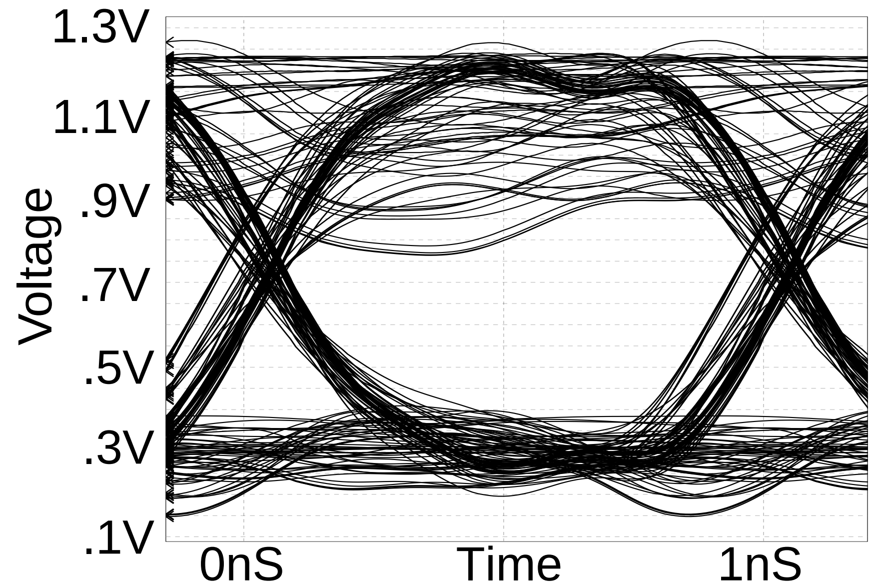




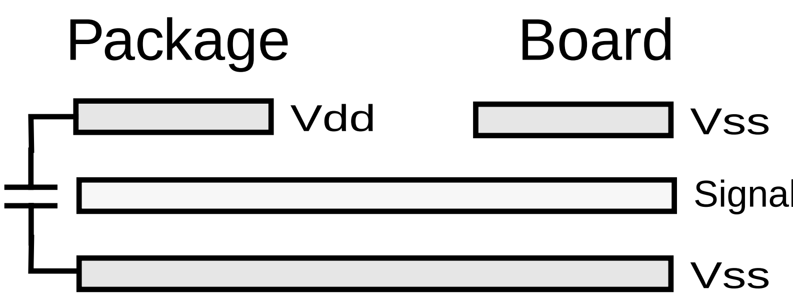
I/O Example

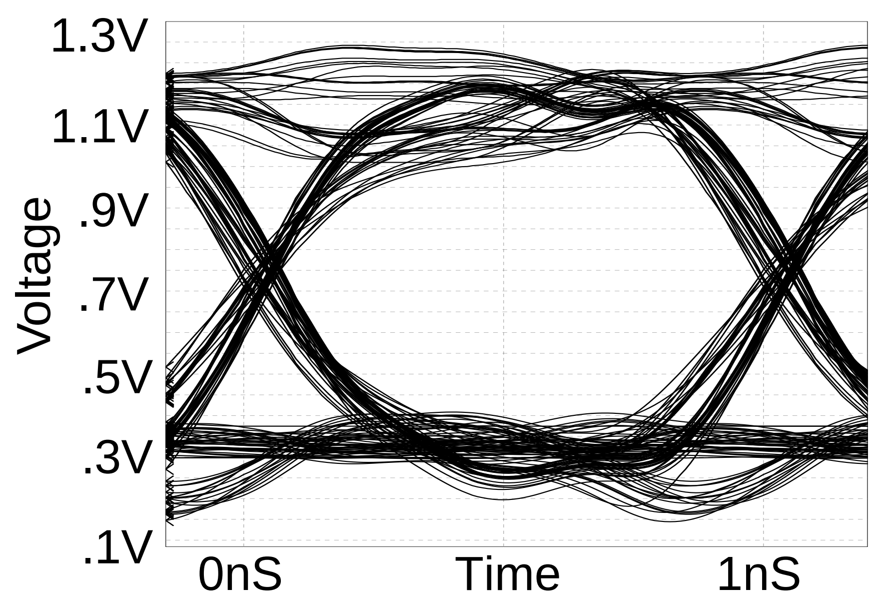
- **How does signal return current get from board (V_{SS} only) to package (V_{DD}/V_{SS})?**





- **Package capacitors to reduce signal return impedance?**





High-Speed I/O Guidelines

- Power Distribution Impedance
  - Same guidelines as core power
- Signal Return Impedance
  - Maximize the power/ground pins in the chip, package, and connector pin-out (under cost constraint)
  - Careful routing to avoid discontinuities
  - Minimize the effects of discontinuities by providing an alternate return path (i.e. through a decoupling capacitor)

Summary

- Several important aspects of delivering clean power
  - Supplying power across a broad frequency spectrum
  - Decoupling capacitor sizing and placement
  - I/O return current discontinuities and supply impedance
  - Solutions encompass board, package, chip
- Modeling concepts
  - Vias, bumps, pins, power planes, capacitors, and processor
- General guidelines for power distribution