E3 Does Moore's Law Apply to Analog? Past, Present, and Future Implications of Technology Progress and Higher Levels of Integration for Mixed-Signal Circuits

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The digital IC world has been "governed" by an increase of integration over time; a steady march obeying what has become know as Moore's law. While this relationship is put forward to describe the level of commercially viable integration, people also extend the notion to cover the continuous increase in processing speeds and reductions in cost per function. Much of this progress is built on the foundation of continuously shrinking lithography—a phenomenon that may run into a wall later this decade, causing much concern amongst the digital IC community.

But does any of this even matter to the "Analog Crowd," who care about SNR and dynamic range. Power dissipation is about much more than CV^2 f. Surely, they have benefited greatly from advances in technology over the last 2 decades, but it is much more complicated than just a march down a lithography curve—or is it?

- The panel explores the important mechanisms behind advances in Analog/Mixed Signal IC technology:
- How much of this progress is process-based, and is there a "free ride" on the coat tails of digital process advances?
- What are the important dimensions of improvement for mixed-signal ICs. Density, speed, and power efficiency are used for digital—but analog is more complicated, is it not?
- Are there hard limits to how much integration makes sense in the mixed-signal world? Are there soft limits?
- Is there a "wall" that designers hit? When do they hit it? Then what happens?

To get an effective handle on these problems, it is necessary to take a hard look at the history of Mixed-Signal IC advances—is there a Moore's law curve there? Does it have the same slope? In keeping with this, panelists are selected who have lived through several generation of IC technology.

It is also necessary to assess where the technology is today (and why), and predict where it is headed.

Panelist Statements

Prof. Bruce Wooley, Chairman, Dept. of Electrical Engineering, Stanford Univ., Stanford, CA.

For more than two decades, analog designers have exploited the benefits and overcome the limitations of MOS VLSI technology to open new markets and enable increasing levels of integration. However, at deep submicron dimensions, the costs of this integration are becoming prohibitive. Nonetheless, the extraordinary scaling of CMOS technology continues to offer new opportunities for innovation in mixed-signal circuit design. But the "end game" for CMOS VLSI, which may span as much as another two decades, is also the end game for those opportunities

Kerry Bernstein, Senior Technical Staff Member, IBM, Essex Junction, VT

Given the trends in technology scaling, analog functions in future processes are toast. Signal distortion and nonlinearity, previously a nuisance, will soon become no fun in a big way. New contributors to unpredictability include self-heating, substrate-potential variation, and electrical-parameter variability. Scaling will continue to promote device characteristics that enhance digital performance, without regard for how miserable life is becoming for analog designers. Arguably, power dissipation with scaling will drive MOSFETs of the future to spend more quality time in subthreshold operation, maximizing nonlinearity. An important qualification for analog designers will be having a good sense of humor.

 0-7803-7335-9

Lew Counts, Vice President, Analog Devices, Wilmington, MA

Yes, Moore's Law does apply to Analog ICs at least in spirit. But then the analog art tends to follow a more meandering path through the wilderness of the physical world. In fact the advances in speed and density of analog ICs are not far behind digital. For example, in the 35 years amplifier bandwidth has increased about 10x per decade, while power and actual cost have decreased. However, at some point, decreasing supply voltages and kT/C noise will compromise dynamic range. Silicon ICs operating at GHz for RF and data communication applications are now commonplace, a direct consequence of the steady advance in process technology noted by Moore. The density of practical RF ICs is often limited by the size of high-Q on chip inductors that usually require metal many microns wide, dwarfing active on-chip devices.

Masao Hotta, Senior Chief Engineer & General Manager of Advanced Analog Technology Div., Semiconductor & Integrated Circuits, Hitachi Ltd. Japan

Reduction of cost per function is always required for not only digital LSIs but also mixed-signal LSIs. Chip area reduction curves exist in the field of high-speed ADCs. This is done by, e.g. improvement of architecture, change of circuit topology and application of advanced technology. However, RF circuits and high-precision circuits have more complicated problems in cost reduction. Factors such as breakdown voltage, hot carrier degradation, noise, Vth mismatch, and integration of passive elements should be considered. These factors impede progress of integration for RF ICs and high-precision mixed-signal LSIs.

Maarten Vertregt, Philips Research Labs, Eindhoven, The Netherlands

The continuous pressure for technology progress means: do more with less. More dynamic range and more speed, higher data rates with less supply voltage, area, power, development time, money, and, people. Progress of integration density in the digital IC world is based on replication of standard blocks. Repetitive use at different levels of abstraction effectively shields the complexity of high-level digital system demands from physical and technological constraints. For analog function implementation, a unified abstraction between analog system demands and physical technology constraints is missing. Digitally enhanced mixed-signal system implementation brings the traditional digital scaling advantage to analog building blocks. In the future, when monolithic density increase no longer proves feasible, technological progress will be gauged differently. At that point, the demand for mixed-signal solutions maintaining a high system innovation rate will be even more challenging.

Steven J. Hillenius, Director- High Performance Structures and Devices Department, Agere Systems, Murray Hill, NJ.

Linear and RF applications will drive the new device structures and innovations in the future. This will happen as the core digital CMOS technologies become more standardized and new products will rely much more on low-voltage linear circuit elements to perform the necessary functions. These new structures will combine the customized design of transistors to optimize performance for specific linear circuit design needs and passive devices that are customized to work with these new device structures.

Ted Tewksbury, Managing Director, High-Speed Signal Processing, Maxim Integrated Products, North Chelmsford, MA.

Moore's law has little relevance to the integration level of high-performance analog circuits. Moore's law concerns lithography, and lithography is only one among many variables that drive the size and density of analog circuits. Fundamental physical properties such as breakdown, noise, isolation, matching, offsets and passive component Qs can be improved by increasing physical dimensions. The contradictory requirements of high-performance analog and high-density digital are, in fact, driving a trend toward *dis*-integration in which packaging and process technologies are separately optimized for each domain. With regard to performance, analog circuits have little or nothing to do with Moore. In addition to lithography, fundamental process improvements such as SiGe, SOI, copper and Si-C drive these advancements. Even after Moore's law runs out of steam, fundamental advances in physics, such as carbon nanotubes, MEMS, Low-Tc superconductors and photonic crystals, will continue to extend the performance of analog.

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