Session 20 Overview

Multi GigaHertz Microprocessor Technologies

Chair: Krste Asanovic, MIT, Cambridge, MA

Associate Chair: William J. Bowhill, Compaq Computer Corp. Shrewsbury, MA

Technology advances and the highly-competitive computer industry are driving rapid advances in processor clock frequencies. Papers in this session present technologies and design methods for Multi-GHz design, including high-speed instruction management and integer execution units. The integer ALU and bypass network often sets the cycle time of a high-performance microprocessor.

Paper 20.6 introduces an innovative solution that pipelines the arithmetic unit to allow instruction issue every half CPU clock cycle. The ALU implements carry pipelining which allows full instruction result forwarding to immediately succeeding ALU instructions. A sophisticated pipeline delivers 4GHz operation.

Paper 20.1 describes a 1.8GHz instruction window unit that performs instruction queuing, renaming, dependency checking and out-of-order issue. The design incorporates an allocation scheme that reduces the number of array access ports required.

Paper 20.2 introduces a low-power charge-recycling scheme to deliver a 32b adder that consumes about 50% the power of a conventional CLA adder.

Silicon-on-isolator (SOI) technologies are gaining wider acceptance with 3 papers reporting on SOI designs. SOI technologies offer speed, density and power-consumption improvements over equivalent bulk technologies. However, additional electrical design issues are introduced. The isolating substrate lowers junction capacitance but allows voltage of the transistor body to vary depending on switching activity. This effect is known as the “history effect” and results in delay variation. Paper 20.3 compares adder designs in bulk and SOI technologies and quantifies the differences.

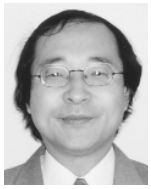
Costs savings and performance improvements from migrating previous designs to advanced technologies continue to be attractive and motivate new methods and analysis for efficient porting. Paper 20.5 discusses the conversion of a microprocessor to SOI technology. Methods for timing and noise analysis are discussed. The chip includes 2.25MB of cache. Column and row redundancy in the memory arrays improves manufacturing yield and further reduces costs.

Paper 20.4 presents a microprocessor that operates at 1.3GHz using copper interconnect for improved interconnect delay. The paper discusses scaling issues and the use of low-threshold-voltage devices. Logic gates implemented with low-Vt devices deliver 15% speed improvement and are used selectively in critical paths.

20.1 A 1.8GHz Instruction Window Buffer **8:30 AM**

J. Leenstra, IBM Entwicklung GmbH, Boeblingen, Germany

An instruction window buffer implements the processor parts for renaming, reservation station and reorder buffer as a 64-entry unified buffer. Using 0.18µm 1.5V CMOS, it supports operation up to 1.8GHz. This frequency is enabled by port reduction techniques, the instruction issue structure, and the use of self-resetting circuits.



20.2 A Low-Power SOI Adder Using Reduced-Swing Charge-Recycling Circuits **9:00 AM**

A. Inoue, Fujitsu Laboratories of America, Inc., Sunnyvale, CA

A low-power clocked static low-swing charge-recycling circuit technique is applied to a 32b carry skip adder and fabricated in 0.08µm SOI CMOS. Power consumption is reduced by 50% with no speed degradation compared to that of a conventional CMOS adder.

20.3 Sub-500ps 64b ALUs in 0.18µ SOI/Bulk CMOS: Design & Scaling Trends **9:30 AM**

S. Mathew, Intel Corp., Hillsboro, OR

A 482ps 64b Han-Carlson ALU in 1.5V 0.18µm bulk CMOS directly ported to 0.18µm SOI offers 14% performance improvement, after a 2% margin is added for reverse body effect. An SOI-optimal redesign using a quaternary-tree architecture improves the speedup to 19%. Scaling the designs to 0.13µm for the two cases results in overall speedup of 9% and 16%, respectively.

20.4 Design and Migration Challenges for an Alpha Microprocessor in a 0.18µm Copper Process **10:15 AM**

R. Hokinson, Compaq Computer Corp., Shrewsbury, MA

An Alpha microprocessor with clock frequency >1.3 GHz is achieved by migrating to a 0.18µm CMOS process with 7 layers of copper interconnect. The technology challenges of converting an aluminum-based design to copper are presented. The circuit and design solutions introduced by the technology are discussed.

20.5 A 1GHz PA-RISC Processor **10:45 AM**

L. Tsai, Hewlett-Packard, Fort Collins, CO

The processor is a leveraged design based on a previous generation of PA-RISC processor. Improvements over the previous design are: a 0.18µm silicon-on-insulator (SOI) process with 7-layer metal interconnects, 2.25MB cache with row and column redundancies, 120-entry TLB, 50% frequency boost, and 45% lower power with the same footprint.

20.6 A 0.18µm CMOS IA Microprocessor with a 4GHz Integer Execution Unit **11:15 AM**

D. Sager, Intel Corp., Hillsboro, OR

A microprocessor with an integer execution unit capable of fully-dependent operations at 4GHz is fabricated in 0.18µm CMOS with 6 Al layers. Micro-architectural and circuit techniques used are described.

