Toward Full Crystal Oscillator Integration for RF Applications

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***Abstract*—This paper presents the performances of an integrated oscillator working at 3.3V power supply for XO applications, extended to OCXO by digital selections. It is realized in a standard 0.35µm SiGe BiCMOS technology from austriamicrosystems AG®. Some experimental characterizations have been performed at 40 MHz and give good agreement with simulations. This die is then used to develop a miniaturized XO design on silicon substrate (8.5x8.5 mm²).**

I. INTRODUCTION

In most of applications (e.g. time base, sensor…), a strong motivation is given to obtain miniaturized and integrated devices in order to reduce both size and global consumption without performance losses compared to devices relying on discrete elements.

An oscillator circuitry based on Colpitts topology has been integrated in a die for low voltage XO and OCXO applications (typ. 3.3V). However in low voltage structures, it is always a challenge to maintain sufficient PSRR at high frequency: most of bandgap architectures based on CMOS amplifier can suffer from this fact with consequences on oscillator phase noise performances. In small-size packaging, low power consumption is necessary to avoid thermal self-heating effects in the case of both XO and OCXO designs.

Some studies have already been performed to realize integrated oscillators on CMOS chips [1]. Unfortunately, these structures involve high silicon die loss (defined by quartz resonator). The miniaturized XO structure developed in the present study is based on small size silicon interface to connect both die and quartz resonator to minimize parasitic influences on its performances.

II. DIE DESIGN

The die shown in Fig. 1 is realized (size: 2 x 2 mm^2) within a 0.35µm SiGe BiCMOS technology from AMS (austriamicrosystems AG®). It is composed of five different integrated structures mixing LF and RF functions (diagram in Fig. 2) working under 3.3V power supply on 1.3 x 1.3 mm^2 active area[1]. Some of these structures are user-configurable to widen the field of application of this die. Integrated functions are listed below:

- ① Oscillator cell,
- ② Adjustable voltage reference,
- ③ Output buffer (50Ω / HCMOS load),
- ④ Resonator thermal control,
- ⑤ External frequency trimming.

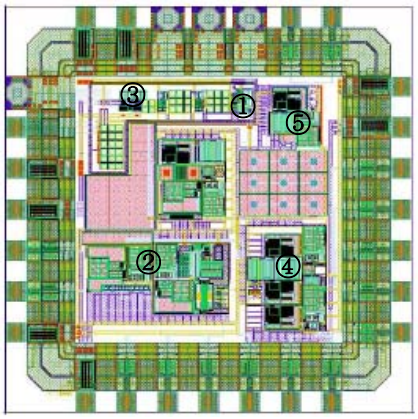

Figure 1. Voltage Die layout

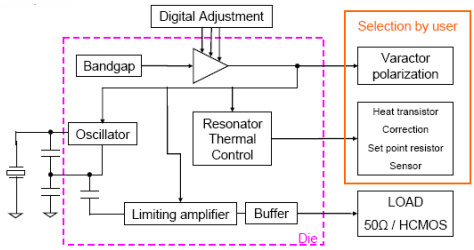

Figure 2. Integrated die diagram.

[1] Remaining area is related to I/O pads and protection ring.

Academic work supported by the European project "Euroscil" from EUREKA programme in collaboration with TEMEX.

A. *Adjustable 2.4V voltage reference*

To provide stable 2.4V supply with low temperature sensitivity and high power supply rejection to analog integrated cells, a voltage reference based on a CMOS bandgap circuit is necessary. Unfortunately, such structures are process-sensitive due to mismatch and mechanical stress (packaging) affecting thermal compensation behavior within the targeted temperature range [2].

According to available AMS datasheet [3], CMOS bandgap output voltage value can fluctuate within 1.11V to 1.31V (typical value: 1.21V). To keep the voltage reference at the chosen nominal value, a control circuit is required. Several methods can be used [2]: zener zap, laser trim, voltage gain adjustment (external resistors or digital trim). A digital adjustment through three bits command (three I/O pads only) gives sufficient accuracy without any external components (Fig. 3).

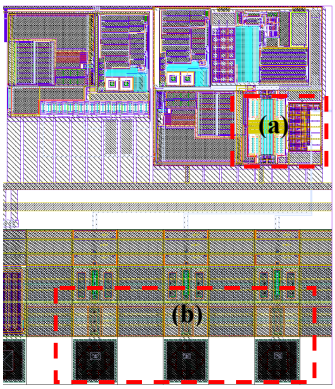

Figure 3. Voltage reference structure: digital command **(a)** and related I/O pads **(b)**.

The layout of RF integrated functions oscillator, limiting amplifier and output buffer shown in Fig. 4 allows applications over 10 MHz to 100 MHz frequency range. All these functions are internally connected to limit the need of external components.

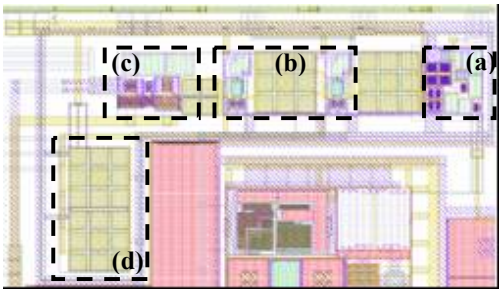

Figure 4. RF integrated functions: oscillator cell **(a)**, limiting amplifier **(b)**, buffer **(c)**, decoupling capacitors **(d)**.

B. *Oscillator cell*

The oscillator cell (Fig. 4a) is based upon a Colpitts topology, for which a simplified schematic is given on Fig. 5. This cell is compacted (106.5 x 120 μm^2) to reduce silicon cost area as well as to improve thermal behavior and to limit parasitic effects. In this design, the C1, C2 capacitors fixing both the amplitude level and the frequency of oscillation are still externally connected with the quartz resonator. As depicted in Fig. 5, the blue dashed area shows integrated part of Colpitts cell.

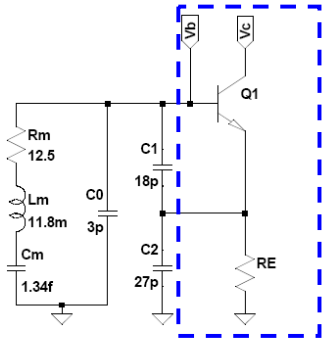

Figure 5. Integrated Colpitts oscillator (simplified schematic).

C. *Limiting amplifier and output buffer*

The buffer output stage (Fig. 4c) can drive 50Ω or HCMOS loads depending on targeted application. A decoupling capacitor has been integrated (Fig. 4d). They meet minimum value requirements and if necessary their value can be externally increased. The area allotted to buffer and limiting amplifier (Fig. 4b) is 541 x 113.7 μm^2.

In oscillator application, to minimize the substrate current injection and LF and RF noise coupling, all integrated functions must be carefully isolated using sufficient number of substrate contacts. Functions described above are the basis in XO design.

D. *Extended oscillator applications*

Furthermore, to widen oscillator's field of application (for example VCXO, OCXO or VC/OCXO), the layout includes an auxiliary 2.4V voltage reference for frequency trimming as well as some elements involved in resonator thermal control. All these functions can be shut down using digital command avoiding excess die's consumption in XO applications.

Nevertheless, the thermal control loop has not yet been fully integrated because of its high thermal design sensitivity relative to packaging. On the other hand, power components can also thermally affect integrated functions reliability. External components requirement are listed below:

- NTC thermistor and the set point resistor related to quartz resonator's inversion point,
- PI structure: function of thermal design time constant,
- Heating power transistor and current sensing resistor.

III. SIMULATION TOOLS AND DESIGN METHODOLOGY

All simulations described in section IV have been performed with AMS mixed signal Hit Kit 3.70 under Virtuoso® Design Framework II platform (Cadence Design System Corporation®).

A. Analog Circuit design

The integrated circuit design involved four major steps [4]: electrical design, physical design, fabrication and finally test and production. Designers must obtain sufficient electrical design robustness prior to perform their layout. Such physical design impact must be always kept in mind during circuit performances tuning. Oscillators are dramatically sensitive to parasitic components becoming more and more important as frequency increases. Before foundry processing, it is necessary to take into account all layout parasitic effects (resistances, capacitances and inductances) involving performance losses. Thus, time consuming post-simulations must be done using layout extracted view.

B. Layout impact on oscillator design and simulation time

Even in their discrete form, oscillators are always strongly affected by all parasitic (board, packaging…) involving unexpected experimental dysfunctions and simulation inaccuracies. In case of oscillator integration, parasitic extraction increases simulation time (transient analysis: steady state depending on Q-factor [5–6]) and sometimes convergence problems at each time step. One of the existing methods to simulate high-Q crystal oscillator and to well predict start up time is the non-linear dipolar method [7–8] which can be performed under ADOQ[2] software [9].

The principle of the dipolar method is based on resonator's motional branch replacement by a sinusoidal current source working at the same frequency. The oscillator cell is then considered as an equivalent dipolar circuit including the parallel quartz capacitance, as well as C1 and C2. The equivalent circuit is given in Fig. 6.

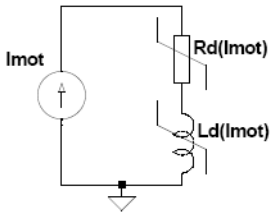

Figure 6. Dipolar equivalent circuit.

Real (R_d) and imaginary ($L_d\omega$) part of the dipolar impedance (1) are both functions of motional current amplitude and operating frequency.

$$Z_{dip} = R_d + jL_d\omega \tag{1}$$

When the oscillator reaches a steady state, an equilibrium is attained between quartz motional branch parameters and dipolar branch. The branch impedance is then given by (2) and (3):

$$Z_{dip} + Z_Q = 0 \tag{2}$$

$$\begin{cases} Rm = -R_d \\ Lm\omega - 1/(Cm\omega) = -L_d\omega \end{cases} \tag{3}$$

Rm, *Lm* and *Cm* are respectively resonator motional resistance, inductance and capacitance.

In case of design shown in Fig. 1, table I summarizes simulation time required to perform dipolar analysis for 100 current amplitude steps:

TABLE I. SIMULATED VIEW EFFECTS

View Type	Number of equations	Simulation time [h]
Schematic view	1900	2.5
Extracted view	14000	18

IV. SIMULATIONS VS EXPERIMENT: PRELIMINARY COMPARISONS

This die must withstand ±10% power supply variations over [–40°C, 85°C] temperature range. Some experimental characterizations have been conducted for both voltage references and RF functions (40 MHz AT-cut 3rd overtone quartz resonator[3]) with a ball-bonded die on PCB (Fig. 7) to minimize packaging effects. Most of the simulations performed in that section are related to die's extracted view unless specified.

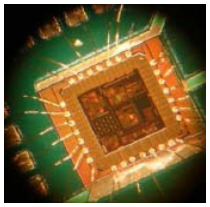

Figure 7. Die connected to PCB by ball bonding technique.

A. Ajustable voltage reference

To characterize the voltage reference cell, three critical parameters must be checked: temperature sensitivity, power supply rejection and noise performances.

1) Temperature sensitivity

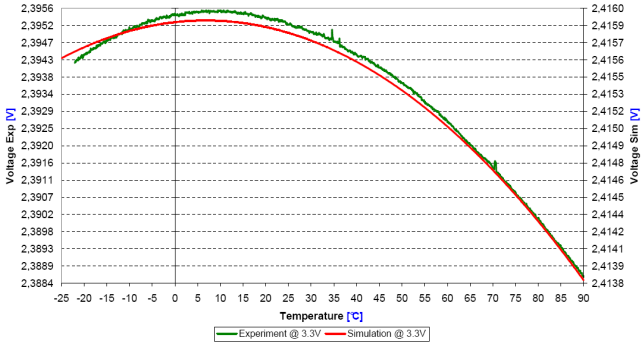

Figure 8. 2.4V LDO experimental and simulated response function of temperature at 3.3V.

[2] ADOQ: "Analyse Dipolaire des Oscillateurs a Quartz"

[3] TEMEX reference: YQ2200-0943-0007

The voltage reference has been experimentally characterized from –20°C to +90°C as shown in Fig. 8 for LDO[4] structure. Temperature sensitivity is evaluated from (4) and final results are summarized in table II.

$$Sensitivity = \frac{1}{V_{REF}\big|_{nom}} \frac{\left(V_{REF}\big|_{\max} - V_{REF}\big|_{\min}\right)}{\left(T_{\max} - T_{\min}\right)} \times 10^6 \qquad (4)$$

TABLE II. REFERENCE VOLTAGES SIMULATED AND EXPERIMENTAL RESULTS @ 3.3V POWER SUPPLY OVER [–20°C, +90°C].

Polarization functions	Simulation		Experiment	
	ΔV_{REF} [mV]	Sensitivity [ppm/°C]	ΔV_{REF} [mV]	Sensitivity [ppm/°C]
Reference 1.21V	1.04	6.6	2.9	18
Oscillator cell	3	9.5	9	34
Varactor	1.9	6.2	9.3	34
Amplifier and buffer	2.1	6.6	7	26

2) Voltage reference noise

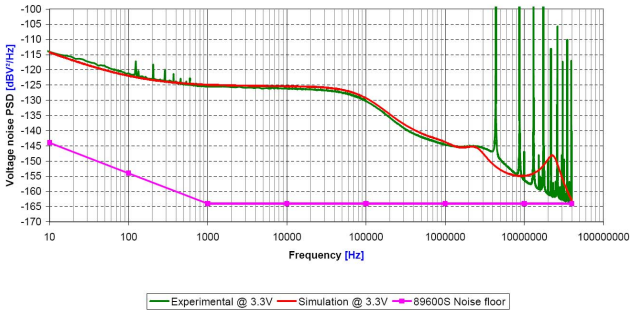

Figure 9. Voltage reference PSD at 3.3V, 27°C.

The voltage noise has been evaluated up to 40 MHz, results are plotted in Fig. 9. As it is shown, noise peaking appears over 1 MHz (*Cf* simulated curve in red). To minimize these effects, some additional compensation capacitors have been integrated in the design (Fig. 10 a and b).

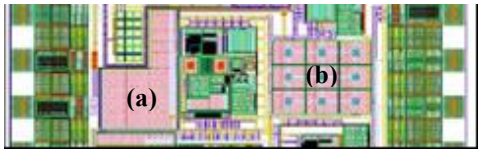

Figure 10. Noise integrated compensations.

Experimental results show good agreement with simulations, thermal and noise responses are not affected by power supply variations. Nevertheless, noise generated by voltage references directly affects phase noise performances. To obtain better results, high frequency noise PSD and PSRR of integrated LDO needs deeper investigation.

B. Oscillator cell

Current amplitude through the quartz resonator has been evaluated to 860 µA peak (Fig. 11) with good power supply rejection (below 1%). According to section III, the simulated transient response (Fig. 12) has been obtained with a schematic view in order to reach steady state without excess simulation time. For that purpose, an initial condition was set to start oscillations [5–6]. Simulated current response was taken to resonator's motional branch assuming that steady state current flows only through this branch. Amplitude was evaluated to 730 µA peak.

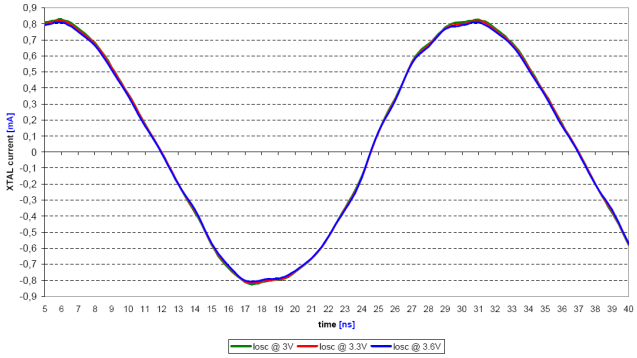

Figure 11. Experiment: current through 40 MHz AT 3rd overtone quartz resonator as function of time for ±10% power supply variations at 27°C.

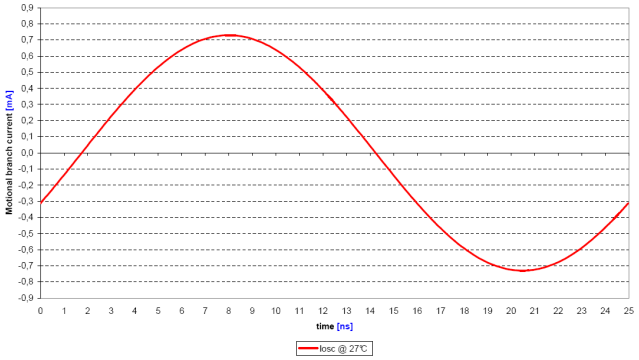

Figure 12. Simulation: current flowing through resonator motional branch at 3.3V, 27°C.

Dipolar analysis was also used to evaluate experimental measurement reliability. According to Fig. 6, resistance and reactance are both plotted as a function of motional current amplitude including quartz parallel capacitance C0 (Fig. 13). According to (3), with quartz resonator motional parameters (Rm = 12.5 Ω, Lm = 11.8 mH, Cm = 1.34 fF and C0 = 3 pF), current amplitude is evaluated to 825 µA peak.

[4] Low Dropout Voltage Regulator.

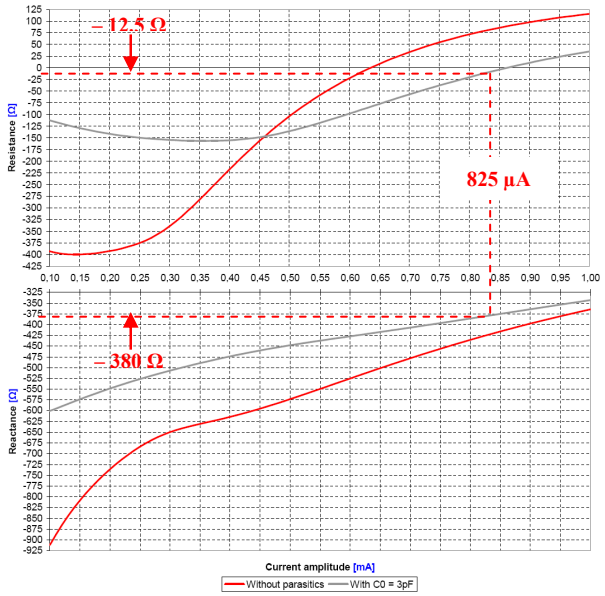

Figure 13. Negative impedance simulated with C0 (green) and without C0 (red).

As signal amplitude is strongly affected by parasitic induced by board, packaging and layout effects, dipolar method was also used in addition to previous transient simulation (schematic view): Current amplitude shown in Fig. 12 must be increased by 100 µA considering extracted view.

Finally, more accurate results are obtained by improving simulated model: including board parasitic and bonding effects.

C. *HCMOS ouput signal*

HCMOS buffer provides a square output signal (Fig. 14) with short transition time (< 1ns). Rise and fall time[5] are evaluated to 550 ps and 411 ps respectively for duty cycle of 51%.

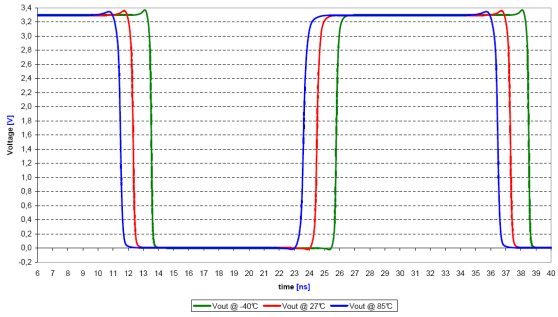

Figure 14. Simulated HCMOS output signal function of temperature at 3.3V.

D. *SSB phase noise simulations*

In order to evaluate die's phase noise performances at 40 MHz, a *PSS*[6] followed by a *Pnoise* analysis have been done on both schematic and extracted views (Fig. 15) without resonator. As it can be seen in Fig. 5, parasitic (R, C) involve additional compensations on LDO cell between 100 Hz and 100 kHz. This effect reduces LDO phase margin while improving noise performances.

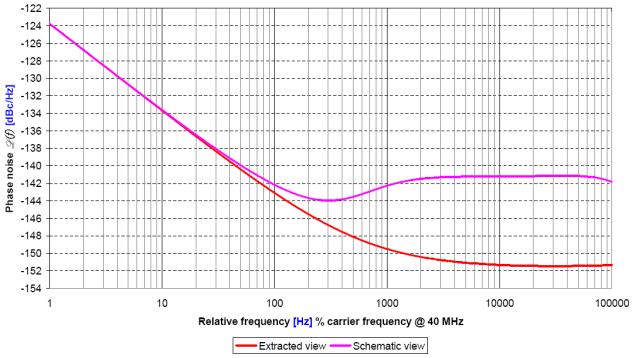

Figure 15. Simulated die phase noise performances at 3.3V, 27°C (schematic and extrated view).

To take into account quartz resonator effect, extrapolated asymptotic phase noise plot is shown in Fig. 16 related to Leeson frequency calculation (5) [10]. Unloaded quality factor is evaluated from this resonator batch and extrapolated results are summarized in table III.

$$f_L = f_0 / 2Q \tag{5}$$

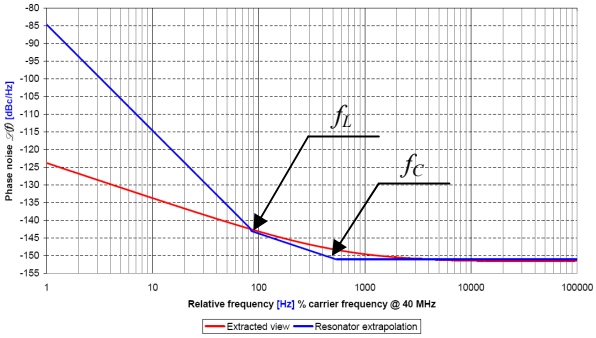

Figure 16. Extrapolated resonator influence on phase noise (related to Leeson frequency calculation).

TABLE III. EXTRAPOLATED PHASE NOISE $\mathscr{L}(f)$% CARRIER FREQUENCY @ 40 MHZ.

Relative frequency [Hz]	Simulation [dBc/Hz]
1	–85
10	–115
100	–140
1000	–150
10000	–151
100000	–151

More investigations must be performed on phase noise characterizations.

[5] Evaluated from 10% to 90% of the output signal amplitude.

[6] Periodic Steady-State.

E. Die's consumption

Die consumption depends on targeted application. Some results are given in table IV for 3.3V ±10% power supply variation at ambient temperature for various die configurations. Quartz resonator drive level at 40 MHz is evaluated to 4.6 µW. Oscillator cell and its internal supply used only 1 mA of the total ASIC current budget.

According to preliminary thermal investigations, die self-heating is an important parameter that cannot be neglected because it affects thermal design for OCXO applications (additional contribution). In that case, the resonator thermal control loop is defined to slightly increase consumption in comparison with XO configuration.

TABLE IV. EXPERIMENTAL DIE POWER CONSUMPTION.

Type of Application	Power Supply		
	3V	*3.3V*	*3.6V*
XO	33.54 mW	39.30 mW	45.68 mW
VCXO	38.10 mW	44.62 mW	51.70 mW
OCXO	45.24 mW	52.97 mW	61.20 mW
VC/OCXO	49.74 mW	58.31 mW	67.32 mW

V. MINIATURIZED XO DEMONSTRATOR

Usually, oscillator performance losses are mostly related to electronic structures distant from the resonator resulting in parasitic increase. For that purpose, a miniaturized XO demonstrator working at 40 MHz and using the die previously characterized is designed (Fig. 17). A strong limitation of discrete components is targeted, so small size SMD and available chip capacitors are used for system compensations and decoupling.

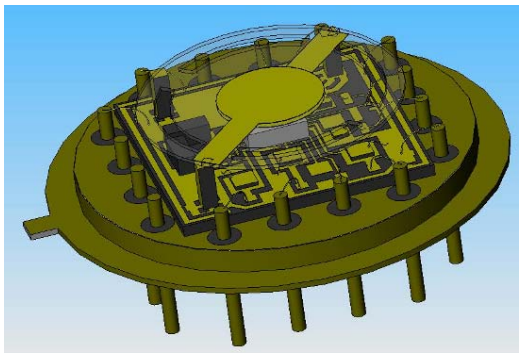

Figure 17. XO demonstrator 3D design.

This demonstrator is realized on a silicon substrate by well known clean room process for flip chip assembly purposes. This method has been chosen for both size and electrical performance improvements compared to common wire bonding techniques (ball or wedge) [11] in particular at high frequencies [12]: minimizing parasitic (R, L, C). This substrate is then stuck on TO-8 base for future tests.

Our goal is to propose a design limited only by quartz resonator outer dimensions: a 40 MHz SC-cut resonator as shown in Fig. 17 (BVA-type). Silicon substrate dimensions are fixed to 8.5x8.5 mm². Multi-modes resonators like SC-cut require externally selective filter (L, C). Realization of this demonstrator is still on going.

VI. CONCLUSION

The integrated user-configurable oscillator circuitry design has been tested at 40 MHz for 3.3V ±10% power supply over [–40°C, 85°C] temperature range. Simulation tools (Cadence®) and AMS electrical models show very good agreement to predict performances and to allow future design optimization. However, more experimental characterizations are required (phase noise…).

Future trends involve lower power supply designs to decrease consumption, voltage noise improvements to obtain better phase noise performances. Furthermore, integration density can be increased by adding MIM bridges and other trim capacitors inside the die.

ACKNOWLEDGMENT

We would like to thanks Philippe Abbe and Gilles Martin from the FEMTO-ST Institute for their help during die's experimental characterizations. We also acknowledge Jean-Jacques Boy (FEMTO-ST) and Olivier Bel (TEMEX) for providing us 40 MHz SC and AT cut quartz resonators during these experiments. Finally, we would like to thanks Professor Remi Brendel for his support and encouragement.

REFERENCES

[1] H. Kim, J. Lim, K. Choi, T. Jackson, and D. Kenny, "Direct mounting of quartz crystal on a CMOS PLL chip," Proc. of 2004 IEEE IFCS and Exposition, pp. 165–168, 2004.

[2] G. A. Rincon-Mora, Voltage References… From Diodes to Precision High-Order Bandgap Circuits, Wiley-Interscience, 2002.

[3] Analog Standard Cell, BG05A - CMOS Bandgap Voltage Reference, Austriamicrosystems datasheet.

[4] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design – 2nd Ed., Oxford University Press, 2002

[5] K. S. Kundert, The Designer's Guide to Spice and Spectre, Kluwer Academic Publishers, 1995

[6] Cadence® documentation, Virtuoso Spectre Circuit Simulator RF Analysis Theory, version 6.2, June 2007.

[7] R. Brendel, D. Gillet, N. Ratier, F. Lardet-Vieudrin, and J. Delporte, "Nonlinear Dipolar Modelling of Quartz Crystal Oscillators," Proc. of 14th EFTF (2000).

[8] M. Addouche, N. Ratier, D. Gillet, R. Brendel, F. Lardet-Vieudrin, and J. Delporte, "Modeling of quartz crystal oscillators by using nonlinear dipolar method," IEEE Trans. on UFFC, vol. 50, Issue 5, pp. 487–495, May 2003.

[9] M. Addouche, N. Ratier, D. Gillet, R. Brendel, F. Lardet-Vieudrin, and J. Delporte, "ADOQ: A quartz crystal oscillator simulation software," Proc. of the 55th IEEE IFCS, Seattle, USA, pp. 753–757, June 2001.

[10] D. B. Leeson, "A simple model of feed back oscillator noise spectrum," Proc. IEEE, vol. 54, pp. 329–330, Feb. 1966.

[11] D. S. Patterson, P. Elenius, and J. A. Leal, "Wafer Bumping Technologies - A Comparative Analysis of Solder Deposition Processes and Assembly Considerations," Advances in Electronic Packaging, ASME. INTERPack 97, EEP 19-1, ASME New York, pp. 337–351, 1997.

[12] K. Boustedt, "GHz flip chip - an overview," 1998 Electronic Components and Technology Conference, Seattle, WA, pp. 1280–1285.