

# EMI Dynamics in High Frequency Crystal Oscillator Circuits

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**Abstract**—The high frequency oscillator circuit is relatively more susceptible to Electro-Magnetic Interference (EMI) in Embedded Systems (ES). The effect of EMI can be both deterministic and random in nature that shows up as jitter in the time domain and translates into the phase noise in the frequency domain. If the impact of EMI is too large, the performance of the entire system would be affected in terms of accuracy, stability, start-up, and phase noise. In this paper, the likelihood of observing such a failure in a noisy electromagnetic environment is discussed for giving brief insights about the EMI dynamics and EMI-induced failure mode of the crystal oscillator circuits. The goals of this paper is to provide the design philosophy by which time jitter and phase noise due to radiated EMI can be reduced to below operational levels.

## I. INTRODUCTION

Designing reference frequency standards with low EMI is critical for reliable system operation and the task of designing an EMI insensitive system is involved and covers almost every aspect of design techniques and layouts. The key to designing for high signal integrity is the reduction of EMI phenomena below certain levels, which may otherwise adversely affect the signal quality [1]-[24].

As system operating frequencies, data path widths, and output drive requirements increase, guaranteeing EMI compliance is becoming a difficult task for design frequency reference standards. The conventional methods used to meet EMI standards require metal shielding, multi-layer printed circuit boards, special casing, and passive components. As a result, the system's bill of materials and manufacturing costs increase but no value is added to the product in terms of features and competitiveness. In addition, using conventional methods of reducing system EMI requires a "trial and error" approach and results in longer time to market. In the worst case, a system must be entirely redesigned in order to satisfy EMI requirements.

A number of international government agencies impose guidelines on the allowable EMI that electronic modules can emit. In the United States of America (USA), the Federal Communications Commission (FCC) has divided EMI for computing electronic devices into two categories: (1) Radiated and (2) Conducted Emission.

Table 1 lists the maximum permissible Radiated Emission (RE) interference from the electronic devices, measured in terms of Electric Field Strength [24]. The maximum permissible limit of Conducted Emission (CE) interference is typically 260  $\mu\text{V}$  over the frequency range of 450 kHz to 30 MHz, and related with the noise interference fed back to the power supply lines [20]-[24].

To meet the FCC regulations, most electronic devices/equipments/systems currently employ a combination of two approaches (source suppression and containment) depending upon the cost factor and tolerable limit of the EMI [19]-[21]. The source suppression techniques enable the design methodology in such a way that only essential signals are to be present in signal interconnections, and unwanted EM energy restricted either by not being generated or attenuated before it leaves device/component/equipment/sub-system.

In this work, we report problems and challenges associated with radiated EMI and basic understanding of how they hinder the performance and reliability as well as how they can be minimized or eliminated. The CAD simulated and experimental results are presented to validate the proposed methodology.

## II. NOISE INTERFERENCES AND DESIGN GUIDELINES

Localization of noise interference sources in electronic system is critical task for designing EMI insensitive electronic products. Fig. 1 shows the typical noise interference sources and propagating channel for understanding the EMI dynamics in the embedded systems. The simplified approach is to eliminate the particular noisy circuit from the design flow chart, thus avoiding filtering, which otherwise is needed to minimize the interference.

Freq. (MHz)	Distance (M)	Field Strength ( $\mu\text{V}/\text{m}$ )
30-88 MHz	3 Meter	100 $\mu\text{V}/\text{Meter}$
88-216 MHz	3 Meter	150 $\mu\text{V}/\text{Meter}$
216-1000 MHz	3 Meter	200 $\mu\text{V}/\text{Meter}$

Table 1 Radiation Limits for class B computing devices (FCC Rules)

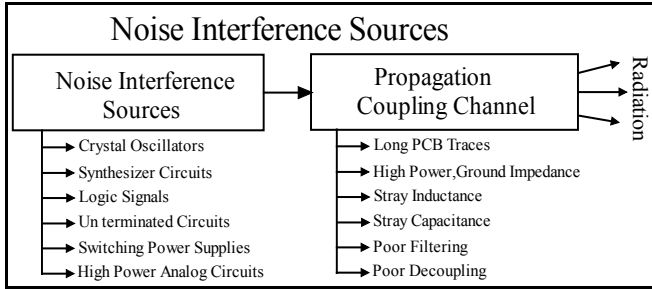


Fig. 1 A simplified representation of noise interference sources and propagation channel in typical RF circuitry and systems

Being aware of their locations in the design flow chart, partial effects can be minimized at the source and in the coupling channel by using filtering and decoupling network.

But in reality, it is not easy steps to eliminate all the components that are responsible for generating or propagating unwanted noise interference as they may be critical modules.

The objective of this paper is to report a design guide lines and understand the problems related to electromagnetic noise interference for the applications in crystal oscillators.

#### A. EMI Radiation and Design Guide Lines

- Frequency generating circuits (XOs, VCXOs, and TCXOs) should be shielded and placed as far as possible from the analog circuitry, video O/P connectors.
- The transition time (rise/fall) must be symmetric to minimize the unwanted modes.
- Mixing of clock buffers and logic modules in the same IC package should be avoided.
- Power supply to crystal oscillator circuit must be isolated by using Ferrite Beads.
- The printed circuit board (PCB) acts as a propagation channel for unwanted noise sources and couples this unwanted noise interference onto other peripheral circuitry, leading to the radiation of generated EMI into free space.

#### B. EMI Insensitive Design Topology

- A transmission line should be designed with low characteristic impedance to reduce the antenna effect (Fig. 2).
- Shielding minimizes the noise and reduces horizontal polarization through shielding by PCB copper planes.
- Radiated emissions are high when transmitted signals exhibit overshoot, undershoot, and ringing. Careful impedance matching must be maintained between drivers and transmission lines and between transmission lines and receivers to minimize these effects.
- When a multi-layer PCB cannot be used, 2-sided PCB must suffice. In such situation, it is advisable to

make a sheet pattern for the Vcc and GND on the whole area or as much of the entire surface as practical.

- For any reason, if we can't use whole area pattern, it is recommended to use half-area pattern in which Vcc and GND are symmetrical patterned on the facing layers, overlapping wherever possible (Fig. 3).
- Noise is the undesirable result of unintentional interaction due to hidden stray capacitances and inductances, resulting undesired electromagnetic couplings (Fig. 4).

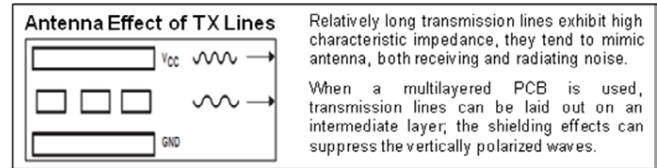


Fig. 2 A typical representation of antenna effect of TX lines

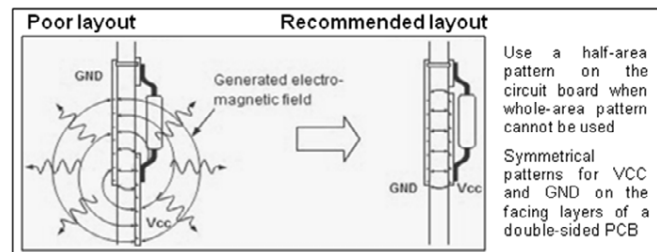


Fig. 3 A typical representation of generated EM field due to poor layout of the component

- Undesired signal interference degrades the phase noise dynamics (Fig. 5). There are a number of factors contribute to jitter that includes broadband noise, spurs, slew rate, bandwidth, and EMI.
- EMI source into PCB translates time domain response into spectrum, and these frequency data as voltage EMI sources. A prior knowledge of PCB resonance characteristics allows EMI insensitive PCB layouts (Figs. 6 and 7).

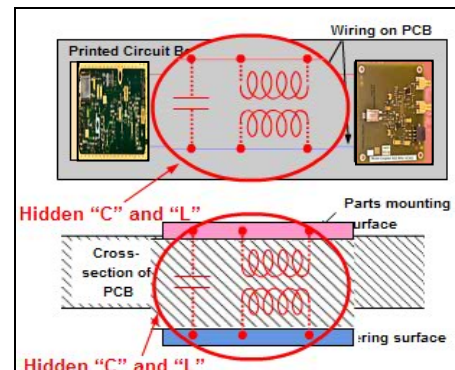


Fig. 4. A typical representation of hidden stray inductances and capacitances causing undesired EM coupling

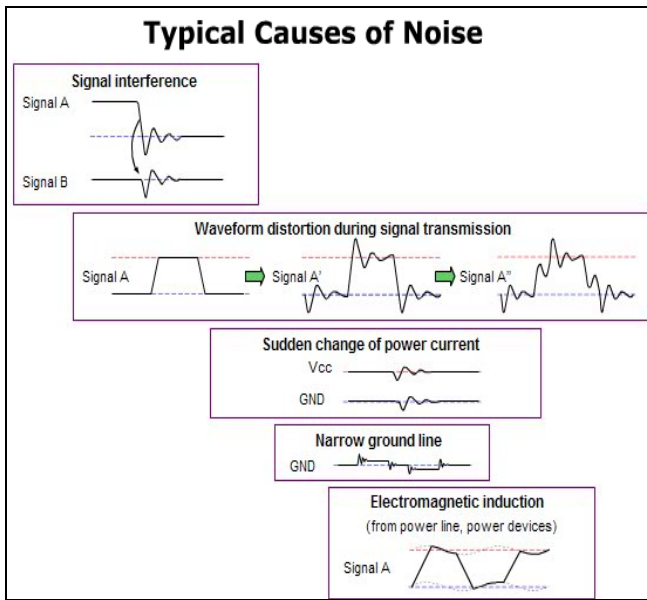


Fig. 5. A typical representation of signal interference causing EMI

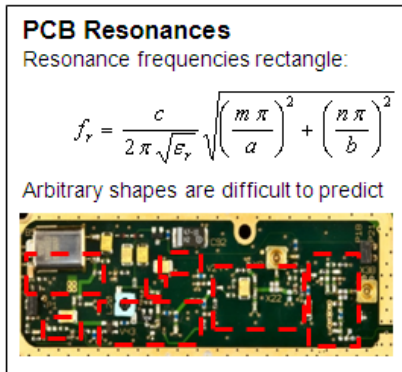


Fig. 6. A typical PCB crystal oscillator layout shows the rectangular cross section for determining the PCB resonance frequency and impact on jitter variations in presence of radiated EMI.

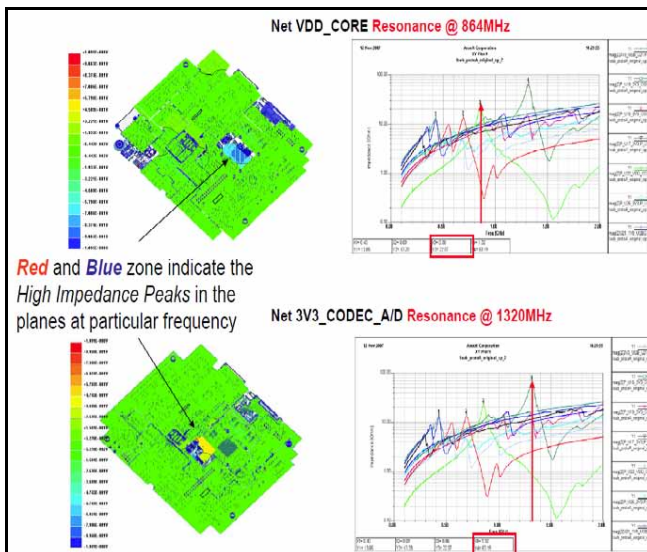


Fig. 7. A typical CAD simulated (Ansoft) data of PCB resonance and EMI characteristics

The high frequency crystal oscillator is more susceptible to time domain jitter and frequency domain phase noise, which directly affects the stability or accuracy of the reference frequency standard in a communication system.

Fig. 8 shows the typical representation of the basic design insights about the EMI noise caused by various identifiable interference signals such as crosstalk and power supply coupling. Electromagnetic Interference (EMI) can be both deterministic and random in nature, which shows up as jitter in the time domain and phase noise in the frequency domain.

### III. EMI AND NOISE DYNAMICS

EMI is generally caused by the generation and radiation of unwanted radio frequency signals that pollute carefully managed radio spectrum. EMI is the electronic equivalent of automotive smog and is emitted by any electronic system that has changing voltages and currents.

The EMI generated by crystal oscillator is the result of high frequency currents in the oscillator circuit. To minimize the EMI, the layout of the crystal oscillator circuit on the printed circuit board (PCB) is designed in such a way that effective loop area ( $S$ ) where RF current flows to be kept relatively small.

Fig.9 shows the typical current carrying loop that translates into the induced noise voltage as

$$v_n(t) = -\frac{\partial \psi}{\partial t} = -\frac{\partial (\int_s (\overline{B} \cdot \overline{S}))}{\partial t} = -\frac{\partial (\int_s (\overline{\mu} \overline{H} \cdot \overline{S}))}{\partial t} \quad (1)$$

Where  $\psi$  is the magnetic flux,  $t$  is the time,  $v_n(t)$  is the induced voltage,  $B$  is magnetic flux density,  $S$  is the coupling area,  $H$  is the magnetic field intensity, and  $\mu$  is the permeability. The relationship between induced noise voltage and jitter can be expressed by

$$\Delta t_{jitter} = \frac{v_n(t)}{m_s} = \left[ \frac{1}{m_s} \right] \times \left[ -\frac{\partial}{\partial t} \int_s (\overline{\mu} \overline{H} \cdot d\overline{S}) \right] \quad (2)$$

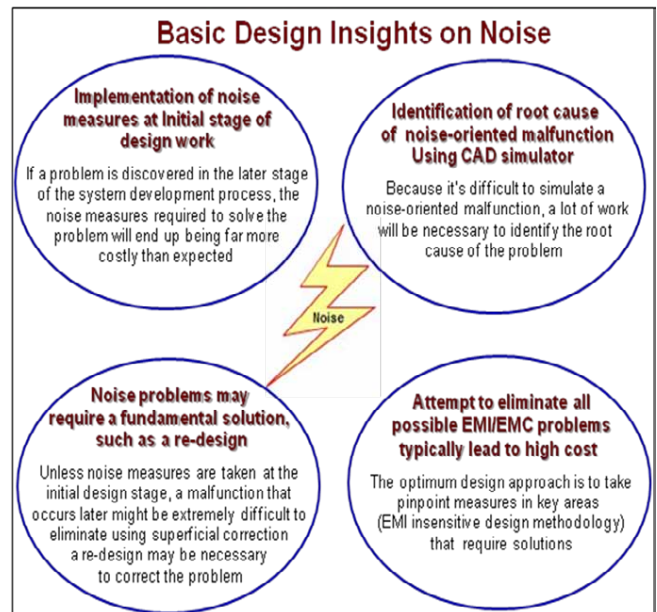


Fig. 8. A typical representation of basic design insights of low EMI circuits

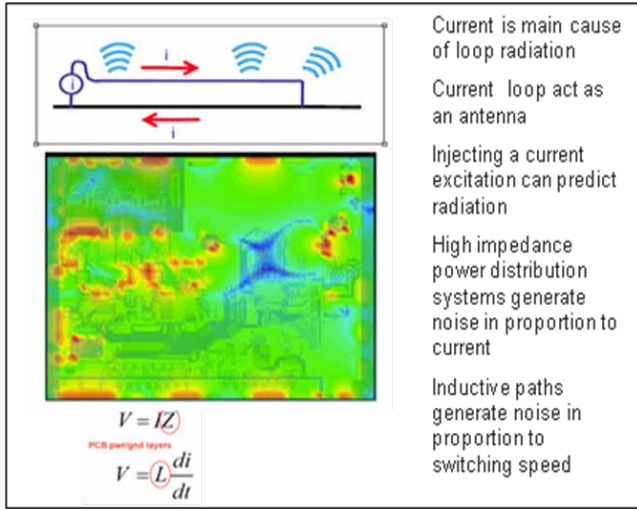


Fig. 9. A typical representation of radiated EMI due to variation in RF current in the current loop

$$\Delta t_{jitter} = f(v_n) \quad (3)$$

Where  $m_s$  is the slew rate and  $v_n(t)$  is the EMI induced voltage at the input of a circuit. Figure (1) shows the model of induced noise voltage generated due to radiated EMI.

Fig. 10 shows the typical representation of the external noise sources (EMI and other noise sources) impacting oscillator noise dynamics.

Fig. 11 illustrates the translation of RMS noise into timing jitter. As shown in Fig. 11, noise voltage ( $\Delta v$ ) at zero crossing the signal  $v(t)$  to reach the threshold  $\Delta t$  earlier, thus produces jitter.

Fig. 12 shows the model of an induced noise voltage generated due to radiated EMI. The simplified expression of oscillator output containing extrinsic and intrinsic noise can be expressed by

$$v_0(t) = A \sin(\omega t) + v_n(t) \quad (4)$$

Where  $A$  is amplitude,  $\omega$  is the angular frequency, and  $v_n(t)$  is noise voltage at time  $t$ .

The random noise  $v_n(t)$  shows Gaussian distribution, the probability distribution  $f(v_n)$  is

$$f(v_{int}) = \frac{1}{\sqrt{2\pi v_{int(RMS)}^2}} e^{-\left(\frac{v_{int}^2}{2v_{int(RMS)}^2}\right)} \quad (5)$$

The probability density as a function of the timing jitter  $\Delta t$  is evaluated by setting  $v_n(t) = A \sin(2\pi f \Delta t)$

$$f(\Delta t) = \frac{1}{\sqrt{2\pi v_n(RMS)^2}} e^{-\left(\frac{A^2 \sin^2(2\pi f \Delta t)}{2v_n(RMS)^2}\right)} \quad (6)$$

Using (2), for  $\Delta t \rightarrow 0$ ,  $\sin(2\pi f \Delta t) \cong 2\pi f \Delta t$ ,  $f(v_n)$  is given by

$$f(\Delta t) = \frac{1}{\sqrt{2\pi v_n(RMS)^2}} e^{-\left(\frac{A^2 (2\pi f \Delta t)^2}{2v_n(RMS)^2}\right)} \quad (7)$$

$$Jitter_{(RMS)}^2(\tau) = \Delta t_{RMS}^2(\tau) = \frac{2T_0^2}{\pi^2} \int_{f_L}^{f_U} \mathcal{F}(f) [\sin^2(\pi f \tau)] df \quad (8)$$

$$Jitter_{(RMS)} = \sqrt{\Delta t_{RMS}^2} \quad (9)$$

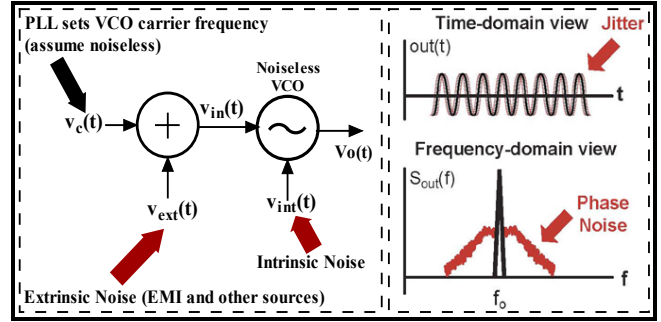


Fig. 10 Typical external noise sources (EMI and other noise sources) impacting oscillator noise dynamics

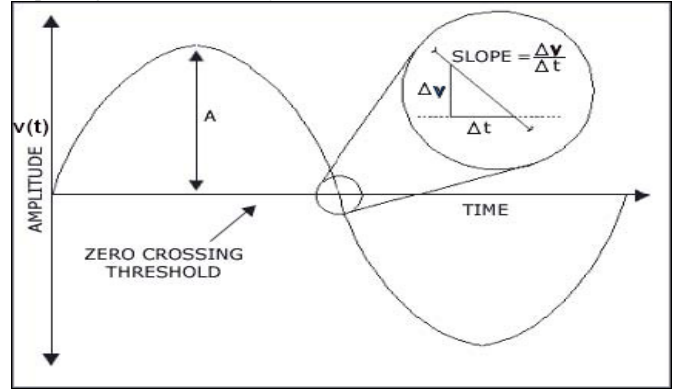


Fig. 11. A typical noise voltage ( $\Delta v$ ) at zero crossing the signal  $v(t)$  to reach the threshold  $\Delta t$  earlier, resulting in timing jitter noise

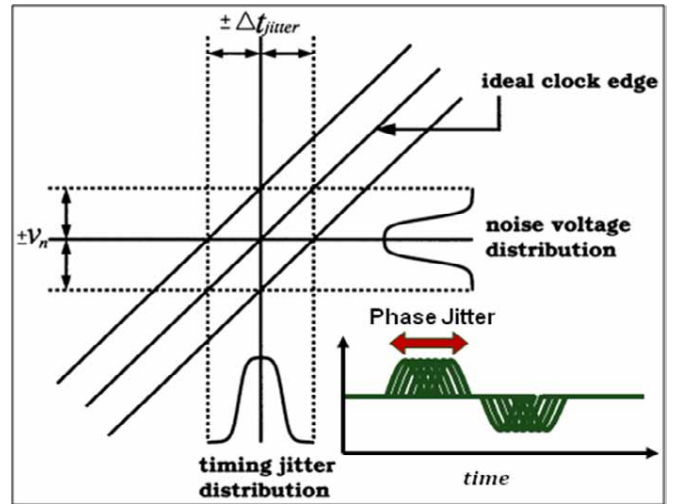


Fig. 12 An equivalent model of the EMI induced noise voltage [7]

Where  $f_L$  and  $f_U$  are the practical lower and upper frequency integration limits. In addition to EMI induced jitter, spurs also contribute to timing jitter, especially in oscillators caused by phase-locked-loop reference spurs, supply coupling, crosstalk from nearby circuitry, and sources. Therefore, each significant spur contribution should be accounted for separately as for the weighted  $k^{\text{th}}$  spur below:

$$\Delta\phi_{RMS\_k}^2 = 8\mathcal{L}(f_k) \times [\sin^2(\pi f_k \tau)] \quad (10)$$

$$\Delta t_{RMS}^2(\tau) = \frac{2T_0^2}{\pi^2} \mathcal{L}(f_k) \times \sin^2(\pi f_k \tau) \quad (11)$$

$$Jitter_{RMS}^2(\tau) = \frac{T_0^2}{\pi^2} \sum_k \mathcal{L}(f_k) \times \sin^2(\pi f_k \tau) \quad (12)$$

Each spur's contribution (EMI, cross-talk, phase-locked-loop reference spurs, coupling and other sources) are then added in sum square fashion as follows:

$$\Delta t_{RMS\_Total}^2 = \Delta t_{RMS\_EMI}^2 + \Delta t_{RMS\_1}^2 + \Delta t_{RMS\_i}^2 + \dots + \Delta t_{RMS\_k}^2 \quad (13)$$

$$\Delta t_{RMS\_Total}^2 = \Delta t_{RMS\_EMI}^2 + \sum_{i=1}^k (\Delta t_{RMS\_i}^2) \quad (14)$$

$$Jitter_{Total}^2 = Jitter_{EMI}^2 + Jitter_{Noise-Floor}^2 + Jitter_{Phase-Noise}^2 \quad (15)$$

From (4)-(15), radiated EMI induced noise voltage influences dynamically the operating resonant modes, transconductance and impedance transfer functions of the crystal oscillator circuit, resulting induced sub-harmonic (lower than the fundamental frequency). In addition to this, EMI induced noise voltage propagates through the circuit gates and this voltage can be amplified or reduced depending on the noise propagation path of the circuits, thus influences the time domain jitter dynamics.

#### IV. EMI MINIMIZATION TECHNIQUES

As system operating frequencies and the need for lower current consumption increases, physics dictates that end applications will also tend to become increasingly susceptible to externally generated EMI sources. These electrical influences can be generated by either radiated or conducted EMI noise sources. Radiated EMI noise sources include anything electrical or electromechanical, including motors, power lines interference, antennas, traces on a Printed Circuit Board (PCB), and even the components on the PCB. Conducted EMI noise sources primarily manifest themselves as electrical "noise" on the power supply lines of an application and can be caused by induced voltage spikes from external devices like those mentioned above, or by RF coupling within the system itself.

The CAD simulation techniques to predict conducted and radiated emission is a difficult and time-consuming task. It is well known that, during system development, critical signal-integrity and EMI (electromagnetic-interference) simulations are difficult, time-consuming, and error-prone due to their reliance on hard-to-predict models and parameter extractions. This situation worsens with every new product generation due

to steadily increasing clock speeds and decreasing supply voltages, resulting in reduced noise margins [19].

An oscillator circuit is commonly significant source of radiated emissions in electronic systems. These emissions are often excited by the current flowing through the power-supply lead of the oscillator.

Fig. 13 shows the typical plot of the conductive and radiated EMI test, which gives comparative insights about the radiated noise before and after noise suppression techniques [20].

Fig. 14 shows the typical EMC test due to radiated EMI for the qualitative analysis of the system immunity against variation in jitter due to unwanted interferences. The measured conducted and radiated noise data as shown in Figs. 13 and 14 are a typical qualitative representation and will vary based upon oscillator topology and the surrounding peripheral electronic circuitry and sub-systems.

In this paper, we studied the circuit techniques based on phase-injection mechanism, which provides immunity towards EMI and jitter for the reference frequency standard applications.

#### V. DESIGN EXAMPLE AND VALIDATION

For the high frequency operation, a method is needed to select a particular resonance mode so that other active modes such as: EMI-induced sub-harmonics, parasitic modes, and overtone modes fail to co-exist and sustained oscillations. The simplified technique is to maximize the negative resistance generated from the active device network for a given particular mode and must yield positive value of resistance for unwanted modes, including EMI-induced oscillations. This can be accomplished by using mode-coupling (tuning the  $L_m$ - $C_m$  at higher order modes) and phase-injection  $\phi(\omega \pm \Delta\omega)$  mechanism for a given mode-coupling and the drive-level  $I_R(\omega)$  (Fig. 15).

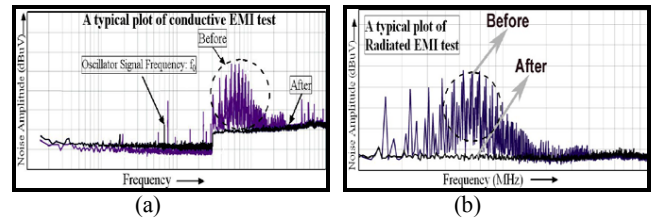


Fig. 13. (a) A typical plot of conductive EMI test, and (b) plot of the radiated noise EMI test

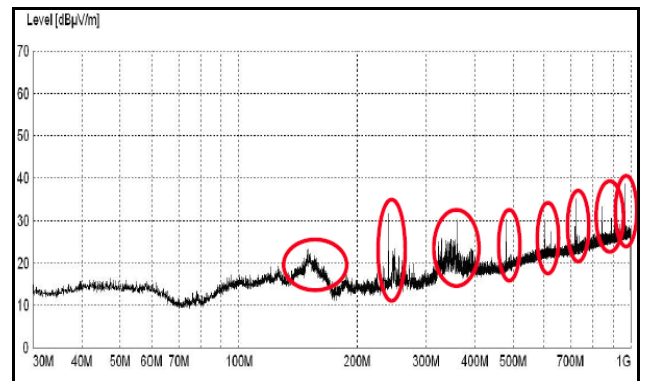


Fig. 14. A typical plot of EMC test due to EMI radiated noise

In general, coupling capacitor  $C_{V1}$  suffice the oscillation growth (without  $C_{V2}$  and  $C_{V3}$ ) but at the cost of slow start-up characteristics and high drive level  $I_R(\omega)$ .

Fig. 16 shows the typical schematic of the mode-coupled phase-injection locked 100 MHz crystal oscillator (XO) circuit, which sets up optimum and noise impedance transfer function by dynamically controlling mode-coupling and phase-injection for a given drive level and star-up time.

As shown in Fig. 16, the higher order mode is coupled through output path and feedback to the point where frequency-drive sensitivity of the crystal resonator shows maximum group delay and faster slew rate, resulting, improved EMI performance with reduced drive-level  $I_R(\omega)$ .

The biggest challenge is the characterization of EMI simulated interference sources for the validation of EMI-induced failure due to frequency shift caused by induction of sub-harmonics into crystal resonator. In addition to this, phase-injection locking mechanism is very critical, slight variation in phase may cause oscillation to cease; therefore, phase-locked-loop (PLL) option can be more practical for commercial applications.

Although, mode-coupling phase-injection restricts the frequency drift to the greater extents still crystal oscillator can induce sub-harmonic response under the influence of external radio frequency interference (RFI) around the crystal oscillator circuit.

Figs. 17, 18, and 19 shows the measured phase noise plot of the 100 MHz crystal oscillator circuit that gives comparative and qualitative insights about the jitter and noise reduction in presence of the radiated EMI. As shown in Fig. 17, the noise floor exhibits bump at 5 MHz offset from the carrier for oscillator circuit that has poor shielding.

Fig. 18 shows improved noise floor (with shielding) as compared to the phase noise plot shown in Fig. 17 (without shielding).

For the validation purpose, mode-feedback and phase-injection mechanism is incorporated for the application of EMI insensitive crystal oscillator topology.

As illustrated in Fig. 19 the novel phase-injection mode-feedback techniques improves the stability and phase noise performance by 5-10 dB. The circuit operates at 5V, 30 mA and also suitable for tunable crystal applications.

In addition to this shielding improves the jitter and phase noise performances, the stability against EMI-induced failure.

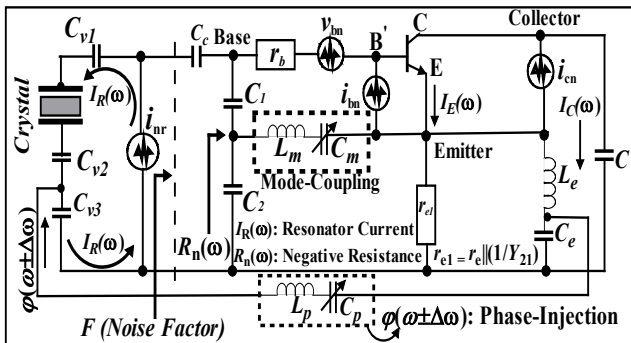


Fig.15. A typical mode-coupled phase-injected  $\phi(\omega \pm \Delta\omega)$  crystal oscillator, including noise contributions (transistor and resonator)

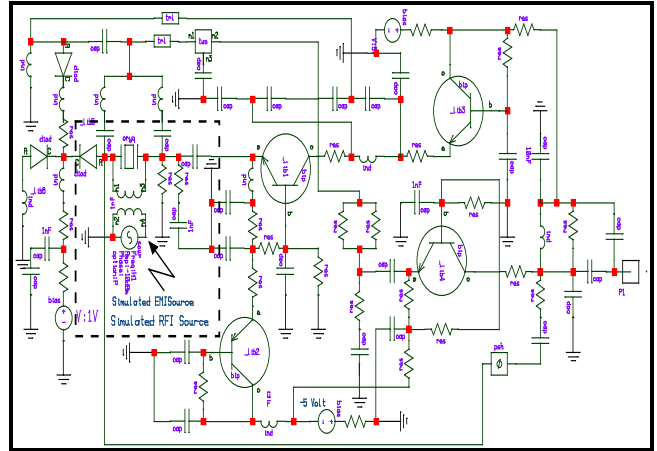


Fig. 16. Schematic of 100 MHz mode-coupled Crystal oscillator

The likelihood of frequency shift and noise floor in a noisy EM environment is far higher, however this paper describes the mode-coupled and phase-injection techniques to restrict the shift up to the acceptable degree due to radiated EMI and also minimizes the phase noise (Fig. 19).

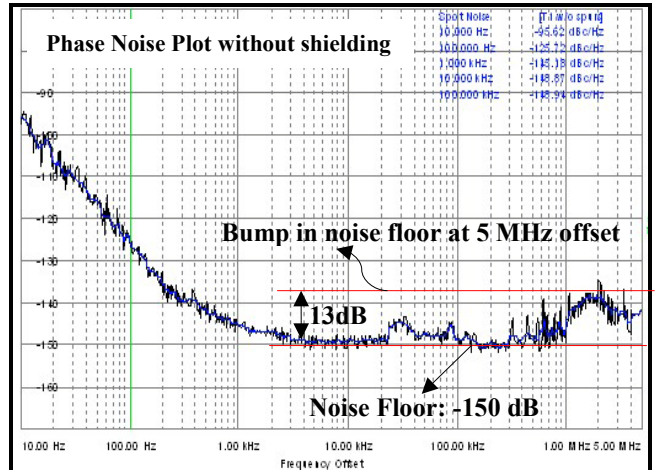


Fig. 17. Measured phase noise plot of 100MHz XO without shielding

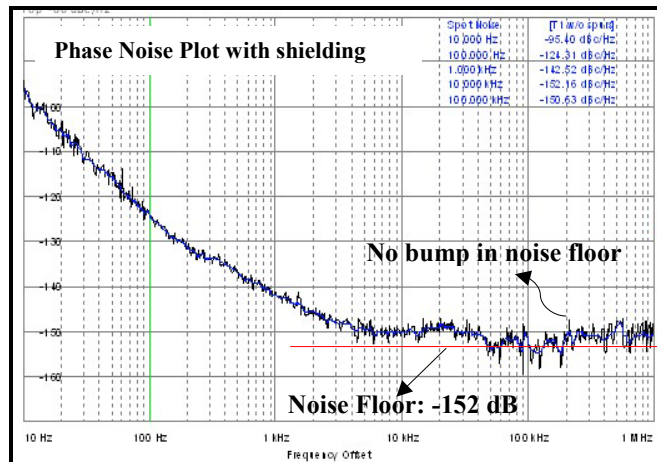


Fig. 18. Measured phase noise plot of 100MHz XO with shielding

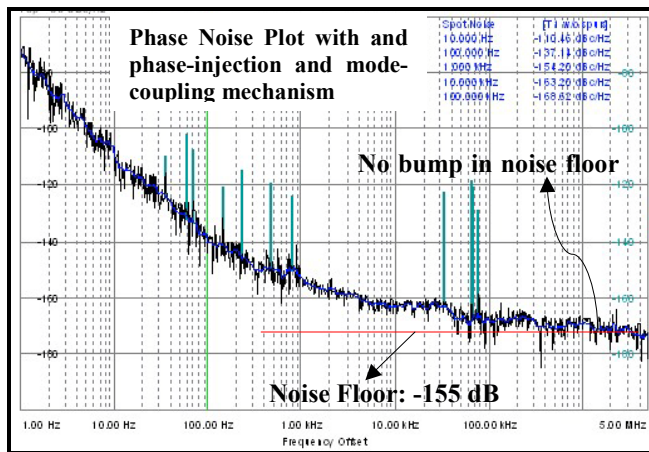


Fig. 19 Measured phase noise plot of 100MHz XO with phase-injection and mode-feedback mechanism.

## VI. CONCLUSION

Modern communication systems are particularly susceptible to electromagnetic interference (EMI), which can induce the crystal oscillator circuits to oscillate at different modes and sub-harmonics. As a by-product of a normal mode of operation, start-up dynamics and stability also deteriorates under the influence of electromagnetic radiation/interference.

This work offers a novel crystal oscillator circuit using mode-coupling and phase-injection techniques for improved electromagnetic interference (EMI), start-up, and drive-level, dynamics for the realization of high frequency reference frequency standards.

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