Design Parameters and Practical Considerations in the Two-Phase Forced-Convection Cooling of Multi-Chip Modules

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Forced-convection boiling was investigated with a dielectric coolant (FC-72) in order to address some of the practical issues related to the two-phase cooling of multi-chip modules. The module used in the present study featured a linear array of nine, 10×10 mm^2, simulated microelectronic chips which were flush-mounted along a 20-mm wide side of a rectangular channel. Experiments were performed with a 5-mm channel gap (distance between the chip surface and the opposing channel wall) at eight orientations spaced 45 degrees apart. Two other channel gaps, 2 and 10 mm, were tested in the vertical upflow configuration. For all these configurations, the velocity and subcooling of the liquid were varied from 13 to 400 cm/s and 3 to 36°C, respectively. Changes in orientation did not affect single-phase or nucleate boiling characteristics, but did have a major impact on CHF. Upflow conditions were found to be the best configuration for the design of two-phase cooling modules because of its inherently stable flow and relatively high CHF values. The CHF value for the most upstream chip in vertical upflow agreed well with a previous correlation for an isolated chip. Combined with the relatively small spread in CHF values for all chips in the array, this correlation was found to be attractive for design purposes in predicting CHF for a multi-chip array. To achieve a given CHF value, it is shown how the strong CHF dependence on velocity rather than flow area allows for a reduction in the required flow rate with the 2-mm, as compared to the 5-mm gap, which also required a smaller flow rate than the 10-mm gap. This reduction in flow rate was significant only with subcooled conditions corresponding to high CHF values.

Introduction

The ability to transfer heat from the hardware of microelectronic systems is a growing problem for designers of today's computer systems. Steady increases in chip heat dissipation and in the packaging densities of multi-chip modules have rendered ineffective the traditional convection-by-air cooling techniques, and attention has been shifted to alternative technologies such as direct immersion cooling (Chu, 1986; Simons, 1987). Direct immersion cooling features an intimate contact between the chip surface and the liquid, which greatly improves heat transfer from the chip. In addition, since direct immersion coolants typically possess low boiling points, heat transfer from the chip can be further augmented through nucleate boiling at the chip surface. However, there is a practical limit to the amount of heat that can be transferred from the chip by nucleate boiling, and this limit is commonly referred to as critical heat flux (CHF).

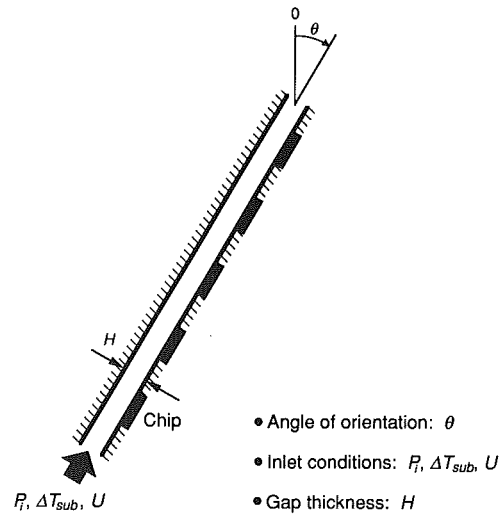

Fig. 1 Experimental parameters in the design of the multi-chip cooling modules

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Critical heat flux is a complex phenomenon that appears to be dominated simultaneously by hydrodynamic interactions of vapor and liquid in the vicinity of the heated surface as well as a process of liquid evaporation on the surface. Several researchers have shown that CHF is induced by the development of a vapor blanket at the heated surface (Vliet and Leppert, 1964a,b; Gaertner, 1965; Mudawar et al., 1987). This blanket hinders the ability of cooler bulk liquid to replenish the evaporating liquid at the heated surface. With increases in surface heat flux, the vapor blanket eventually promotes dryout of the heated surface, spawning rapid increases in surface temperature. It is well-known that increases in either liquid velocity or subcooling serve to postpone development of the vapor blanket, thus expanding the range of heat fluxes in which practical systems can operate (Gunther, 1951; Vliet and Leppert, 1964a,b; Yilmaz and Westwater, 1980; Maddox and Mudawar, 1989). Mudawar and Maddox (1989) constructed a semi-empirical CHF model for an isolated simulated microelectronic chip in a flow channel as given as

$$q_m^{**} = \frac{\dfrac{q_m''}{\rho_g U h_{fg}}}{\left(\dfrac{\rho_f}{\rho_g}\right)^{15/23}\left(\dfrac{L}{D}\right)^{1/23}\left(1+\dfrac{c_{pf}\Delta T_{sub}}{h_{fg}}\right)^{7/23}\left(1+0.021\dfrac{\rho_f}{\rho_g}\dfrac{c_{pf}\Delta T_{sub}}{h_{fg}}\right)^{16/23}} = 0.161\ (\mathrm{We})^{-8/23} \qquad (1)$$

Equation (1) has been successful in correlating CHF data for flush-mounted heaters from several studies (McGillis et al., 1991; Gu et al., 1989). Mudawar and Maddox (1989) were successful in using Eq. (1) to correlate the CHF data of Umaya (1983) for a small flush mounted cylindrical heater.

Several researchers have tested the effects of surface orientation in pool boiling (Nishikawa et al., 1983; Chen, 1978; Githinji and Sabersky, 1963). Heat transfer increased, noted by a decrease in wall superheat, as the boiling surface was rotated from the horizontal, upward-facing position to beyond the vertical position. The increase in heat transfer was attributed to the agitation of the superheated liquid layer by passing bubbles as they moved along the surface. With further rotation of the surface to the horizontal downward-facing position, heat transfer rapidly deteriorated because the bubbles no longer moved but accumulated on the boiling surface.

Mishima and Nishihara (1985) studied the effects of upflow and downflow of water at low velocities on CHF in thin rectangular channels. For upflow, the lowest value of CHF occurred at zero flow rate and then increased almost linearly with increasing mass velocity. For downflow, the lowest value of CHF did not occur at zero flow rate, but at some low, yet finite critical mass velocity which caused bubbles to be suspended motionless in the channel. Mass velocities smaller than the critical value slightly increased CHF as the bubbles experienced counterflow, and substantial increases in CHF occurred for mass velocities above critical. Critical heat flux values for a given upflow mass velocity were always greater than those for downflow.

The effect of gap thickness available for liquid flow above the heated surface in boiling systems has been studied by some researchers. Hung and Yao (1983) found CHF decreased for a constant mass velocity as the gap size of their R-113 cooled annuli decreased from 2.58 to 0.32 mm. Tolubinskiy et al. (1969) examined water cooled annuli with gap widths varying from 0.1 to 1.3 mm. CHF also decreased with decreasing gap width for a constant mass velocity.

The rapid escalation in surface temperature that accompany CHF can easily damage the integrity of a microelectronic chip. For this reason, designers of direct immersion cooling systems are often confronted with the need to accurately predict the occurrence of CHF in their system. Figure 1 illustrates five of the parameters which must be considered when designing a two-phase cooling system for a given multi-chip module. First, the angle at which the circuit board is oriented with respect to gravity will affect bubble trajectories and flow patterns. The inlet flow conditions determine pumping costs and the size and complexity of the system plumbing and heat exchangers. Increased subcooling has the benefits of increased CHF and decreased void fraction throughout the system but requires additional system hardware. The need to prevent air entrainment into the dielectric fluid and the fragile structure of electronic hardware limit the freedom in setting inlet pressure to values slightly above atmospheric. Lastly, the gap (channel) thickness introduces an optimization problem of increased fluid velocity for a constant flow rate at the expense of a higher pressure drop and a higher void fraction. Though several studies have been conducted on boiling heat transfer for isolated heat sources (e.g., Maddox and Mudawar, 1989; Samant and Simon, 1989), only a few studies have focussed on the investigation of multi-chip configurations which simulate circuit boards (McGillis et al., 1991; Willingham et al., 1991; Willingham and Mudawar, 1992a,b).

The present paper will address the parametric effects associated with designing two-phase direct immersion electronic

Nomenclature

A_w = chip wetted area (10×10 mm^2)
A_x = channel flow area
c_p = specific heat at constant pressure
D = hydraulic diameter of channel, $4A_x/P_{wet}$
H = channel gap thickness (2, 5, or 10 mm)
h_{fg} = latent heat of vaporization
L = chip length in flow direction (10 mm)
n = number of chips in a multi-chip array (nine in the present study)
P_{wet} = wetted perimeter of channel
P_i = fluid pressure at the channel inlet
Q = volumetric flow rate
q'' = wall heat flux
q_m'' = critical heat flux
q_m^{**} = nondimensional critical heat flux
T = temperature
ΔT_{sat} = wall superheat, $T_w - T_{sat}$
ΔT_{sub} = inlet liquid subcooling, $T_{sat} - T_{f,in}$
ΔT_w = temperature gradient between the chip surface and inlet liquid, $T_w - T_{f,in}$
U = mean inlet liquid velocity
W = channel width (20 mm)
We = Weber number, $(\rho_f U^2 L)/\sigma$
x_e = thermodynamic equilibrium quality
α = void fraction
ϵ = ratio of total power dissipated by chip array to the sum of sensible and latent heat of liquid at the module inlet
ρ = density
σ = surface tension
θ = orientation angle measured from the vertical position

Subscripts

f = liquid
g = vapor
in = inlet to multi-chip module
sat = saturated
w = mean chip surface condition

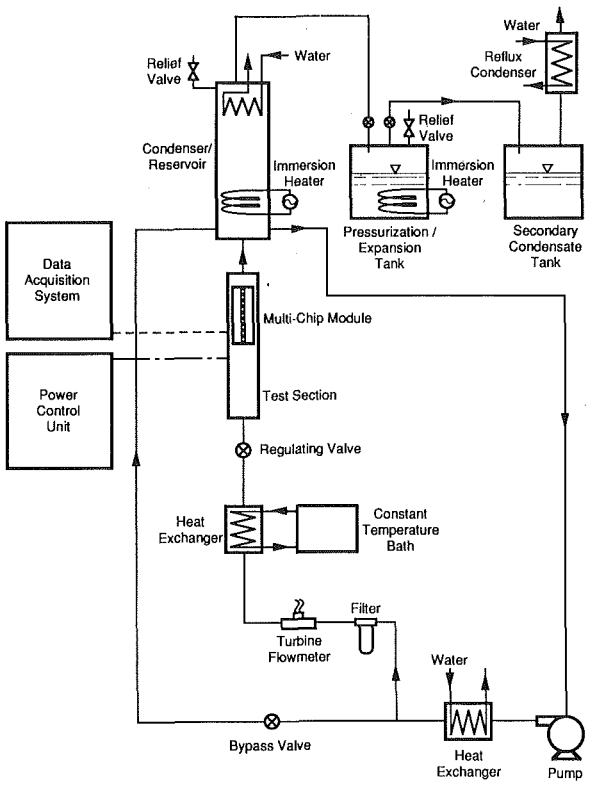

Fig. 2 Flow loop

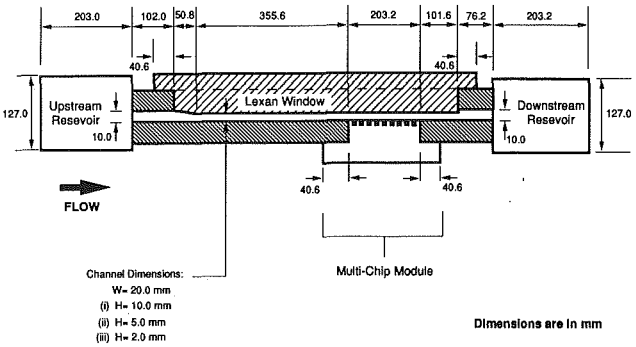

Fig. 3 Longitudinal section of flow channel

cooling systems that have not been discussed previously, particularly as the design parameters influence CHF. The discussed findings are based upon experiments involving forced-convection boiling of FC-72 from a linear array of nine simulated microelectronic chips. Addressed are the effects of orientation, θ, inlet velocity, U, subcooling, ΔT_{sub}, and channel gap, H. Practical considerations associated with thermal interactions between the chips in multi-chip modules will also be discussed.

Experimental Methods

Test Section. A two-phase flow loop, shown in Fig. 2, was constructed in order to circulate the dielectric coolant and maintain the desired system conditions. Two flat plate heat exchangers served to fine tune the fluid temperature at the inlet to the test section. An immersion heater in the pressurization/expansion tank along with an immersion heater and water-cooled condenser in the condenser/reservoir maintained steady system pressure during all tests. Figure 3 illustrates the test section which was comprised of the flow channel, upstream and downstream reservoirs, and multi-chip module. The upstream reservoir helped straighten the inlet liquid flow and break up turbulent eddies. Located at the exit of the channel, the downstream reservoir allowed the two-phase mixture to exit the channel without disturbing the flow upstream. The primary function of the flow channel was to hydrodynamically develop the liquid flow before it reached the chip array. The body of the flow channel was comprised of a three-piece G-10 fiberglass assembly. A Lexan window served as one wall for most of the channel length, and the multi-chip module formed the opposite wall at the location of the chips. The channel width was 20.0 mm, while variations of channel gap, 2.0, 5.0, and 10.0 mm, were made possible with three different window designs.

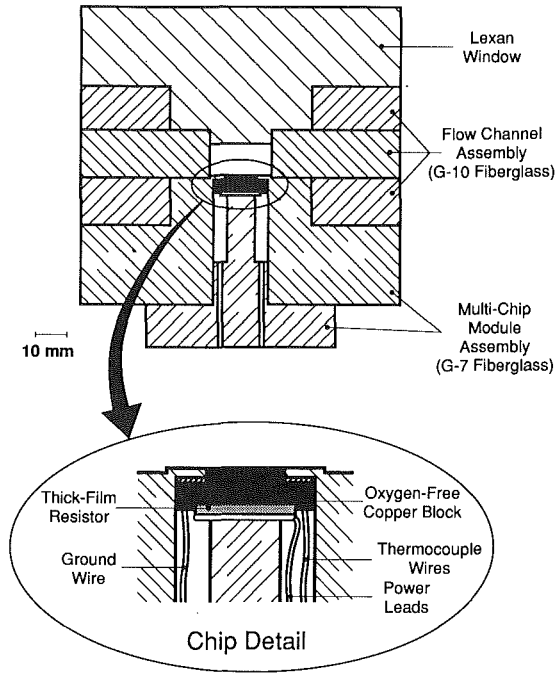

Fig. 4 Cross-sectional view of test section illustrating construction of the simulated microelectronic chip

The test section was rotated in 45-degree increments by means of a support frame. The vertical position with the fluid flow opposing gravity (upflow) was designated as the 0-degree reference. The magnitude of orientation angle increases from 0 as the test section rotates in both directions, with positive angles referring to orientations in which the chip surfaces were upward-facing with respect to gravity and negative angles to downward-facing chip surfaces.

Multi-Chip Module. The most upstream edge of the first simulated microelectronic chip was positioned 524.5 mm downstream of the channel inlet. The multi-chip module consisted of a G-7 fiberglass assembly which provided easy access to the chips. Figure 4 shows a cross-sectional view of the test section, with the chips flush-mounted and centered along one wall of the flow channel. To identify specific chips within the array, a nomenclature was established that referred to Chip 1 as the most upstream chip in the array. The remaining chips were sequentially assigned numbers up to nine that increased with distance downstream of Chip 1.

Each chip was fabricated from oxygen-free copper such that the cross-sectional dimensions of the chip surface in contact with the liquid were 10.0 mm × 10.0 mm. The pitch between consecutive chips was 20.0 mm which made the distance between the upstream edge of Chip 1 to the downstream edge of Chip 9 a total of 170 mm. A thick-film resistive heater with similar surface area and approximate resistance of 90 Ω was soldered to the underside of each copper block. The voltage

across each chip was equivalent, while the current through each chip varied according to the actual resistance of the thick-film resistor. Prior to operation, a variable resistor in-line with each individual chip was trimmed such that the power dissipated in each resistive heater was the same. The chips were also instrumented with three Chromel-Alumel thermocouples for determining the chip surface temperature. The three thermocouples were embedded along the chip centerline with respect to the flow direction at a depth of 0.81 mm beneath the chip surface. During operation, an area-weighted average of the three thermocouple measurements was determined by accounting for the fraction of surface area corresponding to each thermocouple, and this average was then corrected for one-dimensional heat conduction between the thermocouple plane and the surface.

Operating Procedure and Experimental Error. Both vapor-blasting of the chip surface and deaeration of the fluid helped to standardize operation procedure. Prior to a series of experiments, the surfaces of the chips were vapor-blasted with fine silica particulates entrained in water flow. The average size of the particulates was 10 μm, and the vapor-blasting created a relatively uniform distribution of micro-cavities on the surfaces of all chips. Each day of experimentation was commenced by heating the fluid to saturation with the system open to the atmosphere. During this time, FC-72 vapor and noncondensible gases were routed from the flow loop to a water-cooled reflux condenser. The condenser allowed the noncondensible gases to escape to the ambient while the FC-72 condensed and dripped back into the condensate tank.

During the tests, a data acquisition system was instructed to obtain temperature and heat flux measurements for the chips, fluid temperature in the upstream reservoir, absolute pressure at Chip 1, differential pressure between the most upstream (Chip 1) and downstream chip (Chip 9), and inlet velocity of the liquid. The degree of subcooling and the mean velocity of the liquid at Chip 1 were maintained constant throughout the experiment. The pressure at Chip 1 was maintained at 1.36 bar (20 psia), which corresponds to a saturation temperature of 66.18°C, and this pressure was used in conjunction with the fluid temperature in the upstream reservoir to determine the inlet subcooling.

Steady-state was assumed when twenty data samples for each of the chip temperatures taken over a twenty-second period had a standard deviation of less than 0.10°C, or for some of the downflow orientations near CHF, when the surface temperature oscillations (±1.5°C) became steady and repeatable over several minutes. As CHF was approached, heat flux increments were lowered to 0.5 W/cm^2, and CHF was approximated by adding one half of the last power increment (~0.25 W/cm^2) to the last stable heat flux. Critical heat flux was signalled by a large and rapid increase in the chip temperature. Once CHF was attained, the power to the chip was shut off, which enabled the experiments to proceed until all nine chips had reached CHF without physical damage to the test section.

Experimental uncertainties resulted from errors in the various instruments used in the measurments. The maximum error associated with each thermocouple reading was estimated to be less than 0.2°C. The parameters in the one-dimensional heat conduction adjustment introduced a maximum uncertainty of ±0.1°C in the chip surface temperature. The voltage and current transducers were calibrated, and the maximum error of the power reading was estimated to be ±3.3 percent at 30.0 W/cm^2 and ±1.6 percent at 120 W/cm^2. A two-dimensional, finite-difference heat loss analysis on the test section determined that the largest heat loss from the chips was 3 percent; thus, no adjustment was made to the chip heat flux. Experimental uncertainty associated with the small (1.3×10^{-6} – 8.2×10^{-5} m^3/s) and large (3.8×10^{-5} – 3.8×10^{-3} m^3/s) flowmeters were at most ±1.0 and ±2.68 percent, respectively. The uncertainty associated with the pressure transducer readings were ±0.0103 bar (±0.15 psi).

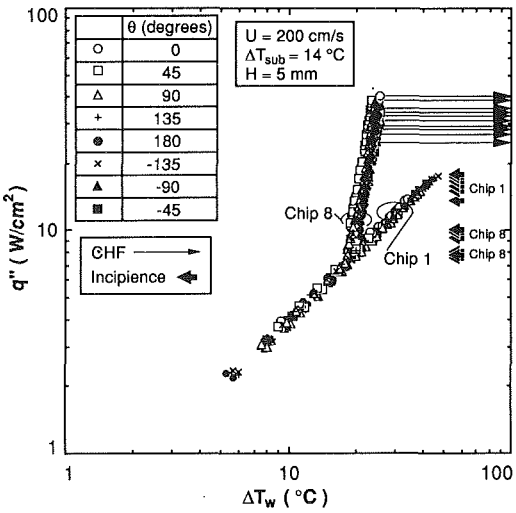

Fig. 5 Boiling curves for Chips 1 and 8 at an inlet velocity of 200 cm/s and 14°C subcooling for all orientations

Results and Discussion

Forced-convection boiling experiments were performed on a linear array of simulated microelectronic chips. The 5-mm channel gap was initially tested at eight angles of orientation at 45-degree increments. Two other channel gaps, 2 and 10 mm, were then investigated in the vertical, upflow position. For each channel configuration, the velocity and subcooling of the liquid were varied from 13 to 400 cm/s and 3 to 36°C, respectively. This section discusses practical considerations associated with the individual parametric effects involved with the two-phase forced-convection cooling of multi-chip modules.

Effect of Orientation. Boiling curves of Chips 1 and 8 are shown in Fig. 5 for all eight angles of orientation. Single-phase and nucleate boiling heat transfer did not appear to be affected by the change in angle as the boiling curves for all eight angles fell on top of each other. Except for the incipience of nucleate boiling, the heat transfer characteristics of each chip in the array were also similar for all orientations as shown in Fig. 5 by the collapsing of all of the boiling curves on one another. Chip 1 had a high incipience temperature drop because the stream-wise warming of the fluid near the wall promoted nucleate boiling for the downstream chips at lower fluxes than for the upstream chips; consequently, the downstream chips had relatively small incipience temperature drops. The only measurable effect of orientation on the performance of the multi-chip array was CHF.

Since the electrical power to each chip could be stopped once CHF was attained, the experiments continued until all of the chips reached CHF. The first chip to progress to film boiling (not necessarily Chip 1) determined the minimum CHF for the multi-chip array. Figure 6 is a polar representation of minimum CHF values for three inlet fluid conditions. At low velocities, critical heat flux decreased as the channel was rotated away from 0, 45, and −45 degrees as illustrated in Fig. 6 for U = 50 cm/s. The largest decrease in CHF occurred for the downward-facing chips subjected to downflow (angles −90, −135, and 180 degrees) while the decreases for upflow and/or upward-facing chips were not as severe. Increasing the subcooling served to dampen the effect of orientation, but there was still a decrease in CHF for downflow and downward-facing chips as evidenced by comparing the cases with ΔT_{sub} = 3 and 25°C

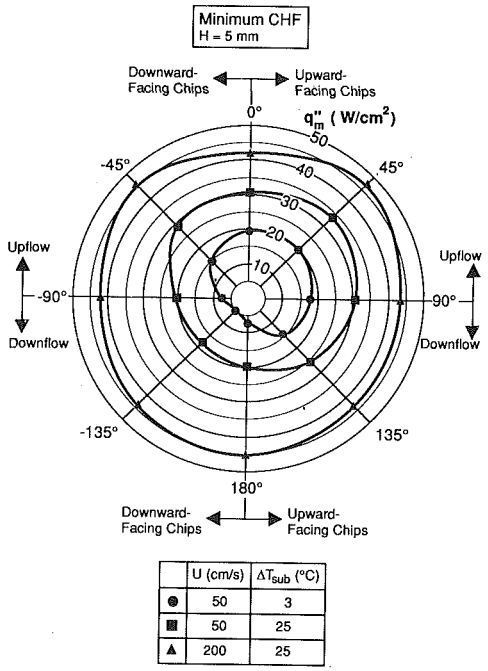

Fig. 6 Polar representation of the velocity and subcooling effects on the minimum critical heat flux value in the multi-chip array

for $U = 50$ cm/s. High velocity was effective at diminishing the orientation effect as shown in Fig. 6 for $U = 200$ cm/s. For near-saturated flow, orientation no longer had a noticeable effect on CHF for inlet velocities greater than 200 cm/s. For highly-subcooled flow, velocities as low as 150 cm/s were not affected by orientation.

Figures 7(a) and 7(b) further illustrate the effects of orientation on CHF. The minimum and maximum CHF values in the multi-chip array are shown in Fig. 7(a) for $\theta = 45$ degrees for near-saturated and highly subcooled flow. Critical heat flux increased with increasing velocity except for a slight leveling of CHF for near-saturated flow around 100 cm/s. Figure 7(b) shows the minimum and maximum CHF values in the multi-chip array for $\theta = -135$ degrees. By comparing Figs. 7(a) and 7(b), the detrimental effect of downflow and downward-facing configurations becomes evident by the reduction of CHF values for the individual chips, the widening of the spread between minimum and maximum CHF values in the multi-chip array, and the adverse relationship between CHF and velocity for low velocities. At the lowest inlet velocity, $U = 13$ cm/s, the bubbles were observed to flow counter to the bulk liquid at $\theta = 135$, 180, and -135 degrees and cause a high degree of fluid agitation in the channel. At times large vapor bubbles commonly observed in slug flow formed over the chips and traveled up through the channel before condensing. Because the larger bubbles quickly passed over the chips, no noticeable effect on the wall temperature was detected; however, the wall temperature of some chips oscillated by up to ± 1.5°C near CHF at these low velocities. By increasing the inlet liquid velocity at these same orientations, the bubbles eventually stagnated over the chip surface as the opposing drag and buoyancy forces acting on the bubble became equal. The stagnant bubbles drastically reduced CHF, as evidenced by the minimum points in Fig. 7(b), by starving the chip surface of liquid. As the inlet velocity was further increased, the bubbles became entrained in the bulk flow, and CHF resumed its usual trend increasing with increasing velocity.

In order to compare the spread in CHF data between test parameters, a CHF bandwidth was defined as the difference

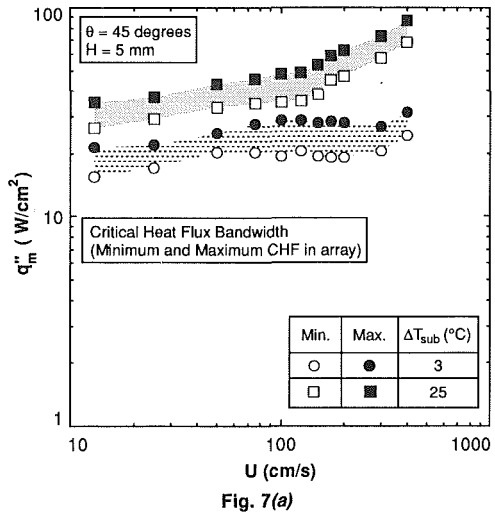

Fig. 7(a)

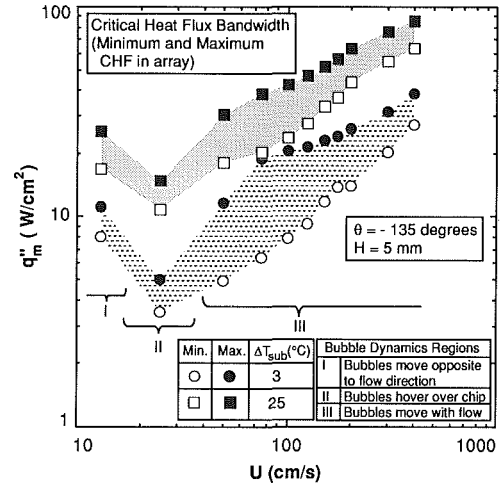

Fig. 7(b)

Fig. 7 Critical heat flux bandwidth for the multi-chip array for inlet subcoolings of 3 and 25°C and orientations of *(a)* 45 degrees and *(b)* −135 degrees

between minimum and maximum CHF divided by the average CHF in the multi-chip module,

$$\text{CHF Bandwidth } (\pm x\%) = \frac{(\text{Maximum CHF} - \text{Minimum CHF})}{\frac{1}{2}(\text{Maximum CHF} + \text{Minimum CHF})} \times (\pm 50\%) \quad (2)$$

The CHF bandwidth tended to decrease as the subcooling increased. For the data in Fig. 7(a) ($\theta = 45$ degrees), the average CHF bandwidth was 15.9 and 13.7 percent for the near-saturated and highly-subcooled conditions, respectively. At $\theta = -135$ degrees, Fig. 7(b), the corresponding bandwidths were 30.6 and 21.8 percent, respectively. In general, downflow configurations had higher average CHF bandwidths, for all velocities and subcoolings combined, of 20.4 to 24.8 percent while upflow had average bandwidths of 12.3 to 15.6 percent.

Flow stability of the two-phase loop is another crucial concern in the design of an electronic cooling system. Ideally, either complete liquid flow or a near-homogeneous liquid-vapor mixture are the best flow patterns from a stability standpoint. At the two horizontal orientations, $\theta = 90$ and -90 degrees, stratified flow was observed to exist in the channel for some experimental conditions. When the liquid and vapor phases are separated, the vapor can travel at a much higher

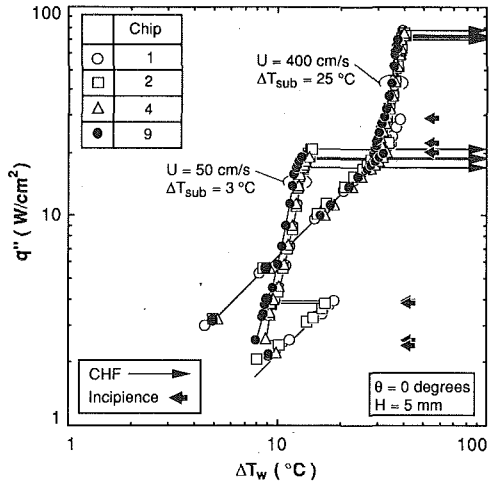

Fig. 8 Velocity and subcooling effects on the boiling curve for Chips 1, 2, 4, and 9 oriented at 0 degrees

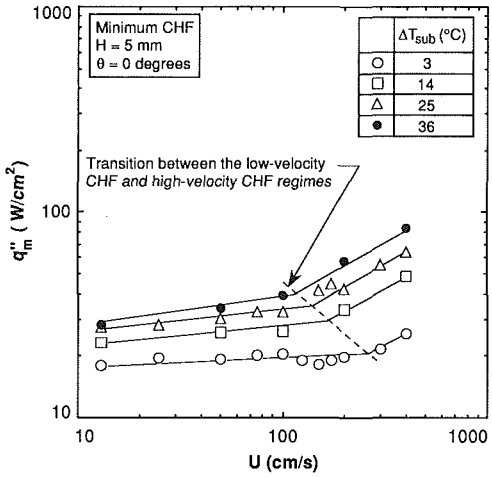

Fig. 9 Minimum critical heat flux values for the multi-chip array in vertical upflow

velocity than the liquid which could lead to interfacial waviness and eventual plug flow. Plug flow is often associated with undesirable pressure oscillations. Another flow stability concern is the counterflow or stagnation of the bubbles at low velocities when the test section is at $\theta = 135$, 180, and -135 degrees; stagnation prevents the vapor from assuming its regular path toward the condenser/reservoir. Vapor can also become trapped in local high junctions located in the system wherever the fluid motion in the two-phase leg of the loop opposes the buoyancy force. Even under seemingly normal operating conditions in the cooling module, the trapped vapor can cause a momentary blockage of the flow which would result in density and pressure wave oscillations in the entire loop. For these reasons, upflow represents the most sensible orientation for the two-phase leg of the cooling system, especially in the cooling module itself. Therefore, the rest of the discussion will focus entirely on the 0-degree (vertical upflow) orientation because the overall CHF performance of this orientation was better than the other two upflow angles (± 45 degrees) despite the data shown in Fig. 6.

Interactions Between Chips in the Multi-Chip Array. The effects of velocity and subcooling on heat transfer from the multi-chip array are shown in Fig. 8 for four chips. As mentioned earlier, all of the chips in the array had roughly the same single-phase heat transfer coefficient as evidenced by the small deviations between the single-phase portions of the boiling curves at each velocity. This suggests the nonheated wall segments between the chips serve to reinitiate the thermal boundary layer on each chip; otherwise, the single-phase heat transfer coefficient would decrease in the stream-wise direction in a manner similar to that of a long heater. Stream-wise warming of the fluid near the wall promotes incipience of nucleate boiling at lower heat fluxes for downstream chips. Throughout the study, Chips 1 and 2 experienced a much higher temperature drop at boiling incipience. From a practical standpoint, a large incipience temperature drop is undesirable when cooling electronic equipment because of the potential for thermal shock to the device. For this reason, installing a heated patch upstream of the chips is suggested as a means to initially preheat the fluid and decrease the incipience temperature drop for the entire array of chips.

Nucleate boiling was similar for all of the chips in the array because the pressure drop in the channel was small. Pressure drop effects on boiling will be discussed in more detail later. For increases in velocity at a given subcooling, the surface temperature of the chip remained roughly the same for a given heat flux, and all of the boiling curves tended to fall on top of each other except for fluxes nearing CHF. With increased subcooling at a fixed velocity, the wall temperature of the chip decreased at a given heat flux. Because the wall-to-inlet fluid temperature difference is plotted with respect to heat flux in Fig. 8, the boiling curves are shifted to higher ΔT_w's even though T_w decreased.

Critical heat flux increased with increases in velocity and subcooling as shown in Fig. 9. The change in slope in the CHF data in Fig. 9 marks the transition between low-velocity and high-velocity CHF regimes. The transition in CHF was first reported by Mudawar and Maddox (1989) for single chip experiments in vertical upflow. The two regimes differed by the mechanisms of vapor layer development and dryout. Lower velocities promoted the formation of a large vapor blanket, causing a cessation of liquid supply to the entire surface. Higher velocities allowed liquid to break through the blanket and wet many spots on the surface even at fluxes slightly smaller than CHF. In each case, CHF occurred when the sum of sensible and latent heat of the supplied liquid could no longer balance the chip electrical energy. Figure 9 shows increasing velocity increased CHF more in the high-velocity CHF regime than in the low-velocity regime.

Since the present experimental apparatus allowed for continued testing until all nine chips had attained CHF, the order of progression to CHF could be carefully examined. For vertical upflow, ($\theta = 0$), the two most upstream chips in the multi-chip array tended to reach CHF first in the near-saturated experiments, and the last two chips tended to reach CHF last. This trend was reversed, though, for highly-subcooled flow. In near-saturated flow, the bubbles emanating from the upstream chips were relatively large and caused significant agitation of the thin, superheated wall layer. Despite the bulk temperature being close to saturation, this agitation could have prevented fluid near the wall from warming up appreciably through the multi-chip module. This, coupled with the stream-wise increase in velocity due to the increased void fraction served to delay CHF on the downstream chips. However, in highly-subcooled flow, the bubbles condensed almost immediately downstream of the chips, resulting in a small void fraction in the bulk flow and negligible stream-wise velocity increase. Furthermore, the suppressed agitation in subcooled flow dampened mixing of the superheated layer with bulk fluid causing the temperature of near-wall fluid to increase appreciably in the stream-wise direction. It is therefore suggested that downstream chips reach CHF earlier because of the greatly diminished subcooling of the liquid adjacent to the surfaces of these chips.

In vertical upflow, Chip 1 should act like an isolated chip since no heating or bubble generation occurs upstream of Chip

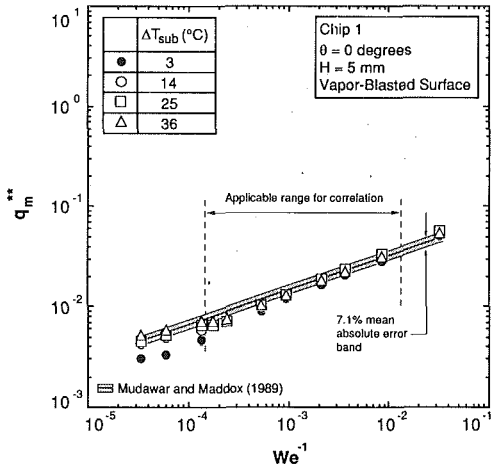

Fig. 10(*a*)

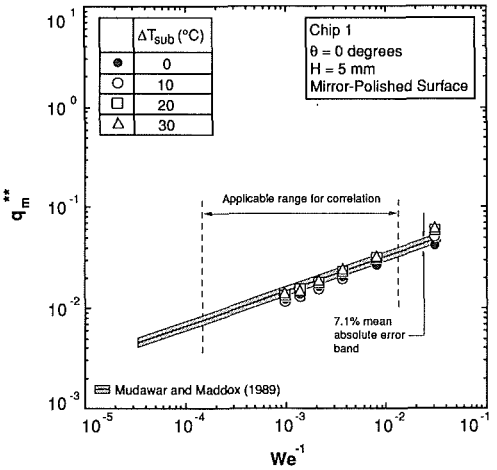

Fig. 10(*b*)

Fig. 10 Comparison of nondimensional critical heat flux data for Chip 1 in vertical upflow with the correlation of Mudawar and Maddox (1989) for *(a)* vapor-blasted surface (adapted from Willingham and Mudawar, 1992a) and *(b)* mirror-polished surface

1. The CHF values of Chip 1 were compared to the correlation of Mudawar and Maddox (1989), Eq. (1), for an isolated chip in a rectangular channel. Figure 10(*a*) shows that the data generally agree with the correlation over the applicable Weber number range. The correlation was slightly better at predicting the subcooled data than the near-saturated data even for velocities outside of the range. Data for chips with a mirror-polished surface from Willingham et al. (1991) are presented in Fig. 10(*b*). For these tests, the chip surface was first sanded with 600 grit sandpaper and then buffed with polishing paste. The correlation was again better at predicting the subcooled data over the near-saturated data. Coupled with the relatively small CHF bandwidth for the multi-chip array, Fig. 7(*a*), good CHF predictability for Chip 1 renders the Mudawar and Maddox correlation an effective tool in designing two-phase cooling systems for multi-chip arrays. This correlation becomes even more accurate with subcooled conditions which are favored in very high flux applications.

Effect of Channel Gap. In addition to the 5-mm channel gap, gaps of 2 and 10 mm were also tested in vertical upflow. There is some pressure drop in the channel associated with the flow over the array of chips. The pressure drop was found to increase with increasing velocity and decreasing channel gap. Highest values of the pressure drop were measured with near-saturated flow corresponding to the largest increase in void fraction in the channel which contributes both to the frictional and accelerational components of the pressure drop. However, the pressure drop was fairly insignificant for all the conditions tested. Table 1 lists pressure drops measured between Chips 1 and 9 for several test conditions. The largest pressure drop was 0.144 bar which was recorded for the 2-mm gap at near-saturated flow and U = 400 cm/s. This pressure drop corresponds to a stream-wise decrease in the saturation temperature of 3.33°C. The relatively small pressure drops in the channel across the multi-chip array indicate that, for design purposes, basing the saturation temperature on the inlet conditions is quite acceptable.

Table 1 Pressure drop (in bar) between Chips 1 and 9 for each channel gap just prior to CHF in vertical upflow for near-saturated and highly-subcooled flow

U (cm/s)	H = 10 mm		H = 5 mm		H = 2 mm	
	ΔT_{sub} (°C)		ΔT_{sub} (°C)		ΔT_{sub} (°C)	
	3	25	3	25	3	25
13	< 0.0068	< 0.0068	< 0.0068	< 0.0068	< 0.0068	< 0.0068
50	< 0.0068	< 0.0068	< 0.0068	< 0.0068	0.010	0.0075
200	0.015	0.010	0.027	0.016	0.065	0.039
400	0.031	0.028	0.059	0.052	0.144	0.129

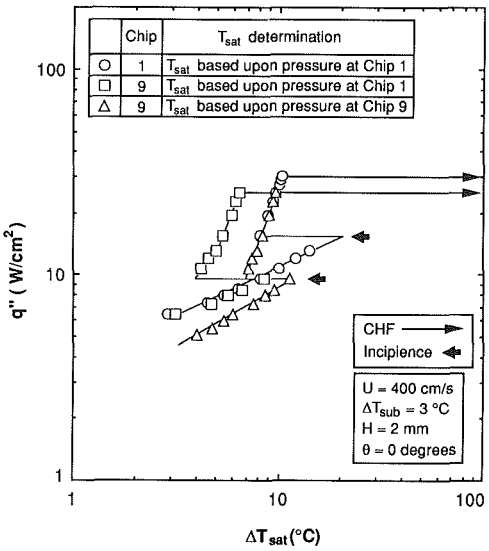

Fig. 11 Effect of pressure drop on boiling curve for 2-mm gap in vertical upflow with near-saturated flow and an inlet velocity of 400 cm/s (adapted from Willingham and Mudawar, 1992b)

The effect of changes in T_{sat} on the boiling curve for this extreme case is illustrated in Fig. 11. Using the saturation temperature corresponding to the pressure at Chip 1, the boiling curve for Chip 9 shows a lower wall superheat, ΔT_{sat}, than for Chip 1. But when the decrease in saturation temperature is accounted by referencing ΔT_{sat} to the measured pressure at Chip 9, the boiling curve of Chip 9 falls directly on the boiling curve of Chip 1 except for the region of incipient boiling.

As stated earlier, the downstream chips were generally the first to reach boiling incipience, and because of their nucleating at smaller heat fluxes, the downstream chips also experienced the smallest drop in surface temperature at incipience. However, with the 2-mm gap, the incipience temperature drops tended to increase as compared to the 10- and 5-mm gaps. Figure 12 illustrates the larger incipience temperature drop on Chip 9 for the 2-mm gap. At near-saturated conditions, the smallest gap also spawned a much larger void fraction in the channel than did the larger gaps. With the 10-mm gap, the bubbles tended to flow directly above the chips in the center of the channel throughout the multi-chip module, but in the

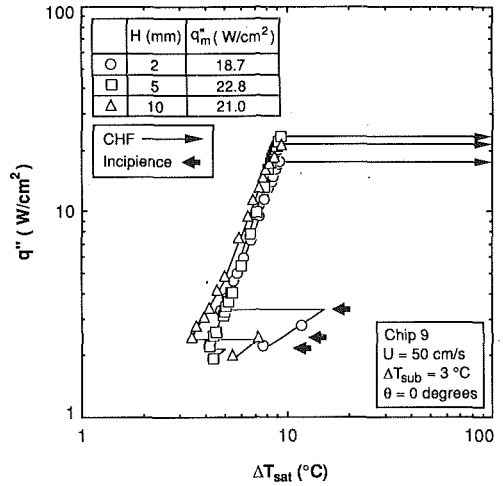

Fig. 12 Boiling curves for Chip 9 for all channel gaps with near-saturated flow, inlet velocity of 50 cm/s, and vertical upflow

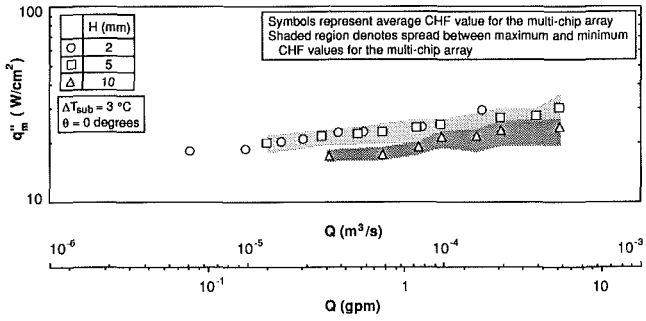

Fig. 13(*a*)

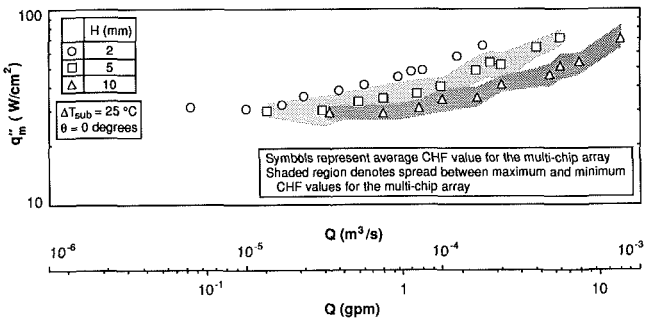

Fig. 13(*b*)

Fig. 13 Variation of critical heat flux in vertical upflow for the three channel gaps with flow rate for an inlet subcooling of (a) 3°C and (b) 25°C

2-mm gap, the bubbles were observed to spread over the entire width of the channel. The result of this excessive void fraction was a premature dryout of the chip surface and, thus, a lowering of CHF for the multi-chip array as shown in Fig. 12. In fact, for a given velocity, the 5-mm gap generally rendered the largest values in CHF for the multi-chip array.

For a given velocity, the entire data base featured CHF values with the 5-mm gap which were greater than for the 2- and 10-mm gaps, suggesting that there is an optimal channel gap associated with forced-convection boiling. Critical heat flux may be lower in the 2-mm gap because of the higher void fraction and a larger stream-wise pressure drop which, in turn, causes a larger decrease in saturation temperature. Also, the smaller flow area of the 2-mm gap results in a smaller mass flow rate for a given velocity. Since the energy dissipated from the chips is being absorbed by less fluid, the bulk liquid temperature will increase more. The decrease in CHF in the 10-mm gap might be explained by considering an idealized, fully-developed liquid velocity profile. The larger flow area would create a lower near-wall velocity, lessening the flow of liquid to the boiling surface and the ability to remove bubbles from the chip surface by shear and drag forces. Also, the 10-mm gap was observed to be less effective at mixing the superheated liquid with, and utilizing the sensible energy of the cooler fluid on the sides of the channel as were the 5- and 2-mm gaps.

Even though velocity is often utilized to correlate CHF in boiling systems, a designer of a two-phase electronic cooling system is more concerned with maintaining a desired flow rate than velocity. Figures 13(*a*) and 13(*b*) illustrate the dependence of CHF on flow rate for $\Delta T_{sub} = 3$ and 25°C, respectively. Intuitively, one would expect that for a given flow rate that the 2-mm gap would have the largest CHF followed by the 5- and 10-mm gaps because of the increased fluid velocity. This was indeed the case for highly subcooled flow as shown in Fig. 13(*b*). Achieving a CHF value of 50 W/cm^2 required a flow rate of 4×10^{-4} m^3/s for the 10-mm gap, and the flow rate was reduced by 55 and 80 percent for the 5- and 2-mm gaps, respectively. However, for near-saturated flow, the 2- and 5-mm gaps rendered approximately the same values of CHF for a given flow rate. As discussed earlier, a large void fraction existed in the 2-mm gap which may have caused a premature dryout on the downstream chips at higher stream-wise velocities than those corresponding to the 5-mm gap. For this reason, designers should exercise care when operating with near-saturated flow.

One measure for the effectiveness, ϵ, of a given channel configuration is the ratio of total power dissipated from all chips in the module to the sum of sensible and latent heat of liquid at the module inlet.

$$\epsilon \equiv \frac{nA_w q''}{(\rho_f U A_x)[h_{fg} + c_{pf}\Delta T_{sub}]} = \frac{q''}{\left[\frac{A_x}{nA_w}\right](\rho_f U h_{fg})\left[1 + \frac{c_{pf}\Delta T_{sub}}{h_{fg}}\right]} \quad (3)$$

where A_x, A_w, and n are, respectively, the cross-sectional area of the flow channel, chip area, and total number of chips in the stream-wise direction (nine in the present study). Clearly, reducing the gap thickness for a given flow velocity reduces A_x and increases the effectiveness of coolant energy utilization.

The maximum values of ϵ were calculated in the present study by setting q'' equal to the measured minimum CHF. For the 5-mm channel, most tests yielded ϵ values below 0.01, which points to the significance of CHF, rather than downstream dryout, in inhibiting the coolant ability to absorb energy from the chips. For the lowest velocity, 13 cm/s, and the largest subcooling, $\Delta T_{sub} = 36$°C, ϵ for the 5-mm channel was 0.11 as compared to 0.054 and 0.27 for the 10-mm and 2-mm channels, respectively. These values illustrate how reducing gap thickness for a given velocity can greatly reduce the coolant flow rate.

The average CHF bandwidths for all vertical upflow experiments were ±12.3 and ±11.8 percent for the 5- and 10-mm channels, respectively. As the channel gap was decreased to 2 mm, the average bandwidth increased to ±15.8 percent (which is still smaller than for the downflow cases discussed earlier for the 5-mm channel). The relatively large bandwidth for the 2-mm channel may be attributed to the large values of void fraction for this small gap. Assuming constant fluid properties based upon the pressure at Chip 1, and homogeneous two-phase flow in the channel, the thermodynamic equilibrium quality and void fraction just downstream of Chip 9 are, respectively,

Table 2 Summary of recommendations

Design Parameter	Concerns	Recommendations
• Pressure, P_i	• Structural integrity of hardware • Spillage of coolant to ambient for pressures exceeding atmospheric • Leakage of air into the system for pressures below atmospheric	• Slightly above atmospheric
• Orientation, θ	• Flow instabilities • Low CHF values • Large CHF bandwidth	• Vertical upflow • If other orientations are imposed by overiding design constraints, $U > 200$ cm/s
For Vertical Upflow		
• Gap width, H	• High void fraction in near-saturated flow • Poor utilization of fluid with a large channel gap • High pressure drop with a small channel gap	• For near-saturated flow use a relatively large gap width • For highly-subcooled flow use a small gap to reduce flow rate
• Velocity, U	• Low CHF at low velocities	• Use the Mudawar and Maddox (1989) CHF correlation to set minimum velocity
• Subcooling, ΔT_{sub}	• Low CHF for near-saturated flow • Subcooled flow increases complexity of cooling system hardware	• Use subcooled flow to reduce void fraction and the coolant flow rate

$$x_e = \frac{nA_w}{A_x}\left(\frac{q''}{U\rho_f h_{fg}}\right) - \frac{c_{pf}\Delta T_{\text{sub}}}{h_{fg}} \tag{4}$$

and

$$\alpha = \left(1 + \frac{\rho_g}{\rho_f}\left[\frac{1-x_e}{x_e}\right]\right)^{-1} \tag{5}$$

where Eq. (5) is defined only in the range $0 \le x_e \le 1$. For near-saturated flow ($\Delta T_{\text{sub}} = 3°\text{C}$) and U = 100 cm/s, Eqs. (4) and (5) predict void fractions based upon a heat flux equal to the minimum CHF in the multi-chip array of 37.6, 55.8, and 73.7 percent for the 10-, 5-, and 2-mm channels, respectively. Clearly, the largest void fraction existed in the 2-mm channels where the flow rate was the lowest for a constant velocity.

These results pose major challenges in designing a two-phase cooling system. While decreasing channel gap thickness can greatly reduce the coolant flow rate required to maintain a given CHF lower limit for the module, this may also promote increases in void fraction, pressure drop, and CHF bandwidth. The packaging engineer should, therefore, consider these factors carefully along with all other system packaging constraints in optimizing the thermal design of the module.

Summary of Design Recommendations. A summary of recommendations important to designing a two-phase cooling system is presented in Table 2. A slightly larger than atmospheric system pressure is recommended to keep air from seeping into the system and affecting cooling performance. Vertical upflow alleviates the instability problems associated with other orientations and flow configurations while yielding the largest CHF values. There is an optimization problem involved with gap width, liquid velocity, and inlet subcooling. For the best overall performance, subcooled flow in a small channel is recommended. Based on the choices for gap width and subcooling, the liquid velocity should be based on the desired CHF value which can be determined from the Mudawar and Maddox (1989) correlation.

Conclusions

Parameters important to the adaptation of two-phase forced-convection in the cooling of high-flux multi-chip modules have been examined. They include flow orientation, flow gap above the chip surface, coolant velocity (and flow rate), and inlet subcooling. The following practical conclusions can be drawn:

(1) Critical heat flux decreased as the channel was rotated from the vertical upflow position. The effect of orientation on CHF was negligible for velocities greater than 200 cm/s. Increases in subcooling slightly dampened the angle effect.

(2) Upflow was found to be the preferred cooling configuration because, unlike downflow and horizontal configurations, it was free of bubble stagnation, counterflow, and other two-phase instabilities. Also, the bandwidth of CHF values in the multi-chip module was smaller for upflow as compared to other orientations.

(3) For all tests, Chips 1 and 2 initiated boiling at higher heat fluxes than the rest of the chips. For this reason, the incipience temperature drop on Chips 1 and 2 were also much larger. It is therefore suggested that a heated patch be placed upstream of the chips in order to lessen the incipience temperature drop on all of the chips.

Because the best orientation was found to be that of vertical upflow (θ = 0 degrees), the hydrodynamic and thermal interaction between the chips and effects of channel gap were investigated for that orientation. Key conclusions from these tests are as follows:

(4) Critical heat flux data for Chip 1 in the 5-mm channel were in good agreement with the Mudawar and Maddox (1989) correlation. Combined with the relatively small bandwidth of CHF values in the multi-chip array, the correlation is recommended for designing two-phase forced-convection cooling systems.

(5) Pressure drop across the array of chips increased with increasing velocity, decreasing subcooling, and decreasing gap thickness. Nevertheless, the pressure drop across the multi-chip array was insignificant. In the absence of an appreciable pressure drop in the channel, the boiling curves were similar for each chip in the multi-chip module with and without adjusting saturation temperature for the stream-wise changes in pressure. These results suggest that, for design purposes, basing the saturation temperature for all chips upon the inlet conditions is quite acceptable.

(6) For a given velocity, the largest CHF values for the 5-mm channel were larger than for the 2-mm and 10-mm channels. The data suggest the existence of an optimum gap thickness which maximizes CHF for a given velocity. A very small gap increased the void fraction in the channel, promoting dryout on the downstream chips. A large gap, on the other hand, resulted in a relatively small void fraction and a concentration of bubbles within the edges of the chips. The suppressed interaction of bubbles with the side wall fluid precluded the utilization of the sensible energy of this fluid compared to a smaller gap resulting in CHF values which were smaller for the 10-mm channel than for the 5-mm channel. Great reductions in flow rate were realized for subcooled flow when aiming for a given CHF design limit. By choosing a small gap, it was possible to increase flow velocity even with a smaller flow rate. However, the detrimental effects of the large void fraction on CHF may make choosing a smaller gap a less attractive measure for reducing flow rate.

Acknowledgments

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