Int. J. Heat Mass Transfer. Vol. 35, No. 11, pp. 2879–2890, 1992
Printed in Great Britain

0017–9310/92 $5.00+0.00
© 1992 Pergamon Press Ltd

Forced-convection boiling and critical heat flux from a linear array of discrete heat sources

T. C. WILLINGHAM and I. MUDAWAR
Boiling and Two-Phase Flow Laboratory, School of Mechanical Engineering, Purdue University, West Lafayette, IN 47907, U.S.A.

(*Received* 10 *April* 1991 *and in final form* 13 *December* 1991)

Abstract—Forced-convection boiling experiments were performed with FC-72, a 3M Fluorinert, at 1.36 bar on a linear array of nine discrete heat sources simulating microelectronic chips, which were flush-mounted in a vertical, rectangular channel. The inlet velocity and liquid subcooling were varied from 13 to 400 cm s^{-1} and 3 to 36°C, respectively. Special design of the experimental apparatus allowed each test to continue until all chips had reached critical heat flux (CHF) without damaging the test section. Boiling incipience and CHF were delayed to higher heat fluxes with increasing velocity and/or subcooling. In general, the position of the last chip to reach CHF moved upstream with increasing subcooling. The average bandwidth of CHF values for the multi-chip array, however, was only $\pm 12.3\%$, proving that the discontinuity in wall heat flux between consecutive chips helped to interrupt the growth of the vapor blanket which commonly results in dryout at the downstream edge of long, continuously heated walls. Also, the small CHF bandwidth allows a correlation previously developed for CHF on an isolated chip to be used for an array of chips as well.

1. INTRODUCTION

THE CONTINUING impetus in the electronics industry is to increase computing power through miniaturization and increased packaging density of microelectronic components in chips, as well as through tighter packaging of multi-chip modules. Corresponding to these aggrandized packaging densities is a steady increase in heat dissipation at the chip, module, and system levels. For example, while heat fluxes for today's state-of-the-art chips range from 5 to 40 W cm^{-2}, it is expected that chips will emerge in the mid-1990s whose heat fluxes will reach the 100 W cm^{-2} level [1, 2]. Traditionally, convection from electronic hardware to the surroundings has been achieved through the natural, forced, or mixed convection of air; however, even with advances in air-cooling techniques, the improvements will not suffice to sustain the expected higher heat fluxes. As an effective and increasingly popular alternative to air cooling, direct immersion cooling features an intimate contact between a liquid coolant and the electronics. Direct immersion applications utilize fluorocarbon liquids because of their chemical and electrical compatibility with the hardware as well as their typically low boiling points, which allow them to be used in pool or forced-convection boiling situations.

The heat flux at which a surface undergoes transition from nucleate boiling to film boiling is termed the critical heat flux (CHF). Since large increases in surface temperature are associated with this transition, CHF is an upper design and operating limit for heat flux in practical electronic cooling applications. Employing flow visualization to understand the mechanism of CHF, Vliet and Leppert [3, 4] investigated forced-convection boiling for both saturated and subcooled conditions while Gaertner [5] studied saturated pool boiling. At heat fluxes just prior to CHF, both described the development of a large coalescent vapor blanket above the heater surface. Bulk liquid had difficulty breaking through this blanket to replenish liquid evaporating in a sublayer between the blanket and the heater surface, spurring transition to film boiling. Mudawar *et al.* [6] observed CHF in falling films and noted that vigorous boiling prior to CHF caused the bulk of the falling film to separate from the heated wall, leaving only a thin liquid sublayer in contact with the wall. Critical heat flux was accompanied by dryout of the sublayer. Mudawar and Maddox [7] described a similar phenomenon for forced-convection CHF in a flow channel for velocities between 22 and 200 cm s^{-1}.

Two important parameters which affect boiling heat transfer with direct immersion applications in a channel are the velocity and subcooling of the fluid. Increases in both parameters are known to increase CHF. Researchers have found varying CHF relationships with velocity and subcooling depending on the geometry of the system [3, 4, 6–9]. Vliet and Leppert found CHF to be proportional to the square root of velocity for saturated flow and directly proportional to velocity for subcooled flow. They also found CHF to vary linearly with the degree of subcooling. Mudawar *et al.* noted that increasing the velocity of a falling film increased CHF according to velocity raised to a power of 0.16.

Recently, Samant and Simon [10] studied heat transfer from a 2.0 mm wide by 0.25 mm long heated patch mounted to one wall of a rectangular channel. Using R-113 and FC-72, a 3M Fluorinert, they

NOMENCLATURE

c_p	specific heat at constant pressure
D	hydraulic diameter of flow channel (8 mm)
g	acceleration due to gravity
h_{fg}	latent heat of vaporization
k	thermal conductivity
L	chip length in flow direction (10 mm)
q''	wall heat flux
q''_m	critical heat flux
q_m^{**}	nondimensional critical heat flux defined in equation (1)
T	temperature
ΔT_{inc}	incipience temperature drop
ΔT_{sat}	wall superheat, $T_w - T_{sat}$
ΔT_{sub}	degree of liquid subcooling, $T_{sat} - T_{f,c1}$
ΔT_w	temperature gradient between chip and liquid, $T_w - T_{f,c1}$
U	mean fluid velocity
We	Weber number, $(\rho_f U^2 L)/\sigma$.

Greek symbols

ρ	density
σ	surface tension.

Subscripts

c1	Chip 1
f	liquid
g	vapor
inc	incipience
m	maximum (critical heat flux)
sat	saturated
sub	subcooled
w	mean chip surface condition.

observed increasing subcooling to extend the nucleate boiling region and postpone the occurrence of CHF. Subcooling increased the collapse rate of bubbles in the flow, thus retarding the development of the vapor blanket. Furthermore, the effect of subcooling was found to be more pronounced at higher velocities.

Mudawar and Maddox [7] examined the effects of velocity and subcooling on CHF from an isolated, 12.7 × 12.7 mm heat source flush-mounted in the wall of a vertical, rectangular channel. Using FC-72, they observed that increasing the velocity from 22 to 410 cm s^{-1} considerably reduced the bubble size as well as the bubble boundary layer thickness, giving more opportunity for the liquid to break through the vapor blanket that hovered above the heater surface. Due to the short length of the isolated heat source employed in their study, boiling on the heat source inside the channel was similar to boiling on a surface with an external flow. Subcooling was varied from 0 to 44°C and was also found to foster a thinning of the bubble boundary layer. They constructed a semi-empirical CHF model which accounted for the effects of velocity and subcooling according to the following expression:

$$q_m^{**} = \left(\frac{q''_m}{\rho_g U h_{fg}}\right) \bigg/ \left(\left(\frac{\rho_f}{\rho_g}\right)^{15/23}\left(\frac{L}{D}\right)^{1/23}\left(1+\frac{c_{pf}\Delta T_{sub}}{h_{fg}}\right)^{7/23}\left(1+0.021\frac{\rho_f}{\rho_g}\frac{c_{pf}\Delta T_{sub}}{h_{fg}}\right)^{16/23}\right) = 0.161\,(We)^{-8/23}. \quad (1)$$

Equation (1) was successful in correlating CHF data for flush-mounted heaters from several studies [11–13]; Mudawar and Maddox themselves proved the correlation works with Umaya's data.

Strom *et al.* [11] investigated the effects of velocity and subcooling on CHF for a linear array of ten 6.4 mm × 6.4 mm heat-dissipating elements in a vertical, rectangular channel using R-113 as a coolant. Rather than employing discrete heat sources, their experimental apparatus featured a rectangular copper slab that was machined on one end to form ten evenly-spaced 'fingers'. These fingers protruded to the channel wall to form the individual heat-dissipating elements. Because of this interconnection of the heaters, the experiments had to be terminated after CHF was reached for any element, thus precluding an analysis of the order of procession to CHF for the remaining heaters as well as a measure of the band-width of CHF values for all ten elements. The velocity and subcooling ranges for their experiments were 9.6–103.9 cm s^{-1} and 20–40°C, respectively. The most downstream heater was virtually always the first to undergo a transition to film boiling, and this was attributed to a stream-wise decrease in local subcooling. Increasing the velocity and/or subcooling significantly extended the nucleate boiling range of the boiling curve for the most downstream element, hence increasing CHF. Their CHF data for flush-mounted elements were in good agreement with the CHF correlation of Mudawar and Maddox for Weber numbers between 100 and 1000 when the local subcooling of the most downstream heater was employed.

In this paper, forced-convection boiling data taken with FC-72 in a vertical, rectangular channel are reported. A linear array of nine simulated micro-electronic chips was flush-mounted along one side of the channel, and experiments were performed at 1.36 bar for velocity and subcooling ranges of 13–400 cm s^{-1} and 3–36°C, respectively; properties of the test fluid at these conditions are given in Table 1. The chips were independently powered and electronically protected with power shut-off relays, allowing the

Table 1. Thermophysical properties of FC-72 at 1.36 bar

$\Delta T_{sub,cl}$ (°C)	$T_{f,cl}$ (°C)	c_{pf}† $\times 10^{-3}$	h_{fg}‡ $\times 10^{-4}$	k_f† $\times 10^2$	ρ_f† $\times 10^{-3}$	ρ_g‡ $\times 10^{-1}$	σ‡ $\times 10^3$
0	66.18	1.112	8.168	5.272	1.599	1.804	8.644
3	63.18	1.107	8.168	5.305	1.605	1.804	8.644
14	52.18	1.090	8.168	5.426	1.627	1.804	8.644
25	41.18	1.073	8.168	5.547	1.649	1.804	8.644
36	30.18	1.056	8.168	5.668	1.670	1.804	8.644

† Based upon $T_{f,cl}$.
‡ Based upon $T_{sat,cl}$.

tests to be continued until each chip had reached CHF without any danger of damaging either the chips or channel hardware. The primary objectives of this study were: (i) to examine the effects of velocity and subcooling on boiling heat transfer and CHF from an array of chips and (ii) to analyze the effects upstream chips have on the boiling performances of the downstream chips. The authors also desired to see if boiling at high heat fluxes on the most upstream chip in the array induces premature dryout on the surfaces of downstream chips.

2. EXPERIMENTAL METHODS

Experimental facility

The flow loop used for this analysis is shown in Fig. 1. A magnetically-coupled centrifugal pump was used to circulate the liquid through the flow loop. A heat exchanger was located immediately downstream of the pump to extract energy that was dissipated by the chips and produced by pipe friction. The liquid flow then bifurcated, allowing some of the coolant to enter the test section while the remainder was routed through the bypass line. Prior to entering the test section, the liquid passed through a 5-μm filter, a turbine flow meter, and another heat exchanger which brought the liquid to the desired temperature at the inlet to the multi-chip module. Two turbine flow meters were used: one for velocities below 100 cm s^{-1} and another for the higher velocities; only one flow meter is shown in Fig. 1. Both the test section and the bypass lines fed coolant into the condenser/reservoir. Pressure in the system was maintained by regulating the energy input of the immersion heater in the pressurization/expansion tank. Fine tuning of the pressure was also accomplished by regulating the flow of cold water into the condenser/reservoir by means of a solenoid valve operated by the data acquisition software.

The test section featured a rectangular flow channel with cross-sectional dimensions of 20.0 mm (width of wall along which the chips were mounted) × 5.0 mm. The first chip was located 0.508 m downstream of the channel inlet. The surfaces of the chips were mounted flush with the channel wall in a G-7 fiberglass substrate module, and the distance between consecutive chips was 10.0 mm as shown in Fig. 2. The chips were positioned in the center of the channel wall with a spacing of 5.0 mm between the edges of the chip and the channel side walls. The chip/substrate interface was sealed with RTV silicone to prevent the formation of artificial nucleation sites.

Simulated microelectronic chip

Figure 3 details the construction and dimensions of the simulated microelectronic chip. Each chip was fabricated from oxygen-free copper such that the cross-sectional dimensions of the chip surface in contact with the liquid were 10.0 mm × 10.0 mm. Three chromel–alumel thermocouples were embedded along the chip centerline in the flow direction at a depth of 0.813 mm underneath the chip surface. One thermocouple was positioned in the center of the chip, and the other two were located 4.29 mm upstream and downstream of the middle thermocouple. Thick-film resistive heaters with an electrical resistance of approximately 90 Ω were fabricated to match the 10.0 mm × 10.0 mm surface area. Each resistor was soldered to the underside of the chip as shown in Fig. 3. The chips were electrically configured in parallel such that the voltage across each chip was equivalent, while the current through each chip varied according to the actual ohmage of the thick-film resistor. Prior to operation, a variable resistor in-line with each individual chip was trimmed such that the power dissipation in each resistive heater was the same. One voltage and nine current transducers were used to measure the power dissipated by the thick-film resistor of each chip.

A two-dimensional numerical analysis was performed to determine the percentage of the energy dissipated by the thick-film resistor that was lost to the surroundings and not conducted to the fluid/chip interface. An upper limit for heat loss was determined by accounting for the additional surface area on the actual chip and by assuming negligible contact resistances between the copper block and fiberglass insulation. The largest heat loss for the conditions of the present study was calculated to be 3%. Therefore, in the light of the small heat losses, no correction was made for the power dissipated by the thick-film resistor in determining the chip heat flux. During the experiment, the thermocouple temperatures were corrected by a one-dimensional heat conduction model to calculate the true chip surface temperature.

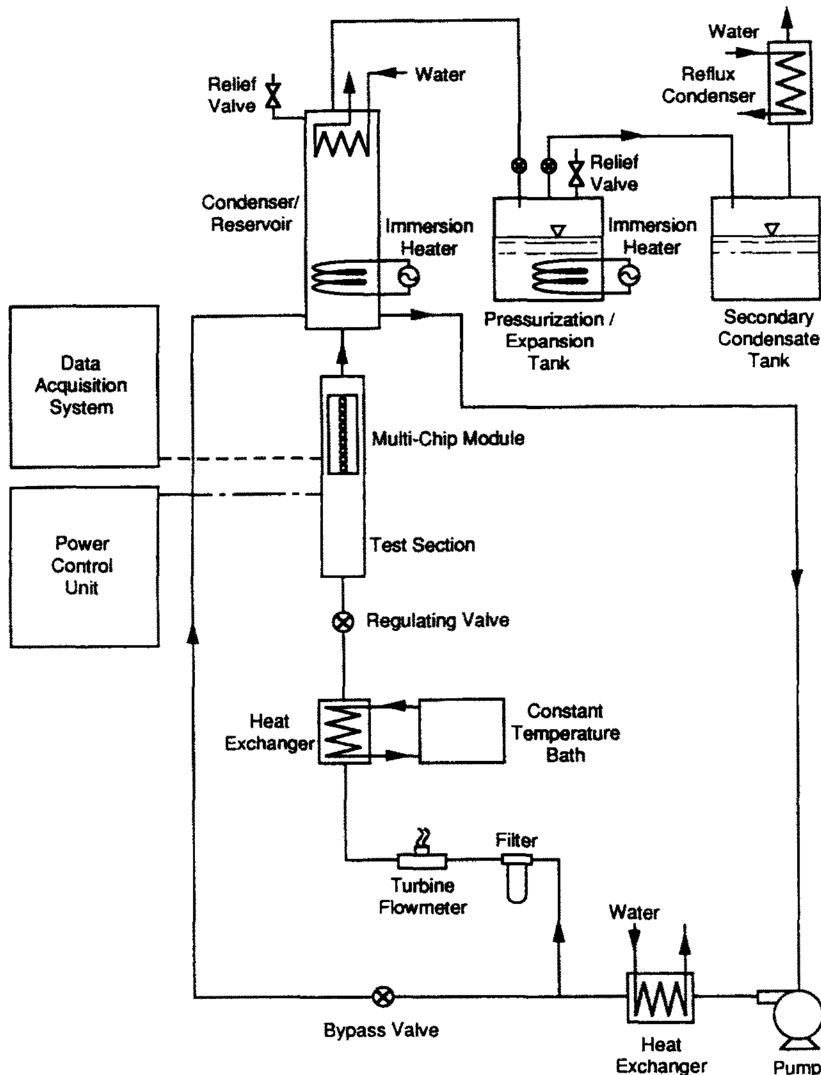


FIG. 1. Experimental flow loop.

Operating procedure

Prior to a series of experiments, the surfaces of the chips were vapor-blasted in order to create a relatively uniform locus of micro-cavities on the surfaces of all chips. The vapor-blasted surfaces were achieved by cleaning them with a vapor blast of fine silica particulates entrained in water flow, where the average size of the particulates was 10 μm. The authors have also performed experiments with mirror-polished surfaces using the same experimental facility [14]. However, these preliminary experiments revealed that regardless of the degree of polish, some residual amount of cavities could still be found on the surfaces of all chips. While uniformity of surface finish was found to be a problem with the mirror-polished surfaces, vapor blasting provided uniform surface texture for all chips.

Periodically throughout the data collection, repeatability was tested by performing benchmark cases as well as reproducing previous results. Every day that the system was operated, the coolant was deaerated by heating the system to saturation and allowing vapor and air to escape into a condensate tank, as shown in Fig.1. From the condensate tank, the vapor and air entered a reflux condenser where the air escaped to the atmosphere and the vapor condensed and returned to the condensate tank. After the deaeration process was complete, the valve to the condensate tank was closed.

Experimental data were collected by a Keithley 500 series data acquisiton system, which was controlled by a Compaq 286 computer. The collected measurements included three temperatures for each of the nine chips, fluid temperature at Chip 1, absolute pressure just upstream of Chip 1, differential pressure from just upstream of Chip 1 to just downstream of Chip 9, frequency of the flow meter, and the power dissipated by the thick-film resistor of each chip. The pressure

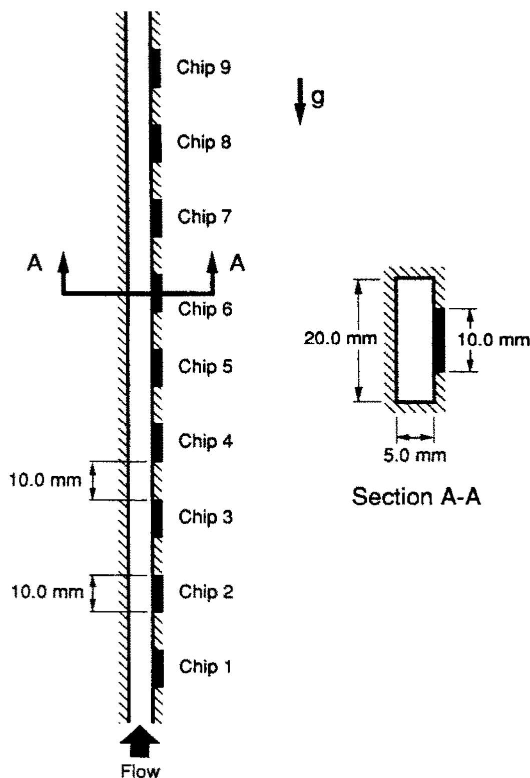


FIG. 2. Multi-chip array.

at Chip 1 was taken to be the reference saturation pressure of the liquid, while the fluid temperature at Chip 1 was used in conjunction with this pressure to determine the degree of subcooling of the liquid. A data point was taken after steady-state was achieved in all measurements; steady-state was assumed when 20 data samples taken over a 20-s period for each of the chip temperatures had a standard deviation of less than 0.10°C.

Experimental error

The maximum error associated with each thermocouple reading was estimated to be less than 0.2°C. Watt and voltage meters with known error bounds were used in the calibration of the current and voltage transducers. The error in measuring the power dissipated by the thick-film resistors was calculated to be a maximum of 0.5%. Calibration accuracies associated with the turbine flow meters for small and large flow velocities were both $\pm 0.05\%$; repeatability for the small and large flow velocities were estimated by the manufacturer to be $\pm 0.1\%$ and $\pm 0.05\%$, respectively. The error associated with the pressure transducer readings was estimated by the manufacturer to be ± 0.0103 bar. Overall errors in the measured inlet subcooling and critical heat flux were less than 0.4°C and 3.26 W cm^{-2}, respectively.

3. RESULTS AND DISCUSSION

Forced-convection boiling experiments were performed with FC-72 at 1.36 bar. Data collected for the array of nine simulated microelectronic chips featured inlet velocities and subcoolings ranging from 13 to 400 cm s^{-1} and 3 to 36°C, respectively. The maximum pressure drop between the most upstream and downstream chips corresponded with the largest flow velocity and was experimentally measured to be 0.0544 bar. This decrease in pressure across the multi-chip array amounted to a stream-wise decrease of 1.3°C in the saturation temperature. Below velocities of 100 cm s^{-1}, the pressure drop was less than 0.00680 bar (which corresponded to less than 0.16°C decrease in saturation temperature). Boiling characteristics of the individual chips as well as the overall performance of the multi-chip array are discussed in this section.

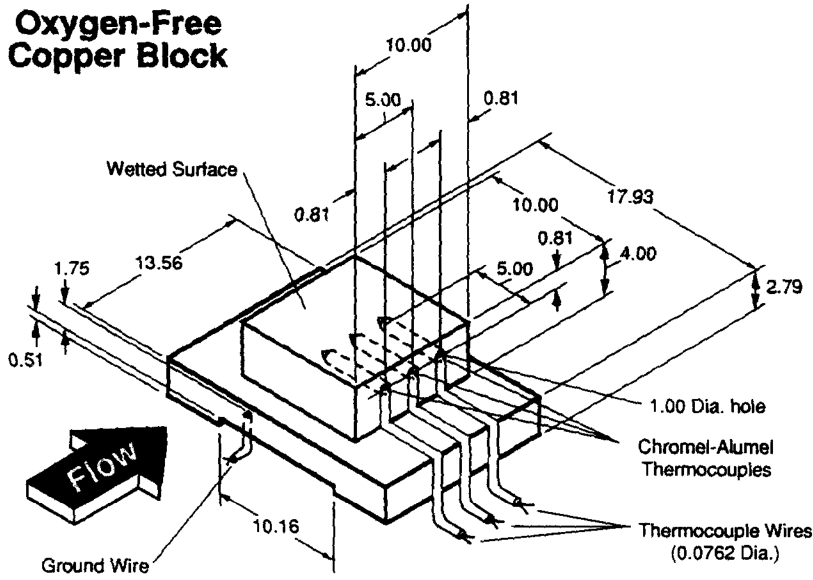
Boiling trends due to interaction between the chips

The boiling curves for Chips 1, 4, and 9 are compared in Fig. 4 for near-saturated flow at an inlet velocity of 50 cm s^{-1}. These curves are representative of the fact that, throughout the study, Chip 9 was generally the first to reach boiling incipience, followed by upstream chips in a fairly monotonic succession. This upstream procession of incipience can be explained by understanding the effects of the thermal boundary layer that develops as the fluid passes over the array of heated chips. The boundary layer causes a stream-wise increase in the fluid temperature paralleled by a slight stream-wise increase in the surface temperature of the chips. This, in turn, leads to a stream-wise decrease in the thermal gradient between the chip surface and the fluid. For a similar distribution of surface cavities on all chips, this decrease in thermal gradient makes conditions more favorable for nucleation on the surfaces of downstream chips.

Figure 4 also reveals that as nucleation was delayed to increasingly higher heat fluxes for upstream chips, these chips also experienced increasingly larger temperature drops associated with incipience. This can be explained by examining the difference in slope between the nucleate boiling curve and the single-phase line. Because of the exceptionally high heat transfer coefficient of nucleate boiling, the slope of the nucleate boiling curve is much greater than that of the single-phase line. Therefore, as the heat flux is increased, the temperature difference between the nucleate boiling curve and the single-phase line also increases, causing chips that experience delayed incipience to require larger drops in temperature to reach the nucleate boiling curve.

Although the CHF value for Chip 1 exceeded that of Chip 4 and Chip 9, Chip 1 was not the last chip to reach CHF; furthermore Chip 9 was not the first to reach CHF. The low and high values of CHF for the multi-chip array were 20.0 and 26.0 W cm^{-2}, respectively. Nevertheless, some general tendencies were observed for the order in which the chips proceeded to CHF. These generalities, as well as CHF data, will be discussed in a later section.

Occasionally, some unusual boiling activity was observed on Chip 1. In a handful of experiments,



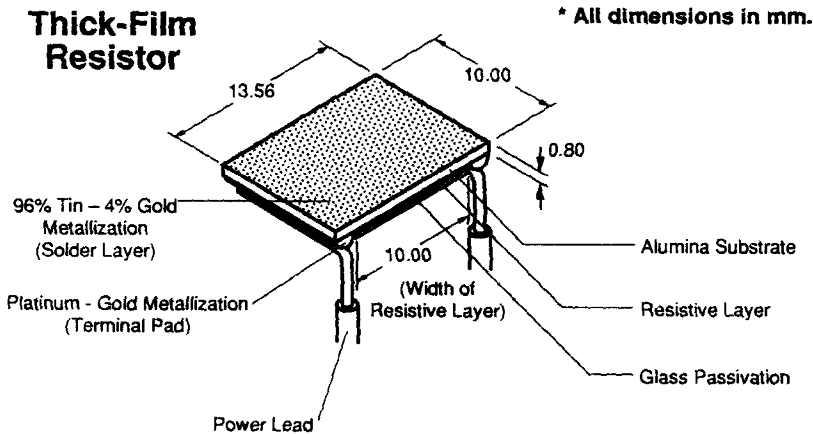


FIG. 3. Construction of the simulated microelectronic chip.

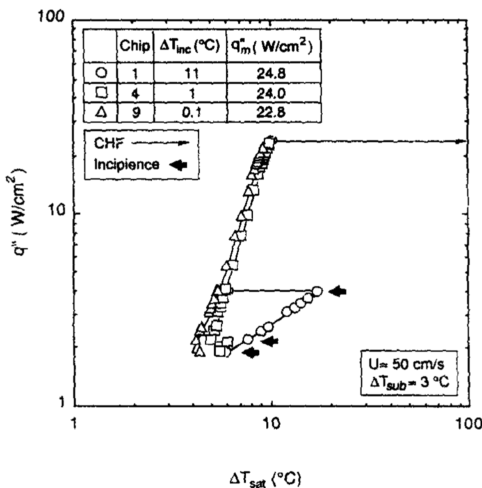


FIG. 4. Boiling curves for Chips 1, 4, and 9 for near-saturated flow at an inlet velocity of 50 cm s^{-1}.

incipience for Chip 1 was delayed to heat fluxes as large as one-third the value of CHF. In several other experiments, the surface of Chip 1 did not completely nucleate until just prior to CHF. This phenomenon occurred primarily at near-saturated conditions and produced a few quasi-incipience points as larger fractions of the surface collectively nucleated. Figure 5 illustrates this gradual propagation of the nucleation front for a near-saturated experiment at 400 cm s^{-1}. Because this unconventional boiling activity was limited in occurrence to Chip 1, the authors believe that electronic cooling applications would benefit from the positioning of a heated patch upstream of the array of electronic chips. It is believed that such a heated patch would provide more uniform and predictable boiling activity on the surfaces of downstream chips.

Velocity effect

Boiling curves for Chips 1, 4, and 9 are shown in Figs. 6(a), (b), and (c), respectively, for near-saturated

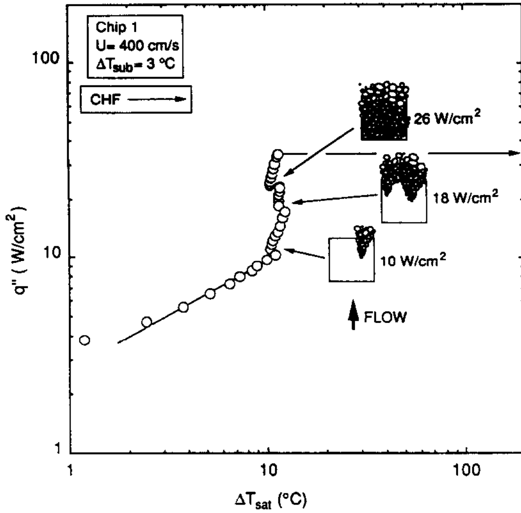
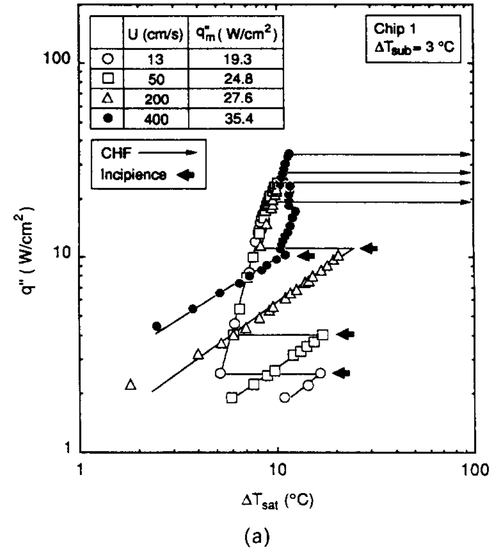


FIG. 5. Gradual propagation of nucleation front occasionally observed for Chip 1.

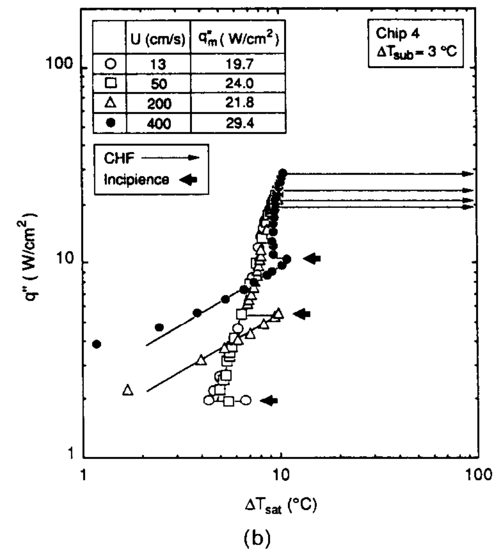
flow at various inlet velocities. These figures illustrate that the effects of velocity on boiling were consistent for all chips in the array, with the exception that downstream chips (Chips 4 and 9) experienced smaller incipience heat fluxes and temperature drops than upstream chips (Chip 1). The convection coefficient for single-phase heat transfer increased with increasing velocity, as evidenced by the upward shift of the single-phase data. Also, incipience was delayed to higher heat fluxes with increases in velocity. Nucleate boiling data for all velocities fell along the same curve, indicating that velocity had little effect on the chip surface temperature in boiling. Finally, CHF increased with velocity for all chips. These trends were also observed for subcooling experiments.

Subcooling effect

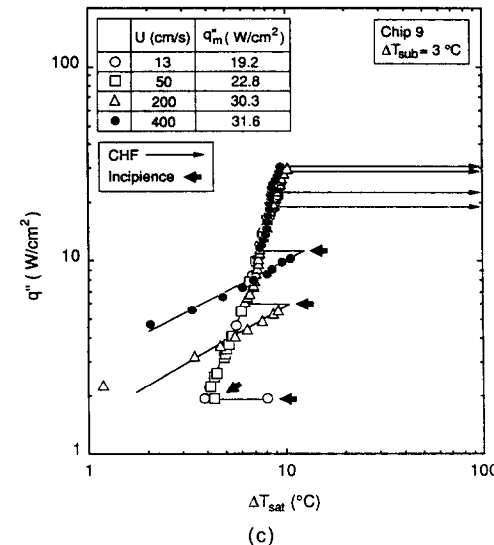
Boiling curves for Chip 1 are shown in Fig. 7 for various subcoolings at an inlet velocity of 50 cm s^{-1}. The corresponding figures for downstream chips are extremely similar, with the exception of the lower heat fluxes and smaller temperature drops at incipience. For large degrees of subcooling, some of the single-phase data at low heat fluxes cannot be displayed because of the negative values of wall superheat (ΔT_{sat}); therefore, it is more desirable to present the boiling data as plotted with respect to the temperature gradient between the chip surface and the liquid (ΔT_w) instead of the wall superheat. For a given heat flux in the single-phase region, the chip surface temperature increased slightly with increasing subcooling. This was spawned by a small decrease in the single-phase convection coefficient due to a change in fluid properties with decreasing fluid temperature. Increasing the subcooling delayed both incipience and CHF to higher heat fluxes, as did increasing the velocity. These trends were also observed at higher inlet velocities.



(a)



(b)



(c)

FIG. 6. Velocity effect on boiling curve at near-saturated conditions for Chip 1 (a), Chip 4 (b), and Chip 9 (c).

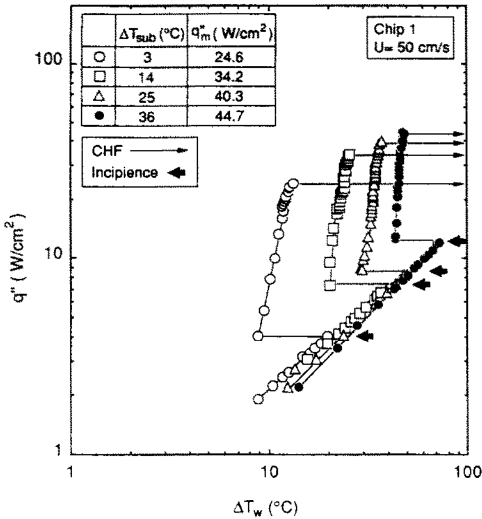


FIG. 7. Subcooling effect on boiling curve for Chip 1 at an inlet velocity of 50 cm s^{-1}.

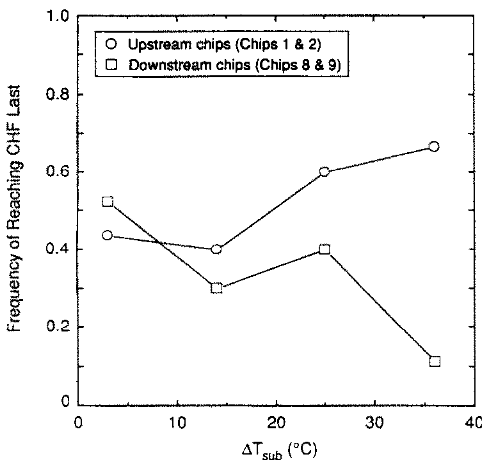


FIG. 8. Frequency of reaching CHF last for upstream and downstream chips.

Critical heat flux

As CHF was approached in the experiments, the increments in heat flux were made smaller, of the order of 0.5 W cm^{-2}. Once CHF was reached on a particular chip, the electrical power to the thick-film resistor of that chip was terminated, and data collection continued until CHF was attained on all nine chips. This facet of the experimental procedure allowed for an analysis of the order of procession to CHF for all of the chips in the array. For the purpose of comparing the behavior of upstream chips with that of downstream chips, Fig. 8 displays the frequency of upstream chips (Chips 1 and 2) and downstream chips (Chips 8 and 9) to be the last to reach CHF. For most of the subcooled experiments, either Chip 1 or Chip 2 was the last chip to reach CHF. As the degree of liquid subcooling was decreased toward saturation, however, downstream chips began to reach CHF last in a larger percentage of the experiments. From 36°C subcooling to near-saturated conditions, the frequency of upstream chips to reach CHF last decreased from 67 to 44%; for the same decrease in subcooling, the frequency of downstream chips to reach CHF last climbed from 11 to 52%. These results indicate that subcooling was, to some degree, influential in determining the location of the last chip to attain CHF. It should be emphasized that cutting off power to a chip upstream of chips which had not yet reached CHF could have had some effect on the occurrence of CHF on the downstream chips, especially at conditions near saturation.

As previously mentioned, the thermal boundary layer that develops as the fluid passes over the array of heated chips causes a stream-wise increase in the fluid temperature. This effect alone would tend to produce a premature occurrence of CHF on downstream chips; however, there is also an effect on CHF from bubbles emanating from upstream chips. At near-saturated conditions, by the time the flow reached Chip 9 it was well-crowded with a substantial bubble population. As the liquid subcooling increased, both the size of individual bubbles and the number of bubbles visible in the flow were considerably reduced due to condensation in the cooler bulk liquid. It is suggested that at near-saturated and low-subcooling conditions, the bubbles emanating from upstream chips serve to increase fluid contact with the chip surface for downstream chips, thus helping to counterbalance the stream-wise decrease in CHF due to the thermal boundary layer. The increasing void ratio also promotes a stream-wise fluid acceleration which, to a lesser extent, further serves to offset the stream-wise decrease in CHF due to the thermal boundary layer. This process is shown in Fig. 9(a). It should be noted that this compensating effect of the bubbles would eventually diminish if a much larger number of chips were lined up in series since a large increase in void ratio would bring about eventual dryout of the wall. For the more subcooled experiments, there was very little interaction between bubble boundary layers formed on adjacent chips and a negligible stream-wise increase in velocity due to phase change; consequently, CHF became sensitive to the stream-wise decrease in local subcooling for downstream chips, as shown in Fig. 9(b). Evidence of this sensitivity with increasing subcooling is displayed in the form of an upstream movement of the position of the last chip to reach CHF.

It was stated earlier that the experimental heater configuration of Strom *et al.* [11] was one of heated 'fingers' rather than discrete heat sources, and this required them to cease an experiment when CHF was reached by any one of the 'fingers'. For the majority of their experiments, which featured inlet subcoolings of 20–40°C, the last heater in the array attained CHF first. For the 25 and 36°C subcooling data of the current study, CHF did not necessarily first occur on Chip 9, but downstream chips were predominantly

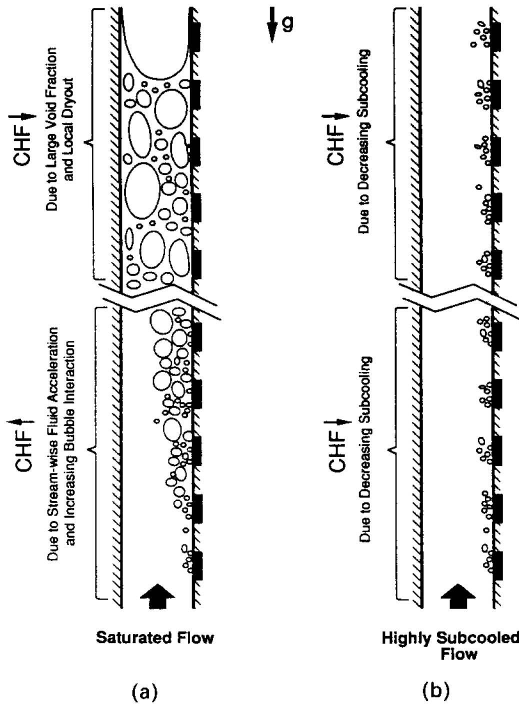


FIG. 9. Multi-chip CHF trends for saturated (a) and highly subcooled (b) flow.

the first to reach CHF. Because their heaters were 46% smaller in width and length than the chips of the current study, the thermal boundary layer which developed in their channel would be thinner in both width and height than that of the current study. By dissipating roughly the same quantity of energy into a smaller boundary layer, a greater stream-wise temperature increase in their R-113 thermal boundary layer occurred. In addition, the smaller density of R-113 and the smaller cross-sectional area of their channel would imply a smaller mass flow rate which, combined with the smaller specific heat of R-113, would also cause a larger decrease in local subcooling for downstream chips. For these reasons, it is expected that Strom *et al.* would be more likely to observe the last heater in the array to consistently reach CHF first.

Critical heat flux data for Chips 1, 4, and 9 are shown in Figs. 10(a), (b), and (c), respectively. All chips in the multi-chip array exhibited the same behavior with increases in velocity and/or subcooling as increases in either parameter served to increase CHF. Furthermore, increases in subcooling had a more significant effect on CHF at larger velocities. In fact, there appears to be a transition from a low- to high-velocity CHF regime similar to that observed by Mudawar and Maddox [7] for an isolated chip. They proposed that the difference between these two phenomena was due to the physical mechanisms which promote CHF. According to Mudawar and Maddox, low-velocity CHF is characterized by dryout of a liquid sublayer beneath a continuous vapor blanket, whereas high-velocity CHF features the dryout of intermittent liquid films beneath small vapor blankets

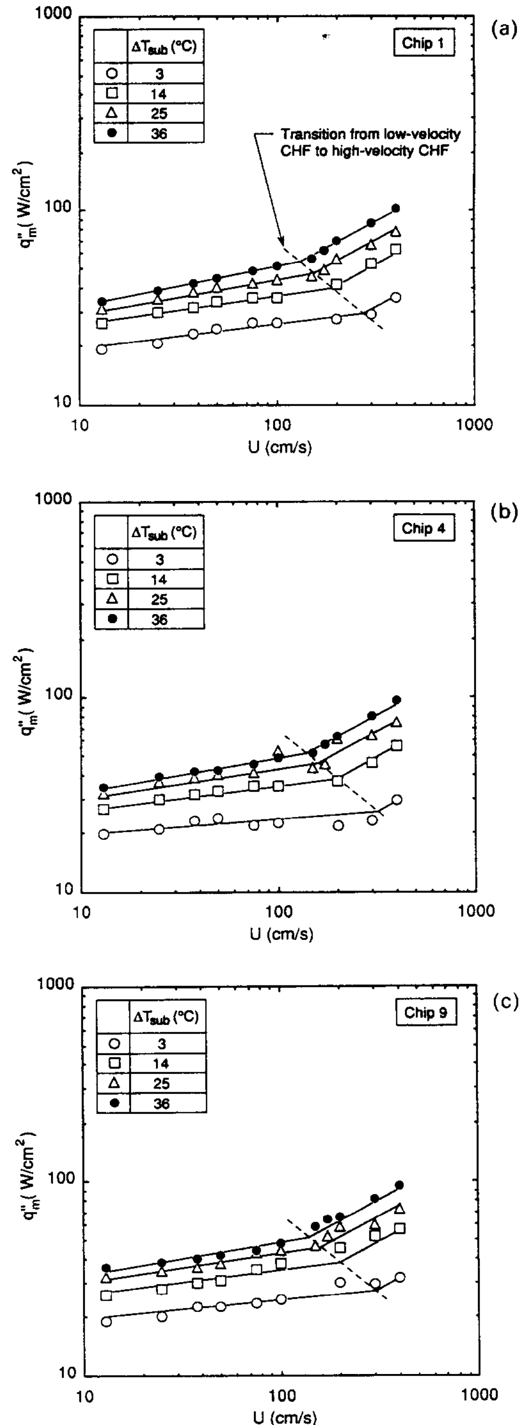


FIG. 10. Critical heat flux values for Chip 1 (a), Chip 4 (b), and Chip 9 (c).

randomly distributed on the chip surface. The largest value of CHF obtained for the multi-chip array was 102.3 W cm^{-2}, which occurred on Chip 1 for 400 cm s^{-1} and 36°C subcooling.

A CHF bandwidth was calculated for each experiment in order to quantify the difference between the high and low values of CHF for the multi-chip array.

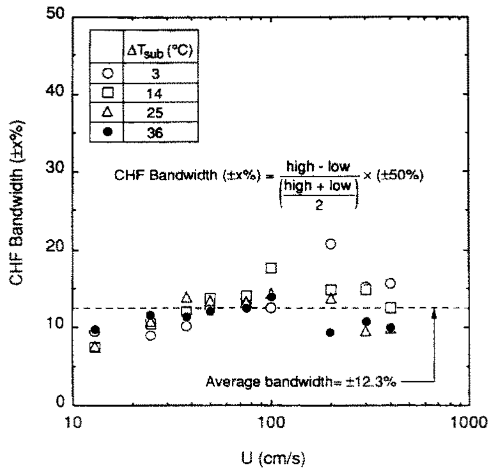


FIG. 11. Bandwidth of CHF values.

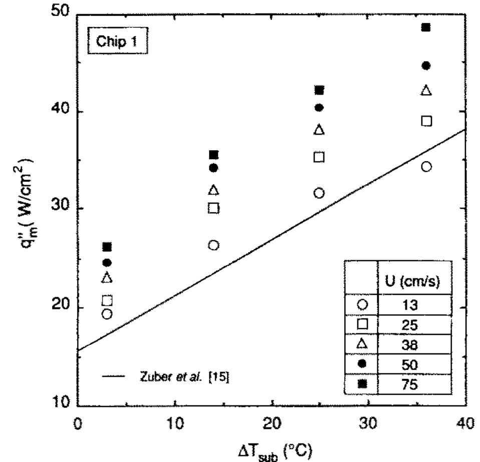


FIG. 12. Comparison of low-velocity CHF data for Chip 1 with the pool boiling limit as predicted by Zuber *et al.* [15].

Figure 11 shows that the average bandwidth of CHF values for all experiments was $\pm 12.3\%$. Although the trend of CHF bandwidth with velocity is small, there appears to be some connection between this trend and the CHF regimes observed at low and high velocities. This small bandwidth proves that the discontinuity in wall heat flux between consecutive chips helped interrupt the growth of the vapor blanket, which commonly results in dryout at the downstream edge of long, continuously heated walls.

As the velocity of the liquid decreases to zero, the predicted pool-boiling CHF of Zuber *et al.* [15] should present a lower bound for CHF:

$$\frac{q''_{m,sub}}{q''_{m,sat}} = 1+5.3\frac{\sqrt{(k_f \rho_f c_{pf})}}{\rho_g h_{fg}}\left(\frac{g\sigma(\rho_f-\rho_g)}{\rho_g^2}\right)^{1/8} \times \left(\frac{g(\rho_f-\rho_g)}{\sigma}\right)^{1/4}\Delta T_{sub} \quad (2a)$$

where

$$q''_{m,sat} = 0.131\rho_g h_{fg}\left(\frac{\rho_f+\rho_g}{\rho_f}\right)^{1/2}\left(\frac{g\sigma(\rho_f-\rho_g)}{\rho_g^2}\right)^{1/4}. \quad (2b)$$

Yet, this lower bound is somewhat nebulous for the vertical channel situation of the present study. In pool boiling, there generally exists a large reservoir surrounding the heated surface; in the present study, however, the volume of fluid that surrounded a single chip was limited by the small dimensions of the channel and affected by the heat transfer and ebullition from other chips.

Figure 12 compares the CHF data for Chip 1 with the Zuber limit for velocities between 13 and 75 cm s^{-1}. At the smallest inlet velocity (13 cm s^{-1}), CHF values for Chip 1 exceeded the Zuber limit in all experiments except one. For the lowest value of CHF in the multi-chip array, the Zuber limit was exceeded at near-saturated conditions only, and the overprediction of CHF by the pool boiling limit grew with increasing

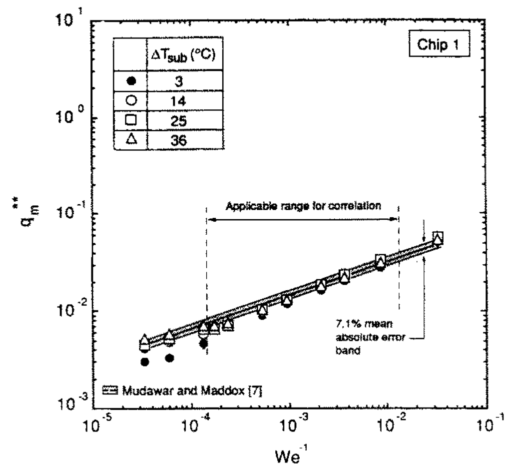


FIG. 13. Comparison of nondimensional CHF data for Chip 1 with the correlation of Mudawar and Maddox [7].

subcooling. It appears that the large bubbles present in near-saturated flow were effective in offsetting the tendency of the thermal boundary layer to decrease CHF. Nevertheless, as these bubbles decreased in size and number with increasing subcooling, the thermal boundary layer engendered premature CHF values that were lower than those that would be obtained for an isolated chip in a pool boiling situation. These results indicate that low velocities are relatively ineffective since a pool boiling situation would render virtually the same values of CHF.

In theory, Chip 1 should behave as a thermally and hydrodynamically isolated chip since there are no chips upstream of it to affect its heat transfer. For this reason, the nondimensional CHF values for Chip 1 are compared in Fig. 13 with the Mudawar and Maddox correlation, equation (1), for forced-convection boiling on an isolated chip. Mudawar and Maddox correlated their data with a mean absolute error of

7.1% for velocities above 22 cm s^{-1} and less than approximately 200 cm s^{-1}. Figure 13 shows that the majority of CHF data for Chip 1 agreed well with the correlation. The maximum deviation of the subcooled data from the correlation was 15.9%. From a practical standpoint, both the good agreement of the correlation with Chip 1 and the small bandwidth of CHF ($\pm 12.3\%$) make the Mudawar and Maddox correlation attractive for electronic cooling design purposes in determining CHF values for any array of chips.

4. CONCLUSIONS

An experimental investigation of heat transfer from a linear array of simulated microelectronic chips in forced-convection boiling was conducted. The following conclusions can be drawn:

(1) For all experiments, Chip 9 was generally the first to reach boiling incipience, followed by upstream chips in a fairly monotonic succession. Upstream chips also experienced larger drops in surface temperature at incipience.

(2) Boiling incipience and CHF for all chips were delayed to higher heat fluxes with increasing velocity and/or subcooling.

(3) Because of some unusual boiling activity on Chip 1, the authors believe that electronic cooling applications would benefit from the positioning of a heated patch upstream of the array of electronic chips in order to provide more uniform and predictable boiling on the surfaces of downstream chips.

(4) The thermal boundary layer that develops as the fluid passes over the array of heated chips tends to promote a slight stream-wise decrease in CHF; however, at near-saturated and low-subcooling conditions the bubbles emanating from upstream chips helped to counterbalance this stream-wise decrease in CHF. In other words, the position of the last chip to reach CHF moved upstream with increasing subcooling.

(5) Comparison of CHF data with the Zuber *et al.* [15] correlation for pool boiling indicates that low velocities are relatively ineffective in forced-convection boiling applications since pool boiling renders virtually the same values of CHF.

(6) A CHF bandwidth was calculated for each experiment in order to quantify the difference between the high and low values of CHF for the multi-chip array; the average bandwidth of CHF values for all experiments was $\pm 12.3\%$.

(7) Critical heat flux data for Chip 1 agreed well with the Mudawar and Maddox [7] correlation for an isolated chip in a flow channel. This fact, coupled with the small bandwidth of CHF for all experiments, makes the correlation attractive for electronic cooling design purposes in determining CHF values for an array of chips.

Acknowledgements—Support of this work by a grant from the Industrial Chemical Products Division of 3M is gratefully acknowledged. The authors also thank Mr James Githens and Mr Douglas Maddox of 3M for their technical assistance.

REFERENCES

1. A. Bar-Cohen, Thermal management of air- and liquid-cooled multichip modules, *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. CHMT-10: 2, pp. 159–175 (1987).
2. R. E. Simons, Direct immersion cooling: past, present, and future, IBM Technical Report, TR 00.3465, Poughkeepsie, New York (1987).
3. G. C. Vliet and G. Leppert, Critical heat flux for nearly saturated water flowing normal to a cylinder, *J. Heat Transfer* **86,** 59–67 (1964).
4. G. C. Vliet and G. Leppert, Critical heat flux for subcooled water flowing normal to a cylinder, *J. Heat Transfer* **86,** 68–74 (1964).
5. R. F. Gaertner, Photographic study of nucleate pool boiling on a horizontal surface, *J. Heat Transfer* **87,** 17–27 (1965).
6. I. Mudawar, T. A. Incropera and F. P. Incropera, Boiling heat transfer and critical heat flux in liquid films falling on vertically-mounted heat sources, *Int. J. Heat Mass Transfer* **30,** 2083–2095 (1987).
7. I. Mudawar and D. E. Maddox, Critical heat flux in subcooled flow boiling of fluorocarbon liquid on a simulated electronic chip in a vertical rectangular channel, *Int. J. Heat Mass Transfer* **32,** 379–394 (1989).
8. S. Yilmaz and J. W. Westwater, Effect of velocity on heat transfer to boiling Freon-113, *J. Heat Transfer* **102,** 26–31 (1980).
9. Y. Katto and S. Yokoya, Critical heat flux of forced convective boiling in uniformly heated vertical tubes with special references to very large length-to-diameter ratios, *Int. J. Heat Mass Transfer* **30,** 2261–2269 (1987).
10. K. R. Samant and T. W. Simon, Heat transfer from a small heated region to R-113 and FC-72, *J. Heat Transfer* **111,** 1053–1059 (1989).
11. B. D. Strom, V. P. Carey and W. R. McGillis, An experimental investigation of the critical heat flux conditions for subcooled convective boiling from an array of simulated microelectronic devices. In *Heat Transfer in Electronics 1989* (Edited by R. K. Shah), ASME HTD Vol. 111, pp. 135–142 (1989).
12. C. B. Gu, L. C. Chow and J. E. Beam, Flow boiling in a curved channel. In *Heat Transfer in High Energy/High Heat Flux Applications* (Edited by R. J. Goldstein, L. C. Chow and E. E. Anderson), ASME HTD Vol. 119, pp. 25–32 (1989).
13. M. Umaya, Critical heat flux for annular channels with small heated length to heated equivalent diameter ratios, M.Sc. Thesis, Dept. of Mech. Engng, University of Tokyo (1983).
14. T. C. Willingham, C. O. Gersey and I. Mudawar, Forced convection boiling from an array of in-line heat sources in a flow channel, *Proc. ASME–JSME Thermal Engineering Joint Conf.* Reno, Nevada, Vol. 2, pp. 365–374 (1991).
15. N. Zuber, M. Tribus and J. W. Westwater, The hydrodynamic crisis in pool boiling of saturated and subcooled liquids. In *International Developments in Heat Transfer*, Part 2, pp. 230–236 (1961).

EBULLITION EN CONVECTION FORCEE ET FLUX THERMIQUE CRITIQUE POUR UN ARRANGEMENT LINEAIRE DE SOURCES DE CHALEUR DISCRETES

Résumé—Des expériences d'ébullition en convection forcée sont conduites avec FC-72, un 3M Flourinert à 1,36 bar sur un arrangement linéaire de neuf sources de chaleur discrètes simulant des chips micro-électroniques qui affleurent sur la surface d'un canal vertical et rectangulaire. La vitesse d'entrée varie de 13 à 400 cm s^{-1} et le sous-refroidissement du liquide de 3 à 36°C. Une conception spéciale de l'équipement expérimental permet de continuer le test jusqu'à ce que toutes les chips atteignent le flux thermique critique (CHF) sans endommager la section d'essai. En général la position de la dernière chip à atteindre le CHF se déplace en avant quand on augmente le sous-refoidissement. La largeur de bande moyenne du CHF pour un arrangement à plusieurs chips est seulement $\pm 12\%$, ce qui prouve que la discontinuité dans le flux pariétal entre des chips consécutives interrompt la croissance de la couverture de vapeur qui résulte de l'assèchement. La faible largeur de bande du CHF permet qu'une formule antérieurement développée pour le CHF sur une chip unique soit utilisée pour un arrangement de chips.

STRÖMUNGSSIEDEN UND KRITISCHE WÄRMESTROMDICHTE AN EINER LINEAREN ANORDNUNG VON DISKRETEN WÄRMEQUELLEN

Zusammenfassung—Es werden Messungen zum Strömungssieden mit FC-72, einem 3M-Fluorinert, bei 1,36 bar an einer linearen Anordnung von neun diskreten Wärmequellen durchgeführt. Damit werden mikroelektronische Chips simuliert, die in einem senkrechten Rechteckkanal bündig montiert sind. Die Eintrittsgeschwindigkeit wird von 13 bis 400 cm s^{-1} variiert, die Flüssigkeitsunterkühlung von 3 bis 36 K. Eine spezielle Auslegung der Versuchsanlage erlaubt es, jeden Versuch ohne Schäden fortzuführen, auch wenn alle Chips die kritische Wärmestromdichte (CHF) erreicht haben. Siedebeginn und CHF werden mit zunehmender Geschwindigkeit und/oder Unterkühlung zu höheren Wärmestromdichten verschoben. Jedoch war die mittlere Bandbreite der CHF-Werte für die Mehrchip-Anordnung nur $\pm 12{,}3\%$. Die Diskontinuität der Wärmestromdichte zwischen aufeinanderfolgenden Chips hilft, das Anwachsen der Dampfflächen zu unterbrechen, welches normalerweise beim Dryout an der stromabwärts gelegenen Ecke einer langen, gleichförmig beheizten Wand auftritt. Die geringe Bandbreite der CHF-Daten erlaubt es auch, die an einem Einzelchip gewonnene CHF-Korrelation auf eine Mehrchip-Anordnung zu übertragen.

КИПЕНИЕ И КРИТИЧЕСКИЙ ТЕПЛОВОЙ ПОТОК ОТ ЛИНЕЙНОЙ ЦЕПОЧКИ ДИСКРЕТНЫХ ИСТОЧНИКОВ ТЕПЛА ПРИ ВЫНУЖДЕННОЙ КОНВЕКЦИИ

Аннотация—Проводились эксперименты по кипению в условиях вынужденной конвекции с использованием FC-72 и 3M Fluorinert при давлении 1,36 бар на линейной цепочке из девяти дискретых источников тепла, моделирующей микроэлектронные чипы, при этом источники установлены заподлицо в вертикальном канале прямоугольного сечения. Скорость на входе и величина недогрева жидкости изменялись соответственно от 13 до 400 см c^{-1} и от 3 до 36°C. Особая конструкция экспериментальной установки позволила проводить каждый опыт до достижения критического теплового потока (КТП) на всех чипах без повреждения экспериментального участка. За счет увеличения скорости и (или) недогрева кипение и КТП могут возникать при более высоких значениях теплового потока. В общем случае положение последнего чипа для достижения КТП сдвигалось вверх по потоку по мере возрастания величины недогрева. Показано, что дискретность теплового потока на стенках между последовательно расположенными чипами способствует прекращению роста паровой оболочки, которая обычно приводит к кризису теплопереноса у дальнего по течению края длинных стенок с постоянным нагревом. Кроме того, обоснована возможность использования для цепочки чипов соотношения, полученного ранее для КТП в случае отдельного чипа.