

Phononic Crystals for Acoustic Confinement in CMOS-MEMS Resonators

Bichoy Bahr*, Radhika Marathe* and Dana Weinstein

EECS, Massachusetts Institute of Technology, Cambridge, MA, USA

*Authors contributed equally to this work

E-mail: bichoy@mit.edu, marathe@mit.edu

Abstract—This work presents the **first implementation of Phononic Crystals (PnCs) in a standard CMOS process** to realize high- Q RF MEMS resonators at GHz frequencies without the need for any post-processing or packaging. The acoustic resonant cavity is defined using a PnC comprising back-end of line (BEOL) materials such as routing metals and the low- k intermetal dielectric. Within this cavity, a MEMS-CMOS Resonant Body Transistor (RBT) is designed for a resonance frequency within the bandgap of the PnC. This results in a greatly enhanced Q at resonance and suppression of spurious modes off-resonance. The first PnC-confined RBT in IBM’s 32nm SOI process is demonstrated at 2.8GHz with Q of 252, spanning a footprint of $5\ \mu\text{m} \times 7\ \mu\text{m}$.

I. MOTIVATION

The integration of resonators in CMOS is an active area of interest for reduced size, weight, and power, substantially reduced parasitics, and improved yield and reliability due to a standardized process. Furthermore, FET-sensing using RBTs has been demonstrated to reach order-of-magnitude higher frequencies than possible with passive resonators [1]. Monolithic integration with CMOS enables the use of low-parasitic, high- f_T FETs for active sensing in resonators necessary to scale to multi-GHz frequencies.

Post-processing or packaging requirements typically pose the biggest obstacle to resonators in CMOS. Traditionally, the integration of resonators requires a release step to create free boundary conditions for the moving structure. This leads to restrictions on materials and thermal budget when fabricating resonators in BEOL, or compromised yield and increased process complexity when fabricated in the front-end of line (FEOL) process. The development of unreleased resonators in CMOS harnesses the advantages of seamless integration of resonators without the complexity of the release step.

II. DESIGN OF PNC IN CMOS

The authors have previously demonstrated unreleased MEMS resonators in a standard CMOS process using Acoustic Bragg Reflectors (ABRs) patterned using Shallow Trench Isolation [2]. However the small aspect ratio of such ABRs and the corresponding small solid angle subtended at the resonator for acoustic reflection resulted in $Q_s \sim 30$ and the presence of spurious modes. In this work, we propose a 3D acoustic reflective structure comprising a PnC (Fig. 1) which surrounds the resonant cavity resulting in better mode confinement and suppression of spurious modes.

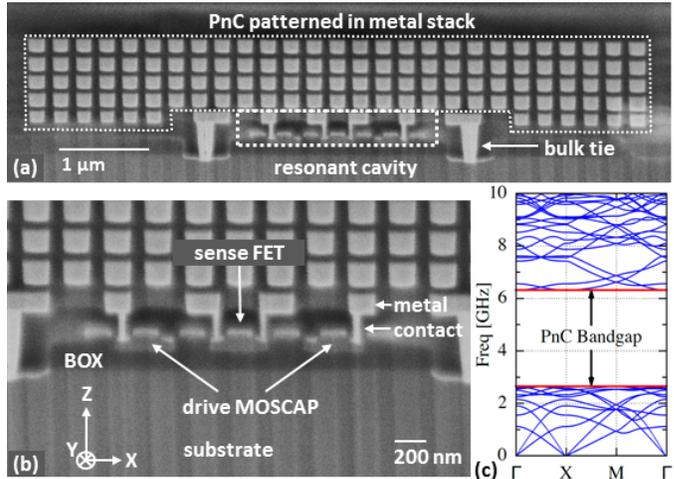


Fig. 1: (a) Cross-section SEM of a CMOS-MEMS resonators showing PnC patterned in metal stack and FEOL resonant cavity (b) details of resonant cavity showing drive and sense transducers (c) COMSOL simulation of the PnC unit cell showing bandgap 2.65 GHz-6.32 GHz.

Material pairs with high acoustic impedance mismatch such as W/SiO_2 or Cu/SiO_2 are necessary for forming PnCs with the wide bandgaps optimal for high reflection [3] and are commonly implemented in 1D ABRs [4]. High acoustic impedance metals such as Cu and W patterned over a low acoustic impedance dielectric such as SiO_2 and $SiCOH$ (Table I) are found in BEOL of integrated circuit (IC) technologies and are ideal for forming PnC reflectors. **In this work, the PnC defining the acoustic cavity was designed in IBM’s 32nm SOI process using the first five metal layers of the BEOL stack.** These consist of Cu surrounded by low- κ $SiCOH$ intermetal dielectric [5]. A simulation of the PnC demonstrates 3.67GHz wide bandgap centered at 4.5GHz (Fig. 1(c)).

III. RESONATOR DESIGN

The foundry-provided analog nFET was chosen to drive and sense the acoustic resonator to utilize the high-quality ultra-thin dielectric and high-performance FETs available in the

TABLE I: Mechanical properties for materials in the CMOS stack

Material	ρ (kg/m^3)	c_{11} (GPa)	Z_{11} ($MRayls$)	c_{44} (GPa)	Z_{44} ($MRayls$)
Poly-Si	2320	182.6	20.6	65.5	12.3
SiO_2	2200	75.2	12.9	29.9	8.1
Tungsten	19250	525.5	100.5	160.5	55.6
Copper	8937	189.4	41.1	47.0	20.5
$SiCOH$	1060	3.96	2.0	1.32	1.18

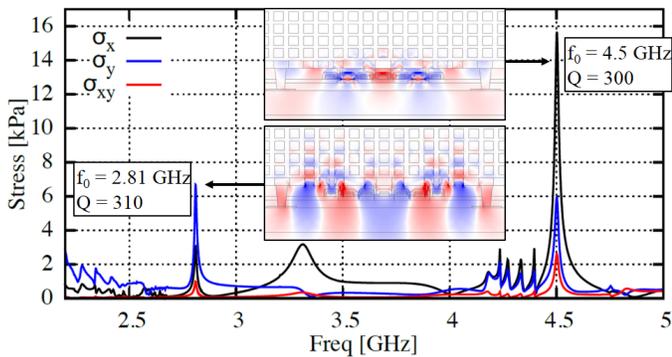


Fig. 2: 2D COMSOL simulation of PnC resonator with resonances at 2.81 GHz (Q of 310) and 4.5 GHz (Q of 300).

FEOL stack. In the ABR-only design from [2], the drive and sense transducers each spanned half the length of the cavity (in the y -direction), resulting in an asymmetric transduction of the longitudinal mode. In the current design, such asymmetry was avoided by configuring two nFETs as MOSCAPs (MOSCAs) extending the entire length of the resonance cavity (in the y -direction). The single sensing nFET was placed at the center of the cavity between the two driving MOSCAPs. The routing for the drive and sense gates was limited to the first metal layer to maintain the periodicity of the PnC in the higher metal levels for optimal acoustic confinement at resonance. Further modifications to layout include removal of some vias from MOSCAP source/drain regions, use of long rectangular wall-like vias spanning the width of the FET (in the y -direction), exclusion of CMP fill above the acoustic structure, and inclusion of bulk ties (vias to substrate) at the transistor level to optimize mode confinement. The resultant mode shape and frequency response from COMSOL simulation is shown in Fig. 2.

IV. EXPERIMENTAL RESULTS

A cross-sectional SEM of the PnC RBT is presented in Fig. 1(a,b). The DC response of the sense transistor is shown in Fig. 3 and exhibits expected FET performance, despite the modifications mentioned in §III. In operation, the driving MOSCAP gates are biased at $V_A = 1$ V with -10 dBm input power. The sense transistor is biased in saturation with drain voltage $V_{DS} = 0.6$ V, gate voltage $V_{GS} = 0.65$ V, and drain

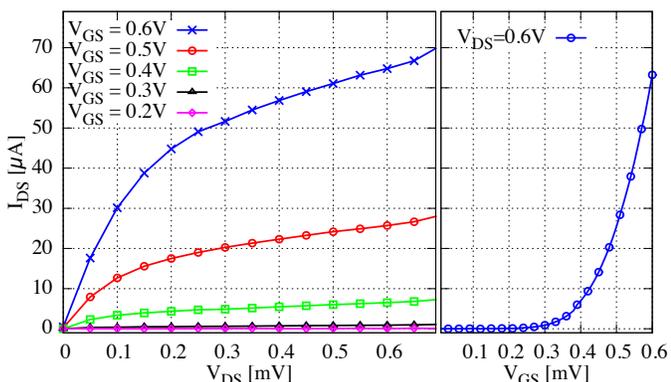


Fig. 3: (left) $I_{DS} - V_{DS}$ characteristics and (right) $I_{DS} - V_{GS}$ of the resonator's sensing FET showing expected transistor response.

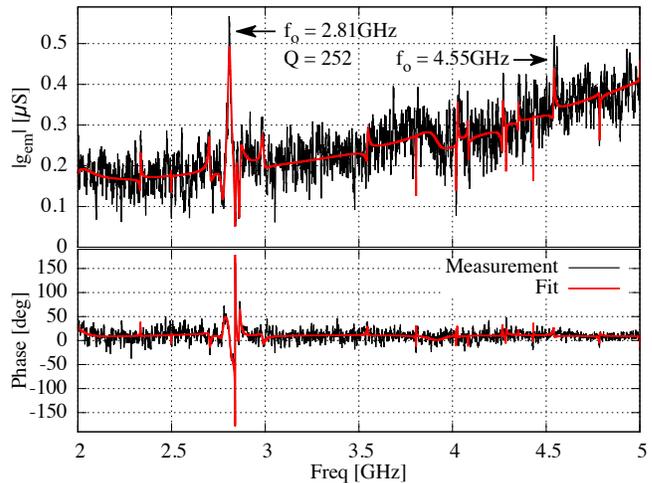


Fig. 4: Measured mechanical transconductance $g_{em} = Y_{21} - Y_{12}$ of the fabricated PnC RBT. The measured response correlates well with simulation, both in frequency and quality factor.

current $I_{DS} = 95$ μ A. At resonance, the acoustic vibrations of the resonant cavity are sensed as the piezoresistive modulation of the FET drain current.

Devices were de-embedded using their response at $V_A = 0$ V on the driving MOSCAPs, corresponds to the resonator “Off” state to suppress the mechanical mode. The frequency response of a 2.8 GHz resonator is presented in Fig. 4 in good agreement with the simulated response in Fig. 2. A 3-point running average is applied to the data for smoothing before fitting a rational transfer function with 24 poles to extract a Q of 252 at the 2.8 GHz resonance. **This shows a $10\times$ boost in Q over the previous generation CMOS-integrated in [2] with only a $2\times$ increase in overall footprint.** The PnC RBT also shows a wide spurious-free spectral range extending up to 4 GHz.

V. CONCLUSION

This first implementation of a PnC in a standard CMOS process to define an acoustic resonant cavity results in a $10\times$ Q improvement of CMOS integrated resonators with greatly improved suppression of spurious modes. This concept may be easily extended to any IC technology with multi-level metal stacks. This facilitates the design of monolithically integrated high- Q hybrid CMOS-MEMS resonators for applications at RF and mm-wave frequencies.

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