Zhengping Jiang

Phone: 765-237-1611
E-mail: z1.jiang@samsung.com
www.linkedin.com/in/zpjiang

PROFESSIONAL EMPLOYMENT

Sr. Engineer, Samsung Semiconductor Inc. January 2016 to present

Research Assistant, ECE, Purdue University Aug. 2008 to December 2015

Research areas: quantum transport in ultra-scaled transistors, TCAD model & software development, semiconductor device physics, high performance parallel computation.
Supervisor: Professor Gerhard Klimeck

Engineer Intern, Samsung Semiconductor Inc. July 2015 to December 2015

Summer Internship, IBM T. J. Watson Research Center Jun. 2012 to Aug. 2012

Modeling of Piezoelectronic Transistors. Study of piezoelectric materials.
Mentors: Glenn Martyna, Dennis Newns

Summer Internship, GLOBALFOUNDRIES U.S. Inc. Jun. 2013 to Aug. 2013

Modeling of InGaAs MOSFETs. Scaling of sub-20nm FinFETs. Effects of alloy scattering on electronic transport.
Mentors: Zoran Krivokapic, Behtash Behin-Aein

EDUCATION

Tianjin University, Tianjin, China
B.S. in Electronic Science and Technology, Adviser: Professor Shilin Zhang July 2008
Purdue University, West Lafayette, USA
M.S. in Electrical and Computer Engineering, Adviser: Professor Gerhard Klimeck May 2011
Ph.D in Electrical and Computer Engineering December 2015
Academic Adviser: Professor Gerhard Klimeck

HONORS

2012-2013 IBM Ph.D. Fellowship Award

2013 GLOBALFOUNDRIES SRC Education Alliance Intern Scholar (For support of 10 week internship)

RESEARCH PROJECTS

Develop all-purpose Nanoelectronics Simulation Toolkit **NEMO5**

- Develop modular structured, multi-level parallelization software toolkit; debug and performance profiling; implementing multi-physics solvers.
- Object-oriented programming with C++; python; high performance parallel computing.

Electronic Transport in Ultra-scaled Tunneling FET

- Explore ultimate scalability of band to band tunneling diode and Tunneling FET.
- Deliver insight on effects that limit device performance.

Electronic Transport in ultra-scaled MOSFET

- Modeling of advanced MOSFETs under 14/10nm technology nodes.
- Effects of alloy scattering in InGaAs MOSFETs.

Simulation of Piezoelectronic Transistors

- *Ab initio* studies on pressure-induced metal insulator transition in Samarium chalcogenides.
- Empirical tight binding parameterization of compound materials for electronic transport.

Simulation of Resistive Random Access Memory (RAM)

- Modeling of filamentary conduction in Cu/SiO_2 based CBRAM.
- Tight binding parameterization of copper and silicon dioxide for electronic transport.

PUBLICATIONS & PRECEEDINGS

1. S. Lee, H. Ryu, **Z. Jiang**, G. Klimeck, *"Million Atom Electronic Structure and Device Calculations on Peta-Scale Computers"* proceedings of the 13th IWCE, Tsinghua University, Beijing, China, May 2009
2. **Z. Jiang**, N. Kharche, G. Klimeck, *"Valley Degeneracy in (110) Si Quantum Wells - Strain and Misorientation Effects"* proceedings of the 14th IWCE, Pisa, Italy, October 2010
3. **Z. Jiang**, N. Kharche, T. B. Boykin, G. Klimeck, *"Effects of Interface Disorder on Valley Splitting in SiGe/Si/SiGe Quantum Wells"* Applied Physics Letters Vol100 issue10, March 2012
4. Y. Tan, M. Povolotskyi, T. Kubis, Y. He, **Z. Jiang**, T. Boykin, G. Klimeck, *"Empirical tight binding parameters for GaAs and MgO with explicit basis through DFT mapping"*, Journal of Computational Electronics, Volume 12, Issue 1, pp 56-60 (2013)
5. **Z. Jiang**, Y. Tan, M. Kuroda, et al., *"Electron transport in nano-scaled Piezoelectronic devices"*, Appl. Phys. Lett. 102, 193501 (2013)
6. B. Rajamohanan, D. Mohata, Y. Zhu, M. Hudait, **Z. Jiang**, M. Hollander, G. Klimeck and S. Datta, *"Design, fabrication, and analysis of p-channel arsenide/antimonide hetero-junction tunnel transistors"*, J. Appl. Phys. 115, 044502 (2014)
7. M. Kuroda, **Z. Jiang**, M. Povolotskyi, G. Klimeck, D. Newns, G. Martyna, *"Anisotropic strain in SmSe and SmTe: Implications for electronic transport"* Phys. Rev. B 90, 245124 (2014)
8. **Z. Jiang**, B. Behin-Aein, Z. Krivokapic, M. Povolotskyi, G. Klimeck, *"Tunneling and Short Channel Effects in Ultra-scaled InGaAs Double Gate MOSFETs"*, Electron Device, IEEE Transactions on, Vol. 62 Issue 2, pp 525-531 (2015)
9. **Z. Jiang**, Y. Lu, Y. Tan, Y. He, M. Povolotskyi, T. Kubis, A. C Seabaugh, P. Fay, G. Klimeck, *"Quantum Transport in AlGaSb/InAs TFETs With Gate Field In-Line With Tunneling Direction"* Electron Devices, IEEE Transactions on 62 (8), 2445-2449 (2015)

BOOK CHAPTER

1. Alan Seabaugh, Zhengping Jiang, Gerhard Klimeck, *"Tunnel transistors"* in *"CMOS and Beyond: Logic Switches for Terascale Integrated Circuits"* Chapter: 6, Cambridge University Press, ISBN:9781107043183, April 2015

CONFERENCE PRESENTATIONS & POSTERS

1. H. Ryu, G. Klimeck, S. Lee, R. Rahman, B. Haley, S.H. Park, N. Kharche, **Z. Jiang**, T. B. Boykin, C. Wellard, J. Cole, L. Hollenberg, G. Lansbergen, S. Rogge, B. Weber, M. Simmons, *"Nanoelectronic Modeling (NEMO) for High Fidelity Simulation of Solid-State Quantum Computing Gates"* Silicon Qubit Workshop, Univeristy of California Berkeley, Aug. 2009.
2. A. Paul, S. R. Mehrotra, **Z. Jiang**, M. Luisier, G. Klimeck, *"Modeling of SiGe material for ultra-scaled CMOS device applications"* MSD, FCRP Annual Review, student poster, MIT, Boston, MA, May 2010
3. T. Boykin, **Z. Jiang**, N. Kharche, G. Klimeck, *"Effects of disorder on the valley-splitting in Si/SiGe quantum wells"* International Workshop on Silicon Quantum Electronics, oral presentation, Denver, CO, Aug. 2011
4. **Z. Jiang**, W. S. Cho, H. H. Park, M. Luisier, T. Kubis, G. Klimeck, Y. Lu, R. Li, G. Zhou，A. Seabaugh, P. Fay, S. Datta, D. Mohata, T. Mayer, D. Pawlik, S. Rommel, *"Atomistic Quantum Transport Modeling in Band-to-band Tunneling Transistors"* MIND review, student poster, South Bend, IN, Aug. 2011
5. **Z. Jiang**, Y. He, Y. Tan, M. Povolotskyi, T. Kubis, G. Klimeck, *"Quantum Transport in GaSb/InAs Nanowire TFET with Semiclassical Charge Density"* IWCE 2012, University of Wisconsin – Madison, May 2012
6. M. Salmani-Jelodar, S. H. Park, **Z. Jiang**, T. Kubis, M. Povolotskyi, G. Klimeck, *"Contact-to-channel Resistance Modeling in HEMT Devices"* MSD review, Boston, MA, May, 2012.
7. **Z. Jiang**, Yu He, K. Miao, Y. Tan, M. Povolotskyi, T. Kubis, and G. Klimeck. *"Quantum Transport in Tunneling Field Effect Transistors"* **2nd prize** poster presentation in NRI review of the MIND center, Notre Dame, IN, Aug. 15, 2012.
8. **Z. Jiang**, Y. Lu, Y. Tan, Y. He, M. Povoloskyi, T. Kubis, A. Seabaugh, P. Fay, G. Klimeck *"Atomistic Simulation of GaSb/InAs Tunneling Field Effect Transistor"* TECHCON, oral presentation, Austin, TX, September 10-11, 2012
9. S.-H. Park, N. Kharche, D. Basu, **Z. Jiang**, S.K. Nayak, C.E. Weber, and G. Klimeck , "*Scaling Effect on Specific Contact Resistivity in Nano-scale Metal-Semiconductor Contacts*", IWCE 2013, Nara, Japan, June 2013

10. **Z. Jiang**, M.A. Kuroda, Y. Tan, D.M. Newns, G.J. Martyna, M. Povolotskyi, T.B. Boykin, T. Kubis, and G. Klimeck, *"Tight-Binding Modeling of Intermediate Valence Compound SmSe for Piezoelectronic Devices"* , IWCE 2013, Nara, Japan, June 2013
11. Z. Jiang, Y. He, G. Zhou, T. Kubis, H. Xing, G. Klimeck, *"Atomistic Simulation on Gate-recessed InAs/GaSb TFETs and Performance Benchmark"* Device Research Conference (DRC), Notre Dame, IN, USA, June 2013