Design ideas for Tunnel-FETs

Objective

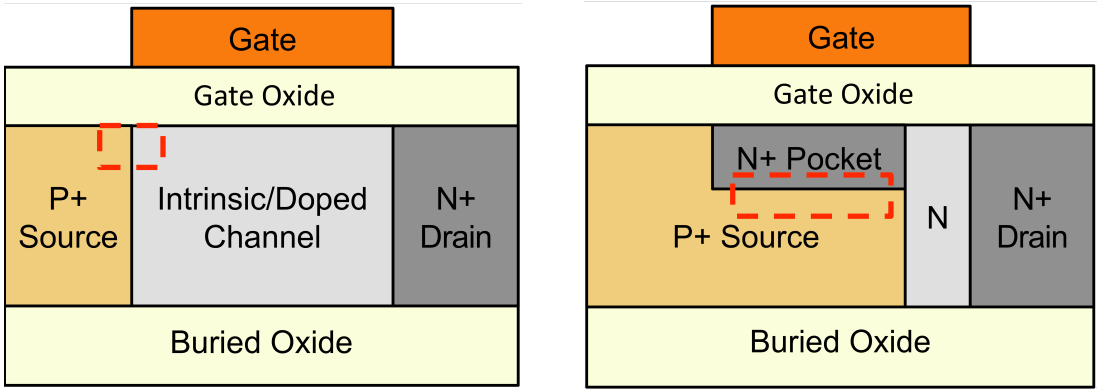
- To explore design ideas for voltage scaling of transistors.

Approach

- V_{DD} scaling : Difficult in MOSFETs, possible in TFETs.
- gFET: Larger tunneling area gives higher I_{ON} than conventional TFETs.
- Modified and optimized gFET design to meet ITRS requirements.

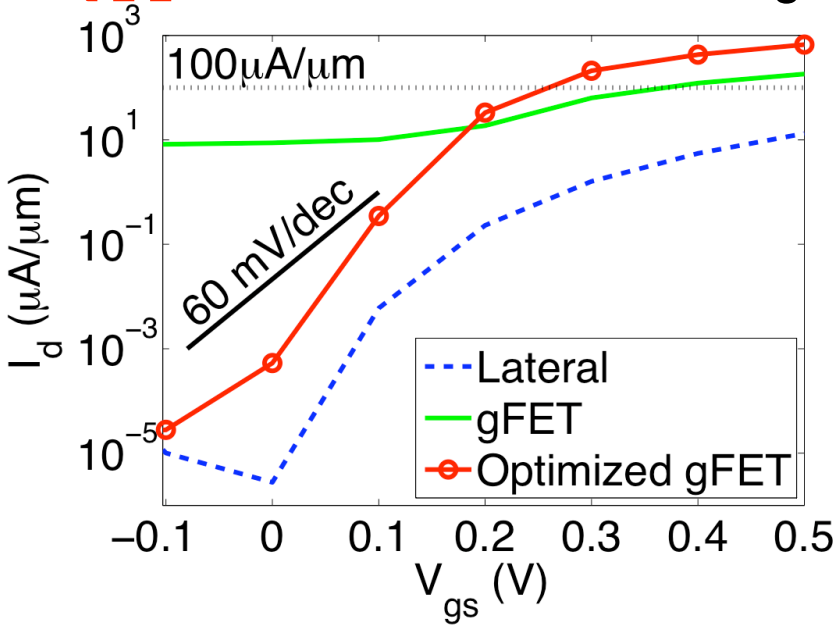
Impact

- gFET with high I_{ON} and low I_{OFF} will provide a viable alternative for V_{DD} scaling to reduce power consumption.



Lateral Tunneling P-I-N TFET vs. Vertical Tunneling gFET

: Band to Band Tunneling region



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