NEMO5

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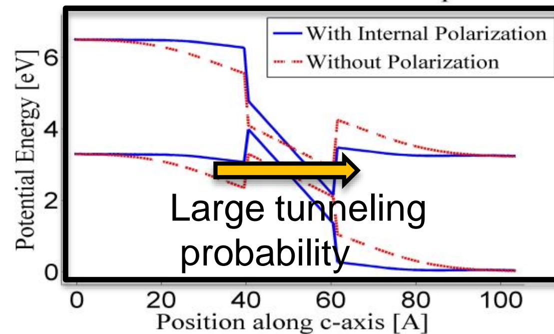
Design optimization of polarization engineered III-Nitride tunnel FETs

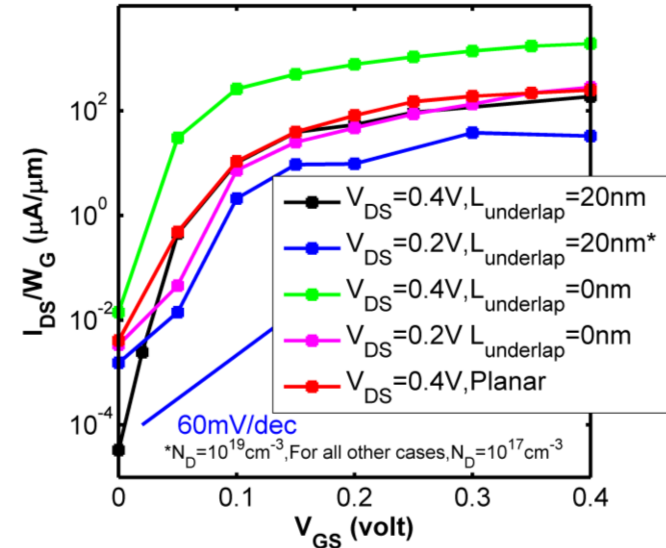
Objective:

- Model optimized TFETs by utilizing polarization induced field in Nitrides (high I_{ON} and low SS at low supply voltage)

Simulation method:

Balistic simulation using Qunatum Transmitting Boundary Method (QTBM)



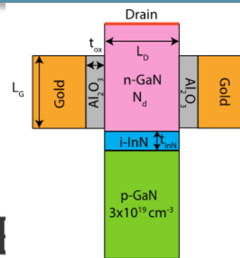


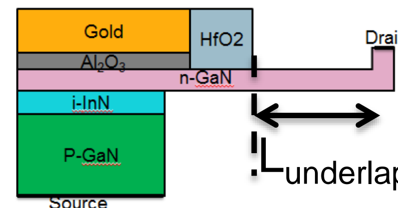
Results:

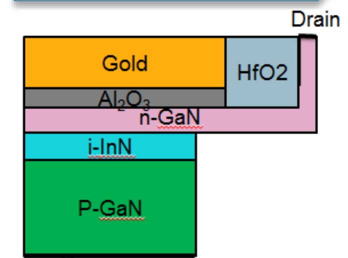
- Geometry with the best gate control (low Subthreshold Swing, SS) and highest I_{ON} is explored.

- Good I-V characteristics observed even at supply voltage as low as 200mV for L-shaped geometry.

Sidewall-gate geometry	L-shaped $L_{underlap}$=20nm	L-shaped $L_{underlap}$= 0nm
SS:25mV/dec I_{ON}:247μA/μm	SS:12mV/dec I_{ON}:187μA/μm	SS:15mV/dec I_{ON}:1911μA/μm







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