Design for Variability Tolerance: On-current Variation in [110] PMOS Nanowires

Objective:

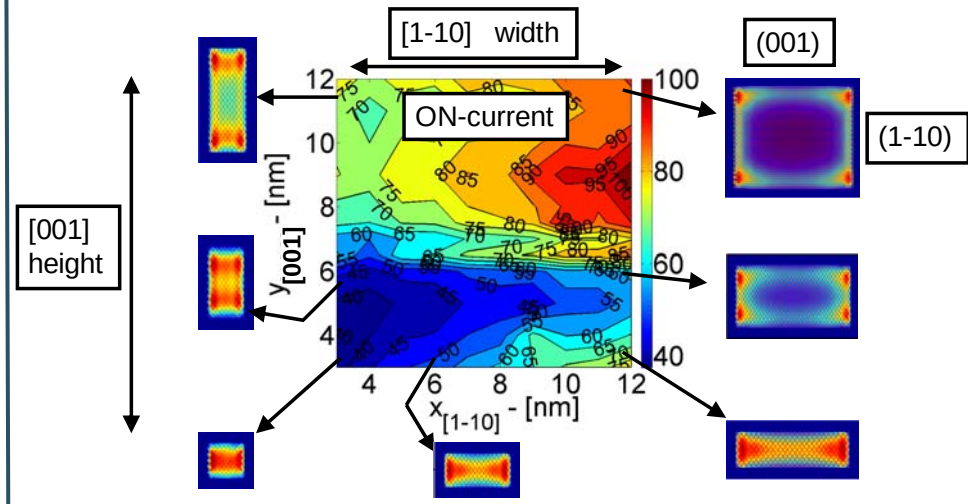
- Investigate mechanisms of ON-current variation cause by the anisotropic bandstructure
- On-current variations at the onset of volume to surface inversion in [110] PMOS NWs

Approach:

- Use the atomistic $sp^3d^5s^*$-SO model with ballistic transport
- Simulate the ON-current of devices of widths/heights 3nm-12nm (all combinations within)
- Form the ON-current variation surface (shown to the right)

Impact:

- Design space has been identified for minimal current variations in [110] PMOS nanowires
- Sharp variations are identified at the onset of volume to surface inversion in [001] heights
- Strain can tune the sensitivity, or shift it in different design regions



Results:

- The ON-current variation surface of [110] PMOS nanowires as the width in [1-10] and height in [001] is varied from 3nm to 12nm
- The charge placement is different for each quantization surface
- Sharp variations are observed at 6nm of height in [001].

Publications:

- Tool at nanoHUB.org Band Structure Lab
- Nano Letters [J115]

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