Performance Analysis of Ultra-Scaled InAs HEMTs

Objective

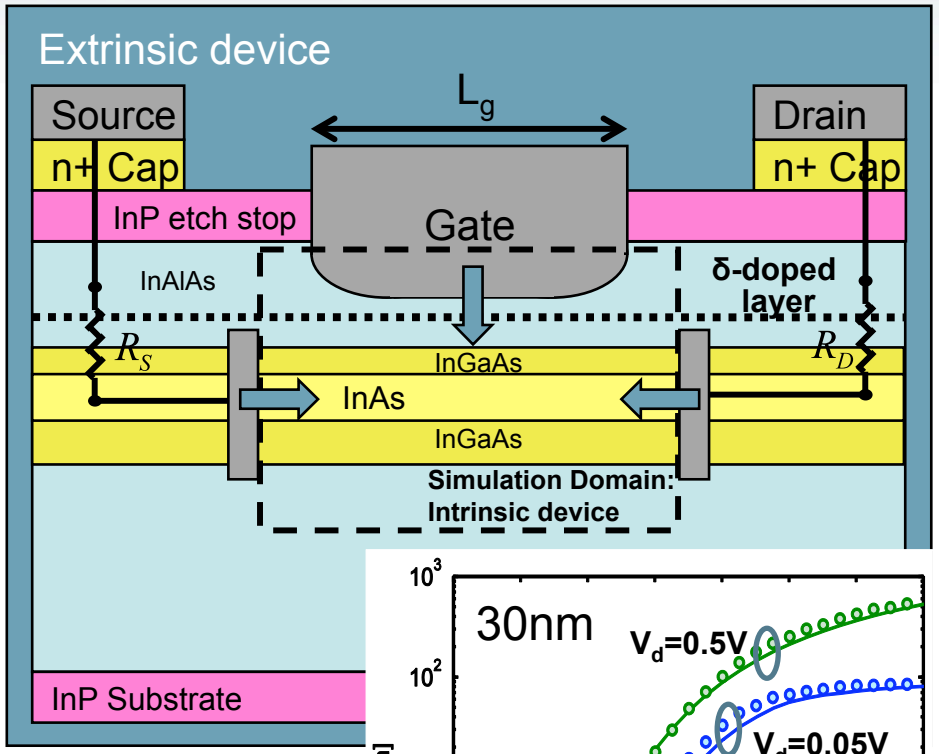
- **Develop:** a methodology to simulate ultra -scaled InAs HEMTs
- **Benchmark:** match experimental I-Vs for different gate lengths ranging from 30 to 50nm
- **Improve:** device design for scaling down to 20nm node

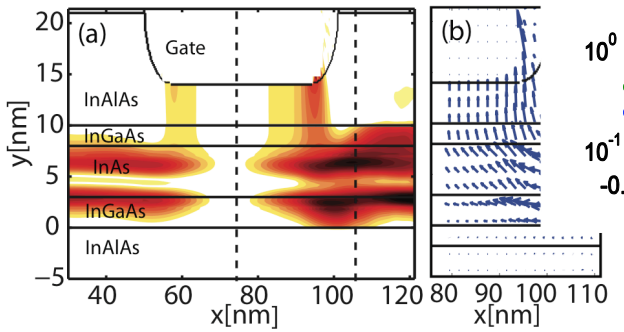
Approach

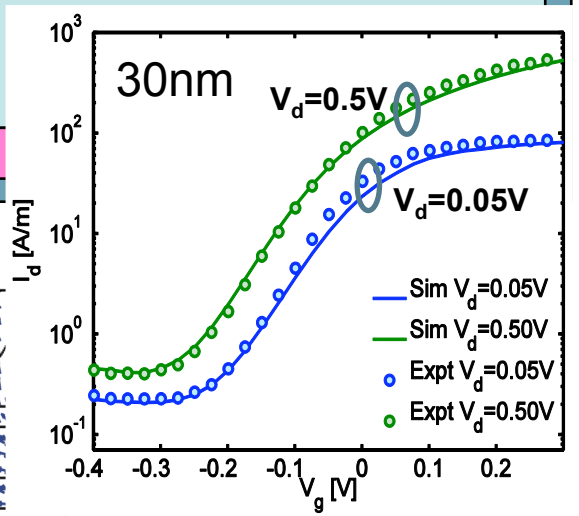
- 2-D Schrödinger-Poisson Solver
- Real-space effective mass quantum transport model
- Injection from Source, Drain and Gate contacts

Results/Impact

- Quantitative match to experiments
- Accurate description of shape of the gate contact is critical to replicate experimental results
- At gate length of 20 nm, best performance can be achieved in thin InAs channel devices by reducing the insulator thickness to improve the gate control while increasing the gate work function to suppress the gate leakage







Ref: *IEDM* 2009