

# Exploring Channel Doping Designs for High-Performance Tunneling FETs\*

#### **Problem:**

- ON/OFF ratio of TFETs is limited by
- (1) low S-C tunneling probability
- (2) high S-D tunneling leakage
- Lowering the drain doping (Nd) is not a scable design
- The source-pocket (SP) design requires a high pocket doping density (Np)

#### **Objective:**

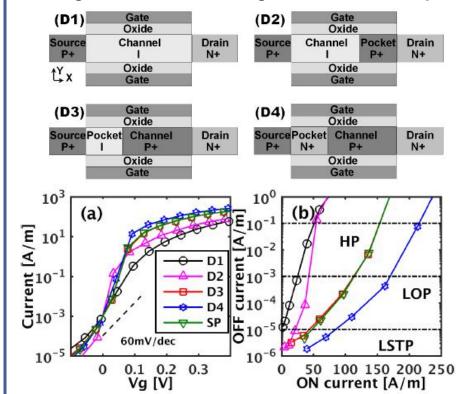
 Exploring different channel doping strategies to improve I<sub>ON</sub>

## Approach:

• (D1): a conventional nTFET with intrinsic channel; (D2): intrinsic channel with a P+ drain pocket; (D3): P+ channel with an intrinsic source pocket; (D4): P+ channel with an N+ source pocket.

### Results / Impact:

- D2 improves the SS (and  $I_{\rm ON}$ ) and it is more scalable than lowering Nd
- D3 performs similarly to the SP design
- D4 further improves I<sub>ON</sub> of the SP design without having to increase Np





\*J. Z. Huang, et al., in Proc. DRC, Jun. 2016, DOI: 10.1109/DRC.2016.7548456