nanoHUB online simulation and more — an NCN project

Benchmarking Top of the Barrier Model using experimental CV data

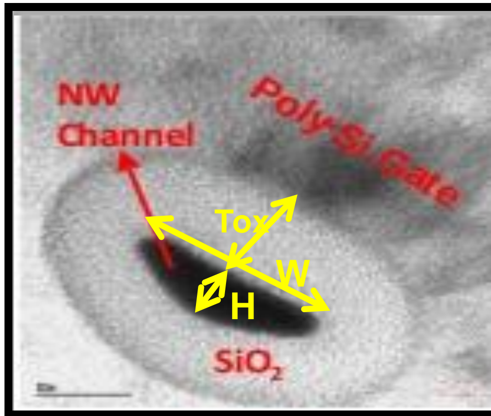
Collaboration between Purdue University & Institute of Microelectronics, Singapore.

Objective :

- Verify experimental CV measurement technique (CBCM*) for single silicon nanowire FETs.
- Benchmarking top of the barrier (ToB) transport model using experimental CV.

* CBCM = charge-based capacitance measurement

Device Details:



TEM image of original single Silicon nanowire FET.

Device Dimensions:
Tox = 9nm
W = 25nm
H = 14 nm
Source/Drain doping :
n-type ,1e20cm^{-3}

Intrinsic <100> oriented Silicon channel.

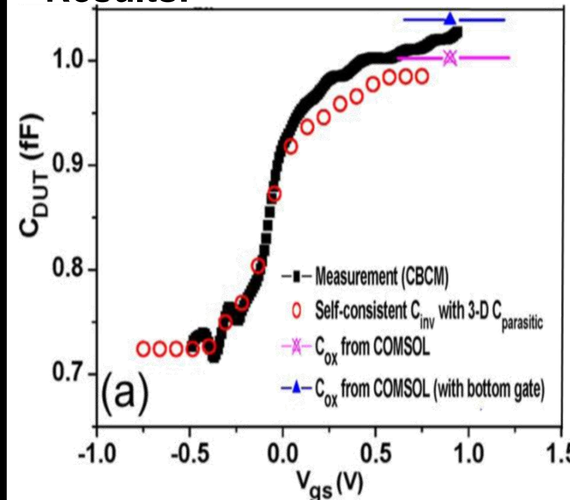
Impact:

- New CV measurement method.
- Top of the Barrier method suitable for CV modeling of Silicon Nanowire FETs.
- Work published in IEEE, EDL VOL. 30, NO. 5, MAY 2009. p.526

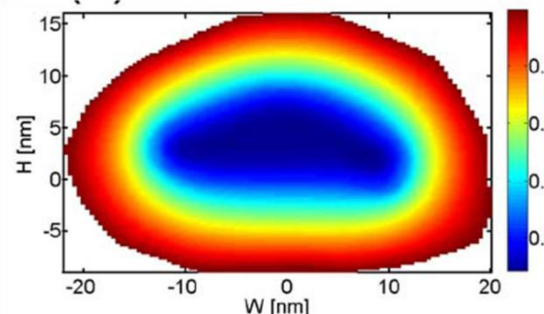
Approach :

- Use sp3d5s* Tightbinding model for electronic structure calculation.
- Perform self-consistent Schrodinger-Poisson (2D) simulations at different gate biases (Vgs) for the actual device size.

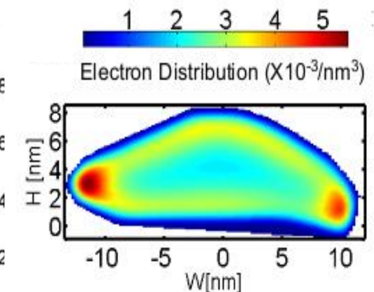
Results:



Measured C−Vgs using the CBCM technique and self-consistent intrinsic SiNW gate capacitance simulated using ToB model added with the 3-D electrostatic capacitance without considering NW obtained from COMSOL



Electrical Potential Distribution.



Electron charge distribution inside the silicon wire.

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