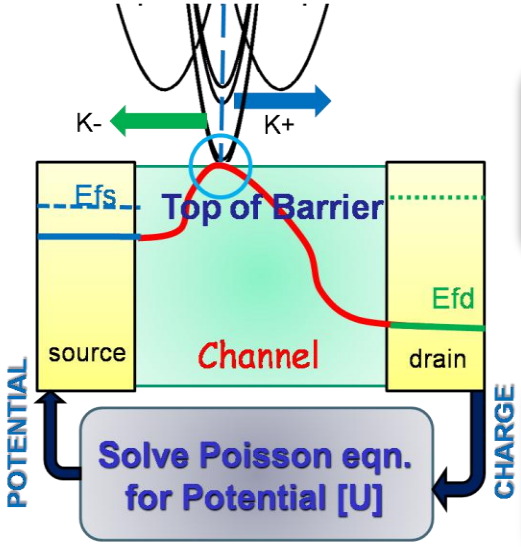
Performance of Trigated Silicon Nanowire pMOSFETs : Surface and Orientation dependence

Objective:

- Study performance of SiNW pMOSFETs.
- Study impact of *surface* and *transport orientation*

Approach & Models :



Electronic structure
10 band sp3s* model with spin orbit coupling.

Transport Model
Ballistic Top of the Barrier model to calculate I_{DS}

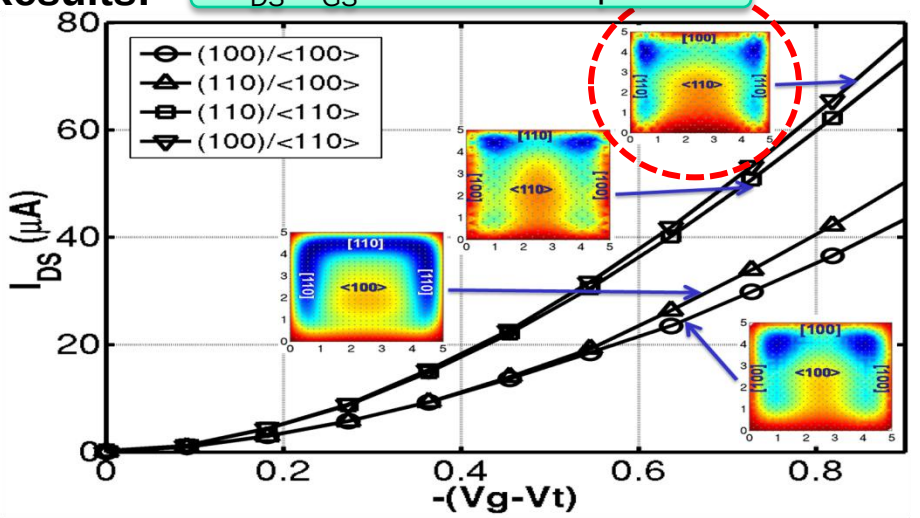
Potential - Charge self-consistent simulation method

Impact:

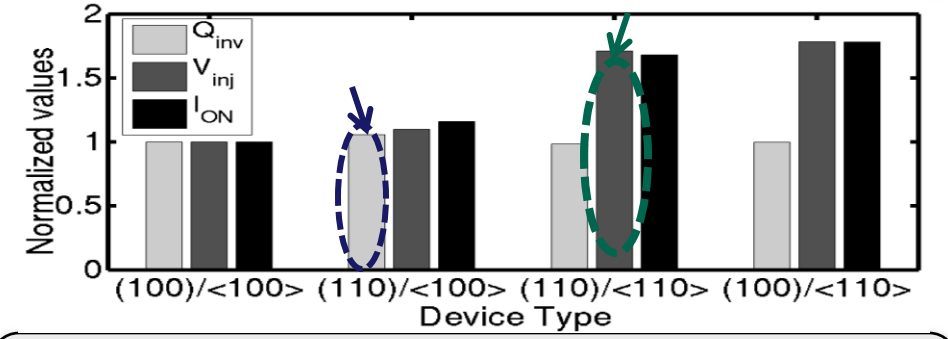
- Channel orientation is more important in nanowire FETs compared to surfaces.
- Need to move to other channel materials like Ge to further improve I_{ON} in PMOSFETs.
- Results presented *in IEEE WMED, 2009* **[P108]**

Results:

I_{DS}-V_{GS} for 4 different pMOS



<110> channel device with maximum number of [110] surfaces shows maximum I_{ON}.



Comparison of 1D charge and carrier velocity V_{inj} at $V_{GS} = V_{DD}$.
- Charge controlled by number of [110] surfaces.
- Higher V_{inj} for <110> orientation

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