Trap density metrology in state of art Si n-finFETs-

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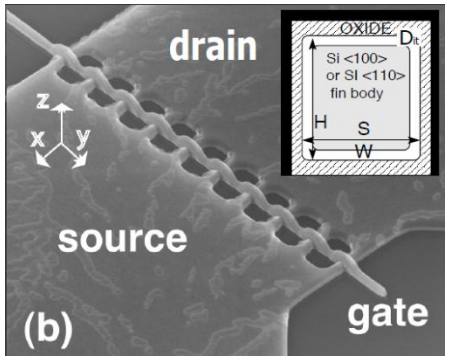
Objective: Direct trap density estimation in actual Si <100>/<110> n-finFETs.

Adv: No special Structure needed

N-finFET TEM image



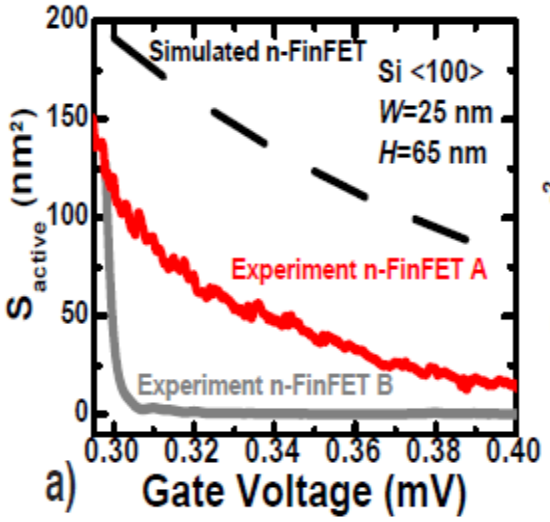
Approach: Using difference between non-ideal (expt.) and ideal (simulated)

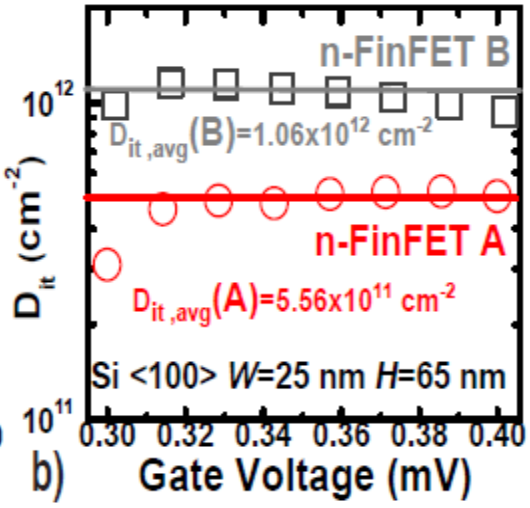
✓Source to channel barrier height (E_b)

✓Active channel area (S).

For trap density (Dit) estimation in [100]/ [110], Si nfinFETs.

Results : Dit estimation in two n-finFETs .





- Typical Dit in 1-10 xe11/cm^2 range
- <110> FETs ~2X more Dit than <100> due to more surface bonds.
- Higher Dit in thinner nFETs (H=65,W=5nm).
- More Dit in 3D FETs compared to planar FETs.
- H2 passivation → ~1.5X reduction in Dit..

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