LOW POWER TRANSISTORS AND QUANTUM PHYSICS BASED ON LOW DIMENSIONAL MATERIALS

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This Thesis is Dedicated to my Parents and Family.

For their endless love, support, encouragement and sacrifices.

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1. INTRODUCTION

1.1 Challenge of Device Scaling

The continuous improvement of modern electronics has been sustained by the scaling of silicon based MOSFETs over the last 4 decades. Fig. 1.1 [1] shows the CPU trends from Intel, in clock speed and number of transistors per unit until 2010. The number of the transistors continues to go up as Moore predicted. However, the clock speed, the frequency of the processors has been saturated since 2005. This prevents us from improving the performance of the processors further, the major reason being the difficulty in dissipating heat from the chips.

The power consumption has already reached the cooling capability limit ($100W/cm^2$). To reduce this power consumption, the transistors need to have a smaller supply voltage V_{DD} at ON state and still maitain a small leakage current at OFF state.

1.2 Challenge of Tunnel FET

MOSFETs are turned OFF by increasing the thermionic barrier. In this way, how fast they can be turned on by gate voltage (Vg) is limited by the Fermi-Dirac distribution. This limits the subthreshold swing (SS, describes how much gate voltage needs to be applied for the current to change by a decade) to be greater than $60mV/dec$. Limited by the lower limit of SS, the MOSFET switches cannot have a smaller supply voltage V_{DD} without increasing the leakage current. This prevents CMOS from further reducing the power consumption.

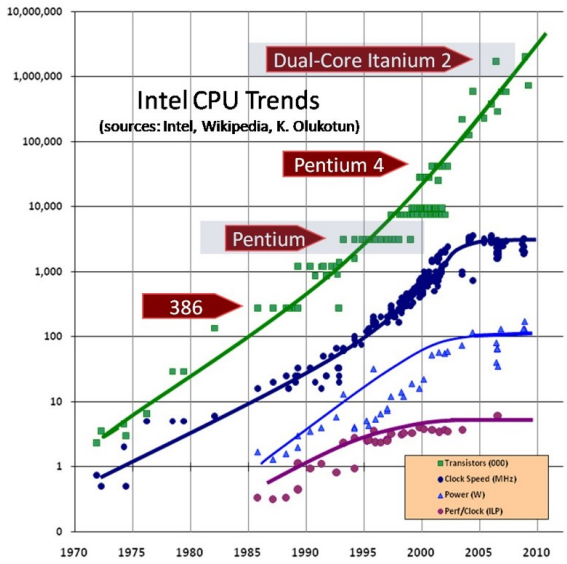


Figure 1.1. Intel CPU Trends. (Source: [1])

Unlike MOSFETs, Tunnel Field-Effect-Transistors (TFETs) are turned on by tunneling current. This allows TFETs to have a SS smaller than 60 mV/dec. Breaking this SS limit in TFETs makes it a possible solution to power dissipation problems. Although, SS¡60 has been demonstrated experimentally in conventional TFETs, they suffer from low ON current, orders of magnitude lower than MOSFETs. The ON current is usually degraded to 0.1 to 100 $\mu A/\mu m$, compared to 1000 $\mu A/\mu m$ in MOSFETs. Hence achieving high ON-current and performance requires novel device structures.

1.3 2D materials

The WKB approximation of the transmission through a triangular well tells us a larger tunnel current would result from a smaller 1. tunnel length λ; 2. band gap Eg; 3. effective mass m^* of the channel material.

A smaller tunnel length λ can result from a smaller channel thickness $t_{channel}$. This brings the emerging 2D material into attention. Low dimensional materials have unique features which can be used to solve the challenges of TFETs.

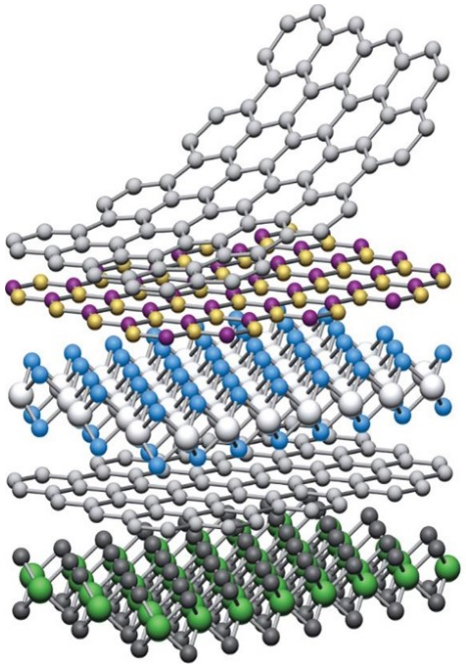


Figure 1.2. Stacking 2D materials. (Source: [2])

Fig. 1.2 shows the different 2D materials stacking together and the connecting bonds are Van Der Waals. The advantages of this stacking structure are 1) Low density of interface defects due to very small amount of dangling bonds at surface; 2) Immunity to energy band gap increasing from vertical quantization due to the 2D nature; 3) Excellent electrostatic control due to the sub-nanometer thickness.

High performance TFET designs based on bilayer graphene in Chapter2, black phosphorous in Chapter 3 published in and vertically stacked 2D materials in Chapter 4 are proposed and studied in this thesis. The quantum physics involved in the transport study is discussed in detail in each chapter.

1.4 Topological Insulators

Topological insulator (TI) materials such as Bi2Te3 have extraordinary surface properties [3–5]. These make them a unique class of materials for applications also as low power electronic devices [6], spintronics [5], and quantum computation [7, 8]. TIs host surface states with the spin perpendicular to the surface normal, spin-locked relative to the electronic in-plane momentum. Backscattering of such surface electrons requires spin-flip processes. In TI devices that are free of magnetic impurities, surface electron backscattering is therefore unlikely.

Such unique properties of TI surfaces make this material also interesting for low power applications. The surface transport in TI nanowires, the Aharonov-Bohm effect and also some novel findings on the surface Fermi Velocites are discussed in chapter 5.

The vertical strain of bilayer graphene work in section 2.2 has been published in [9]; the electrical doping effect on bilayer graphene is published in [10]; the bilayer graphene TFET design is published in [11]. Thickness Engineered TFET based on phosphorene discussed in chapter 3 is published in [12]. The method of modeling MoS2-WTe2 interlayer TFETs in section 4.3.2 has been published in [13], this abstract has won the best student poster award when presented in 2016 ICPS. The work about topological insulator Bi2Te3 nanowire in chapter 5 is published in [14, 15]. The rest results including the transport based on tunable band gap in bilayer graphene in section 2.2.2; the bilayer graphene PN junction collaboration with experimental group work in section 2.3; the NDR results from Gr/BN/Gr structure in section 4.2; the operation mechanism in section 4.3.3 and 4.3.4 of MoS2-WTe2 interlayer TFETs; the capacitance in section 4.3.5 and the device performance study of MoS2-WTe2 interlayer TFETs in section 4.3.6 are still under the process of publishing and are not available online up to date.

2. BILAYER GRAPHENE

2.1 Introduction

Being a two-dimensional material, graphene has attracted great interest for its extraordinary physical, chemical, and electrical properties [16–18]. Its many unique features include high mobility, excellent electrostatic control due to to 2D nature, and ease of top-down fabrication. All these make it a promising candidate for many electronic and optoelectronic applications. Due to the lack of a bandgap, however, graphene transistors cannot be completely turned off. By adding one more graphene layer with specific AB stacking order and applying a vertical electric field across the two layers, a sizable bandgap in the range of 0 to 300 meV can be achieved in bilayer graphene (BLG), in agreement with previously published reports [19, 20]. It is then of our interest to investigate the transport properties of bilayer graphene FETs in the presence of the dynamically tuned bandgap.

This report first evaluates the bandgap of the BLG from tight-binding calculations. A bandgap is created by an electric field in this zero bandgap semiconductor up to 300 meV at a displacement field of $6V/nm$. A saturation of the bandgap is observed at larger fields. A BLG transistor with a top and a bottom gate is then considered to exploit the tunable band gap behavior. The electric field is created through the voltage difference of these two gates. The transmission of this transistor is shown to follow the corresponding electric-field dependent band structure. This verifies that the tunable band gap behavior is captured in the transport model.

The simulation data reveal the following: 1) an on/off ratio of 100 can be achieved in the double gated BLG FET, in contrast to a ratio of 10 for a similar FET without

the tunable band gap effect; and 2) a shift of the current-voltage (I-V) characteristics as a result of the electrostatic control by the back gate. Similar work can be found in [21, 22], however our paper focuses on the performance of the tunable band gap effect in the BLG FET.

2.2 Tight Binding Model

Here, the AB (Bernal) stacked BLG is shown in Fig. 2.1, with 4 atoms A, B, A' and B' in each unit cell, and the inter-plane distance c.

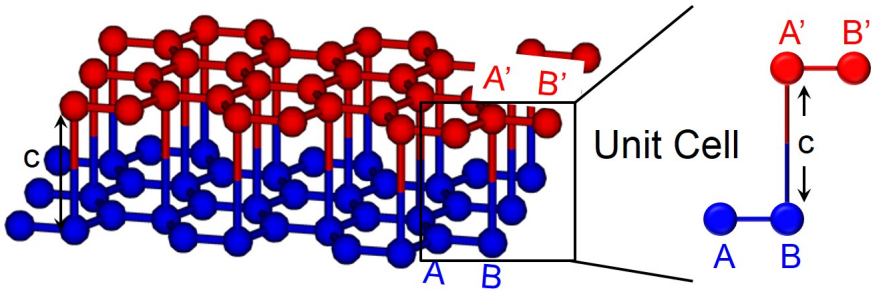


Figure 2.1. Atomic structure and unit cell of bilayer graphene

Hamiltonian is constructed based on the p_z orbital nearest-neighbor atomistic tight-binding model, which contains only in-plane and inter-plane hopping terms, γ_0 and γ_1.

$$H = \begin{pmatrix} +V & \hbar v_f k e^{i\phi(k)} & \gamma_1 & 0 \\ \hbar v_f k e^{-i\phi(k)} & +V & 0 & 0 \\ \gamma_1 & 0 & -V & \hbar v_f k e^{-i\phi(k)} \\ 0 & 0 & \hbar v_f k e^{i\phi(k)} & -V \end{pmatrix}$$

$\phi(k)$ equals to $\pi/6$ at Dirac point. v_f is the Fermi velocity of graphene, $1\times10^6 m/s$. This gives the inner-plane coupling γ_0.

The hopping paramters and material properties of BLG under vertical field extracted from bandstructure for the maximum band gap Eg are list in the table below.

Table 2.1.
Bilayer graphene material properties: in-plane and inter-plane hopping parameters γ_0 and γ_1, maximum bandgap Eg, electron effective mass me*, in-plane and out-plane relative dielectric constant σ_r^{in} and σ_r^{out}, inter-layer distance c.

Parameters	γ_0 (eV)	γ_1 (eV)	Eg (meV)	m_e (m_0)	σ_r^{in}	σ_r^{out}	c (nm)
Bilayer Graphene	2.75	0.3	275	0.038	3	3.3	0.335

Fig. 2.2 plots out the eigenvalues in the 2D k space of bilayer graphene. We are going to focus on the Dirac cone of bilayer graphene in the text later.

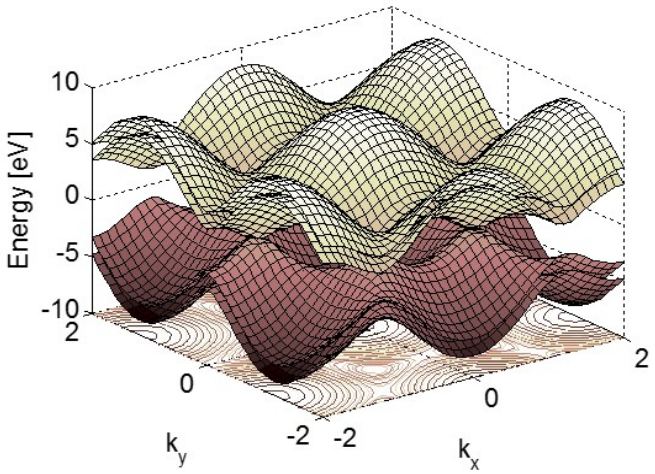


Figure 2.2. Bilayer graphene band diagram in 2D k space

2.2.1 Vertical Strain

Perpendicular strain ϵ, associated with a change from the interlayer distance c to $c' = c(1+\epsilon)$, is applied to bilayer graphene. The atomic structure change and unit cell is shown in Fig. 2.3.

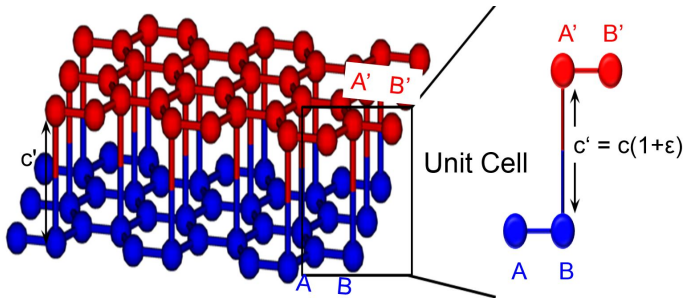


Figure 2.3. Bandgap of bilayer graphene changing with a vertical electric field. The bandgap increases with an increasing field up to a saturation point.

The associated change is in included in the Hamiltonian below:

$$H = \begin{pmatrix} +V + c\frac{\partial V}{\partial c}\epsilon & \hbar v_f k e^{i\phi(k)} & \gamma_1 + c\frac{\partial \gamma_1}{\partial c}\epsilon & 0 \\ \hbar v_f k e^{-i\phi(k)} & +V & 0 & 0 \\ \gamma_1 + c\frac{\partial \gamma_1}{\partial c}\epsilon & 0 & -V + c\frac{\partial V}{\partial c}\epsilon & \hbar v_f k e^{-i\phi(k)} \\ 0 & 0 & \hbar v_f k e^{i\phi(k)} & -V \end{pmatrix}$$

The variation of hopping parameter γ_1 with interlayer distance c, $\frac{\partial \gamma_1}{\partial c}$ is estimated using Boykin's model [23]. $\frac{\partial V}{\partial c}$ is evaluated in Ref. [24]. All the other parameters can be found in 5.1.

In the Hamiltonian presented above, the change of onsite energy of different layers due to vertical electric field is presented by the constant +V and –V. In the four

atom unit cell, vertical strain breaks the symmetry of the two atoms within a layer since only one of these two atoms is connected to the other layer. Interestingly, the Hamiltonian displays a possibility of opening a strain induced band gap. Verberck et al. examined this possibility and found out that in specific conditions strain by itself can open a band gap: $|c\frac{\partial V}{\partial c}\epsilon| > \gamma_1 + c\frac{\partial \gamma_1}{\partial c}\epsilon$ [24].

2.2.2 Tunable Band Gap

The vertical strain in this section is a direct copy of ref. [9]. The rest about tunnable band gap in bilayer graphene without strain is unpublished.

Fig. 2.4 shows how the band structure of BLG changes with a vertical electric field applied between the two graphene layers. The bandgap increases linearly with the small electric fields and saturates at 300meV for high electric fields. Notice that the band edge without electric field is at K point. However, band edges moves away from K-point by increasing the field.

Fig. 2.5 presents the bandgap as a function of the displacement field. The bandgap of BLG can be adjusted from zero up to 300meV and saturates at a displacement field of 6V/nm. The average displacement field in simulation and experiment are calculated differently. In the simulation, the effect of electric field is calculated by setting constants +V and –V as the onsite energies of the top and bottom layer atoms. Average vertical displacement field, D_{av}, then equals 2V/c. c is the inter-layer distance, equals to 0.335nm here. Experimentally, the average displacement field of top and bottom gates are considered:

$$D_{av} = \frac{1}{2}[\epsilon_o x \frac{\dot{V_{TG}}}{t_{topoxide}} - \epsilon_o x \frac{\dot{V_{BG}}}{t_{botoxide}}]$$

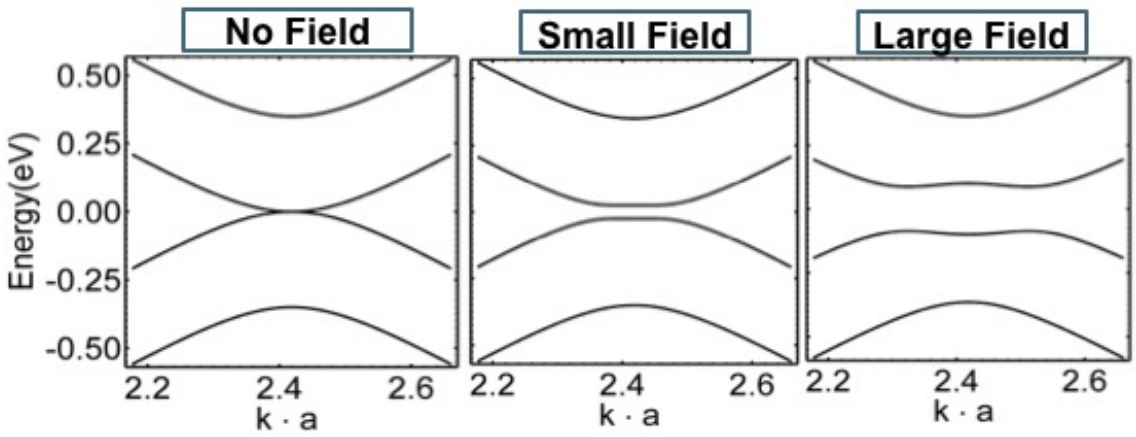


Figure 2.4. Bandgap of bilayer graphene changing with a vertical electric field from [25]. The bandgap increases with an increasing field up to a saturation point.

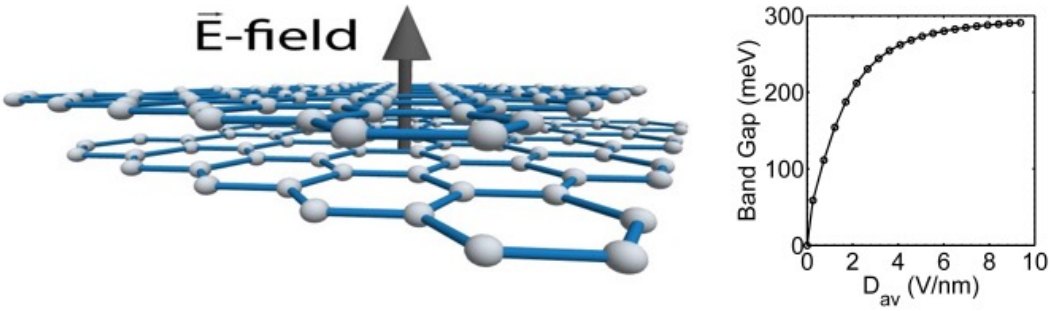


Figure 2.5. Tunable band gap in BLG as a function of the displacement field from [26].

As shown in Fig. 2.6, strain has two major impacts on the band structure of BLG. 1) Producing asymmetric conduction and valence bands. This is due to the fact that in the presence of vertical strain, the onsite energies of the in-plane carbon atoms in each layer of graphene become asymmetric. 2) Creating a larger band gap in the presence of a vertical electric field. Electric field here is evaluated using the inter

plane distance c' after straining.

Based on the band structure calculations, one can open a larger band gap by pulling apart the two layers of graphene in the existence of vertical electric field. Similar conclusion can also be found in Ref. [24].

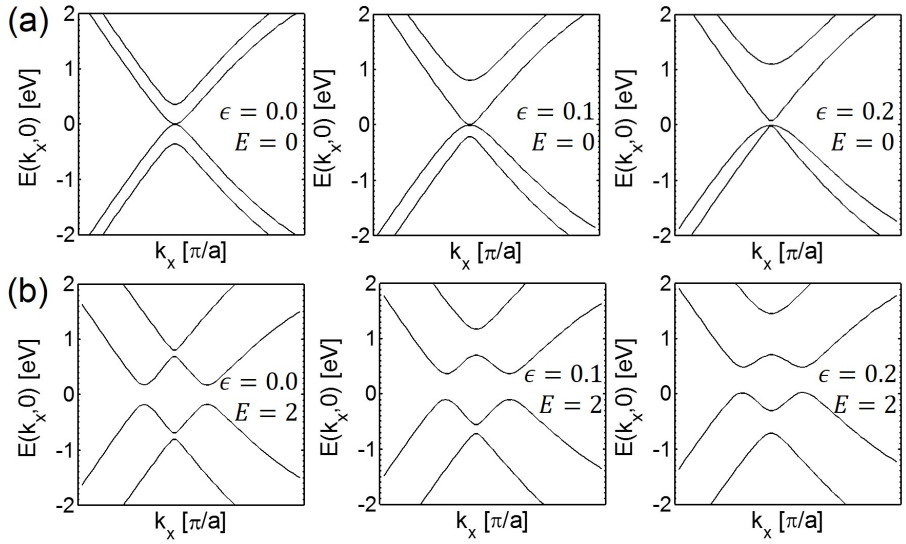


Figure 2.6. Band structure of strained bilayer graphene without (a) and with (b) vertical field [V/nm]. Left, middle and right figures correspond to band structures of bilayer graphene with different strain values.

The effect of strain and vertical field are demonstrated in Fig. 2.7 more clearly. Fig. 2.7a shows that the application of strain can increase the band gap when the vertical field is higher than 0.4V/nm. Moreover, the impact of strain is more significant in the higher vertical field values. Fig. 2.7b shows the band gap as a function of vertical field for different strain values; higher the strain, larger the maximum value of the band gap. This effect indicates that with a vertical strain, it is possible to achieve a higher ON/OFF ratio in bilayer graphene transistors.

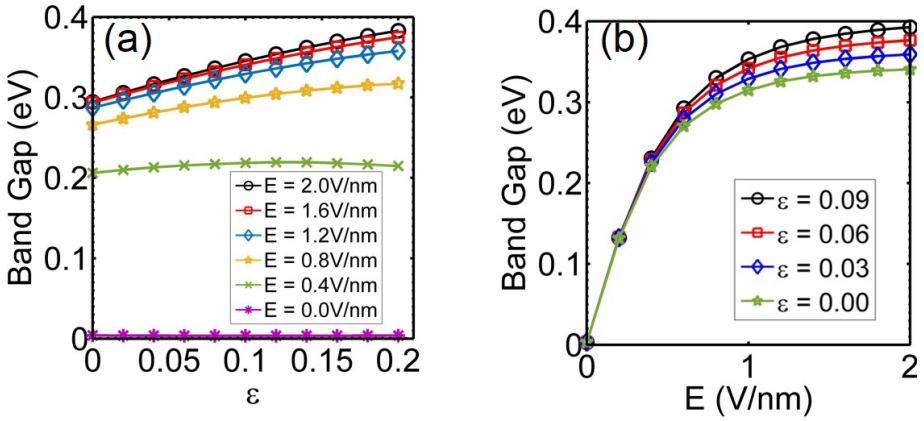


Figure 2.7. (a) Band gap changes with strain applied in different vertical fields E[V/nm]. (b) Band gap increases with vertical field. Saturation band gap increases with larger strain.

2.2.3 Transport

Bilayer graphene FETs have been simulated using the self-consistent Poisson-Non-Equilibrium Green's Function (NEGF) method in our Nano-Electronic MOdeling (NEMO5) tool [13-15].

If not stated otherwise, all the transport results are for the double gate bilayer graphene device structure demonstrated as Fig. 2.8.

Fig. 2.9 shows the transmission results from NEGF and the corresponding band structures. Two scenarios are presented: 1) Without an electric field, the transmission through the zero bandgap BLG is finite. 2) In contrast, a bandgap opens up with an electric field of 1V/nm and results in zero transmission through the bandgap. This verifies the formation of a transport gap besides the optical gap in BLG under vertical field.

Fig. 2.10 shows the transfer characteristics of BLG FET at temperature of 300 K obtained from Poisson-NEGF method. V_{DS} is 10mV, and the Fermi level is fixed

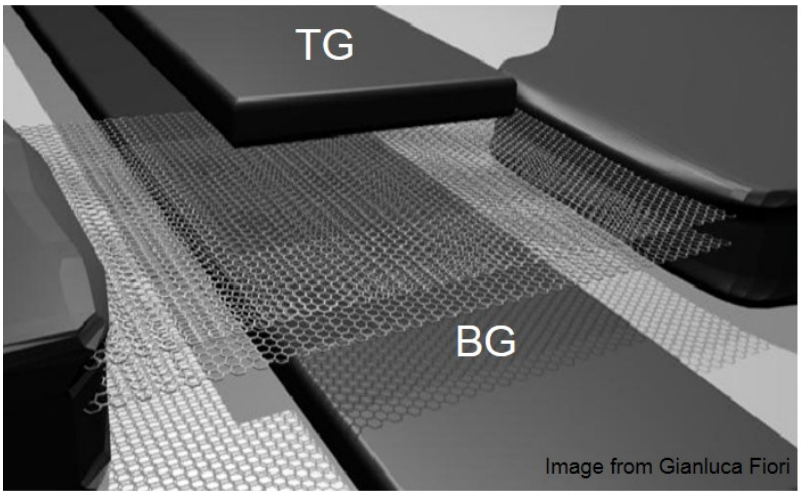


Figure 2.8. Double layer device structure with one top gate and one bottom gate.

to 0eV. The back gate voltage V_{BG} is set to 2V. Despite the band gap increasing with the top gate voltage (V_{TG}), the device is ON, then OFF, and ON again (marked as 1, 2 and 3 respectively) with the sweeping of top gate and generates a V shaped I-V characteristic. From the potential energy at top and bottom graphene layers, extracted from self-consistent simulations, one can calculate the conduction and valence band edges which are called "local band structure" here. "Local band structure" is plotted in Fig. 2.10 by extracting the band edges for each unit cell. Not only does an increase in the top gate bias pull down the band edges in the channel, but it also increases the bandgap. Despite this monotonic increase in the bandgap, the OFF state occurs when the middle of the bandgap aligns with the Fermi level (shown as (2) in Fig. 2.10). Further increase in V_{TG} and consequently the band gap does not decrease the current since the band gap is not blocking the thermal window (shown as (3) in Fig. 2.10).

Graphene transistor usually has an ON/OFF ratio of 10, it is clear that, having the tunable band gap effect can increase the device ON/OFF ratio from 10 to 100. The larger the effective bandgap in the OFF state, the smaller the OFF current. Since the bandgap is controlled by both the top and the bottom gates, the change of back gate voltage (V_{BG}), also affects the top gate voltage (V_{TG}) needed to align with

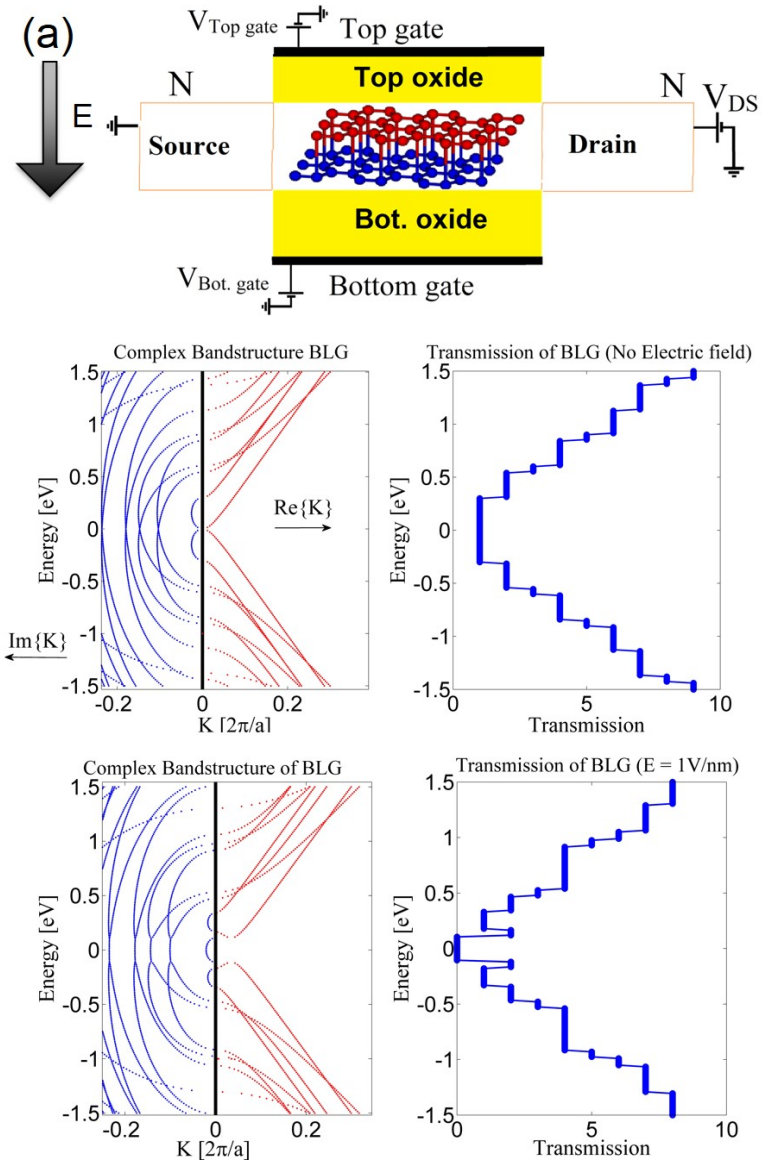


Figure 2.9. (a): Bilayer graphene FET device and atomic structure. Bandgap and transmission for a BLG device in a small (b) and large (c) electric field.

the Fermi level. Thus, V_{BG} would cause a shift of the valley of the V shaped IV as shown in Fig. 2.11(a).

Fig. 2.11(b) shows the transfer characteristics of a double gated bilayer graphene transistor. The devices with higher applied strain can achieve a higher ON/OFF

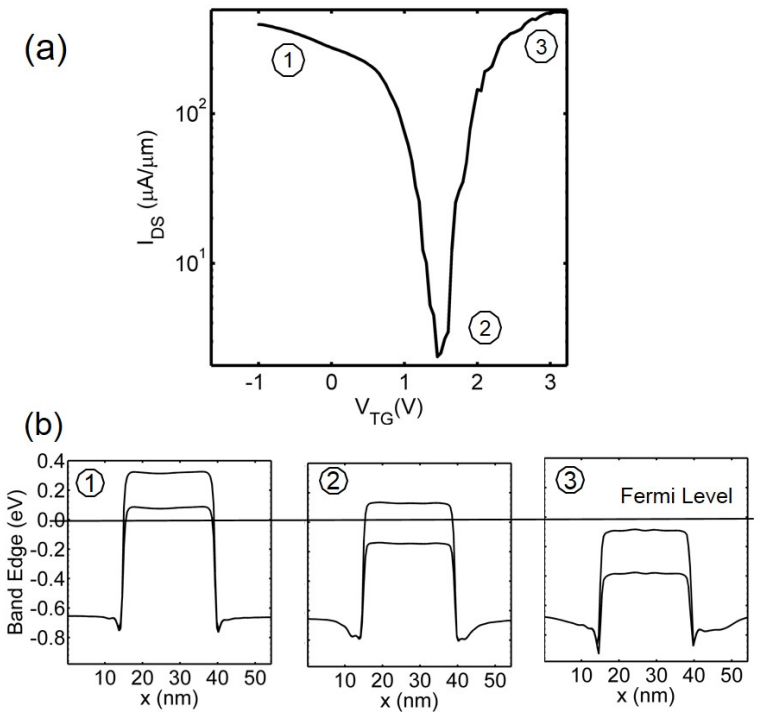
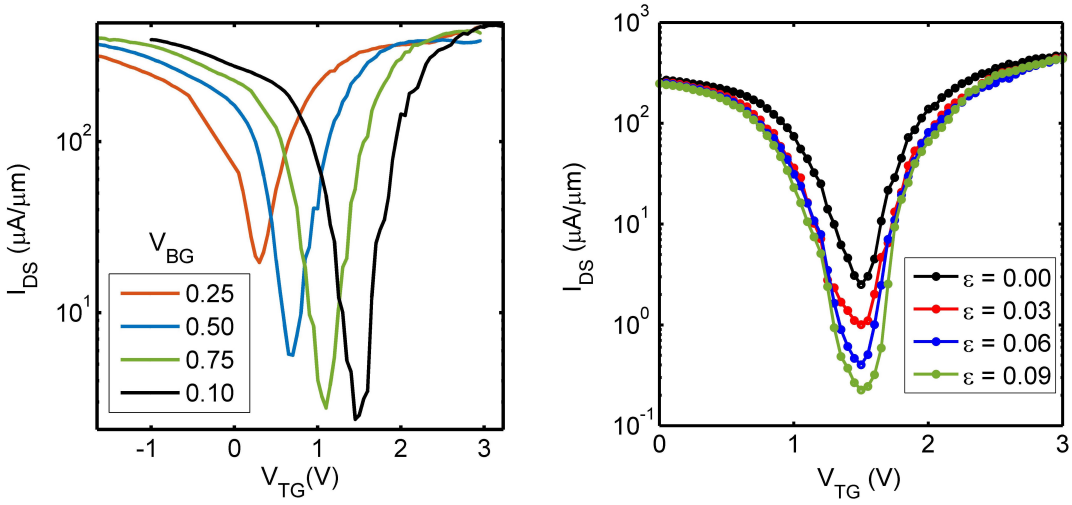


Figure 2.10. (a): V shaped transfer characteristics of bilayer graphene double gate FET. (b): band edge plot along transport direction for the ON, OFF and ON state.

ratio. A 9 percent strain leads to ON/OFF ratio of 10^3, compared to 10^2 without strain. Notice that the strain mainly reduces the OFF current and keeps ON current intact since the strain impacts the band gap.

2.3 Bilayer Graphene p-n tunneling junction

It has been experimentally challenging to realize a tunnel FET (TFET) with high on-current and a steep subthreshold slope simultaneously, especially with a low supply voltage (V_{DD} about 10mV).



(a) (b)

Figure 2.11. (a) A shift in the valley of the V shaped transfer characteristics due to the change of bottom gate voltage V_{BG}.(b) IV curves for double gate bilayer graphene devices applied with different vertical strain.

The high current can be achieved by bringing the transmission probability through the source-channel tunneling barrier close to unity, which can be achieved by bringing the effective mass of the channel material and the screening length across the tunnel barrier [27, 28]. Regarding the requirement of small effective mass, bilayer graphene (BLG) is almost an ideal candidate. However, despite its small effective mass, impressive mobility and initial promise for high performance electronic devices [29, 30], a lack of intrinsic bandgap prevents graphene transistors from switching off.

Although sizeable bandgaps were demonstrated in graphene nano-ribbons (GNRs) [31–33], the edge roughness and device-to-device variations due to the lack of atomic level control in top fabrication pose a tremendous challenge for technology development [33–36].

On the other hand, BLG can have a tunable bandgap larger than 200meV created by an electric field [37,38]. BLG hetero-structures can thus be artificially created by applying different effective electric fields at different regions [21,39,40]. Avoiding edge roughness effects, BLG appears to be a better TFET channel material than GNRs.

Single layer and BLG p-n junction devices with one local top gate have been demonstrated [41, 42]. Without a bandgap in the single layer graphene or un-gated bilayer region, this so-called p-n junction relies on local gate control of carrier type and density. A BLG p-n junction is fabricated which has two top gates with an extremely scaled gap of 20nm in-between together with the global bottom gate. By applying different gate voltages on the two top gates (V_{TG1} and V_{TG2}), a BLG p-n junction with electrically induced band gap is created.

Experimentally, the current of this BLG p-n junction is demonstrated to have a non-linear behavior with V_{TG1}. This non-linear behavior is shown to be consistent at various V_{TG2}. Simulation results of Id-V_{TG1} at different V_{TG2} values are first demonstrated to be able to catch the experimental trend. Detailed simulation density of states (DOS) plots are then presented to show this non-linear current behavior is the result of tunnel current changing with the tunnel length. Simulation effort is also demonstrated in showing a BLG p-n junction with small SS should have separate back gates.

To conclude, an experimental observation of tunnel current in this BLG p-n junction with electrically induced band gap is reported here. In order to have a small SS device, back gates should be separated in each region of the p-n junction.

2.3.1 Device Fabrication

Fig. 2.12 shows the device configuration we investigate. It consisted of BLG channel sandwiched between bottom and top gates. BLG channel is defined as 100nm ribbon structure to suppress the percolation current [38]. 20nm HSQ (one type of SiO2) bar with height of 80nm electrically isolated the two top gates and can stand a voltage difference up to 5V. The fabrication process of our devices is similar to what has been described earlier [43].

The BLG is micromechanically cleaved from natural graphite on 90nm SiO2 substrate. The layer number is first identified by optical contrast and then verified by AFM and Raman [44]. Contact electrodes are made by e-beam lithography and e-beam evaporated Ti/Pd/Au metal stack (1nm/20nm/30nm). The top-gate oxide is 10nm HfO2 by ALD. Afterwards, one more e-beam lithography step is to define the 20nm HSQ bar. Then a Ti/Au metal (5nm/15nm) stack is e-beam evaporated perpendicularly onto the sample.

2.3.2 One Gate Measurement

Conventional measurements using one single top gate, either top gate 1 or top gate 2, as shown in Fig. 2.13a. Fig. 2.13b shows the $I_D V_{TG}$ transfer characteristics with back gate as a constant potential at 77K for conventional measurement. The on/off ratio of $I_D V_{TG}$ at V_{BG} =-70V(Dav 3.1V/nm) is 300 at 77K and the activated gap size is 50meV smaller compared with the bandgap extracted from optical measurements

As reported previously [45], transport in band gap is dominated by hopping, and there existed numerous inter-band states induced by disorder. These inter-band states also provide a feasible path for direct tunneling of band gap. The mean free path

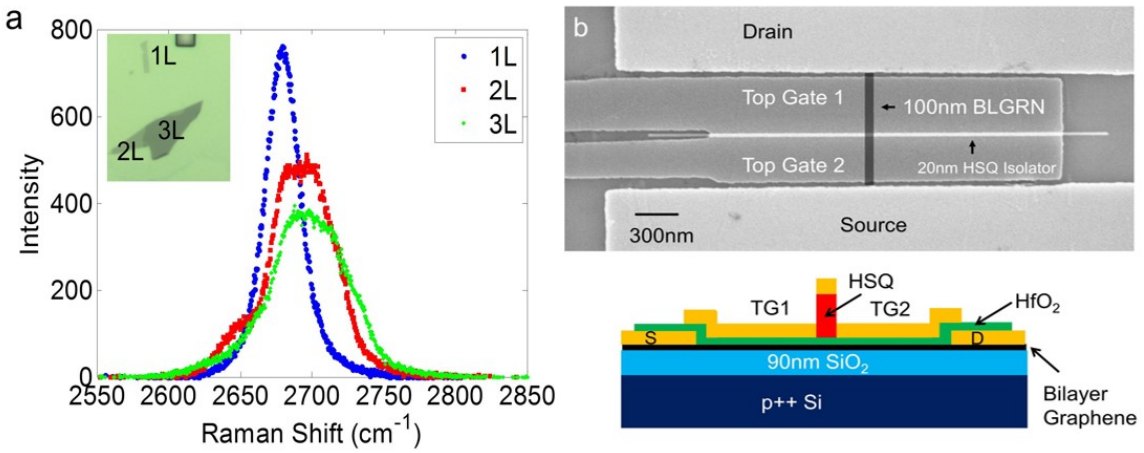


Figure 2.12. Bandgap of bilayer graphene changing with a vertical electric field. The bandgap increases with an increasing field up to a saturation point.

in the bulk of the channel, mean free path $lm > 100nm$, was extracted from the relationship between conductivity and momentum. As lm is smaller than the gap region between the two gates, we expect a significant portion of ballistic transport in the gap region. Without much scattering, the conductance is mainly determined by the tunneling transmission probability trough the energy barrier and the density of state (DOS) of the BLG p-n junction.

In absence of gating, the pristine electronic structure of BLG near the Fermi level features conduction bands above touch valence bands below. The bandgap is zero. Upon electrical gating perpendicular to the channel, a bandgap can be introduced and continuously tuned.

$I_D V_{TG}$ curve swept by top gate 1 are almost identical to that of top gate 2. This indicates the unintentional chemical doping of graphene channel regions under top gate 1 and 2 are uniform and the device hysteresis is small. With VBG changing

from 0V to -70V, the $I_D V_{TG}$ curves shift from negative to positive top gate voltages with increasing p-type (hole) currents. In addition to this electrostatic effect, average electric field Dav becomes larger when the top and back gate voltage difference increases, resulting in a continuous decrease of the device off-currents. The slightly asymmetry in the current levels of n and p branch is likely associated with the P/N junction induced by the contact metal. In the interface between graphene and Pd metal contact, there is a p-p junction for hole branch and p-n junction for electron branch [46].

Note there are several plateau features appearing in the measured IV curves and become apparent for the large Dav. And these plateaus are observed mainly in the electron branches with nearly equal spacing. This is probably due to the formation of 1D sub-bands in graphene ribbon [47]. The bandgap significantly reduces the off-state current and makes the plateau features more pronounced. In contrast to the single layer graphene ribbon, in which the plateau features are symmetric in both electron and hole branches, they are asymmetric for BLG ribbon. This asymmetry can be understood by the distinct electronic structure of BLG, especially under a large vertical electrical field or a disorder enhanced interlayer screening [47] associated with a three dimensional structure of BLG [48].

2.3.3 Two gates Measurement

Transport of BLG p-n junction is studied by tuning two top gates, fixing the bottom gate. The measurement configuration is described as following: The bottom gate voltage is constantly -70V and by combining with a top gate voltage, a band gap is expected to be open in both side of p-n junction. The voltages of TG1 region near the source contact are set as a constant for every single I_D-V_{TG2} curve and vary from -1.8V to 1V with a step of 0.2V.

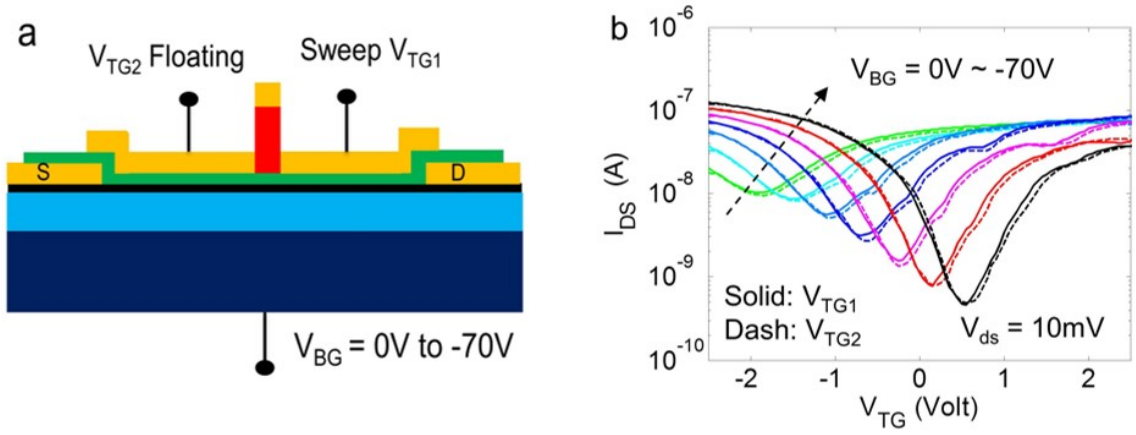


Figure 2.13. Bilayer Graphene PN junction one gate measurement

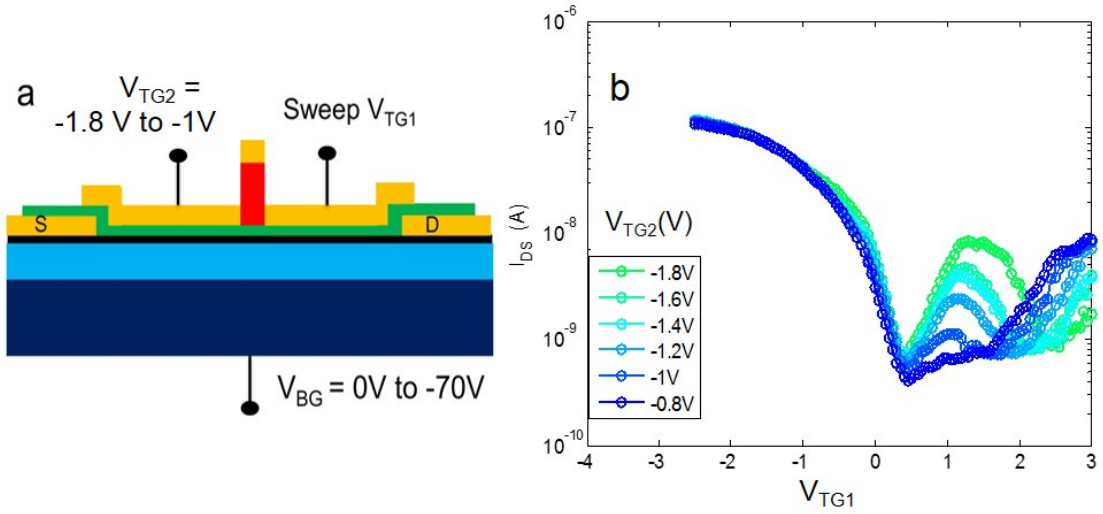


Figure 2.14. Bilayer graphene PN junction two gate measurement

2.4 Simulation Work of BLG p-n junction

2.4.1 Simulation of p-n junction two gate measurement

Electrically doped p-i-n BLG structure used in simulation shown in Fig. 2.15. Oxide thickness are all scaled down to 10 nm. EOT are kept the same if the thickness

is changed from experimental setup. Middle region is of 20nm to be consistent with experiment. Right and left region are scaled from 1um to 20nm since 20nm is the enough to block direct tunneling.

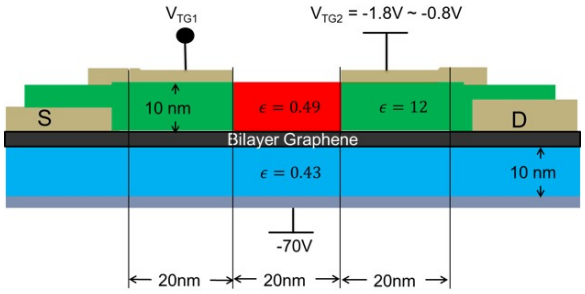


Figure 2.15. Electrically doped BLG PN junction structure used in simulation.

Fig. 2.16 shows $I - V$ characteristics of electrically doped BLG PN junction for different V_{TG2}. Each curve differs from previous one by $0.2V$.

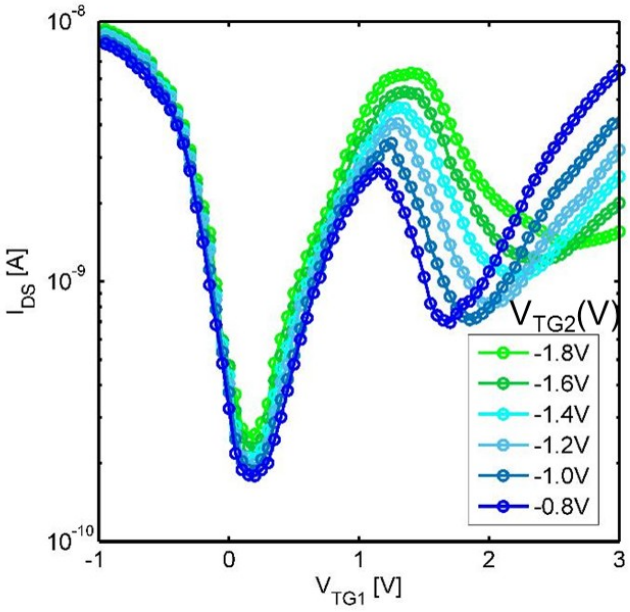


Figure 2.16. I-V characteristics of electrically doped BLG PN junction for different V_{TG2}. Each curve differs from previous one by 0.2V

2.4.2 Density of States and Explanation

Firstly, the IV results from simulation (Fig. 2.16) is shown to be in agreement with experiments (Fig. 2.14), two valleys are observed from Id-Vg when sweeping V_{TG1} and keeping V_{TG2} constant.

Fermi level has been kept at 0eV, Vds equals to 10 meV. Temperature is 77K. A fermi window from -0.1eV to 0.1eV is sufficient for quantum transport. Density of states (DOS) plot with energy resolved current aligned at five different V_{TG1} points are illustrated in Fig. 2.17(a). From DOS plots, inside the Fermi window, the role change of TG1 and HSQ from a quantum well to a tunnel barrier in different periods (1-5 as marked in Fig. 2.17(a) are the reason this non-linear behavior in Id-Vg. Details for 1-5 periods are in Fig. 2.17(b)-(f).
Within the Fermi window, the situations for different periods are as illustrated in Fig. 2.17(b)-(f):
(1) - (3): TG1 area is a simple double gate device with the sweep of V_{TG1}.
(3) - (4): Middle HSQ region is pulled down by V_{TG1}. It changes from a quantum well to tunnel barrier. Total current drops due to the blocking of this region.
(4) - (5): Tunnel barrier width of HSQ region decreases. This results in an increase in current.

In summary, with the sweeping of V_{TG1}, TG1 becomes a tunnel barrier and later HSQ. The two distinct valleys (2) and (4) are the results of a tunnel barrier from TG1 and middle HSQ respectively. The amplitude of each valley is determined by the length of tunnel barrier length in total. When the HSQ region became as a tunnel barrier, the barrier length is shorter than TG1 barrier. This is why the amplitude of second valley is smaller.

Secondly, in consistent with experimental measurements. As the $|V_{TG2}|$ goes smaller, both local maximum (3) and second minimum (4) happen at a smaller V_{TG1}

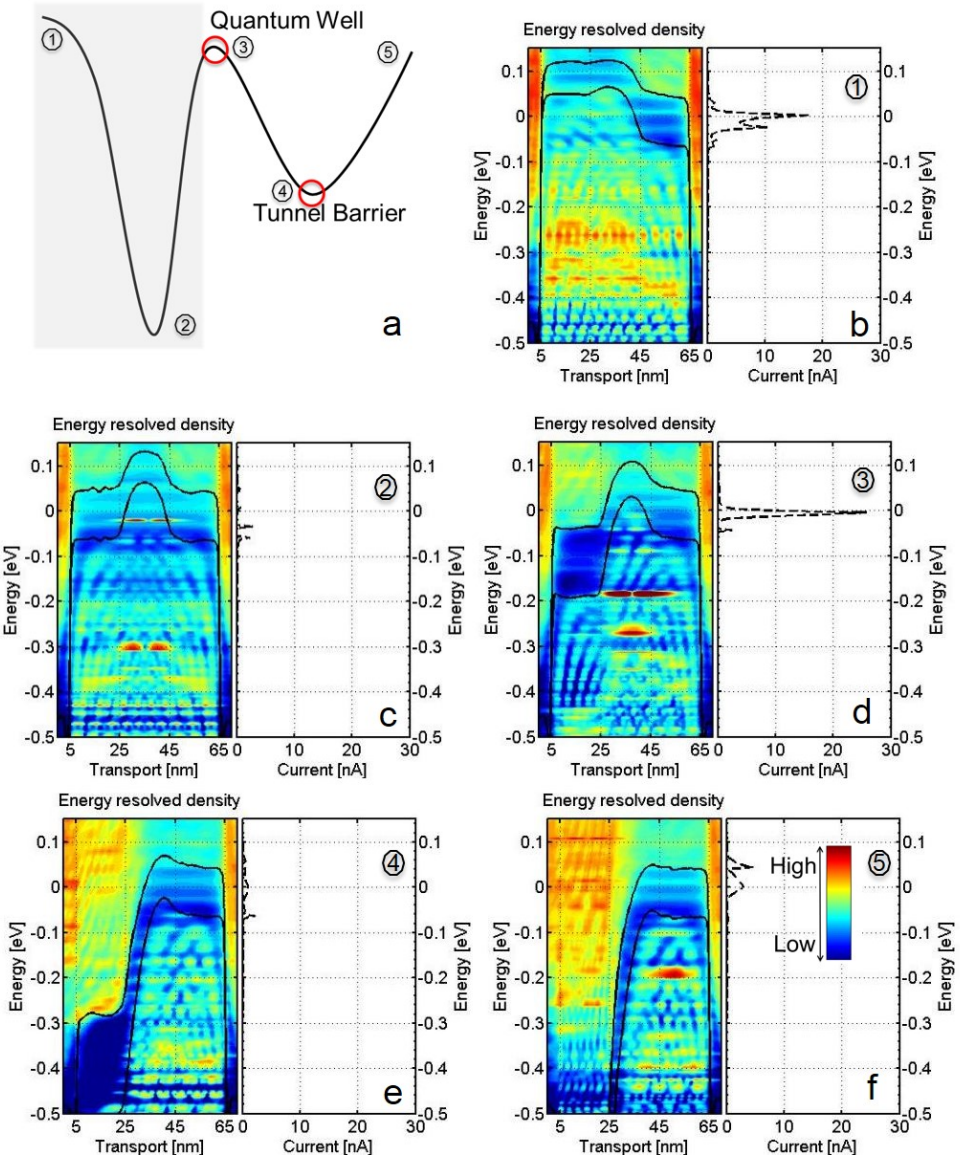


Figure 2.17. Density of states (DOS) plot with energy resolved current aligned at four different V_{TG1} for a fixed V_{TG2} value.

value with a smaller current.

Fig. 2.18 shows with a decreasing $|V_{TG2}|$, the electrostatic potential of region TG2 is pulled down. Thus it severs as a stronger confinement for HSQ quantum well. For the middle HSQ quantum well right region, TG2 forms a stronger confinement. In

this way, the confinement needed on the left side is comparably smaller for confining the same level state. This is why (3) and (4) happens at a smaller V_{TG1} value. With a smaller V_{TG1} value, the density of states that aligned with fermi level is smaller. This causes (3) and (4) to have a smaller current. This is shown in Fig. 2.18b-c.

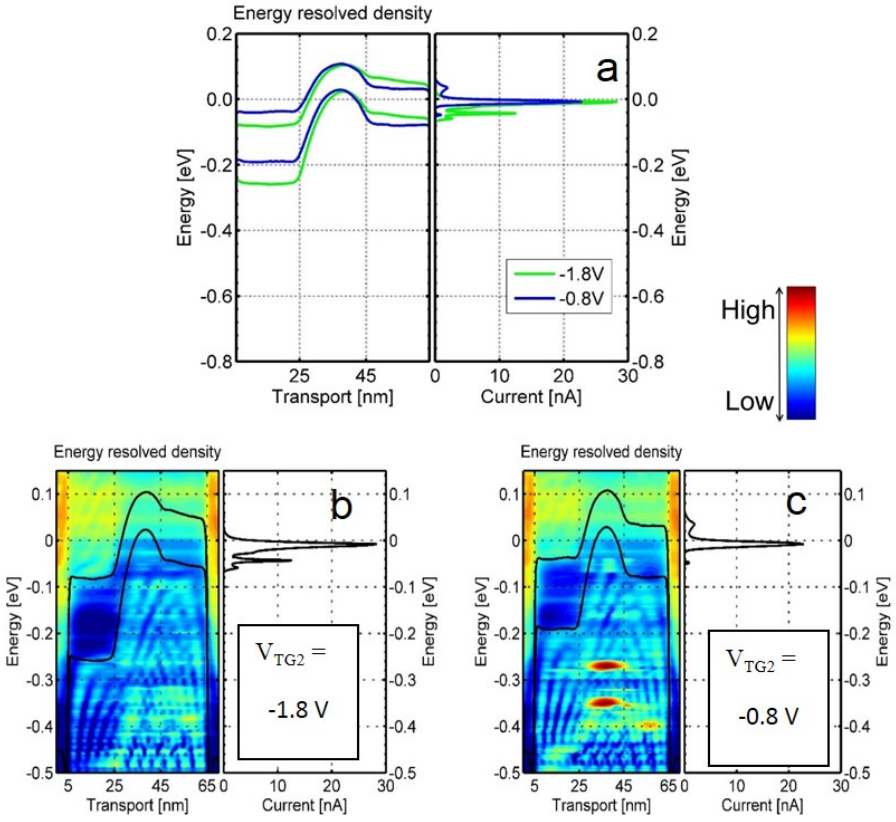


Figure 2.18. (a) A comparison of potential profiles and current for two different V_{TG2} values. (b, c) Density of states (DOS) plot with energy resolved current aligned at local maximum (3) at these two different V_{TG2} values

2.4.3 Towards Steep Slope

We proved an observation of tunnel current in BLG PN junction device. Our goal is to achieve steep slope devices. What is the key element here that prevents us to get steep slope? In this section, we show to achieve steep slope, a single gate structure

should be avoided.

BLG PN junction structure shown in Fig. 2.19a, we separate the single back gate by putting a low EOT oxide in between the two bottom gates. By carefully adjusting the voltages applied on each gate, steep slope can be achieved as shown in Fig. 2.19b.

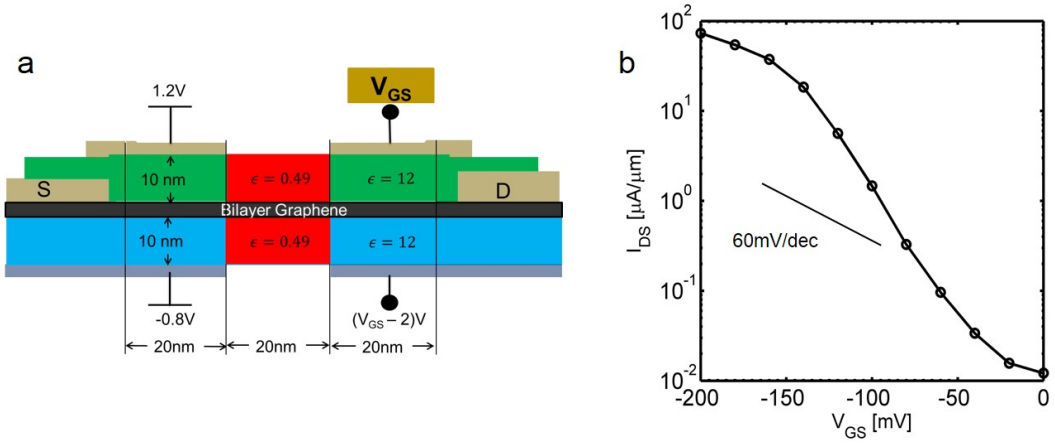


Figure 2.19. BLG PN junction with steep slope.

In Fig. 2.20, we show the band diagram and energy resolved current for both ON and OFF states of a carefully designed steep slope PN junction. The band of P and N regions aligned around Fermi level and formed a large effect barrier that blocks thermal current at OFF state. In the ON state, a gap opens in between the bands from P and N region, allowing a tunnel current to go through.

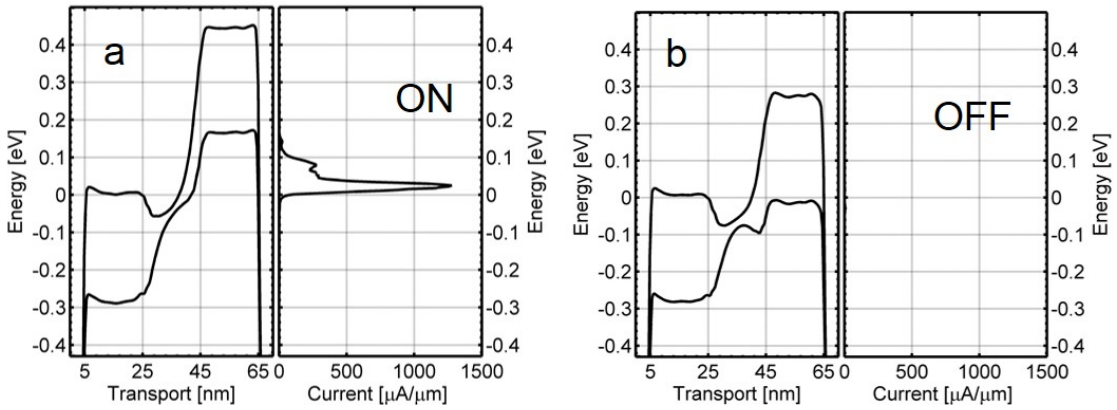


Figure 2.20. Energy resolved current aligned with band diagram at the ON and OFF of BLG PN junction with steep slope.

2.5 High Performance Bilayer Graphene Electrostatically Doped -Tunnel FET device

This section is a modified version of ref. [11]. In this section, a bilayer graphene based electrostatically doped tunnel field-effect transistor (BED-TFET) is proposed. Unlike graphene nanoribbon TFETs in which the edge states deteriorate the OFF-state performance, BED-TFETs operate based on bandgaps induced by vertical electric fields in the source, channel, and drain regions without any chemical doping. The performance of the transistor is evaluated by self-consistent quantum transport simulations. This device has several advantages: 1) ultra-low power (V_{DD}=0.1V), 2) high performance ($I_{ON}/I_{OFF} > 10^4$), 3) steep subthreshold swing ($SS < 10mv/dec$), and 4) electrically configurable between N-TFET and P-TFET post fabrication. The operation principle of the BED-TFET and its performance sensitivity to the device design parameters are presented.

Here, BED-TFET as a high performance steep SS device which enables V_{DD} to scale down below 0.1V is proposed. Accordingly, an excellent energy-delay product is

obtained in this device. Compared to previous bilayer graphene TFET designs [21,40], BED-TFET has the following advantages: 1) Being electrostatically configurable post fabrication between a P-TFET and a N-TFET. 2) Avoiding the experimentally challenging chemical doping in 2D materials (i.e. bilayer graphene). 3) Being immune to threshold variations due to dopant fluctuations which is critical for low threshold voltages. 4) Avoiding dopant states within the bandgap which deteriorates the OFF-state performance of the TFETs [49]. 5) Providing an artificial heterostructure without interface states.

The device structure is shown in Fig. 2.21(a). The left and right regions are con-

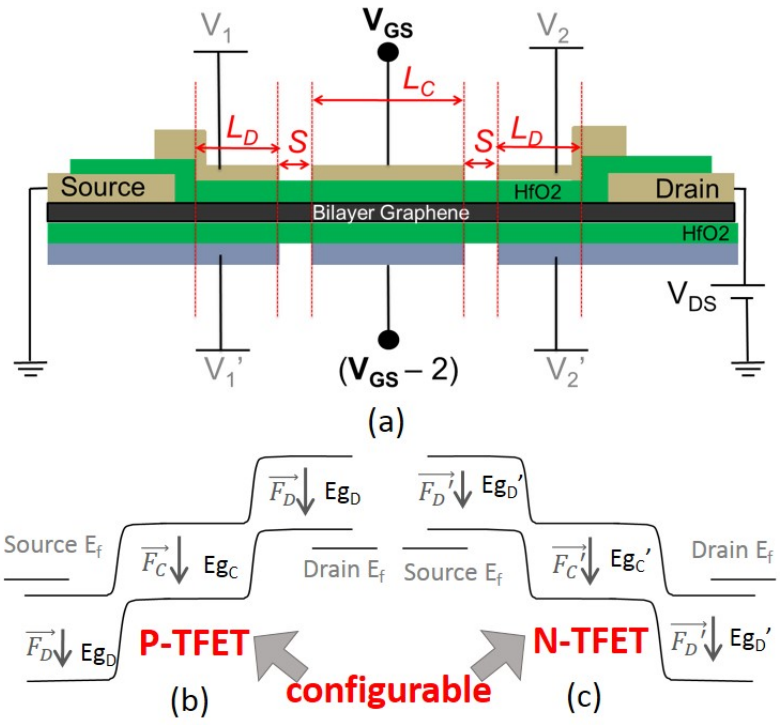


Figure 2.21. a) Physical structure of an electrically doped p-i-n BLG TFET. The band diagram in the OFF state of BED-TFET as a b) N-TFET, c) P-TFET.

trolled by $V_1, V_1\prime$ and $V_2, V_2\prime$, respectively, and act as the electrostatically doped source and drain regions for the TFET. By adjusting $V_1 \cdots V_2\prime$, the proposed device is configurable between an N-TFET and a P-TFET as shown in Fig. 2.21(b) and Fig. 2.21(c).

The bandgap size of each region is also tunable by the voltage difference (δV) between the top and the bottom gates in that region. The induced band gaps are denoted by Eg_C and Eg_D. Accordingly, an artificial heterostructure can be made as long as the electric fields of different regions are different, ($F_D \neq F_C$). Advanced workfunction engineering techniques [50] may be used to reduce the number of gates, however, a detailed investigation of such technique are beyond the scope of this thesis.

2.5.1 Energy Delay comparison

One of the main advantages of the BED-TFET is its very low energy-delay product. Fig. 2.22 benchmarks the energy-delay of a 32 bit adder [51] based on different steep devices. The benchmarking methodology is described in [51] for beyond-CMOS devices. The BED-TFET has the least energy-delay product among the studied devices. This is due to the steep IV and high ION obtained in the BED-TFET even with a low V_{DD} of 0.1V. This shows the importance of low band gap materials for low V_{DD} steep devices. Notice that the parasitic capacitances between the gates can be significantly reduced by using a low-k dielectric ϵ_s between the gates [52] and increasing the spacing (S); e.g. a 10nm air gap spacer can reduce parasitic capacitances about 2 orders of magnitude smaller than gate capacitance ($\epsilon_s/S \ll \epsilon_{ox}/t_{ox}$).

2.5.2 Device Operation

The BED-TFET shown in Fig. 2.21(a) is composed of a bilayer graphene layer sandwiched between two layers of 3nm thick HfO2 with a relative dielectric constant of $\epsilon_r = 20$. The maximum field within HfO2 in current BED-TFET design is about 3MV/cm which is less than the breakdown field of HfO2 (8.5MV/cm) [58]. The three gated regions from left to right have lengths of 25, 40 and 25 nm. δV in the middle region is fixed to 2V to reach the maximum bandgap (i.e. 275meV in BLG).

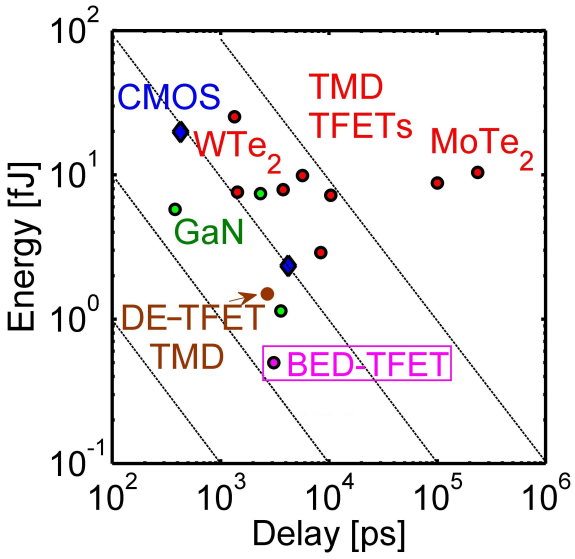


Figure 2.22. Energy-Delay comparison of BED-TFET (pink dot) with Dielectric Engineered (DE) WTe2 TFET (brown dot) [52], Nitride TFET (green dots) [53], TMD TFETs (red dots) [54–56] and Si MOSFET (blue dots) [51, 57]

Notice that, $V_1 \ldots V_2'$ are fixed throughout the device operation to achieve the desired electrostatically doping. Only the gate voltages in the middle region are swept to switch the device between ON and OFF.

All the results here are for BED-TFET with P-FET configuration in Fig. 2.21(b); V_1, V_1' and V_2, V_2' are fixed at 1.1V, -0.1V and 0.4V, -0.8V respectively to form the electrostatically doped source and drain regions.

Fig. 2.23 shows the local band diagram along the transport direction (left) and energy resolved current for the ON-state (right) of the device. There is a tunnel window of about 210 meV in the ON-state. Due to the small band gap at the tunnel junction, the ON-current is high. In the OFF-state, the middle region blocks the tunneling window as shown in Fig. 2.23(b). Consequently, the OFF-current is mainly the result of the thermionic electron and hole currents. The electrically induced band

gaps at the source and drain regions in conjunction with the band gap of the channel make an effective barrier height of about 350meV which is large enough to reduce the thermal current at 300K to the desired range.

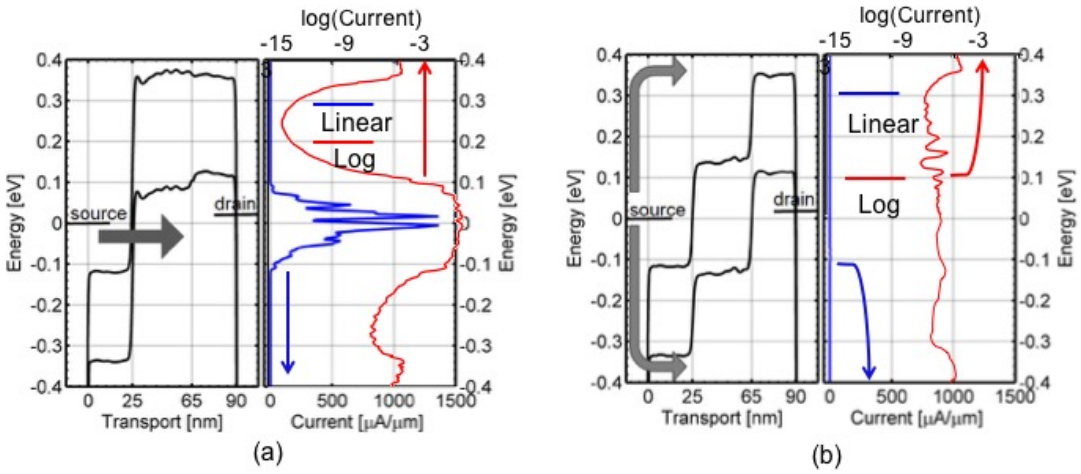


Figure 2.23. The band diagram along the transport direction (left) and the energy resolved current (right) in (a) ON state and (b) OFF state.

2.5.3 IV performance

Fig. 2.24(a) shows the transfer characteristics of the BED-TFET for different V_{DS} values. Increasing $|V_{DS}|$ from 10mV to 100mV increases both the ON and OFF currents. Fig. 2.24(b) shows that this device achieves a small SS value of $8mV/dec$ and high I60 (the current value where SS becomes $60mV/dec$) value of $24\mu A/\mu m$ for a V_{DS} of -100mV. Notice that this value of I60 is much higher than that of other 2D material TFETs even with a V_{DD} of 0.5V [21]. Notice that increasing $|V_{DS}|$ from 10mV to 100mV does not deteriorate the small SS. Fig. 2.24(c) plots the output characteristics of the device. ID-V_{DS} curves show that there is no late turn on problem in BED-TFET and the linear region of ID-V_{DS} starts from V_{DS}=0V. Moreover, the current

saturates for $|V_{DS}|$ values above 50mV. Fig. 2.24(d) shows that an increase in $|V_{DS}|$ decreases the ON/OFF ratio from 5×10^4 at V_{DS}=-10mV to 2×10^4 at V_{DS}=-100mV, which is not substantial.

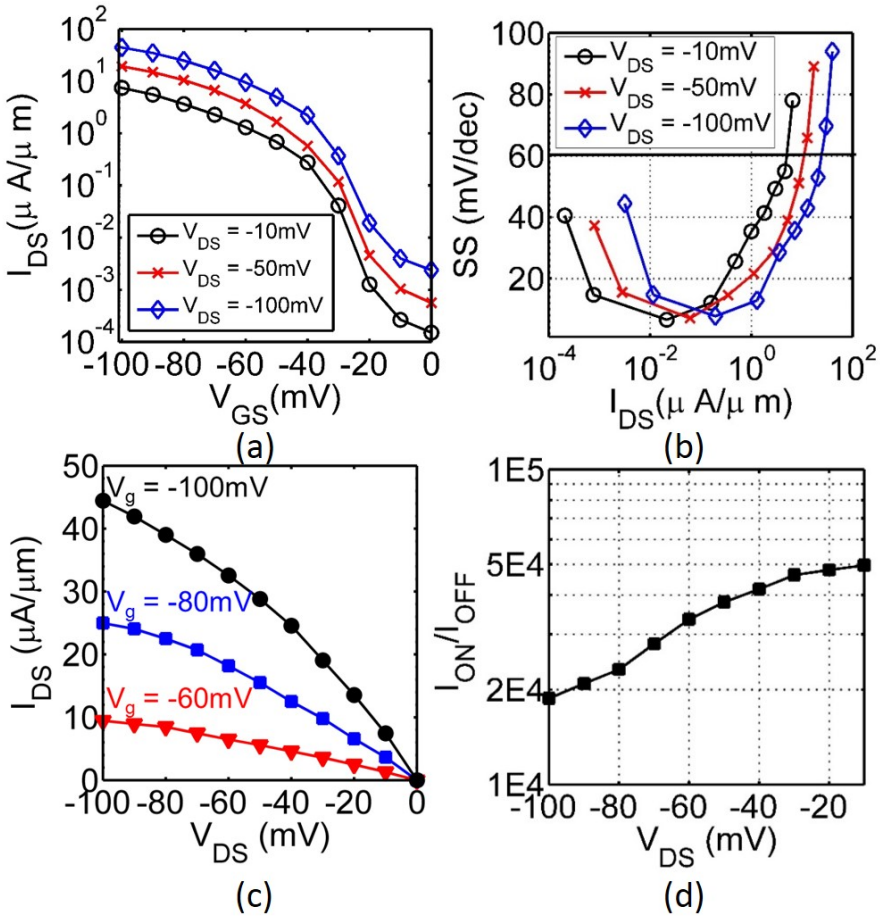


Figure 2.24. a) Transfer characteristics of the BED-TFET with different drain-to-source voltages V_{DS}. b) SS-Id plot with different drain-to-source voltages V_{DS}. c) Output characteristics of the TFET at several gate voltages Vg. d) ON/OFF ratio with source-drain voltage V_{DS} for the BED-TFET. L_C, L_D and S are kept at 40nm, 25nm and 0nm, respectively.

2.5.4 Geometry Sensitivity

In the BED-TFET, several design parameters are identified to be critical for the device performance and fabrication: 1) the channel length L_C, 2) the length of the electrostatically doped source and drain regions L_D, and 3) the spacing between these gated regions S. In the transfer characteristics demonstrated in Figs. 2.25 a-c, L_C, L_D and S are kept at 40nm, 25nm and 0nm respectively, unless mentioned otherwise. Fig. 6(a) shows that reducing L_C to 40nm increases the OFF-current. Below, the performance is not sensitive to S as shown in Fig. 2.25(b) for S in the range of 0nm to 20nm. Fig. 2.25(c) shows that a L_D value below 25nm can impact the OFF-state performance. The sensitivity to L_C and L_D originates from the direct tunneling of carriers through the channel potential barrier due to the small effective mass of the BLG. The optimized channel length is longer than the ITRS requirements. Hence, to keep the footprint of the BED-TFET small a vertical structure (e.g. conventional vertical TFET structure) could be used.

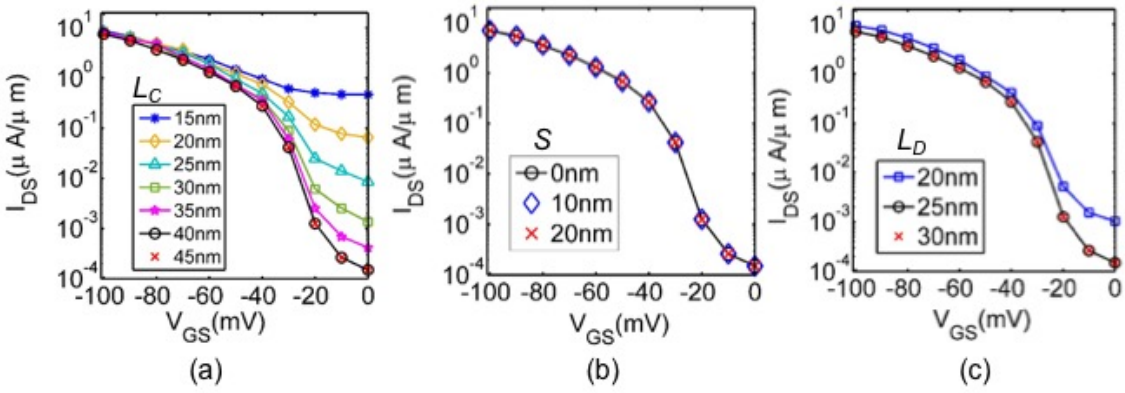


Figure 2.25. L_D, L_C and L_D are the gate length of the left/middle/right region in Fig. 1(a) (doping region/channel/doping region), respectively. The spacing between the gates is S. Transfer characteristics of the TFET with different a) channel length L_C (L_D = 25nm, S=0nm), b) spacing S (L_C = 40nm, L_D =25nm) and c) doping region length L_D (L_C = 40nm, S = 0nm).

2.6 Conclusion

The BED-TFET is proposed as a high performance, ultra-low power, steep transistor to overcome the problems associated with GNRs. The electrically tunable band gap of BLG makes this transistor highly configurable. The performance of this device is evaluated through rigorous quantum transport simulations based on NEGF. It is shown that with the right device design, the BED-TFET can achieve ON/OFF ratios of more than 10^4, ON-current of $45\mu A/\mu m$, and a subthreshold swing around $10mV/dec$, all at a low overdrive voltage of V_{DD} =0.1V at room temperature.

Though the device can operate in a very low power, it faces the challenge of scaling. The minimal channel length 90nm to keep the device performance is too large for mordern technology.

I acknowledge the guidance and help in the BED-TFET work form Dr. Hesameddin Ilatikhameneh. The experimental work including the data and figures are from our collaboration Tao Chu from Prof. Zhihong Chen's team. Part of the work discussed in this charpter are published in [9,11]. This work was supported in part by the Center for Low Energy Systems Technology (LEAST), one of six centers of STARnet, a Semiconductor Research Corporation program sponsored by MARCO and DARPA. The use of nanoHUB.org computational resources operated by the Network for Computational Nanotechnology funded by the US National Science Foundation under grant EEC- 1227110, EEC-0228390, EEC-0634750, OCI-0438246, and OCI-0721680 is gratefully acknowledged.

3. THICKNESS ENGINEERED TUNNEL FIELD-EFFECT TRANSISTORS BASED ON PHOSPHORENE

This chapter is a modified version of ref. [12].

3.1 Introduction

A thickness engineered tunneling field-effect transistors (TE-TFET) as a high performance steep transistor is proposed in this chapter. This device exploits the property of layer thickness dependent energy bandgap (Eg). With a spatially dependent layer thickness, TE-TFET based on phosphorene naturally yields a heterojunction structure that avoids the interface states and lattice mismatch problems and in the meanwhile boosts the ON current to $1280\mu A/\mu m$ with 15nm channel length. TE-TFET shows a scalability down to 9nm with constant field scaling $E = V_{DD}/L_{ch} = 30V/nm$. With a higher ON current, it also outperforms the homo junction phosphorene TFET and the TMD TFET in energy-delay product of 32 bit adder. The operation principles and its performance sensitivity to the design parameters of TE-TFET are also investigated by full-band atomistic quantum transport simulation in this chapter.

3.2 The advantages of Thickness Engineered TFETs

Tunnel field-effect transistors (TFETs), operating based on band-to-band tunneling (BTBT) mechanism appears to be promising solution in reducing V_{DD} ever since their first experimental proof of $SS < 60mV/dec$ [47]. However, TFETs used Si as a channel material have low ON-state due to the large Eg. Smaller band gap channel

material such as Ge can improve the I_{ON} , but they also increase the I_{OFF}, thus degrades the I_{ON}/I_{OFF} ratio [59]. Improved TFET designs have been employed by using Si as channel material and small Eg as source to improve I_{ON} while keeping I_{OFF} small. Unfortunately, the large lattice mismatch [60, 61]and interface states [62–64]in between the materials prevents the formation of a high quality of hetero-junction. Natural hetero-junction can be achieved by varying the width of GNR [65]. However, the edge roughness and device-to-device variations due to the lack of atomic level control in top down fabrication pose a tremendous challenge for technology development [33, 35, 37].

On the other hand, 2D materials show a band gap size (Eg) dependence on layer thickness [66–68]. Natural hetero-junctions can be achieved by spatially varying the their layer thickness [69]. Unlike the fabrication of width dependent GNR hetero-junction, this spatially varying layer thickness can be easily achieved during these 2D material exfoliation [70, 71] . Therefore, a layer engineered TFET (TE-TFET) exploiting this spatially varying layer thickness technique is proposed in this chapter. TE-TFET is engineered to have a smaller Eg in source and the channel near source and large Eg in the rest of device. TE-TFET can be applied on any material that has a band gap dependence on layer thickness. In this chapter, phosphorene is chosen to be the channel material due to its reported high ON-current [72] and the band gap of phosphorene remains to be direct with the layer thickness [73]. TE-TFET has several advantages: (1)spatially dependent layer thickness naturally yields an hetero-junction structure, which avoids lattice mismatch and interface states problems in conventional hetero-junctions; (2) the ON-state current can be enhanced due to the small tunnel distance; (3) the OFF-state current keeps to be low due to the large Eg barrier inside the channel.

The device structure the TE-TFET based on phosphorene is demonstrated in Fig. 4.7a. The layer thickness and the length of the small band gap region inside channel is denoted by L_{ext} and T_{ext}. The device performance based on these design parameters and device scaling based on L_{ch} will be discussed in details in section III.

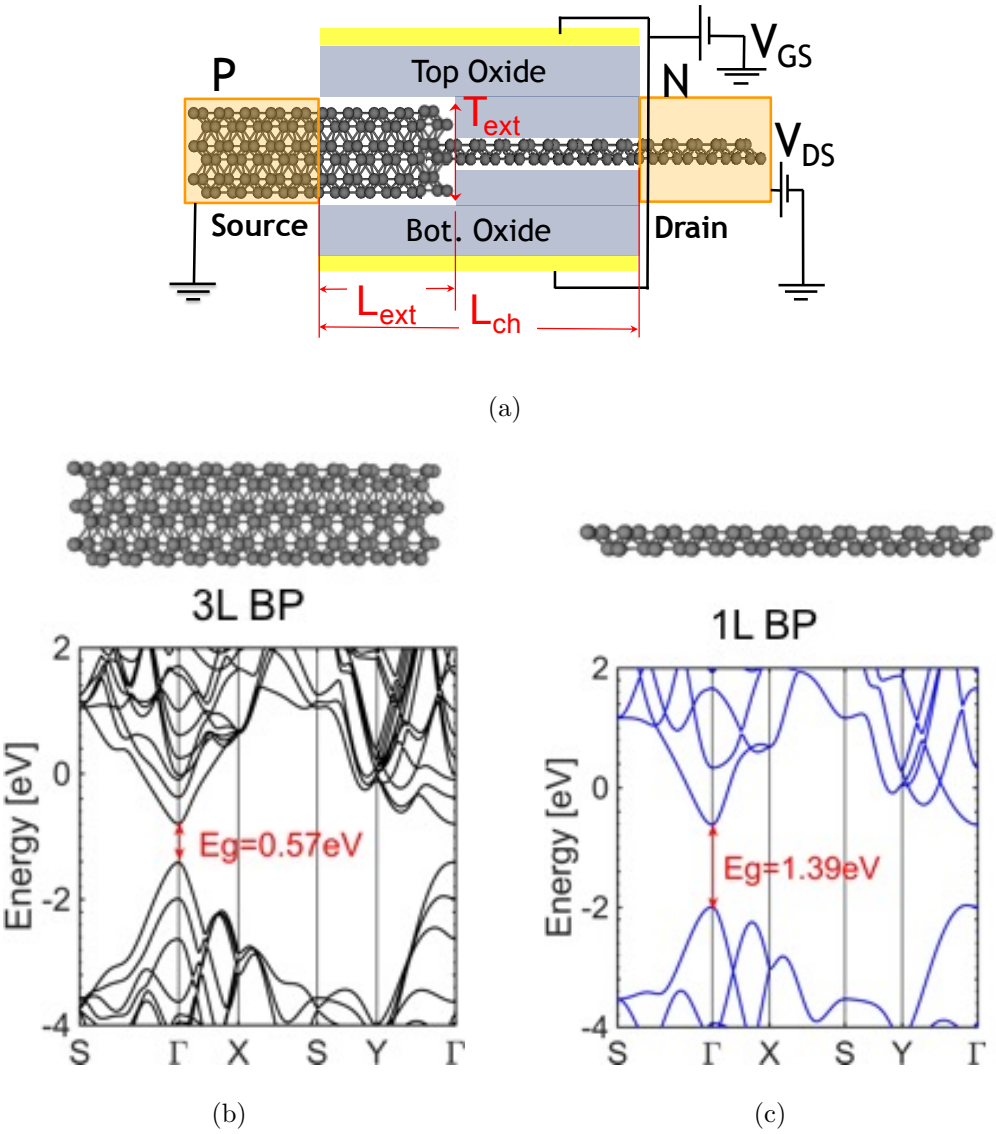


Figure 3.1. (a) The cross-sectional device structure of layer engineered TFET (TE-TFET) based on phosphorene. It has a small Eg region at the source and the channel region near the source and a large Eg region in the rest of the device. The layer thickness of the length of the small band gap region inside channel is denoted by L_{ext} and T_{ext}. The band structure of (b) 3L phosphorene with Eg = 0.57eV; (c) 1L phosphorene with Eg = 1.39eV.

The capacitance vs. voltage and energy delay product comparison with homojunction phosphorene TFETs will also be discussed. In section III, full-band quantum

transport simulations are performed for TE-TFET. The performance sensitivity of TE-TFET to the layer thickness in the small Eg region, the channel length, device scaling is discussed. The capacitance vs. voltage and energy delay product comparison with homojunction phosphorene TFET is also discussed. It is shown smaller Eg channel material 3L-phosphorene not only improves the ON-current but also degrades the I_{OFF}.

3.3 Simulation Details

The Hamiltonian of phosphorene is represented using a 10 band $sp^3d^5s^*$ second nearest neighbor tight binding model. The tight-binding parameters are well calibrated to match the band structure and effective mass from density function theory (DFT) HSE06 by the standard mapping method [74]. The tight-binding bandstructure of 3L and 1L can be seen from Fig. 4.7b and Fig. 4.7c respectively. The Eg size for different layer numbers in Table 3.1. The relative permittivity for both in-plane ϵ^{in} and out-of-plane $\epsilon^{out}$are taken from [75] and also listed in Table 3.1. All the transport characteristics of the TE-TFET have been simulated using the self-consistent Poisson-Non Equilibrium Green′s Function (NEGF) method with the Nano-Electronic MOdeling (NEMO5) tool [76].

TE-TFET has the device structure schematic shown as Fig. 4.7a, with L_{ch}, L_{ext} and T_{ext} being $12nm$, $4nm$ and 3L respectively. V_{DS} is kept 0.4V for L_{ch} 12nm. Source and drain are doped with p-i-n configuration with doping level to be $10^{20}cm^{-3}$. Equivalent oxide thickness (EOT) is designed to be 0.5nm. Constant field scaling E $= 30V/nm$ is performed for device scaling, where $E = V_{DD}/L_{ch}$. These parameters are assumed to be the same unless mentioned otherwise.

3.4 TE-TFET Device Performance

The transfer characteristics of TE-TFET compared with 1L, 2L, and 3L phosphorene TFET is shown in Fig. 4.10. All the curves except for the 3L-TFET are shifted

Table 3.1.
Multi Layer Phosphorene Parameters: Bandgap Eg, in-plane and out-plane relative dielectric constant ϵ^{in} and ϵ^{out}.

Layer	1	2	3	4
Eg(eV)	1.390	0.803	0.570	0.481
ϵ^{in}	4.56	7.41	8.77	9.98
ϵ^{out}	1.36	1.52	1.80	2.04

to have the same $I_{OFF} = 10^{-4}\mu A/\mu m$. The minimum current in $Id - Vg$ sweep is 3L-TFET is $4.131\mu A/\mu m$, which is larger than the requirement of I_{OFF} of standard shifting. It is shifted with the same amount of voltage with TE-TFET.

From Fig. 4.10, TE-TFET can keep the small I_{OFF} as 1L-TFET and achieve the high ON current as 3L-TFET. The I_{ON} TE-TFET can achieve at $V_{DD} = 0.4V$ is about $700uA/um$, which is one time larger than 2L-TFET. The I_{60}, where SS becomes $60mV/dec$ of TE-TFET is about $10\mu A/\mu m$. Compared to the I_{60} of 2L-TFET, it improved by two orders.

A comparison of TE-TFET with 3L-TFET at ON state and 1L-TFET at OFF state is performed. Band diagram aligned with energy resolved current is shown in Fig. 3.3. At OFF state, as shown in Fig. 3.3a and b, compared to 3L-TFET, TE-TFET has a barrier in the starting from the 1L region, blocking all the leakage current. In this way, TE-TFET is able to achieve a small OFF current. At ON state, as shown in Fig. 3.3c and d, compared to 1L-TFET, TE-TFET has a smaller tunnel distance. Thus, TE-TFET is able to achieve a higher ON current. By exploiting the 1L-barrier to block the leakage current at OFF and turned by a smaller tunnel distance near the source region, TE-TFET can achieve $SS = 15mV/dec$ over four decades of current change. The ON current of TE-TFET is still outperformed by 3L-TFET due to 1L barrier inside channel blocking current as shown also in Fig. 3.3c

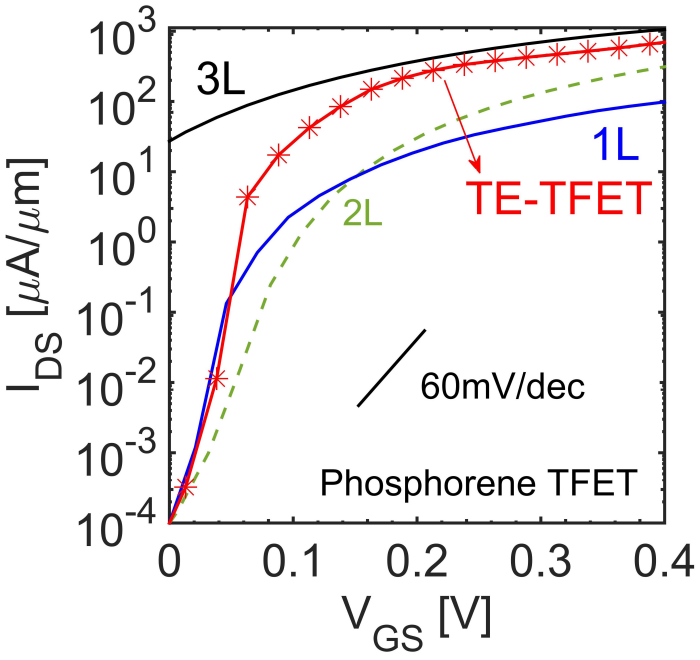


Figure 3.2. The transfer characteristics of TE-TFET compared with different layer thickness TFET based on phosphorene.

and d.

3.5 Device Scaling

The impact of design parameters T_{ext} and L_{ext} are studied the for $L_{ch} = 12nm$. As shown in Fig. 4.12a, the Eg in extension region is set to be 0.481eV, 0.570eV and 0.803eV by using 4L, 3L and 2L phosphorene respectively. The ON current can be improved from $700\mu A/\mu m$ to $800\mu A/\mu m$ by replacing 3L with 4L in the extension region. Using 2L instead would make TE-TFET still achieve the same ON current with 3L but the I_{60} will be degraded by two orders. On the other hand, as shown in Fig. 4.12b, the ON current improves by an order when L_{ext} increases from 1nm to 2nm and kept to be the same from 2nm to 4nm. This is because when L_{ext} is too

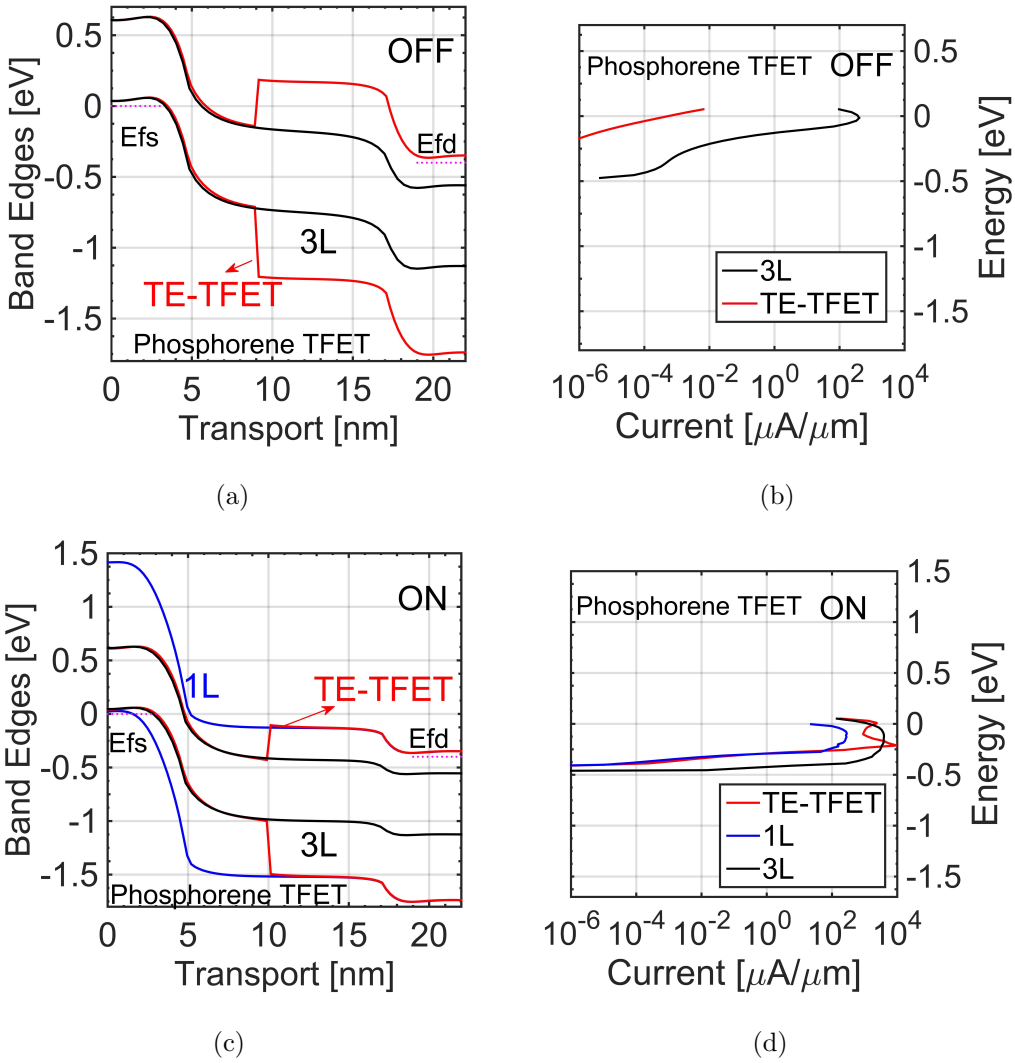


Figure 3.3. The band edges of (a) TE-TFET with 3L TFET at OFF state and (b) TE-TFET with 1L and 3L TFET at ON state aligned with the energy resolved current (c) and (d) respectively.

small, the small Eg region is not long enough to cover the region where the tunneling happens.

The I_{ON}/I_{OFF} dependencies on T_{ext} and L_{ext} for $L_{ch} = 12nm$ and $6nm$ are plotted in Fig. 4.12c. When the channel length is reduced to 6nm with V_{DS} set to be 0.2V to perform constant field scaling, the trend is similar with when $L_{ch} = 12nm$. When $L_{ch} = 6nm$ is the OFF current is degraded to be larger than $10^{-4}\mu A/\mu m$due

to the 2nm-4nm 1L barrier inside the channel is not long enough to block the leakage current. To make a better comparison, the I_{ON} is kept to be $10^2 \mu A/\mu m$ for T_{ext} study; whereas the I_{OFF} is kept to be $10^{-3} \mu A/\mu m$ for L_{ext} study. It is worthwhile to mention here, there is a very small range of V_{GS}, when the SS is smaller than $60mV/dec$. It is due to the fact for small V_{GS} , when 1L barrier is still higher than Ef_s, the current increasing results from electron tunneling through the 2nm barrier. The small amount of current increasing comes from the tunnel current increasing from the change of the barrier shape before there is a sudden increase when 1L barrier is lower than Efs.

3.6 Capacitance and Charge Distribution

Constant field scaling E = $30V/nm$ is studied on TE-TFET, where $E = V_{DD}/L_{ch}$. As shown in Fig. 4.12d, the I_{ON}/I_{OFF} of TE-TFET keeps to be 6 orders when L_{ch} scales down to 9nm and there is an increase of I_{OFF} when channel length is 6nm. Fig. 4.13a shows for this constant field scaling, the total gate capacitance changes with V_{GS}. The gate capacitance is comparably smaller than most TMD materials. This results from the small effective mass of phosphorene [72]. The CV curve is different from homo-junction due to the plateau region. The reason of the plateau is formation of the continuum of bond states inside the quantum well region. As shown in Fig. 4.13(b), the carrier density decreases in between two continuum of bond states. This decrease in the quantum well region compensates the increase inside the 1L region and forms the plateau in the C-V curves. The length of the plateau region is different for different L_{ch} since the carrier density is also influenced by the carrier injection from drain [77].

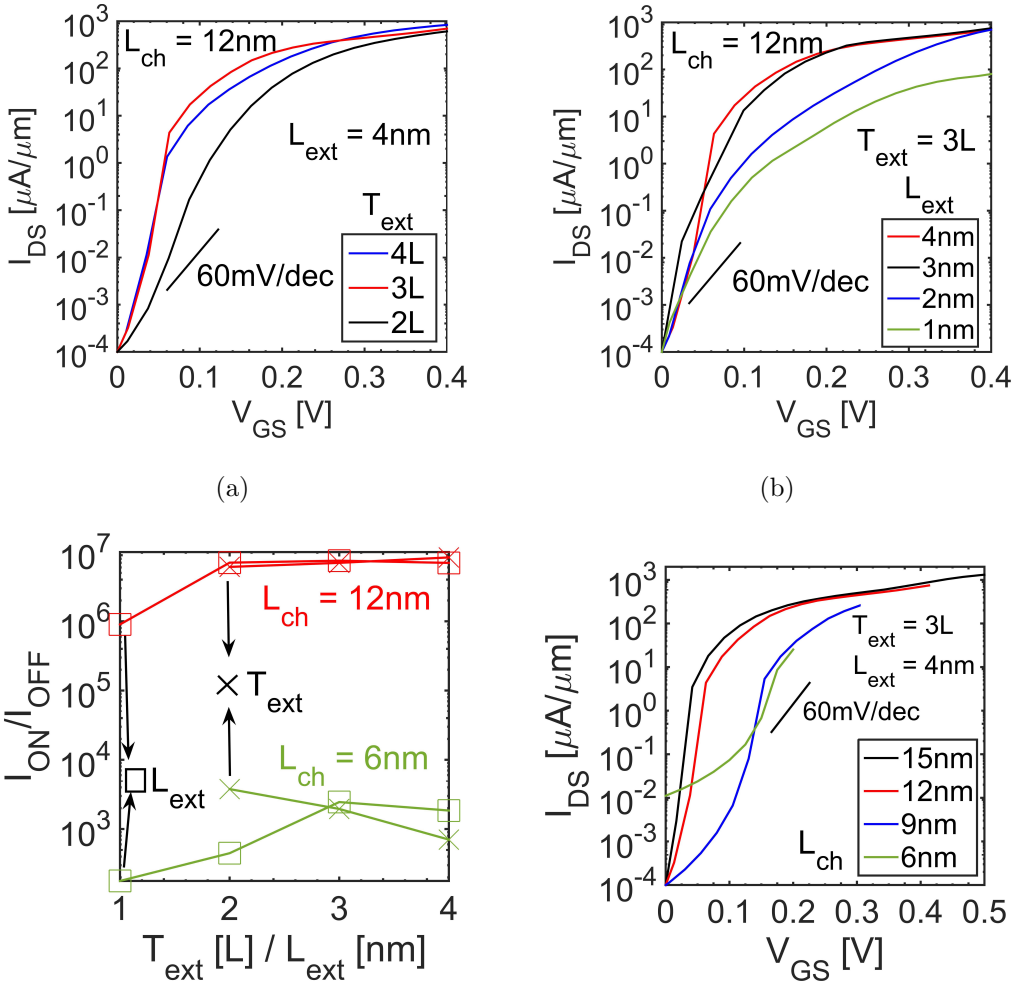
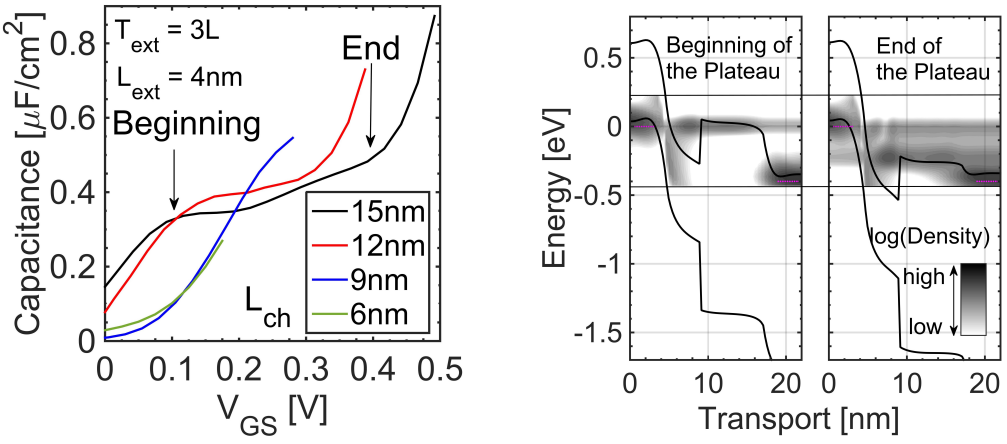


Figure 3.4. Id-Vg curves for TE-TFETs of $L_{ch} = 12nm$ with different (a) T_{ext} and (b) L_{ext}. (c) The I_{ON}/I_{OFF} change with respect to T_{ext} and L_{ext} for $L_{ch} = 12nm$ and $6nm$. (d)The transfer characteristics with L_{ch} of TE-TFETs with constant field scaling ($E = V_{DD}/L_{ch} =$ 30V/nm) from 15nm to 6nm.

3.7 Energy Delay Product

Compared to homojunction phosphorenene TFET [72], TE-TFET has a slightly higher capacitance, but the ON current is higher too. This translates into an improvement of 32 bit adder energy-delay product as shown in Fig. 3.6. The 32-bit



(a) (b)

Figure 3.5. (a) The transfer characteristics and (b) C-V of with L_{ch} of TE-TFETs with constant field scaling ($E = V_{DD}/L_{ch} = 30\text{V/nm}$) from 15nm to 6nm.

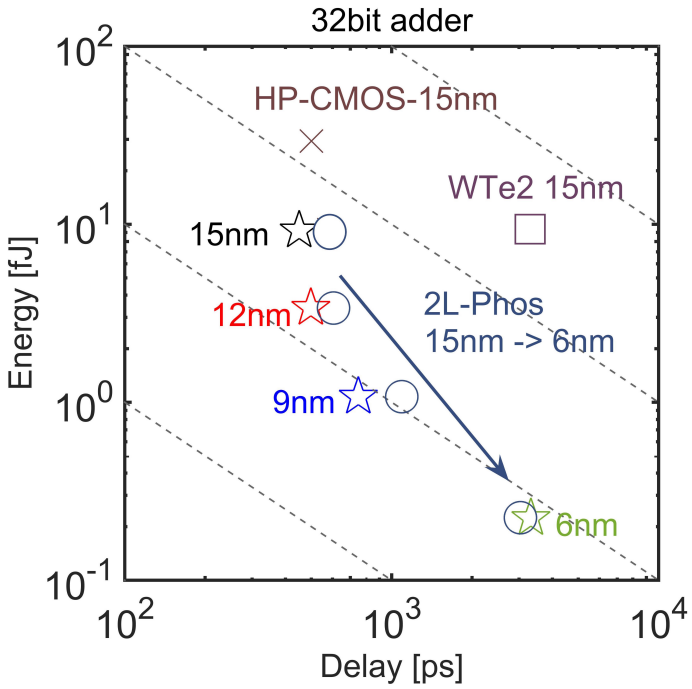


Figure 3.6. Energy-Delay product of TE-TFETs in comparison 2L-TFETs [72] with their L_{ch} scaled from 15nm to 6nm and a 15nm WTe2 TFET.

adder energy delay produce is calculated by using BCB 3.0 [51], where the parasitic capacitances and interconnects are taken into account. The scaling of circuit parameters as a function of gate length is taken from ITRS 2011 roadmap.

3.8 Conclusion

In conclusion, thickness engineered tunneling field-effect transistor (TE-TFET) is proposed and evaluated in this work. By taking advantage of flake-thickness-dependent direct bandgap in phosphorene, an artificial heterostructure TFET can be achieved. The absence of interface, between different materials in artificial heterojunctions, allows TE-TFET to avoid the interface states and lattice mismatch problems observed in conventional heterojunction TFETs while providing similar boost in the

ON-current of $1280\mu A/\mu m$ with a 15nm channel length. TE-TFETs are scalable down to 9nm with constant field scaling E = $V_{DD}/L_{ch} = 30V/nm$. Offering higher ON-current, TE-TFETs outperform the best homojunction phosphorene TFETs and TMD TFETs in terms of circuit energy-delay product.

This work is published in [12].

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4. INTERLAYER TFETS

4.1 Interlayer TFETs from vertically stacked 2D materials

Sarkar et al [78] demonstrated a tunnel-FET (TFET) that combines an atomically thin, two-dimensional semiconducting crystal with a 3D germanium substrate and shows excellent turn-on performance at only 0.1V. At room temperature, this TFET achieves a very steep SS ($31.1mV$ per decade of current, averaged over 4 decades); the minimum value reached is $3.9mV$ per decade of current. This $2D$ semiconducting heterojunction ranks as one of the most promising materials for the fabrication of switches that could operate with supply voltages as low as $0.1V$, resulting in a reduction in power consumption of more than 90 percent compared with conventional FETs. [79]

The device structure can be illustrated as the schematic in Fig. 4.1. The source and drain region are p and n doped respectively. The tunneling width is determined by the distance of the two layers λ.

The currently believed [78, 80–83] device operating mechnism is as following. Assuming the band aligns as shown in Fig. 4.2(b) based on the band gap and electron affinity of each material; forming a staggered vertical heterojunction. White regions means forbidden gaps, or zero density of states (DOS). When in the OFF state, electron from the valence band of the bottom layer cannot transport to top layer owing to the zero DOS in top layer. At higher energies, where there are DOS available in the top layer, zero DOS is available in the bottom layer, again forbidding electron flow. With a further increase in energy reaching the conduction band of bottom layer, DOS are available in both layers. However, the number of the electrons available in

the conduction band of the bottom layer is negligible owing to the exponential decrease in electron concentration with increase in energy above fermi level according to Boltzmann distribution. Thus, very few electrons can flow from bottom layer to top layer, leading to a very low OFF-state current. As the top gate voltage increases, the conduction band of the top layer is lowered below the valence band of the bottom layer as shown in Fig. 4.2(a). In this way, the electrons starts to flow, resulting in a sharp increase in the current.

The reasons in achieving steep slope in this 2D Vertical Hetero-structure TFET are 1) Low density of interface defects due to very small amount of dangling bonds at surface; 2) Immune to energy band gap increasing from vertical quantization due to the 2D nature; 3) Excellent electrostatic control due to the sub-nanometer thickness. Another advantage this device structure can gain is the possibility of achieve high ON current from heterojunction by stacking different TMDs as shown in Fig. 4.3.

However, the ON current of this device is about $0.001\mu A/\mu m$. What are the possible ways to increase ON current experimentally is unclear. A similar device structure has been fabricated earlier [84]. Here, the steep slope transition didn't show up. Experimentally, when we try to grow this heterostructure, is there going to be a preferred angle? And is the Van der Waals force in forms in between the layers strong enough to strain the material? Usually, there is a up to 10 percent difference in lattice constant of the graphene like 2D materials. Is there a strain in each layer, or can the lattice mismatch be ignored when the difference is small enough? And how small is this critical mismatch? These are the challenges we are going to face in terms of modeling.

In this chapter, the transport of tunnel field-effect transistors (TFETs) based on vertically stacked hetero-structures from 2D transition metal dichalcogenide (TMD) materials is investigated by atomistic quantum transport simulations. One of the major challenges of TFETs is their low ON current. 2-D material-based TFETs can

have tight gate control and high electric fields at the tunnel junction, and can, in principle, generate high ON-currents along with a subthreshold swing (SS) smaller than 60 mV/decade. Our simulations reveal that high-performance TMD TFETs not only require good gate control, but also rely on the choice of the right channel material with optimum bandgap, effective mass, and source/drain doping level. Unlike previous works, a full-band atomistic tight-binding method is used self-consistently with 3-D Poisson equation to simulate ballistic quantum transport in these devices. The effect of the choice of the TMD material on the performance of the device and its transfer characteristics are discussed. Moreover, the criteria for high ON-currents are explained with a simple analytic model, showing the related fundamental factors. Finally, the SS and energy delay of these TFETs are compared with conventional CMOS devices. In order to make sure our model does not standy too far away from experiments, we have picked Gr/hBN/Gr vertical tunneling device to compare.

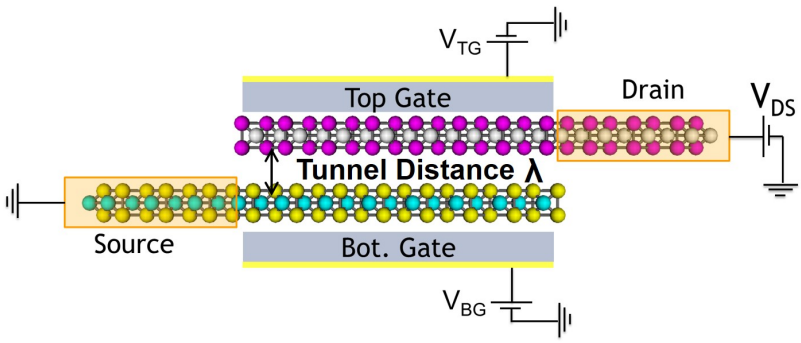


Figure 4.1. Schematic diagram illustrating the cross-sectional view of 2D Vertical Hetero-structure TFET.

4.2 Gr/hBN/Gr Resonant Tunneling

Graphene/hexagonal Boron Nitride /Graphene (Gr/hBN/Gr) is one of the first experimentally observed vertically stacked devices [86,87]. Graphene and hBN are both of hexagonal structure, which makes them suitable candidate for vertical stacking.

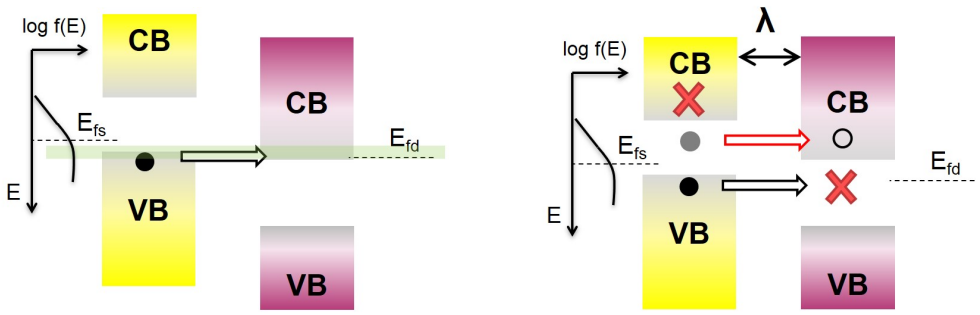


Figure 4.2. Band diagrams along the vertical direction in Fig. 4.1 are shown in (a) ON and (b) OFF status

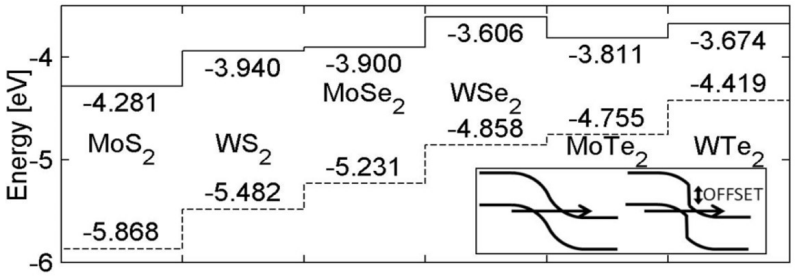


Figure 4.3. The band alignments of different TMD materials based on electron affinity. Figure from [85].

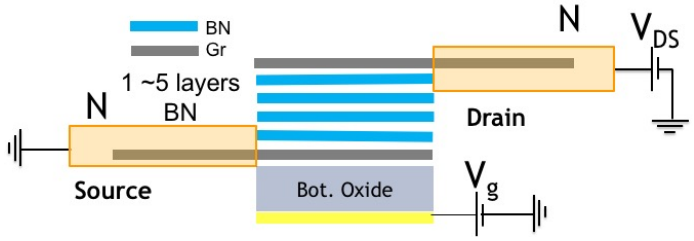


Figure 4.4. The Structure of Gr/hBN/Gr Resonance Tunneling Devices. The number of BN layers can vary from 1 to 5 in the simulation study in order to compare with experiments.

Britnell et al have experimentally investigated Gr/hBN/Gr structure and observed resonant tunnelling behaviour in these structures [87]. Since then several group have

developed theoretical model to understand and investigate the effects of physical parameters like device geometry, lattice mismatch and rotation angle [88–91]. Even though these models have been successful in simulating several aspects of experimental observations neither of them could match the current level of the experimental measurement [88]. Moreover, none of them could account for the trend in the background current of the system. In this work, we address these issues by modelling the vertical transport in Gr/hBN/Gr structure using atomistic quantum transport simulation based on semi-empirical tight binding approach. By using a linear combination of the well-known coupling parameters between C-B and C-N, we could accurately model the current level as well as the trend in background current. Moreover, we varied the number of hBN layers and established an empirical formula for dependence of current on the number of hBN layers. Finally, we determined the relation of Peak-to-Valley (PVR) ratio with the number of hBN layers.

4.2.1 Vertical Tunneling Model

The Hamiltonian of both graphene and hBN has been represented using pz nearest neighbour tight-binding model. We used the previously established parameter to model intralayer transport [92]. To model the vertical transport, we used a linear combination of the coupling parameter of C-B and C-N. All the transport properties have been simulated by first evaluating the poisson equation to get the potential which was then passed into quantum transport boundary method (QTBM) in the multi-scale Multiphysics Nanoelectronic modelling tool NEMO5 [76]. To validate our one pass method, we compared our transport calculation with self-consistent Poisson-QTBM method for a few bias points and found significant similarity.

4.2.2 Negative Differential Resistance (NDR)

Fig. 4.4 shows our simulated structure with a hBN layer sandwiched between two graphene layers. Our overlap region is $25nm$ with source and drain extension of

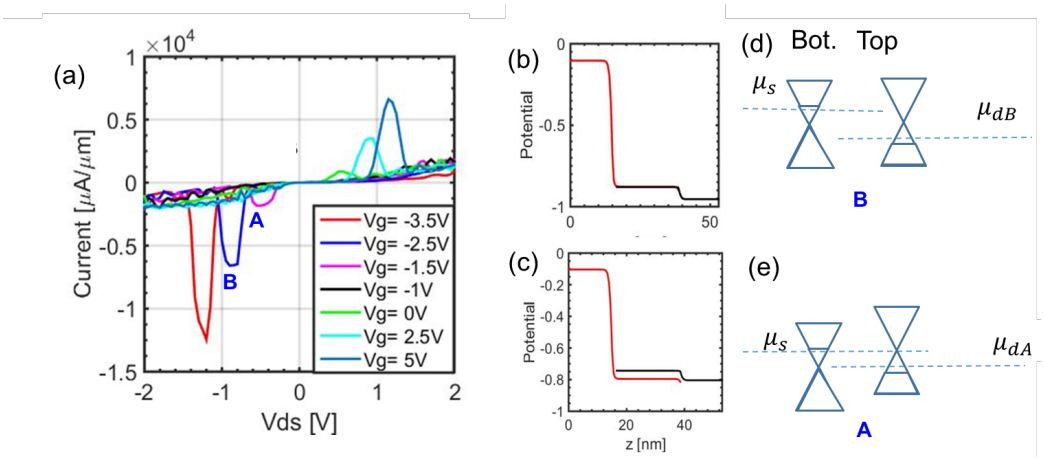


Figure 4.5. (a) Id-Vg curve for different gate voltage of a Gr/2 Layer hBN/Gr structure. We can see the NDR peaks. (b)-(c) Alignment of the potential of top and bottom layer where the the NDR peak is observed and the corresponding transmission. (d)-(e) The Dirac Cone of top and bottom layer alignment. When two dirac cones do not have momentum mismatch, the resonance peak appears.

$15nm$. Our back gate is underneath the overlap region with effective oxide thickness of $0.5nm$. We have considered doping of $1e13$ in the source and drain graphene region. Fig. 4.5(a) shows the $I_d - V_d$ curve for different gate voltage. We can see prominent negative differential resistance (NDR) peak whose value and position shifts with gate voltage. The NDR results from the alignment of the Dirac cones of the top and bottom layer which enables momentum conserved tunnelling. This is consistent with the experiment and previous theoretical models [87, 88]. Fig. 4.5(b) shows the matching potential of the top and bottom layer where we observed the peak current. This results in high transmission as shown in Fig. 4.5(c). Fig. 4.5(d) shows that a slight mismatch is the potential of the two layer results in drastic decrease in transmission.

4.2.3 Calibrating to Experiments

Fig. 4.6(a-d) shows how the number of hBN layers effect the current. We observe that the current reduces exponentially with the number of hBN layers which is consis-

tent with the tunnelling mode of transport [93]. For smaller bias voltage, we observe an exponential id-vd dependence. However, for $|Vd| > 0.8V$ the current becomes linear with bias voltage. To develop a model for layer dependent transport, we have formulated an empirical piecewise model:

$$\Delta I_{DS} = \begin{cases} Ae^{cV_{DS}} \cdot e^{-3.3n} & |V_{DS} < 0.8V| \\ B \cdot e^{-3.3n} & |V_{DS} \geq 0.8V| \end{cases} \tag{4.1}$$

Where A, B and c are constants to fit the simulation results and n is the number of layers. As we can see the current has an exponential dependence on the number of layer $exp(-3.3n)$. This is consistent with DFT based previous where it is shown that transmission has a $exp(-3.4n)$ dependence on the number of layer. Fig. 4.6(e) show the simulation result for 1 to 4 layers of hBN. Our empirical model matches with the simulation for different layers. Importantly, we used our model to predict the transport for barrier of 5 hBN layers. Our model successfully predicted the experimental results obtained by Britnell et al. [87] as shown in Fig. 4.6(e). It should be noted that we observed secondary peak around the main one which can be attributed to the lateral maxima of the spectrum of the rectangular well-like confining potential [94].

Next, we analysis the dependence of the NDR peak on the gate voltage and number of hBN barrier layers. Gate voltage shift the potential of the bottom layer and drain voltage shift the potential of the top layer. If higher bias voltage is required to align the Dirac cones of both the layers, it results in higher tunnel current flows due to the availability of more states. This is reflected in the linear relation of the PVR with gate voltage. However, the slope is much higher in the negative gate bias regime compared to the positive gate bias regime. This is because it takes higher drain voltage to align the Dirac cones when the gate bias is negative resulting in more current. On the other hand, PVR increases drastically with the number of layers. Moreover, the width of the peak decreased with the number of layers. This can be understood by the uncertainty of the wavefunction. It should be mentioned that our PVR value is much higher than experimentally observed one. This is because we didn't take into account several scattering mechanisms like electron phonon scattering and the effect

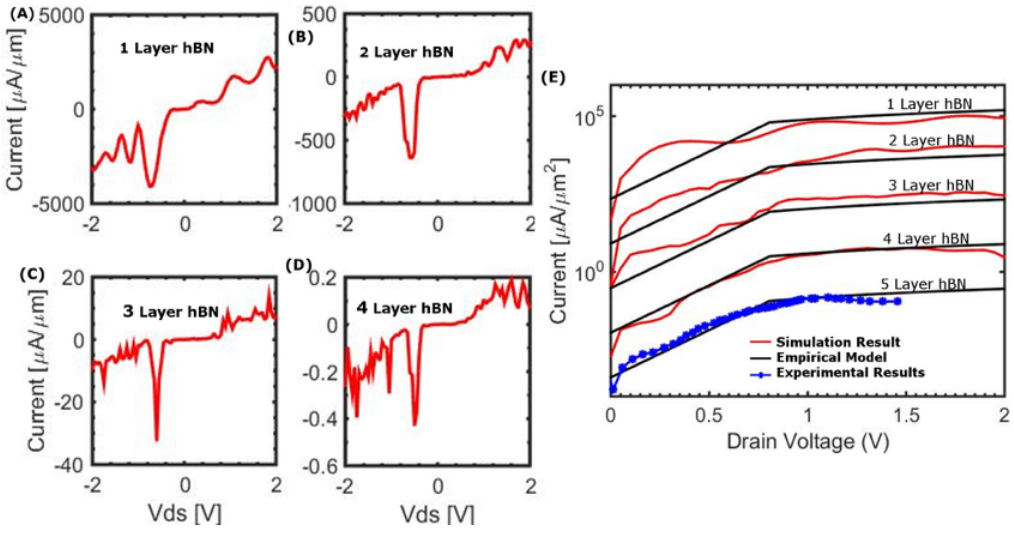


Figure 4.6. (a-d) Current vs drain voltage for different barrier thickness starting from one layer hBN to four layer hBN. (e) Current vs drain voltage is compared for simulation, empirical model and experimental results. Our empirical model could accurately explain the experimental results.

of the substrate. These non-idealities can destroy the coherence of the wave function reducing the amount of tunnelling current.

4.2.4 Conclusion

We have modelled vertical tunnelling transport in Gr/hBN/Gr heterostructure by using a linear combination of vertical coupling parameters of the constituent atoms. Our simulation results are successful in modelling the trend of the background current as well as the current levels from previous experiments. This technique can be extended to vertical transport in other two-dimensional materials system. Moreover, prediction about electronic properties can be made for various possibilities of vertical stacking using this method. I want to acknowledge Md Sharafat Hossain in helping getting all the modeling results and contributing to the paragraphs in this Gr/hBn/Gr work.

4.3 MoS2-WTe2 Interlayer TFETs

In this section, the transport of tunnel field-effect transistor (TFET) based on vertically stacked hereto-structures from 2D transition metal dichalcogenide (TMD) materials is investigated by atomistic quantum transport simulations. WTe2-MoS2 combination was chosen due to the formation of a broken gap hetero-junction which is desirable for TFETs. There are two assumptions behind the MoS2-WTe2 hetero-junction tight binding (TB) model: 1) lattice registry. 2) The $S-Te$ parameters being the average of the $S-S$ and $Te-Te$ parameters of bilayer MoS2 and WTe2. The computed TB bandstructure of the hetero-junction agrees well with the band-structure obtained from density functional theory (DFT) in the energy range of interest for transport. NEGF (Non-Equilibrium Green′s Function) equations within the tight binding description is then utilized for device transfer characteristic calculation. Results show 1) energy filtering is the switching mechanism; 2) the length of the extension region is critical for device to turn off; 3) MoS2-WTe2 interlayer TFET can achieve a large on-current of $1000\mu A/\mu m$ with $V_{DD}=0.3V$, which suggests interlayer TFET can solve the low ON current problem of TFETs and can be a promising candidate for low power applications.

We simulate a band-to-band tunneling field-effect transistor based on a vertical heterojunction of single-layer MoS2 and WTe2, by exploiting the non-equilibrium Green′s function method and including electron phonon scattering. For both in-plane and out-of-plane transport, we attempt to calibrate out models to the few available experimental results. We focus on the role of chemical doping and back-gate biasing, and investigate the off-state physics of this device by analyzing the influence of the top-gate geometrical alignment on the device performance. The device scalability as a function of gate length is also studied. Finally, we present two metrics for the switching delay and energy of the device. Our simulations indicate that vertical field-effect transistors based on transition metal dichalcogenides can provide very small values

of sub-threshold swing when properly designed in terms of doping concentration and top-gate extension length.

4.3.1 The advantages of interlayer TFETs

The fast growth of today′s technology has been sustained by continuous scaling of silicon-based MOSFETs. The scaling of transistors face two major challenges nowadays: the degradation of gate gate control and the fundamental thermionic limitation of the steepness of sub-threshold swing (SS). 2D materials have emerged as promising channel materials for transistors, as they can maintain excellent device electrostatics at much reduced channel length and thickness [95]. Interlayer tunnel field effect transistors (TFETs) based on vertically stacking 2D materials have also been shown to break the thermionic limitation of sub-threshold swing (SS) [82, 83]. However, experimentally demonstrated vertical TFET with small SS still suffer from low current levels [78]. TFET designs exploiting different 2D material properties [10–12, 52, 72, 96, 97] have been proposed to increase the tunneling current. Theoretical works also demonstrated the possibility of a high ON current in interlayer TFET′s [80, 81]. Yet, an understanding of device physics of interlayer TFETs such as the effect from device geometry, lattice mismatch, twisted angles [98] and Van der waals bonding in order to provide a guideline for interlayer TFETs to achieve high ON currents experimentally. In this work, an interlayer TFET based on vertically stacked MoS2 and WTe2 as shown in Fig. 4.12) is studied. The model assumptions are described in details and have been carefully examined. The switching mechanism and performance of the device are then investigated and evaluated. This material combination was chosen as WTe2-MoS2 forms a broken gap hetero-structure as desirable for TFETs. The assumptions of the model are described in detail and have been carefully benchmarked against $ab-initio$ calculations. The band diagram aligned with transmission is plotted for understanding the switching mechanism. The MoS2-WTe2 interlayer TFET

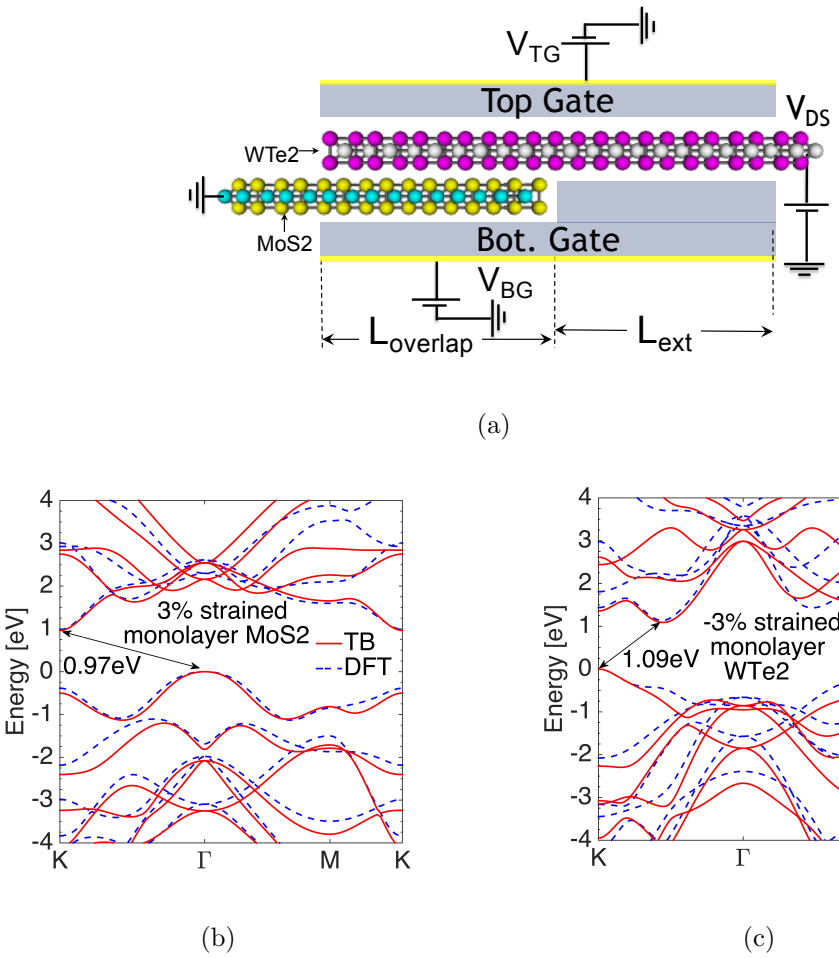


Figure 4.7. A comparison of band structure plots for vertical MoS2-WTe2 hetero-junction from tight binding (TB) and density function theory (DFT). They match well along the band edge at K point.

shows a SS smaller than $60mV/dec$ and the extension region is critical for the device to turn off. The device geometry is then optimized and demonstrates an ON current of $1000\mu A/\mu m$ with $V_{DD} = 0.3$.

4.3.2 Approach

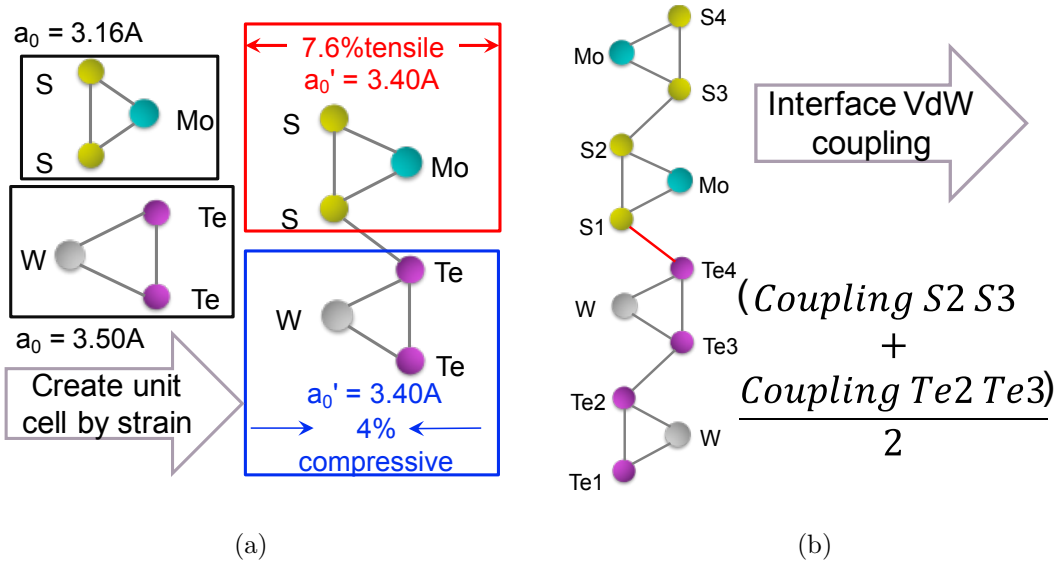
This section is a copy of [13]. The Transistion Metal Dichalcogenide (TMD) Hamiltonian (strained) is represented by an $sp3d5$ second nearest neighbor tight-

binding (TB) model including $spin-orbit$ coupling. DFT-guided TB model is adapted to reduce computational expense and system size compared to $ab-initio$ calculations [74]. The PBE functional is used in the density functional theory (DFT) calculations since it is known to produce band gap comparable with experimental measurements for TMDs [56]. The Van der Waals correction for the interlayer coupling of multilayer MoS2 or WTe2 is included by the optB88 functional [99].The TB parameters are well calibrated to match the band structure and effective mass from DFT by a well-established mapping method [74, 100]. The TB parameters are general and capture the band structure of both the bulk and monolayer TMDs [56, 76].

There are two major assumptions to obtain the TB parameters for the hetero-junction: 1) The materials are lattice matched by applying 7.6 percent tensile strain to MoS2 and 4 percent compressive strain to WTe2 as shown in Fig. 4.8(a); 2) The interlayer coupling parameters between the Sulphur and the Telluride atoms are obtained by averaging the coupling parameters of S-S in bilayer MoS2 and and Te-Te in WTe2 as shown in Fig. 4.8(b).

A strained TB model is developed to fulfill the lattice registry. The relation of TB parameters with strain percentage is obtained by fitting to a set of strained DFT MoS2 or WTe2 monolayers. This model is then carefully examined by reproducing the DFT bandstructure under different strain. In order to obtain the DFT band structure of MoS2-WTe2 interface for benchmarking, an ionic relaxation was carried out on the supercell until all the atomic forces on each ion were less than $0.0001eV/nm$. Subsequently, the EK diagram was obtained for the relaxed configuration. This calculation was performed with a generalized gradient approximation (GGA) and PBE functional with a vdW correction as implemented in VASP (DFT-D2).

All the transport characteristics of the MoS2-WTe2 TFET have been simulated using the self-consistent Poisson-semiclassical approach to obtain the potential profile and then this potential is passed to quantum transmitting boundary method (an equivalent of non-equilibrium Green′s function method for ballistic transport) in the multi-scale [15] and multi-physics [9, 14, 101] Nano-Electronic MOdeling (NEMO5)



(a) (b)

Figure 4.8. (a) Assumption I : MoS2 and WTe2 layers have been strained to the same lattice constant to be registered. (b)Assumption II : Interface VdW coupling of vertical MoS2-WTe2 hetero-junction is the average of the VdW coupling of the two materials.

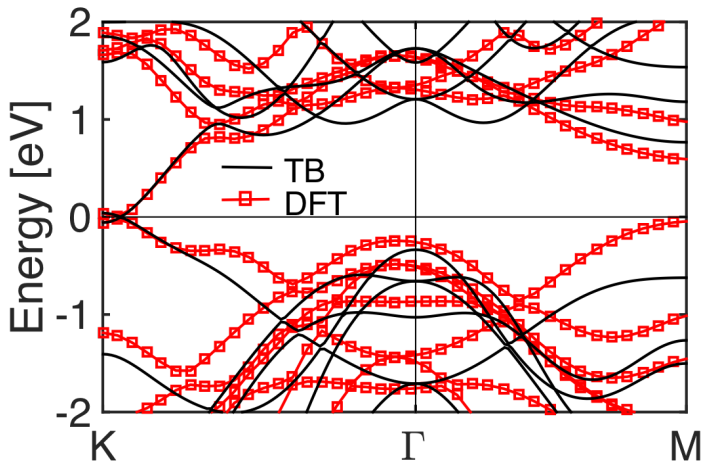


Figure 4.9. A comparison of band structure plots for vertical MoS2-WTe2 hetero-junction from tight binding (TB) and density function theory (DFT). They match well along the band edge at K point.

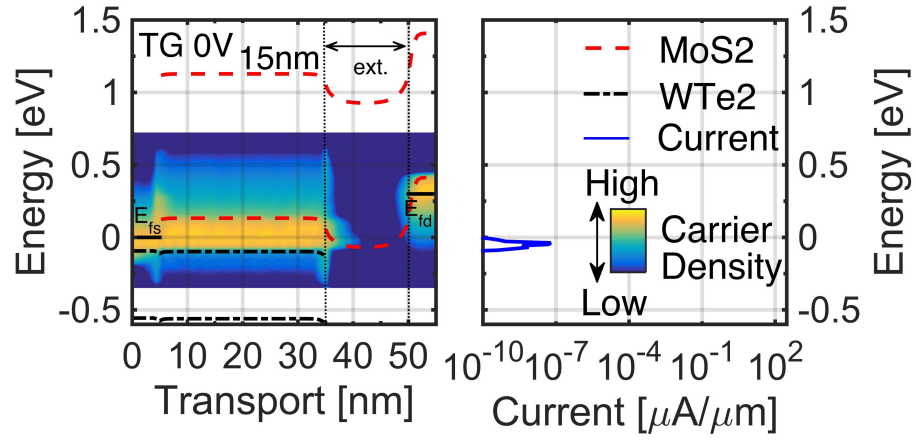
tool [76]. The default source and drain regions are doped with the doping level of $10^{20} cm^{-3}$. Equivalent oxide thickness (EOT) is set to 0.5nm.

4.3.3 Device Operation Mechanism

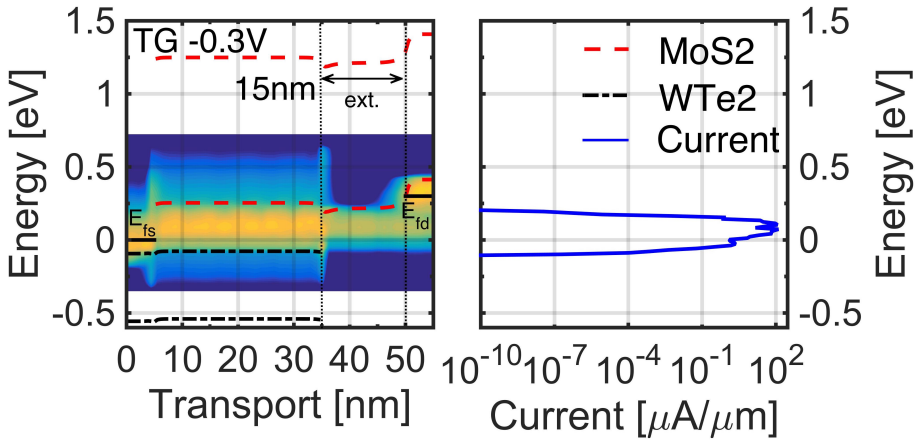
The DFT band-diagram of a relaxed MoS2-WTe2 vertical hetero-junction is plotted in Fig. 4.9. The zero band gap in the band diagram shows MoS2 and WTe2 forms a broken bandgap junction. The conduction and valence band edges meet at K point which provides the density of states for carrier transport. Furthermore, the TB band diagram computed under the assumptions agrees well with the DFT results in the energy range that is important for transport.

The tight-binding material model developed in this manner was used to simulate quantum transport for the device shown in Fig. 4.7(a). The device geometry parameters of the MoS2-WTe2 interlayer TFET $L_{overlap}$ and L_{ext} shown in Fig. 4.7(a) are optimized to be $30nm$ and $15nm$ respectively. The extension region is critical for the device to turn off. A zero L_{ext} would cause a high leakage current such that the small SS can not be observed. The leakage current mainly comes from the edges states. Fig. 4.11(a) shows that the transfer characteristics for a supply voltage of -0.3 V. The striking feature is the large ON current of $1000\mu A/\mu m$, which is significantly higher than the homo-junction 2D TFETs simulated thus far. The SS is around $20mV/dec$ in 4 orders of magnitude of current change.

So far, the interlayer TFET device operation mechanism has been understood to be as following [78,80–83]: at ON state, WTe2 Ev is higher than MoS2 Ec. This opens a window for electrons to flow and it has a non-zero current as shown in Fig. 4.10(b). At OFF state, WTe2 Ev is lower than MoS2 Ec. No electrons can go through and it has a low current as shown in Fig. 4.10(a). In this way, the electrons start to flow, resulting in a sharp increase in the current.



(a)



(b)

Figure 4.10. The band edges of a MoS2-WTe2 interlayer TFET at OFF (a) and ON (b)state aligned with the energy resolved transmission respectively. At ON state, WTe2 Ev is higher than MoS2 Ec. This opens a window for electrons to flow and it has a non-zero transmission. At OFF state, WTe2 Ev is lower than MoS2 Ec. No electrons can go through and it has a zero transmission.

4.3.4 The importance of extension region

If this is really the device operating mechnism, then we should expect a very good performance with the device structure shown in Fig. 4.1. However, the current cannot be turned off if the device structure is not revised to include an extension region as shown in Fig. 4.7(a).

Fig. 4.11(a) shows how the off current is degraded with the length of extension region L_{ext} decreasing from 15nm to 5nm. As we can see from Fig. 4.12(b), at the OFF state, where a 0V is applied on V_{TG}, the electron density in the top layer is tuned by the gate but not to zero. When $L_{ext} = 15nm$, the current is totally blocked by the extension region. Compared to Fig. 4.12(b), where the same voltage is applied in a device that $L_{ext} = 5nm$, the current is leaking at the OFF status. This concludes that the extension region is crucial for interlayer TFETs to achieve low OFF current. This indicates an energy filtering switching mechanism [102], which is completely different from the shifting story [78, 80–83].

Besides the low OFF current, the extension region also helps with the small SS as shown in the comparison of MoS2-WTe2 interlayer TFETs with an extension region from 5 to 15nm in Fig. 4.11(b). Long extension regions are more efficient in blocking leakage current. As a result, a smaller SS can be achieved.

4.3.5 Negative Capacitance

Fig. 4.11(c) indicates there is a negative capcacitance region in both the OFFF state and ON state. Also there is a decrease in the capacitance with top gate voltage in the device operation region. This trend is very similar for all the interlayer TFETs with 5-15nm extension length. From the OFFF state to ON state as shown in Fig. 4.12(a)-(c), the hole density in the bottom layer is barely moduated as shown

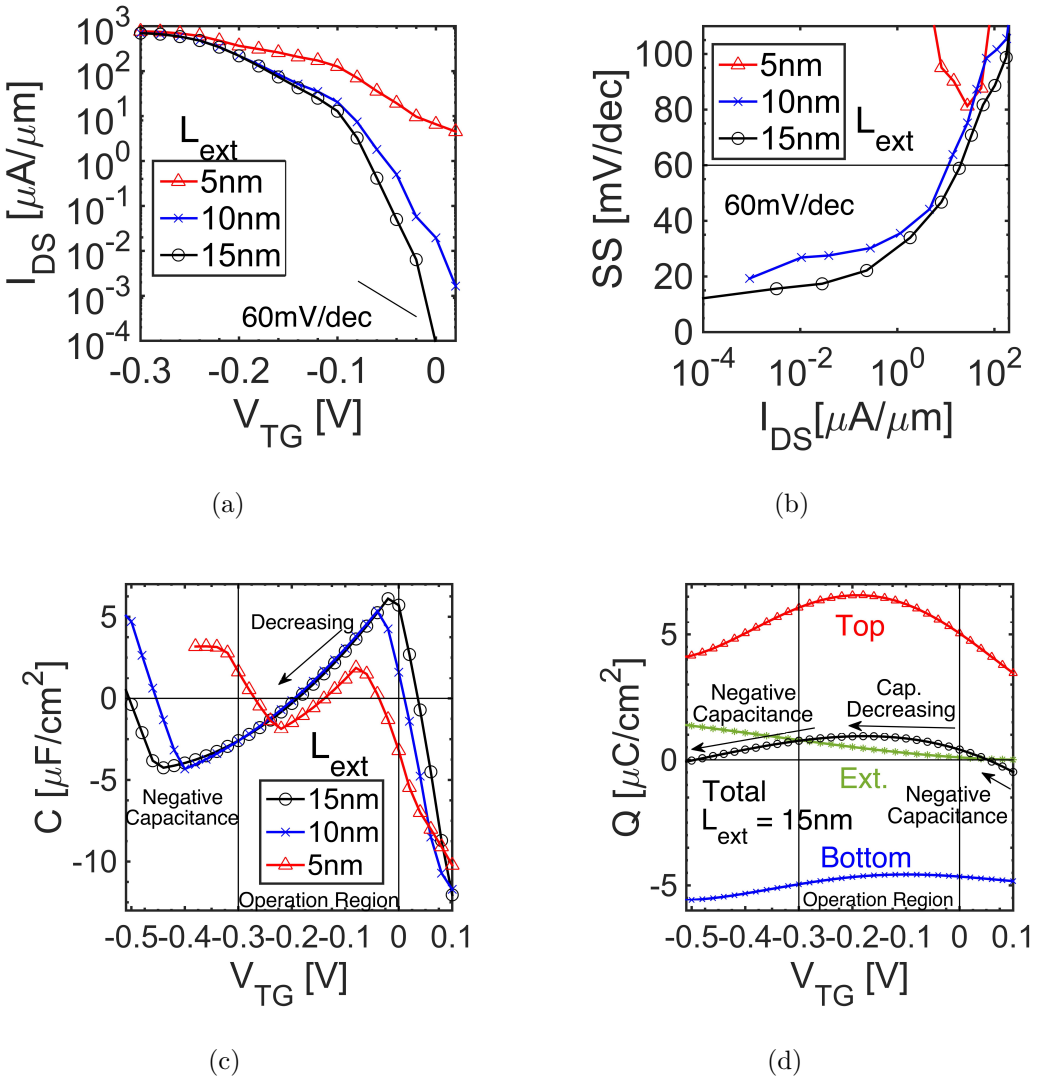


Figure 4.11. (a)The transfer characteristics ($Id-Vg$); (b) The SS-Id plot and (c) The capacitance-voltage plot of a MoS2-WTe2 interlayer TFET with the extension length L_{ext} ranging from 5 to 15nm. (d)The Charge-voltage plot of a MoS2-WTe2 interlayer TFET with $L_{ext} = 15nm$.

in the blue crossing in Fig. 4.11(d). Whereas the electron density in the top layer (excluding the extension region) increases to a saturation point and start to decrease as indicated by the red line in Fig. 4.11(d). The initial increase of the top layer electron neutralize the hole density in the bottom layer, resulting a decrease of the total

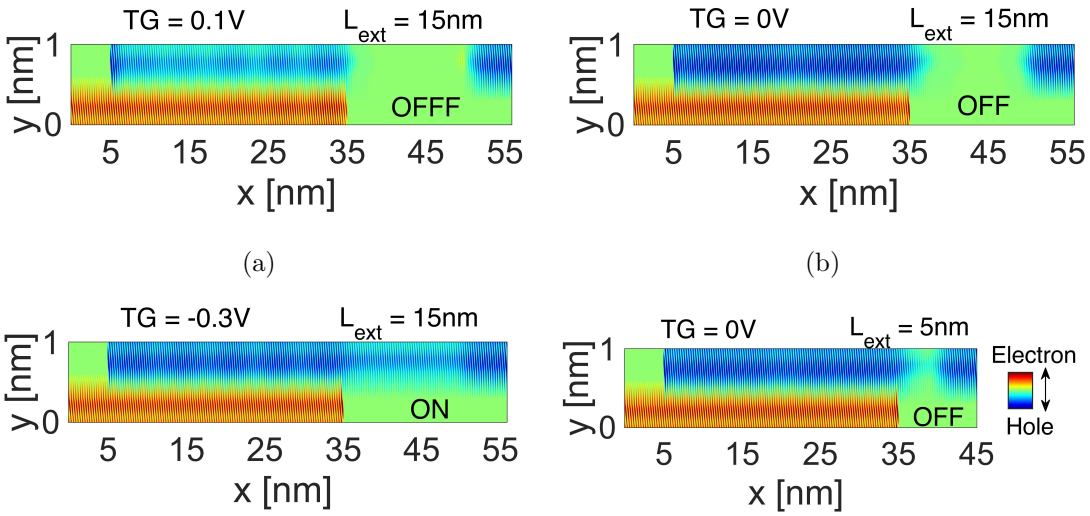


Figure 4.12. Position resovled electron/hole density for MoS2-WTe2 interlayer TFETs with $L_{ext} = 15nm$ at (a) OFFF state when $V_{TG} = 0.1V$ (outside device operation region); (b) OFF state when $V_{TG} = 0.0V$; and (c) ON state when $V_{TG} = -0.3V$; (d) with $L_{ext} = 5nm$ at OFF state when $V_{TG} = 0.0V$. Red and blue represents the electron and hole density respectively.

net charge. This is why we see the negative capcacitance in the OFFF state.

At the device operation region, when the top layer potential contiues to be pulled up by the top gate. The barrier between the extension region to the overlap region decreases as we can see from Fig. 4.10(a) to (b). This results in the saturation and derease in the electron density in the top layer and ultimately results in the decreasing capcitance and negative capacitance in the operation region.

The electron density in the extension region continues to increase the whole time with the top gate.

4.3.6 Device Scaling and energy delay product

The device geometry discussed in this work has been kept to be $30+15nm$, which is too long for the modern transistor. The L_{ext} has kept to be longer than 10nm as discussed to keep both the OFF and SS performance. If the $L_{overlap}$ is scaled, the ON current would be scaled linealy with it. The energy-dleay product of a 32-bit adder that is composed of MoS2-WTe2 interlayer TFETs scaled from $30+15nm$ to $30+10nm$ to $5+10nm$ with operation voltage $V_{DD}=0.3V$ is plotted in comparsion with BP-TFETs [12, 72] with their L_{ch} scaled from 15nm to 9nm, a 15nm WTe2 TFET [56] and high performance CMOS in Fig. 4.13. The NMOS and PMOS performances are assumed to be the same in this circuit. The 32-bit adder energy delay product is calculated by using BCB 3.0 [51], where the parasitic capacitances and interconnects are taken into account . The scaling of circuit parameters as a function of gate length is taken from ITRS 2011 roadmap.

Although MoS2-WTe2 stay charged even during OFF state, the negative capacitance resulting from the top layer charge neutralizing the bottom layer charge com-

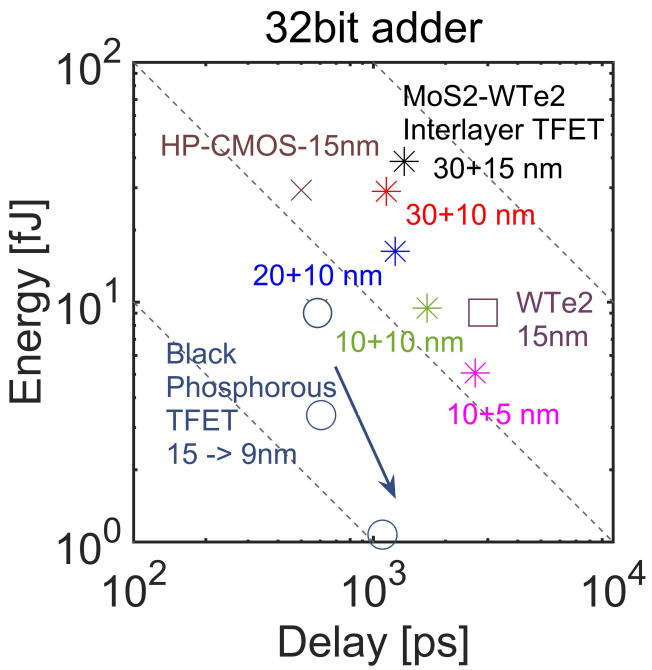


Figure 4.13. Energy-Delay product of MoS2-WTe2 interlayer TFETs with device channel scaled down from 55nm to 15nm in comparison BP-TFETs [12, 72] with their L_{ch} scaled from 15nm to 9nm, a 15nm WTe2 TFET [56] and high performance CMOS.

pensates the total capacitance. As a result in the energy-delay product, MoS2-WTe2 interlayer TFETs show a bit improvement from WTe2 and HP-CMOS. However, overall energy-delay performance of interlayer TFETs still cannot beat the BP-TFET.

4.3.7 Conclusion

In conclusion, MoS2-WTe2 interlayer TFET is studied. The model assumptions have been carefully examined. The band diagram aligned with transmission shows the switching mechanism is the energy filtering. The MoS2-WTe2 interlayer TFET shows a SS smaller than $60mV/dec$. The extension region is critical for the device to turn off. An optimized device can achieve an ON current of $1000\mu A/\mu m$ with

$V_{DD} = 0.3$.This suggests MoS2-WTe2 interlayer TFET as a promising candidate for low power applications. The energy-delay product of a 32 bit adder made of such interlayer TFETs shows a improvement from WTe2 and HP-COMS, but still needs improvement compared to BP-TFETs.

Part of this work is published in [13]. I acknowledge the help from Daniel Valencia and Dr. Yaohua Tan in getting the DFT simulations in Fig. 4.9 and also Dr. Yaohua Tan in getting Fig. 4.7(b) and (c). This work was supported in part by the Center for Low Energy Systems Technology (LEAST), one of six centers of STARnet, a Semiconductor Research Corporation program sponsored by MARCO and DARPA. The use of nanoHUB.org computational resources operated by the Network for Computational Nanotechnology funded by the US National Science Foundation under grant EEC-1227110, EEC-0228390, EEC-0634750, OCI-0438246, and OCI-0721680 is gratefully acknowledged.

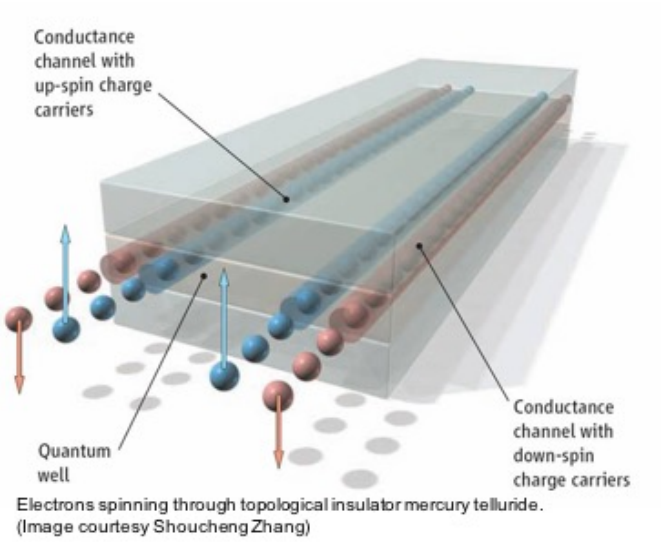


Figure 5.1. The edge states of a topological insulator. The surface states usually has the spin momentum lock, in which electron transport in one direcion can only have one spin direcion. Figure from [103].

5. TOPOLOGICAL INSULATOR

This charpter is a modiefied version of ref. [14, 15].

5.1 Introduction to Topological Insulators

Topological insulator (TI) materials such as Bi2Te3 have extraordinary surface properties [3–5]. These make them a unique class of materials for applications such as low power electronic devices [6], spintronics [5], and quantum computation [7, 8]. TIs host surface states or edge states with the spin perpendicular to the surface normal, spin-locked relative to the electronic in-plane momentum as shown in Fig. 5.1.

Backscattering of such surface electrons requires spin-flip processes. In TI devices that are free of magnetic impurities, surface electron backscattering is therefore unlikely. Then, the surface conductance is expected to be limited by the Fermi velocity [104]. Experimental values of the Fermi velocity of Bi2Te3 surfaces show more than 25 percent variation [105–107]. Experiments that determine Fermi velocities and other TI surface properties are often implicitly assuming different TI surfaces host the same physics [8, 108, 109]. Even many theoretical studies of TI wires assume all wire surfaces are equivalent due to rotational wire symmetry [110–114]. This assumption is only true for wires grown along [001] direction. In contrast, fabricated Bi2Te3 nanowires are grown in [110] direction as shown in Fig. 5.2 and often have rectangular cross sections [115, 116]. The crystal structure of [110] Bi2Te3 nanowires shows different chemical surface composition: Some surfaces are composed of Te atoms only and other surfaces contain both Te and Bi atoms. To capture this important fact of the surface chemistry requires atomistic simulations. Only then, the important effect of in-surface confinement of surface states can be simulated. It is shown in this work for Bi2Te3 nanowires that this effect confines surface states to wire surfaces with specific chemistry. It is expected that similar situations hold for other TI-materials and geometries. If experiments are set to surfaces that are unfavorable to the surface states, where the topological insulator surface states have a low density of states, the experimental setup can be effectively insensitive to the TI physics.

In this charpter, atomistic sp3d5s* (20 band, spin-orbit coupling included) tight binding bandstructure calculations of Bi2Te3 nanowires are presented. In agreement with literature the band gap of the Bi2Te3 nanowires is observed to close when the magnetic flux through the wire cross section is a half-integer flux quanta. [110–114] Deviations from literature are found in the details of the surface state energies and surface Fermi velocities: Fermi velocities of chemically different surfaces differ and create an effective surface-state confining potential around the wire surface. Guided by the atomistic results, the analytical Fermi velocity model of Ref. [110] is augmented

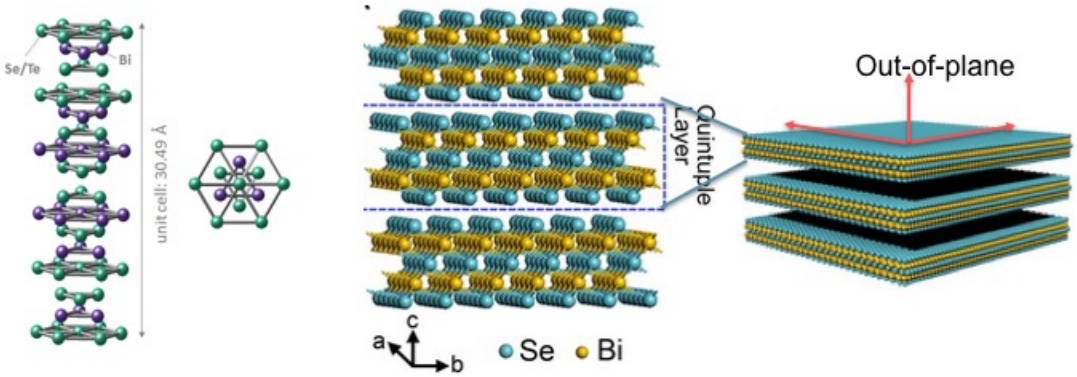


Figure 5.2. Atomistic structure and the quintuple layers of Bi2Se3 (similiar to Bi2Te3). Firgure come from [117]

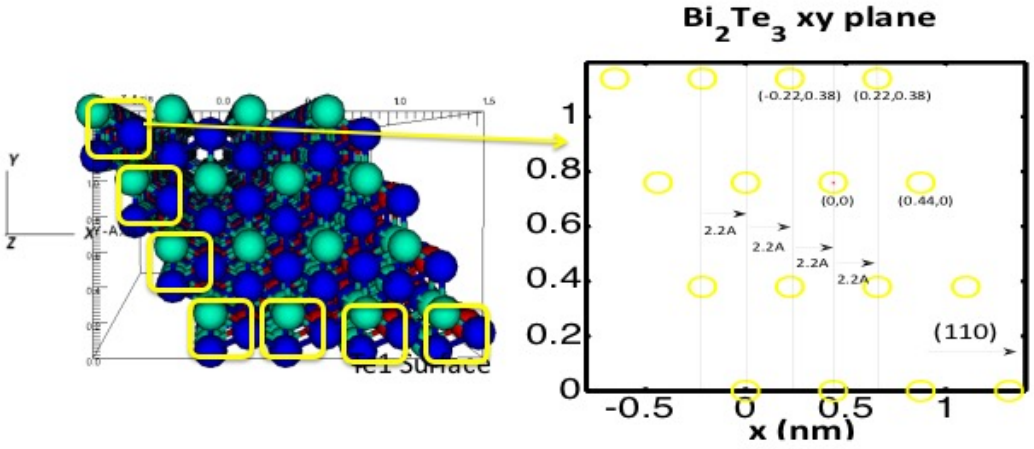


Figure 5.3. The crystal direction [110] for Bi2Te3.

to cover these differences of the wire surface chemistry.

In the following section, the two methods used in this work are presented. This covers the atomistic tight binding features of NEMO5 and the analytical model of Ref. [110] augmented to cover variations in the wire surface chemistry. In this chapter, the atomistic tight binding bandstructure results of NEMO5 for Bi2Te3 nanowires in the presence of magnetic fields are verified against literature [110]. Bandstructures of

rectangular Bi2Te3 nanowires with different ratios of pure Te and mixed atom type surfaces are presented then. These bandstructures serve as fitting targets for the surface Fermi velocities of the analytical model. Confinement effects of the surface states are shown after that. The analytical model is then used to explain this confinement of the wire surface states. Finally the paper concludes with a summary of the finding.

5.2 Method

In this work, atomistic $sp3d5s*$ (20 band, spin-orbit coupling included) tight binding bandstructure calculations of Bi2Te3 nanowires are calculated with the multipurpose NanoElectronics Modelling Tool (NEMO5) [76]. A quintuple layer of Bi2Te3 consists of a sequence of five atomic layers: Te1, Bi, Te2, Bi, and Te1. "Te1" and "Te2" both denote Tellurium, but they differ in the chemical surrounding: The neighbor layers of Te1 consist of Te1 and Bi, whereas the Te2 atom layer lies between two Bi atom layers. Tight binding parameters for Bi2Te3 are taken from Ref. [118]. The framework of NEMO5 and tight binding parameters give a surface Fermi velocity of $4.04 \times 10^5 m/s$ for a 15nm thick Bi2Te3 layer which agrees well with experimental data of Ref. [119] as shown in Fig. 5.4. Pairs of degenerate states are combined into symmetric and anti-symmetric states. Magnetic fields are included with the Peierl's phase in symmetric gauge [120]. All presented atomistic calculations are numerically very intense and require typically about one million CPUs on the Blue Waters supercomputer.

To ease understanding of the tight binding results, the analytical model of Refs. [110–114] is augmented to support nanowires that are not rotationally symmetric along the transport axis. Typical examples for such wires are grown along [110] direction and are rectangular in the cross section. Such wires have two different types of facets: one type contains atoms of all types ("mixed surface"), while the second

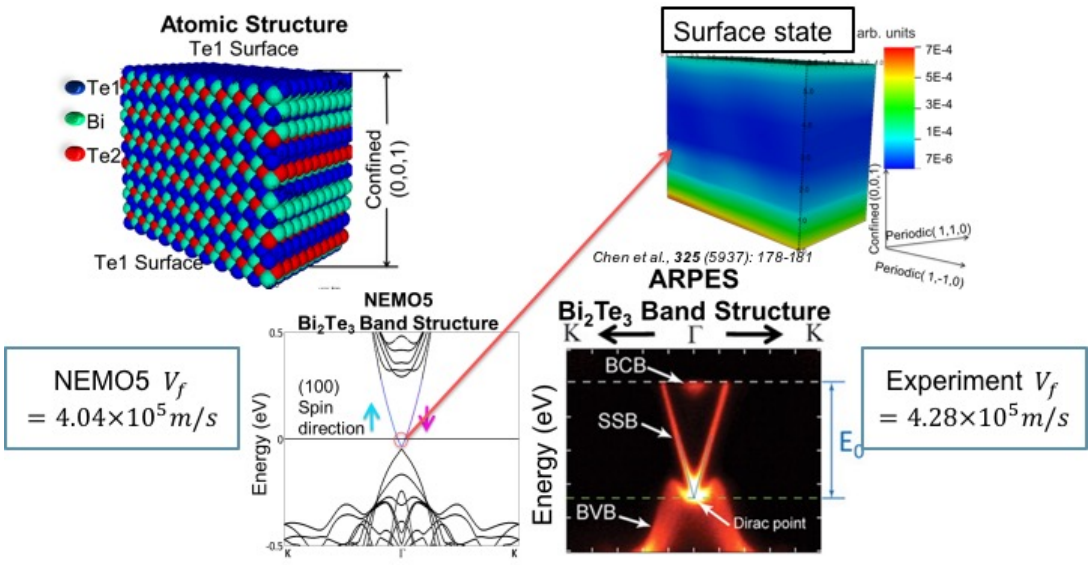


Figure 5.4. The band structure and the spin momentum lock of 3D TI material Bi2Te3. The Fermi Velocity calcuated from NEMO5 is matching the result from ARPES [119].

consists of Te1 atoms (referred as "Te1 surface"). For these surface types, different Fermi velocities are assumed: v_{f1} for the mixed surface and v_{f2} for the pure Te1 one. The energy difference of the wire surface states ΔE with vanishing momentum (k = 0), is assumed to be

$$\Delta E = \begin{cases} \frac{V_{f1} \cdot h}{P} & \text{Type I , } W > T \\ \frac{V_{f2} \cdot h}{P} & \text{Type II, } T > W \end{cases} \tag{5.1}$$

Here, P is the perimeter of the wire, equals to $(2W + 2T)$; W is the dimension of one mixed surface ("width of the wire") and T is the dimension of one pure Te1 surface ("thickness of the wire"). The two Fermi velocities are fit to match the surface state quantization of the tight binding results.

If not stated otherwise: all figures show tight binding results. All considered Bi2Te3 wires are grown along [110] direction.

5.3 Aharonov-Bhom Effect in TI nanowires

It is an accepted rule in literature that the band gap of TI nanowires closes when the magnetic flux through the wire cross section agrees with half integer multiples of the magnetic flux quantum ($\Phi_0 = h/e$). The largest band gap of the TI wires is expected with magnetic fluxes equal to integer multiples of the flux quantum as shown in Fig. 5.5.

However, this knowledge is based on non-atomistic models (i.e. envelope function approximations). Fig. 5.6 show the atomistic tight binding bandstructures of Bi2Te3 nanowires with varying magnetic fields along the wire growth direction. Here, the smaller facets are pure Te1 type. The atomistic calculations indeed follow the rule of vanishing and maximal band gaps as a function of the magnetic flux. Equivalent behavior was observed for atomistic tight binding calculations of Bi2Te3 nanowires for a great variety of cross sections (ranging from $12 \times 3nm^2$ to $150 \times 30nm^2$). Atomistic tight binding calculations showed that different geometries and facet configurations do not alter the rule for band gap maxima and minima.

The atomistic tight binding model with the Peierl's phase factor of NEMO5 reproduces the band gap dependence on magnetic fields as discussed in Ref. [110] The calculated oscillations of the magnetoconductance in these nanowires for different gate voltages agree qualitatively with experimental data of Ref. [116] (see Fig. 5.8). One dimensional helical states are observed in the wires agreeing with Ref. [121] (see Fig. 5.7).

In addition, a calibration of NEMO5 results to experimental conductance as a function of magnetic field is done as shown in Fig. 5.8. Experimental data is obtained from our collaboration Luis Jauregui from Prof. Yong Chen's lab in Purdue. Bi2Te3 nanowire FET transporting along [110] direction is fabricated. The channel potential

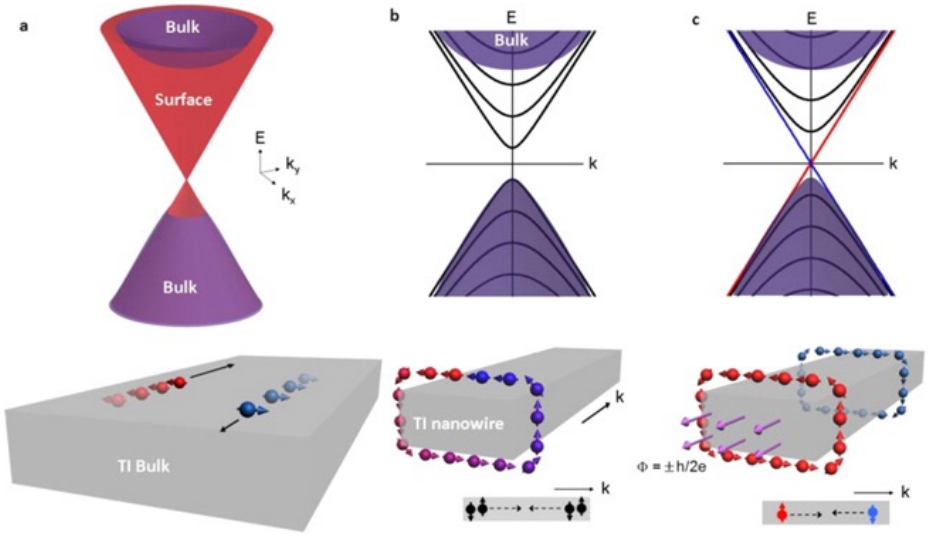


Figure 5.5. Topological surface band evolution in TI nanowires. (a) Top: Schematic band structure of bulk topological insulator. Surface states (red) exist in parallel with bulk conduction/valence band (purple). Bottom: electrons in the surface band are moving in two-dimensional surface, of which spin is defined by electron momentum (no spin degeneracy). (b) Top: band structure of a topological insulator nanowire (with no magnetic field). Topological surface band transforms to discrete 1D subbands (black color bands) with spin degeneracy. Bottom: electron spin is constrained in the tangent plane picking up a π Berry′s phase by a 2π rotation of electrons along the perimeter, which opens a gap in the 1D modes. (c) Top: band structure of a topological insulator nanowire (with magnetic flux $\Phi = \pm h/2e$). The gapless bands (red and blue) is not spin degenerated and topologically nontrivial, referred as 1D helical mode. Bottom: electrons of opposite spin orientations propagate in an opposite manner. Figure from [121].

is tuned by gate voltage Vg. Since the density of states start to increase for both energies that are above and below the Dirac point (Fig. 5.8(b)), the conductance reaches to minima when the fermi level is aligned with Dirac Point (Fig. 5.8(a)). If we choose the different V_g, and apply magnetic field along the transport direction, the conductance would osscilate with magnetic field with a periodicity of Φ_0. This is confirmed both experimentally and theoretically (Fig. 5.8(c) and (d)).

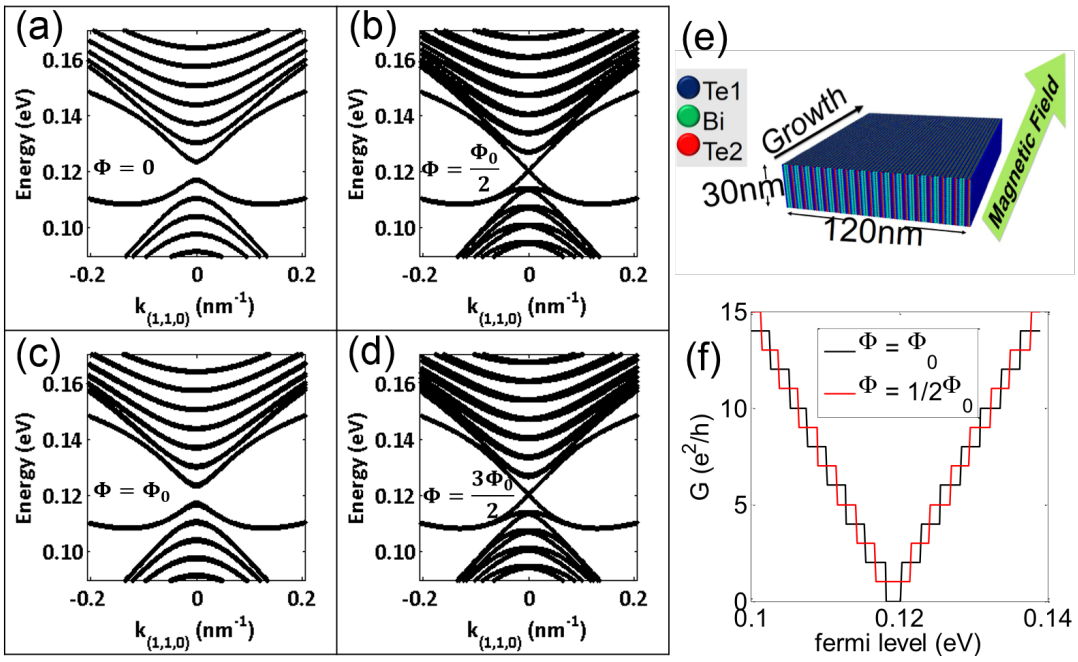


Figure 5.6. Bandstructures of $12 \times 48nm^2$ Bi2Te3 nanowires (type I) with varying magnetic field along the wire axis. The wire banstructure without a magnetic field (a) or with a magnetic field corresponding to the magnetic flux quantum (c) has the largest band gap and every state is double degenerate. Bandstructures with magnetic fields corresponding to 0.5 (b) and 1.5 (d) magnetic flux quanta have disappearing band gap and are only degenerate at k=0.(e) Device structure of a Bi2Te3 with a cross sectional area of $30 \times 120nm^2$. The direction of the magnetic field is in parallel with the growth direction [110]. (f) The conductance of (e) with different magnetic fields.

5.4 Surfaces of Different Atomic Compositions in TI nanowires

Although different wire configurations follow the same rule for the band gap with magnetic fields, the band structure details depend significantly on the ratio of pure Te1 and mixed facet dimensions. This is exemplified in Fig. 5.9(a) compare the atomistic structure of two Bi2Te3 nanowires that differ in the size of the pure Te1 and mixed facets. For later reference, wires with larger mixed than pure Te1 facets are termed "Type I", the other cases as "Type II". The bandstructures of the two cases in Fig. 5.9(b) show an energy difference of the wire surface states with vanishing mo-

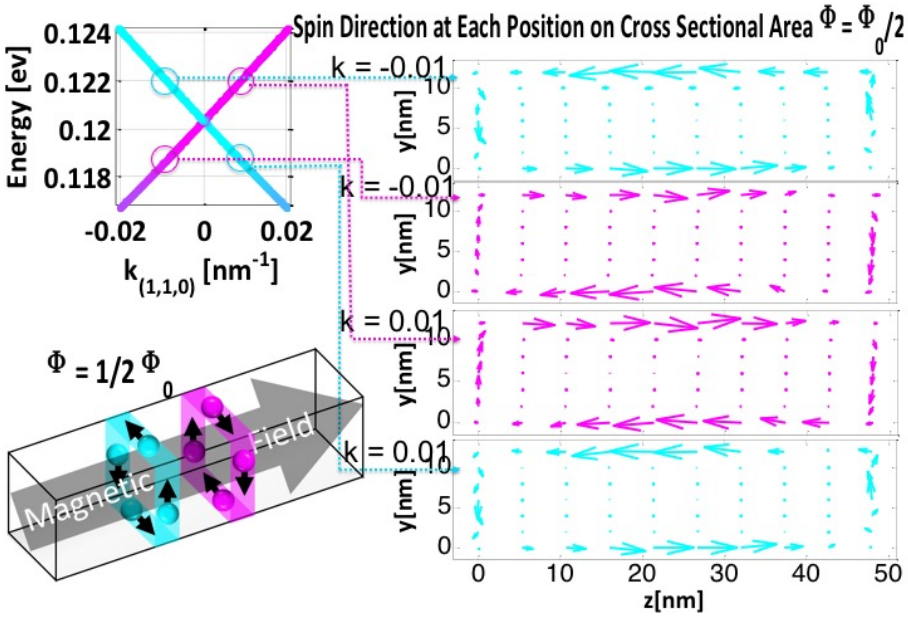


Figure 5.7. 1D helical surface states of a $48 \times 12nm^2$ Bi2Te3 nanowire with a magnetic field of 3.5949T solved with NEMO5 for the two (E,k) tuple as indicated in the bandstructure in (a). The color represents different spin orientations in (b). Electrons of the same energy and opposite spin orientation propagate into opposite direction as illustrated in (c).

mentum of 6.2meV for the type I and 10.5meV for the type II nanowire of Fig. 5.9(a). This difference is in contrast to non-atomistic models that cannot distinguish wires of type I and type II. Fig. 5.10 illustrates differences in the bandstructures of type I and type II rectangular Bi2Te3 nanowires with a cross sectional area of $150 \times 60nm^2$.

5.5 Different Fermi Velocities for Different Surfaces

Fig. 5.11 show the as a function of the perimeter of Bi2Te3 nanowires grown in [110] (a) and [001] (b) direction. In all cases, the longer edge of the wire cross section is kept constant to 48nm, while the smaller edge varies. For [110] grown wires of type I, the mixed surface is kept constant, while for type II wires, the pure Te1 surface is constant. Please note that all surfaces of [001] wires are of mixed atom

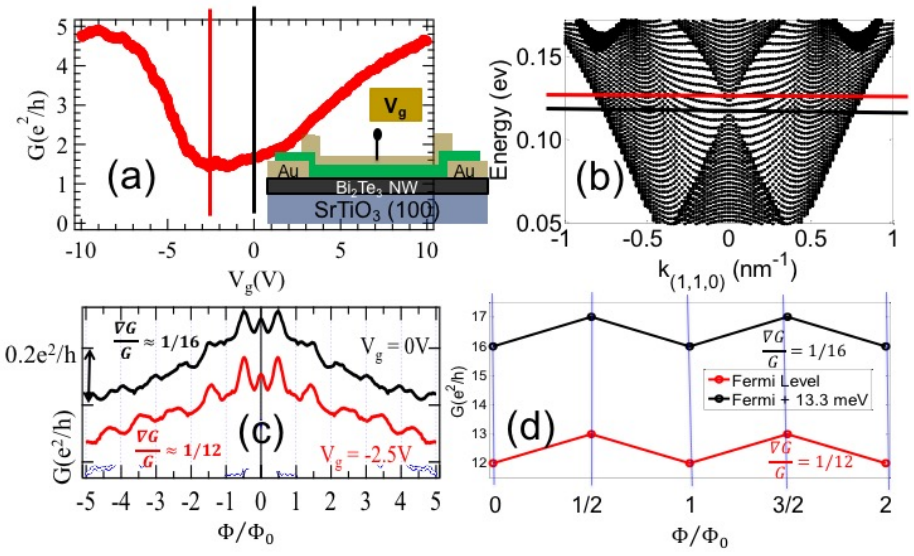


Figure 5.8. (a)Experimental measurement of conductance as a function of gate voltage by shifting Fermi level. (b) The conductance minima corresponds to the gate voltage that aligns the Fermi level to the Dirac Point. (c) Experimental Magnetoconductance as function of magnetic flux Φ in units of magnetic flux quanta $\Phi_0 = h/e$ for magnetic fields applied parallel to the axis of the nanowire in Ref. [116,122] at two different gate voltages. NEMO5 simulation results (d) agree qualitatively with (c).

type and equivalent. Therefore, a type I and type II distinction is meaningless for [001] wires, i.e. the surfaces A and B are equivalent. Therefore, nanowires grown in [110] direction show a strong dependence of on the facets ratio configuration, while of [001] wires is virtually independent of that. Due to the linear nature of all results shown in Fig. 5.11, the analytical model discussed in the method section gives an almost perfect fit to the numerical atomistic tight binding data. It turns out, the Fermi velocities for the [110] wires are $V_{f1} = 1.28 \times 10^5 m/s$ and $V_{f1} = 4.36 \times 10^5 m/s$ and and for the [001] wires $V_{f1} = V_{f2} = 1.28 \times 10^5 m/s$. Note that mixed surfaces that are chemically equivalent (i.e. having the same portion of Te1, Te2 and Bi atoms) have always the same Fermi velocity, irrespective of the wire growth direction.

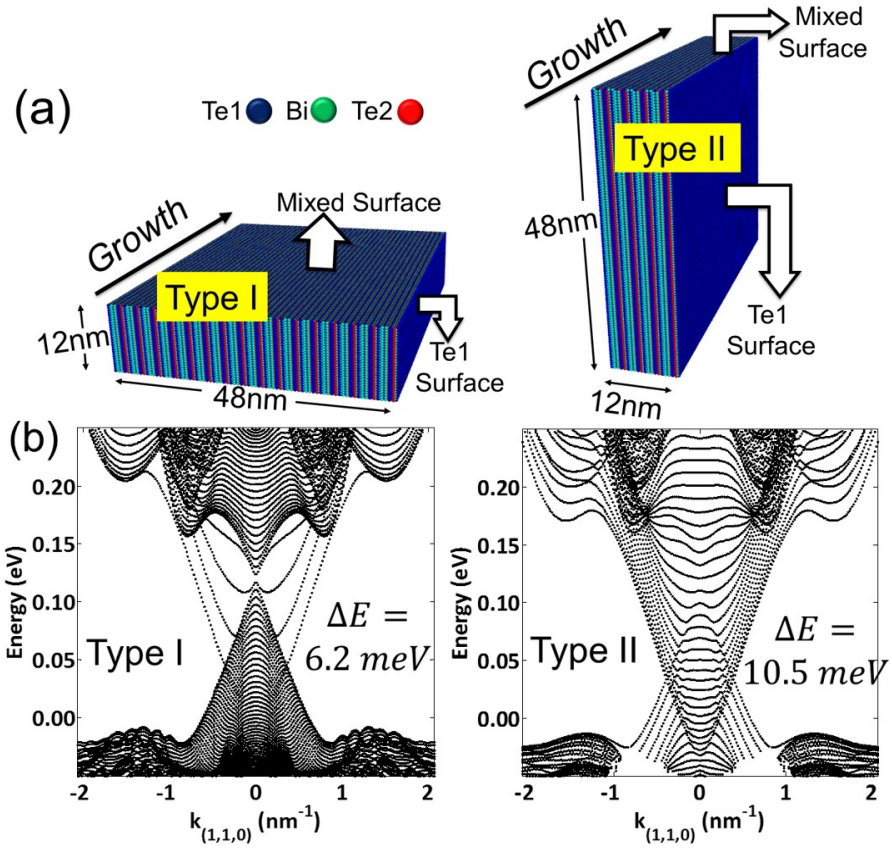


Figure 5.9. (a) Atomic structures of 12x48 nm2 Bi2Te3 nanowires grown along the [110] direction in the two possible surface configurations. In the type I wire, the pure Te1 facet is much smaller than in the type II configuration. (b) Bandstructures of the nanowires of (a) show different quantization energies for the surface states at k=0.

The values of the Fermi velocities vary with the size of the bigger facet (kept constant in Fig. 5.11. For instance, if the bigger facet has the dimension of 120 nm the following Fermi velocities are found $V_{f1} = 1.39 \times 10^5 m/s$ and $V_{f1} = 4.50 \times 10^5 m/s$ as shown in Fig. 5.12 and Fig. 5.13.

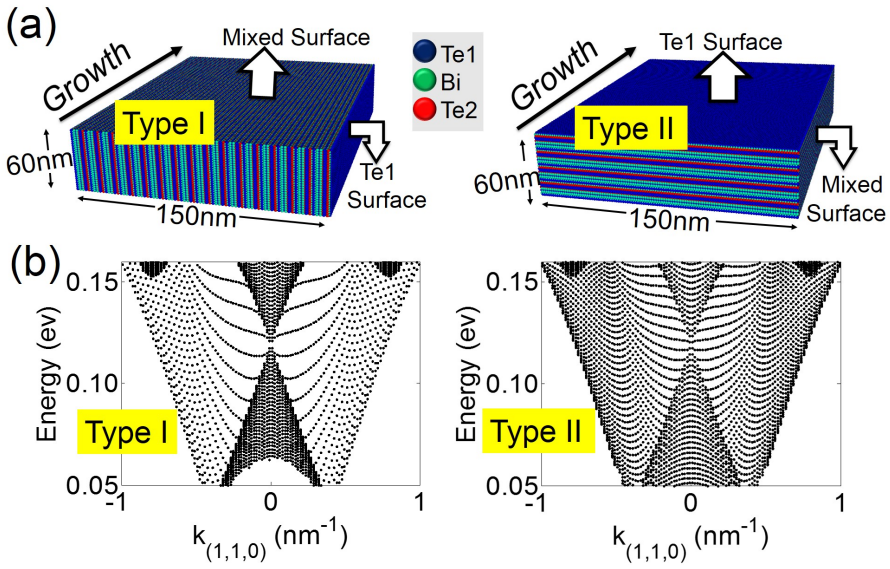


Figure 5.10. (a) Atomic structures of $60 \times 150nm^2$ Bi2Te3 nanowires grown along the 110 direction. The facets with only Te1 atoms are larger in type I than in type II wires. (b) Bandstructures of the nanowires of (a).

5.6 In-surface Confinement of Wavefunctions

This change in the Fermi velocity indicates confinement effects within the wire surface. This in-surface confinement is illustrated in Fig. 5.15 which show the absolute squared wavefunctions for the first 3 surface states of the type I nanowire in Fig. 5.14 with energies above about $0.12eV$ and momentum $k = 0.025nm^{-1}$. The surface states are delocalized over the total wire surface, but they are mainly located at the mixed type facets. The number of minima of the surface states envelope (shown in Fig. 5.15(b)) increases with the state's energy – similar to confined electronic states in quantum wells. The calculations also show stronger in-surface confinement effect with increasing momentum. The in-surface confinement vanishes at the Γ-point. This finding can be understood with the analytical model of Eq. 5.1: The dispersion difference of the two different nanowire facets (pure Te1 and mixed type) yields an effective, momentum dependent potential between the facet types (see schematic of

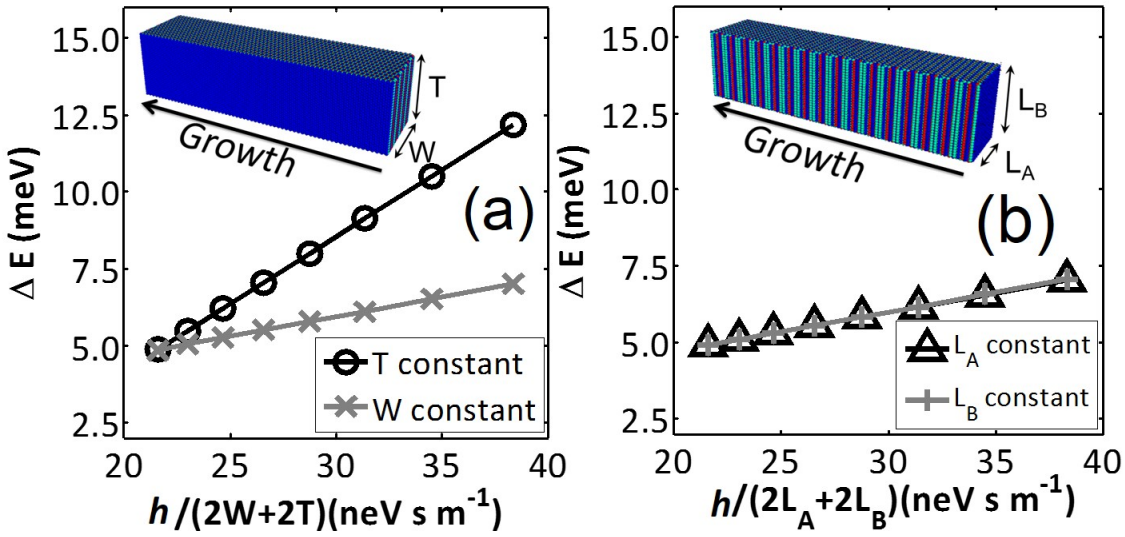


Figure 5.11. Surface state quantization energies as a function of the inverse wire perimeter for Bi2Te3 nanowires grown in [110] direction (a) and in [001] direction (b). Different facets of [110] wires differ in their chemistry and give different quantization energies. This is in contrast to [001] wires. Surface Fermi velocities result from linear approximations to these data.

Fig. 5.16(a)). This potential vanishes at the *Gamma*-point and increases with finite momenta. This potential effectively creates a system of 2 quantum wells within the wire surface (see schematic of Fig. 5.16(b)). The surface states envelopes′ confinment is typical for such quantum wells.

5.7 Conclusion

In this chapter, NEMO5's atomistic tight binding models are applied on Bi2Te3 nanowire bandstructures for wires grown along [110] and [001] direction. The atomistic representation unveils for experimentally common, rectangular [110] nanowires two chemically different types of surfaces. It is imaginable that TI wires with other than rectangular geometries still host in-surface confinement if the facets are chemically distinct enough. Chemically distinct surfaces host topological insulator surface

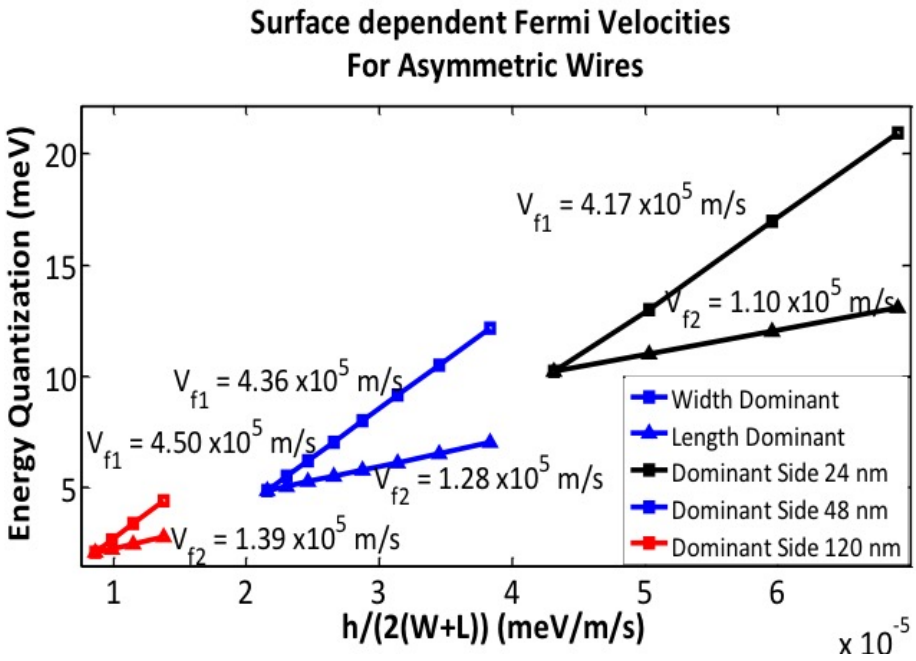


Figure 5.12. Surface state quantization energies as a function of the inverse wire perimeter for Bi2Te3 nanowires grown in [110] direction with different cross sectional areas. Different facets of [110] wires differ in their chemistry and give different quantization energies. This is in contrast to [001] wires. Surface Fermi velocities result from linear approximations to these data.

states with different Fermi velocities. The surface states spread over all facets, but they are subject to momentum-dependent in-surface confinement. This finding is critical for experiments on TI-surfaces: TI-properties should be measured only on TI-favorable surfaces. It is imaginable that variations of measured Fermi velocities in Bi2Te3 might trace back to the different Fermi velocities of the different surface kinds. This situation is different in [001] wires due to their chemically equivalent facets. Both situations can be well reproduced with an analytical model presented in this work as well. This work is published in [14, 15].

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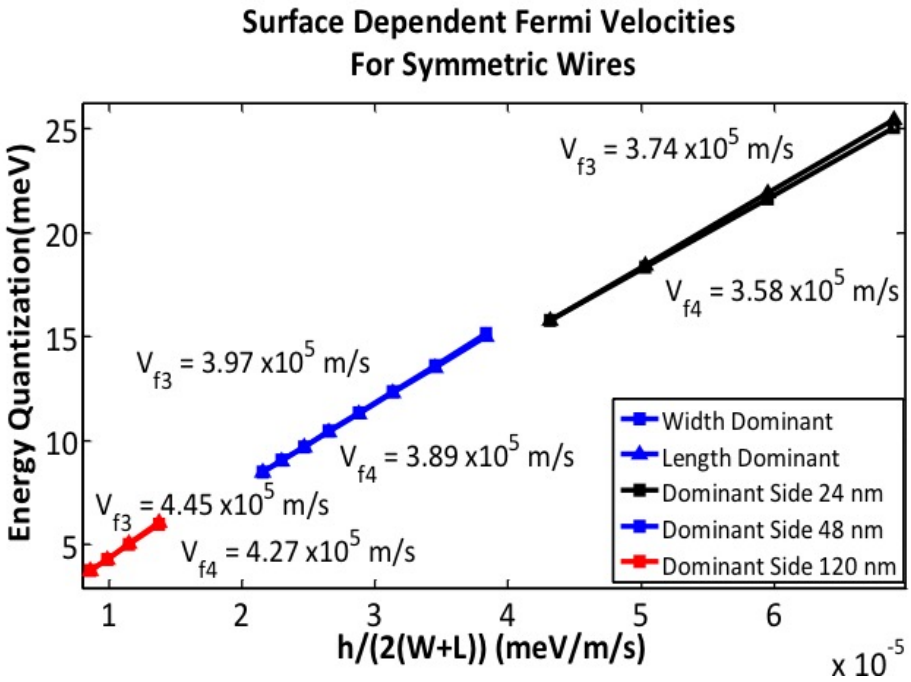

Figure 5.13. Surface state quantization energies as a function of the inverse wire perimeter for Bi2Te3 nanowires grown in [001] direction with different cross sectional areas. Surface Fermi velocities result from linear approximations to these data.

Semiconductor Research Corporation's (SRC task 2141) Nanoelectronics Research Initiative and National Institute of Standards and Technology through the Midwest Institute for Nanoelectronics Discovery (MIND), and the Intel Corporation.

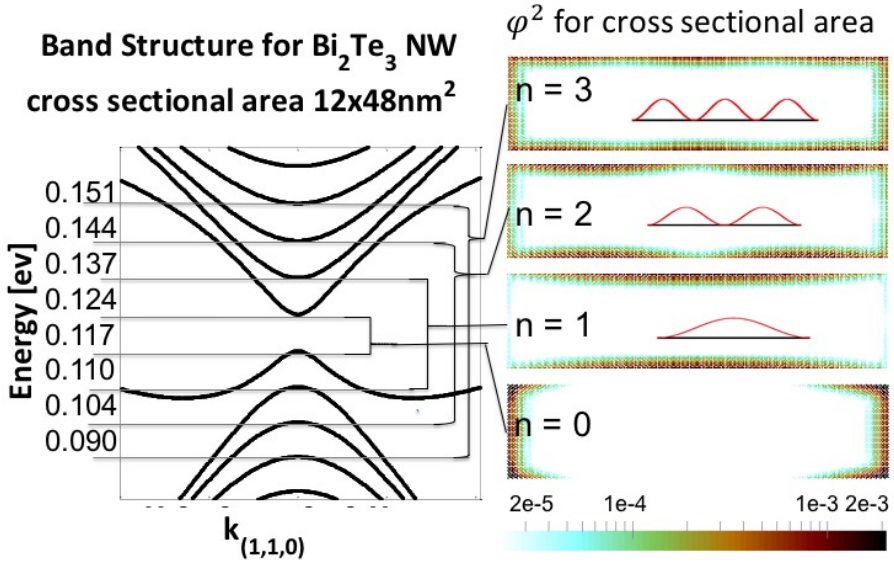

Figure 5.14. (a) Contour plot of the absolute squared wavefunctions of the 3 surface states right above the Dirac point of the type I Bi2Te3 nanowire of Fig.2(a) for the momentum $k = 0.025nm^{-1}$ in corresponding to the energy points in the EK diagram.

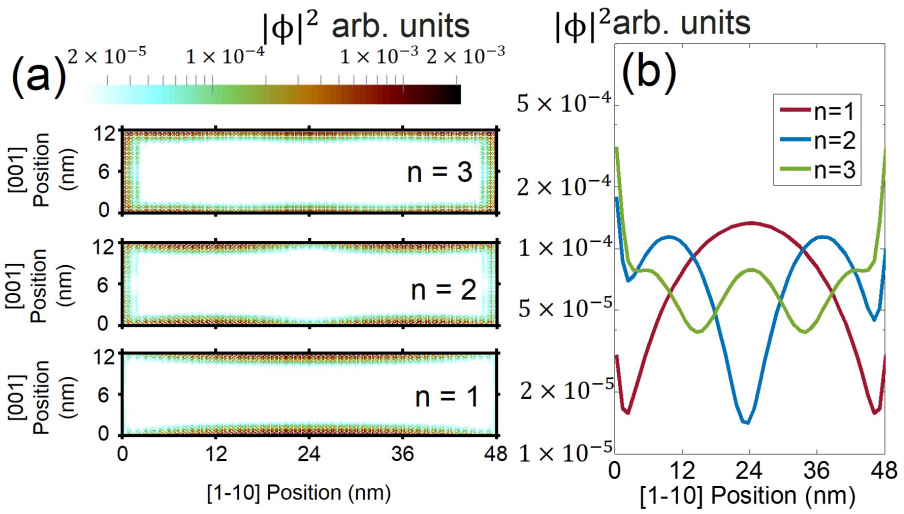

Figure 5.15. (a) Contour plot of the absolute squared wavefunctions of the 3 surface states right above the Dirac point of the type I Bi2Te3 nanowire of Fig.2(a) for the momentum $k = 0.025nm^{-1}$. (b) Unit-cell average of the surface states in (a) along the [001] wire coordinate. "n" represents the subband index and the number of maxima of the surface states envelope.

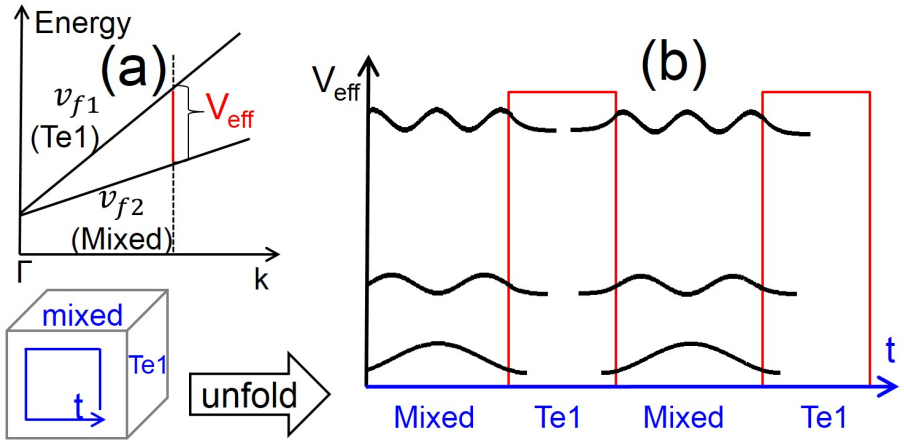

Figure 5.16. (a) Schematic surface state bandstructure of Bi2Te3 nanowires grown in (110) direction as shown in Fig. 5.9(b) with different Fermi velocities for the pure Te1 and the mixed surfaces. The different Fermi velocities cause an effective potential offset between the two surfaces for finite momenta (highlighted with V_{eff}). (b) The effective potential V_{eff} (red line) of (a) along the unfolded nanowire perimeter confines the surface states predominantly on the mixed surface (illustrated with schematic wavefunctions in black).

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