Ph.D Defense

Low power transistors and Quantum Physics based on Low Dimensional Materials

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Agenda

Motivation	• Why Tunnel FETs based on 2D materials
Method	• Non-equilibrium, Open Boundary Simulator NEMO5
Bilayer Graphene	• Experimental Benchmark • Electrostatically Doped Tunnel FET proposal
Interlayer TFETs	• Model Assumptions and Validation • MoS2-WTe2 interlayer Tunnel FET Device physics &Performance
Black Phosphorous	• Thickness Engineered Tunnel FET proposal

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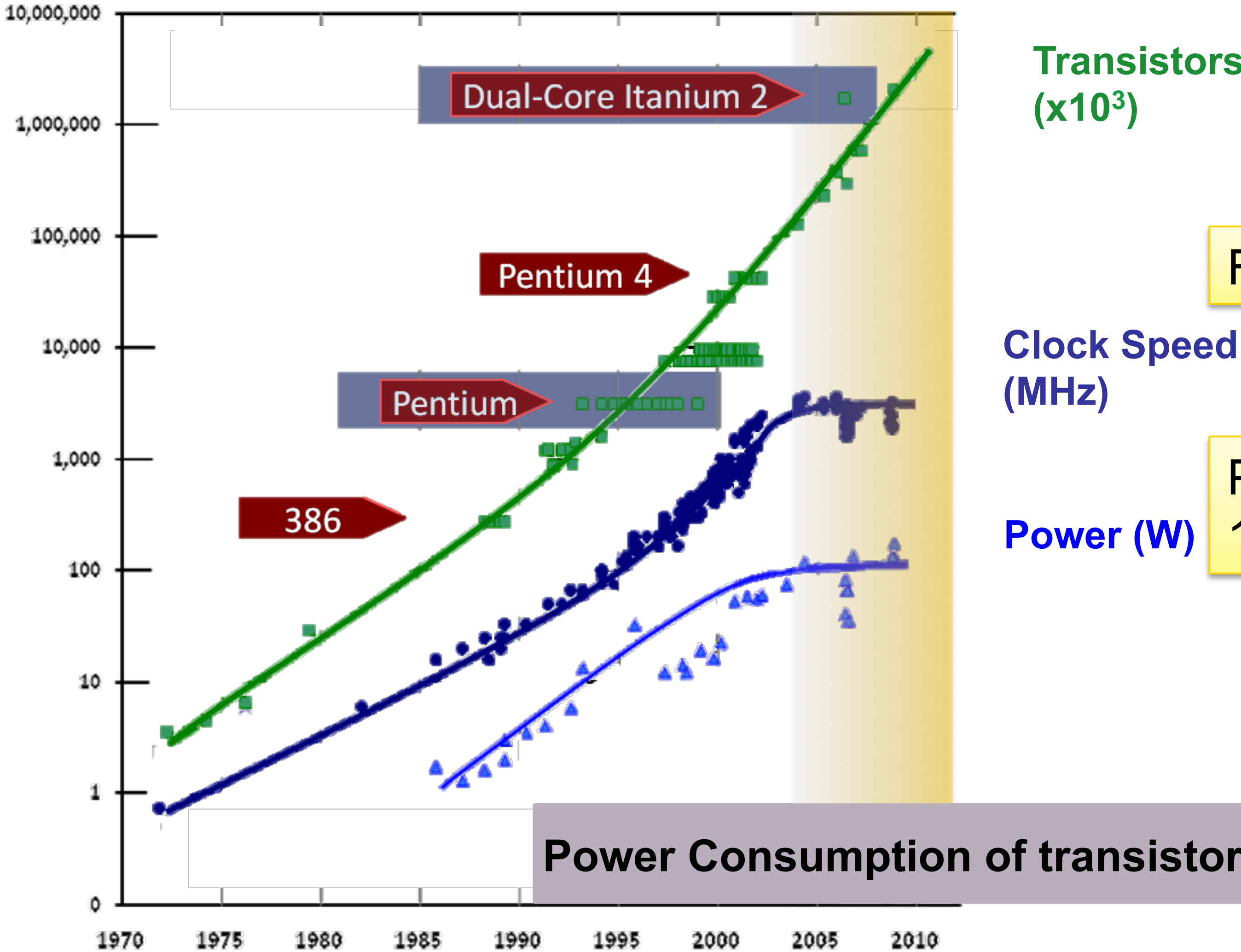
Challenges for Modern Electronics: Power Consumption

More transistors, but not faster processors



No. of Transistor ↑

Frequency Saturated

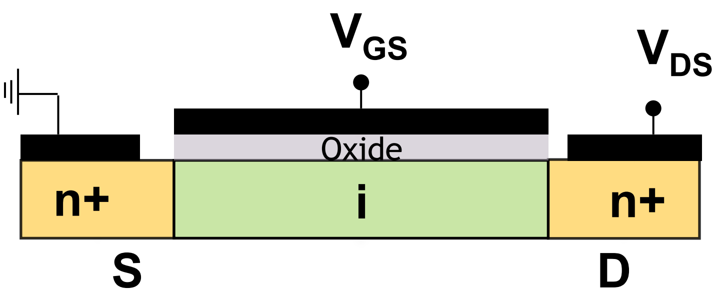
Power Dissipation Limit 100W/cm2

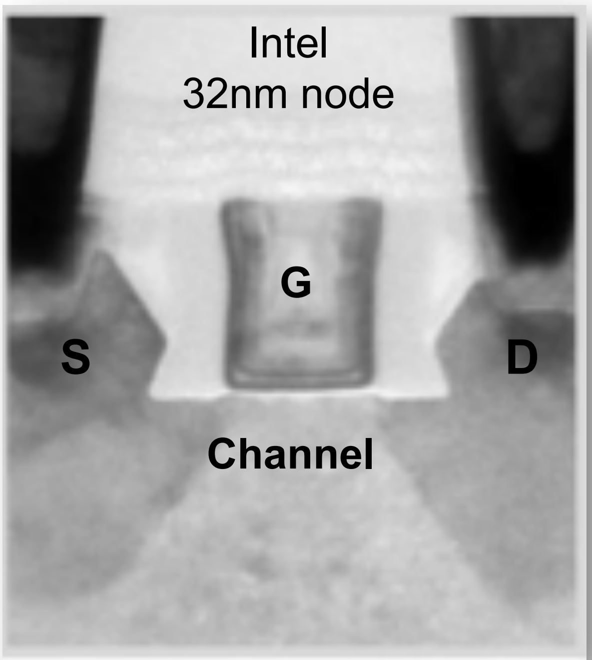
Power Consumption of transistors need to be reduced

Intel CPU Trends
(source: Intel, Wikipedia, K. Olukotun)

Reduce Power Consumption in conventional MOSFETs

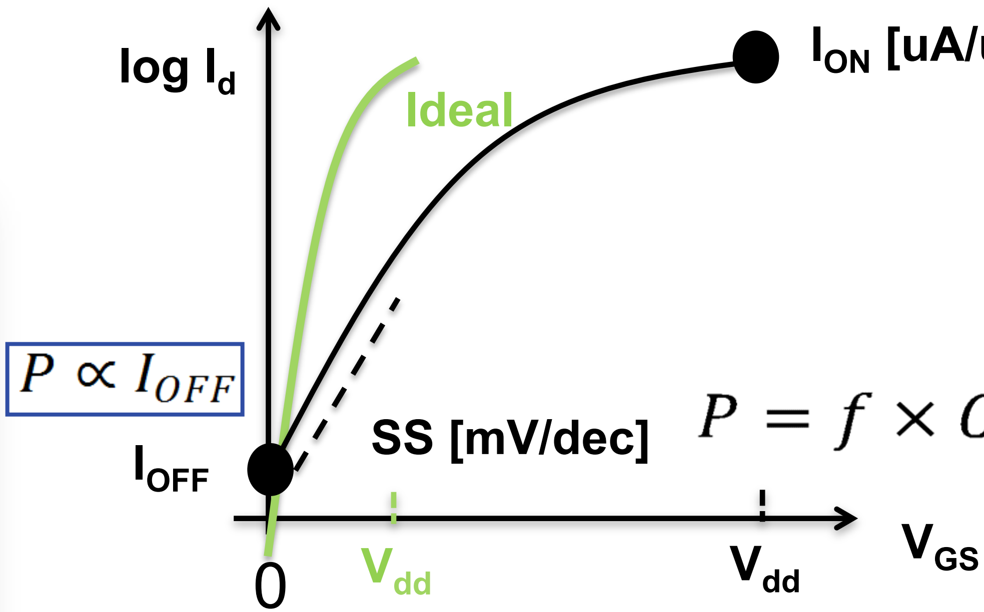
Transistor





Victor Moroz Berkeley Seminar 2011

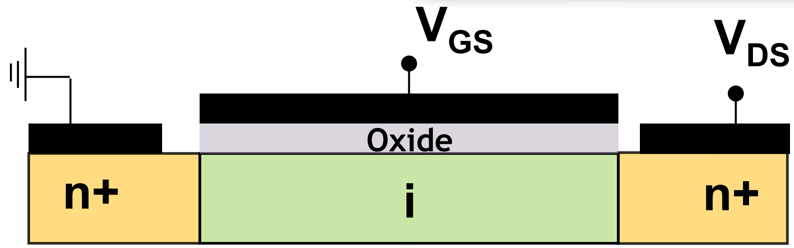
How to reduce the power consumption in a transistor?



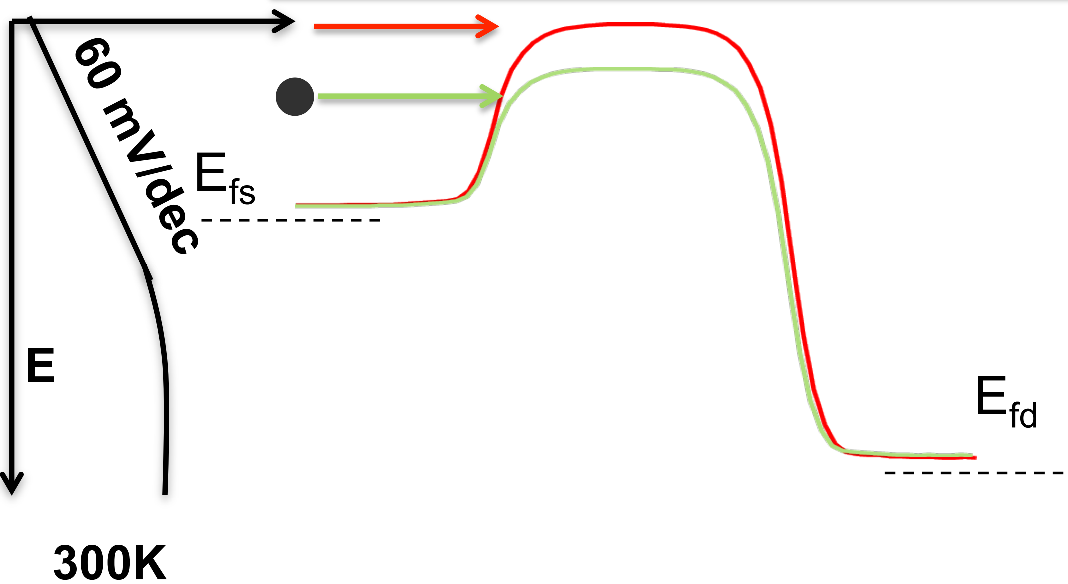
$$P = f \times C \times V_{dd}^2$$

Power Consumption ↓ → Vdd ↓; it requires:
(1) Keep Low I_{OFF} (2) Keep High I_{ON} (3) Small SS

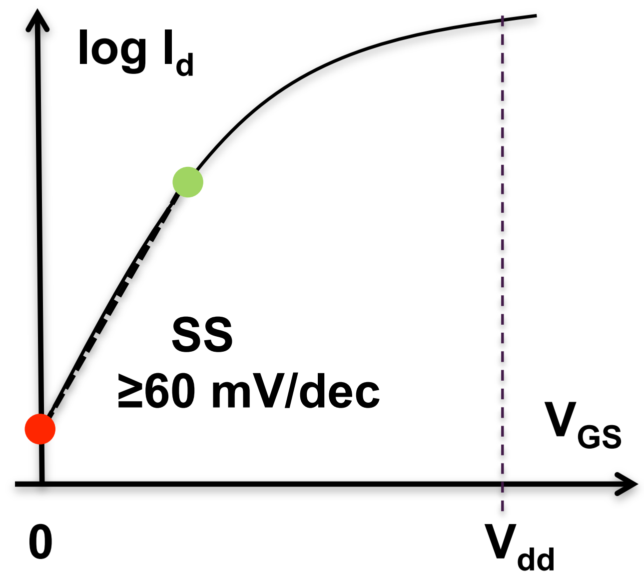
Fundamental limitation of MOSFETs



Thermionic Emission:
Electron: E >> Ef , at Fermi Tail



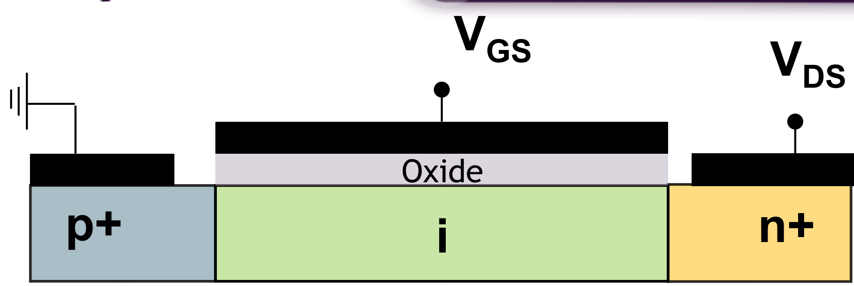
MOSFET



MOSFET: Thermionic emission → SS > 60 mV/dec

Solution to Steep Transistor Tunnel FET (TFET)

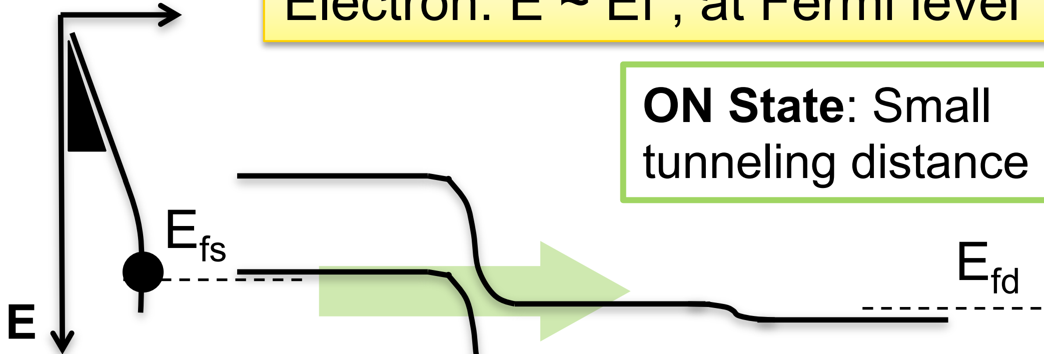
TFET



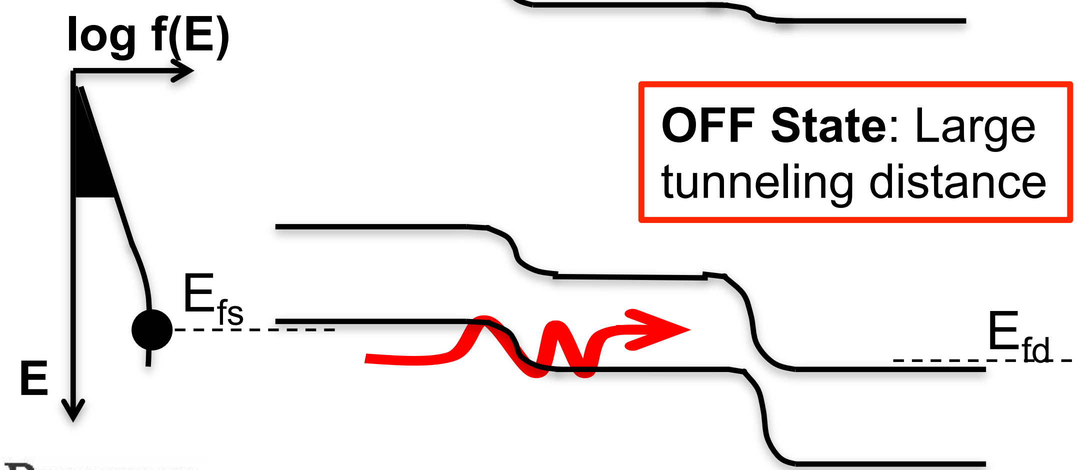
TFET → SS < 60 mV/dec → Vdd ↓ possible

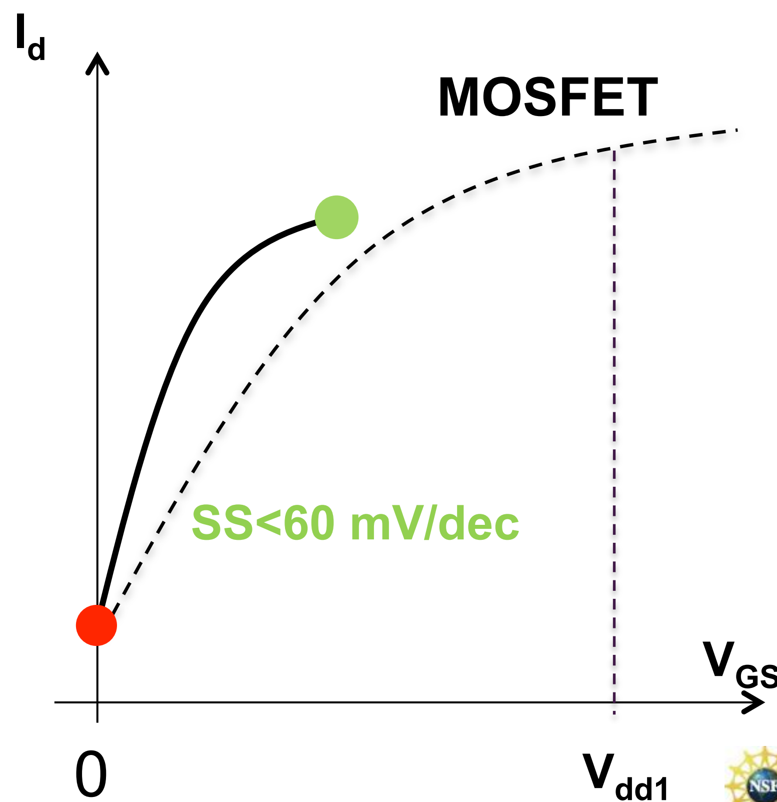
Electron: E ~ Ef , at Fermi level

ON State: Small tunneling distance



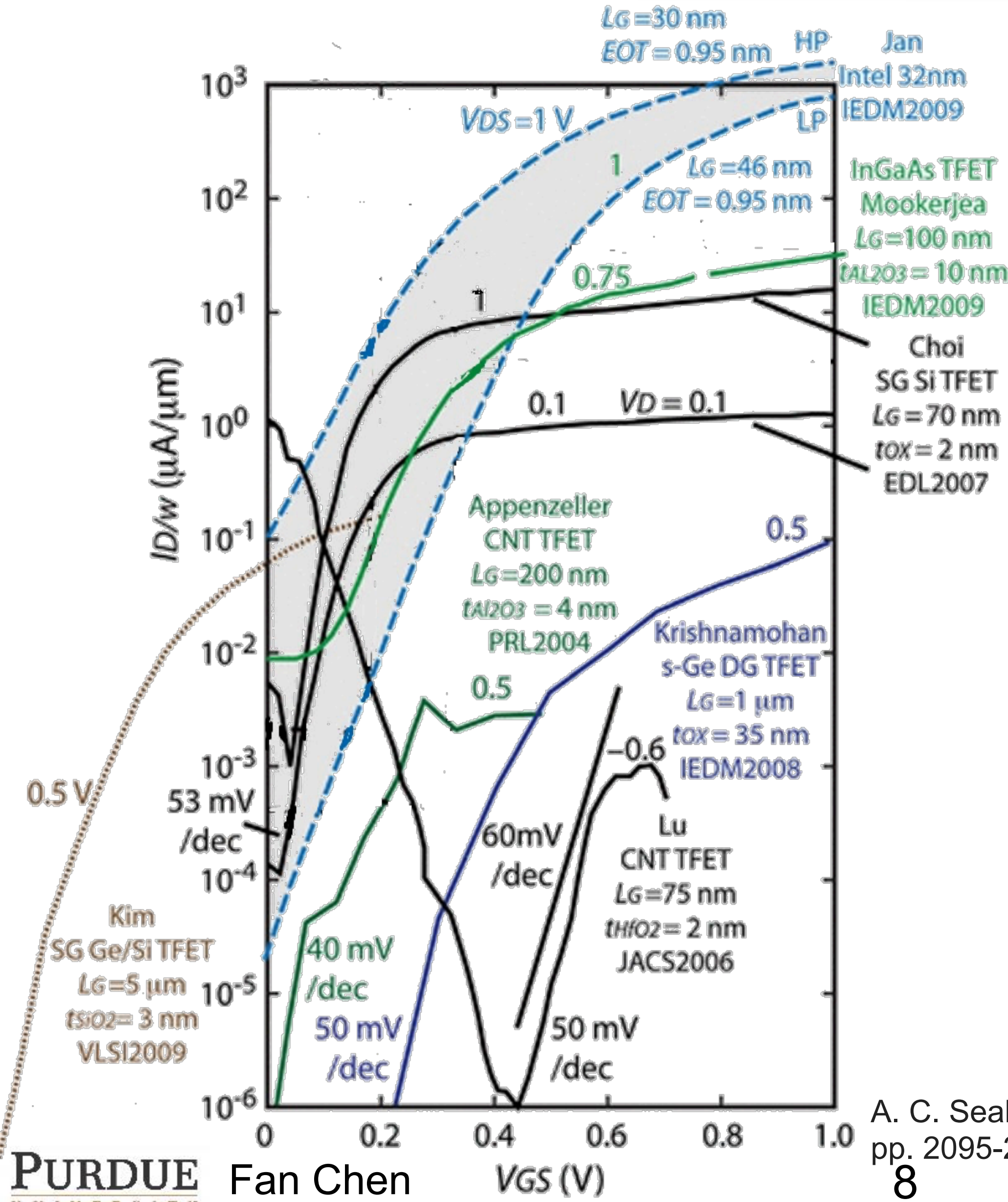
OFF State: Large tunneling distance

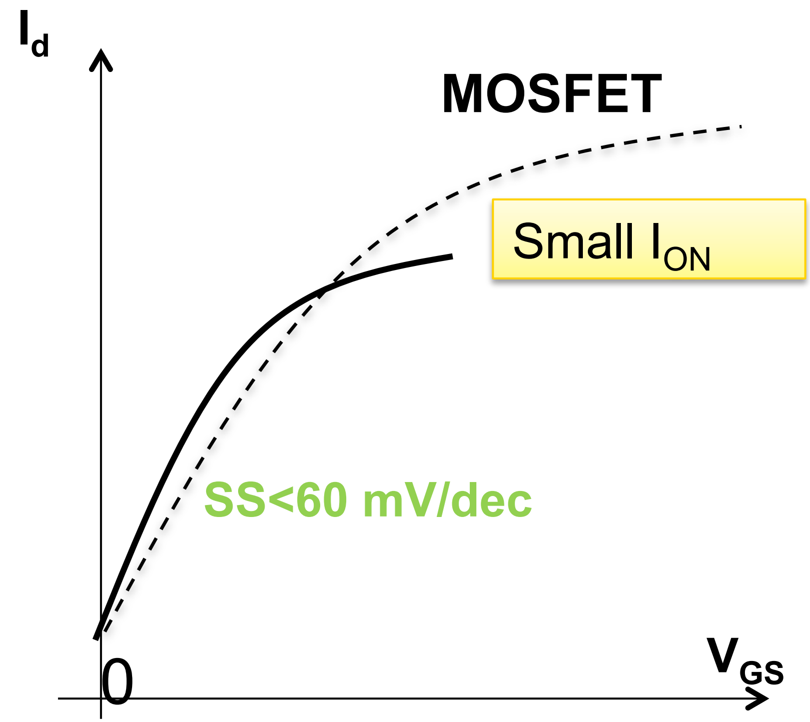




Major Challenge in TFETs

- MOSFET: I_{ON} ~ 1000 uA/um
- TFET: I_{ON} ~ 0.1-10 uA/um



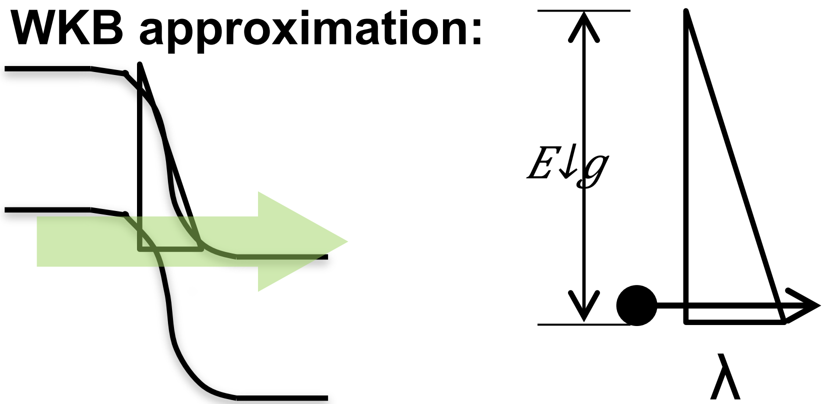


Challenge for TFETs: Small I_{ON}

A. C. Seabaugh, and Q. Zhang, Proc. of IEEE, 98, No. 12, 2010, pp. 2095-2110.

High ON requires small Tunnel Distance

WKB approximation:

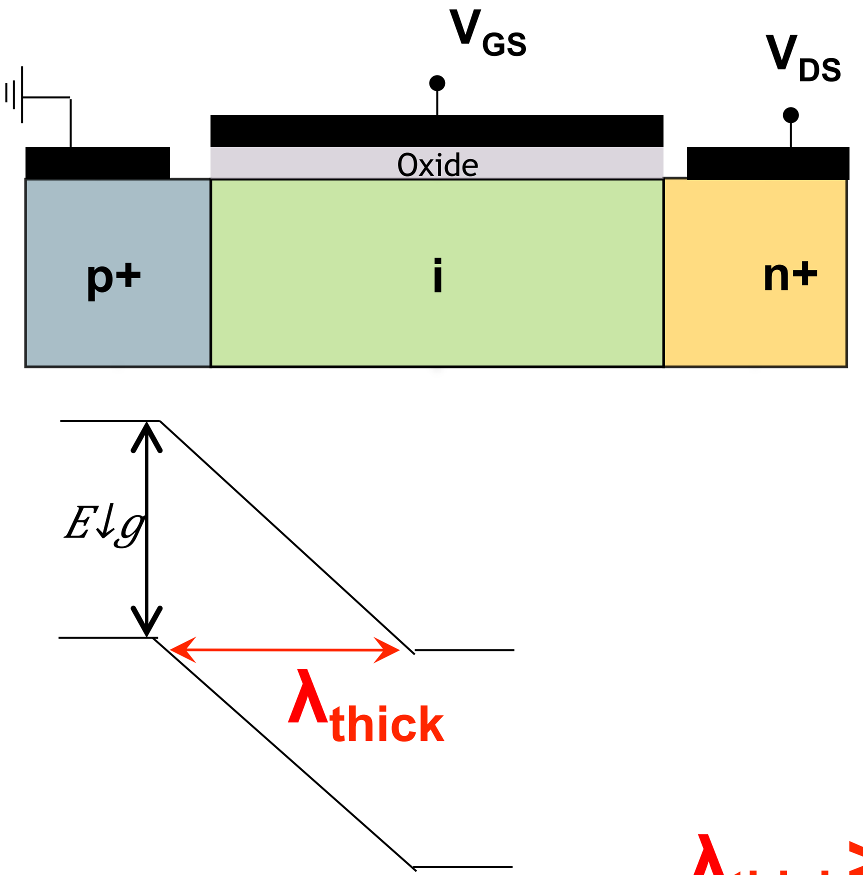


$$Trans \propto \exp\left(-\lambda \cdot \sqrt{m^* \cdot E_g}\right)$$

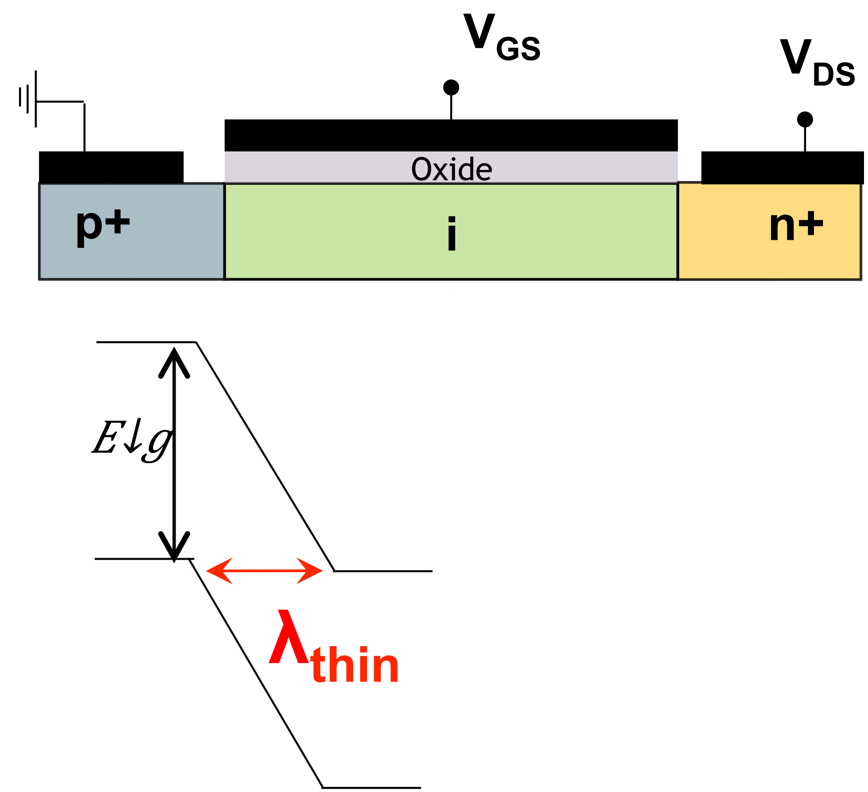
High ON needs Small Eg, small m*, shorter tunnel distance λ

Thin Channel has Smaller Tunnel Distance

Thick channel



Thin channel

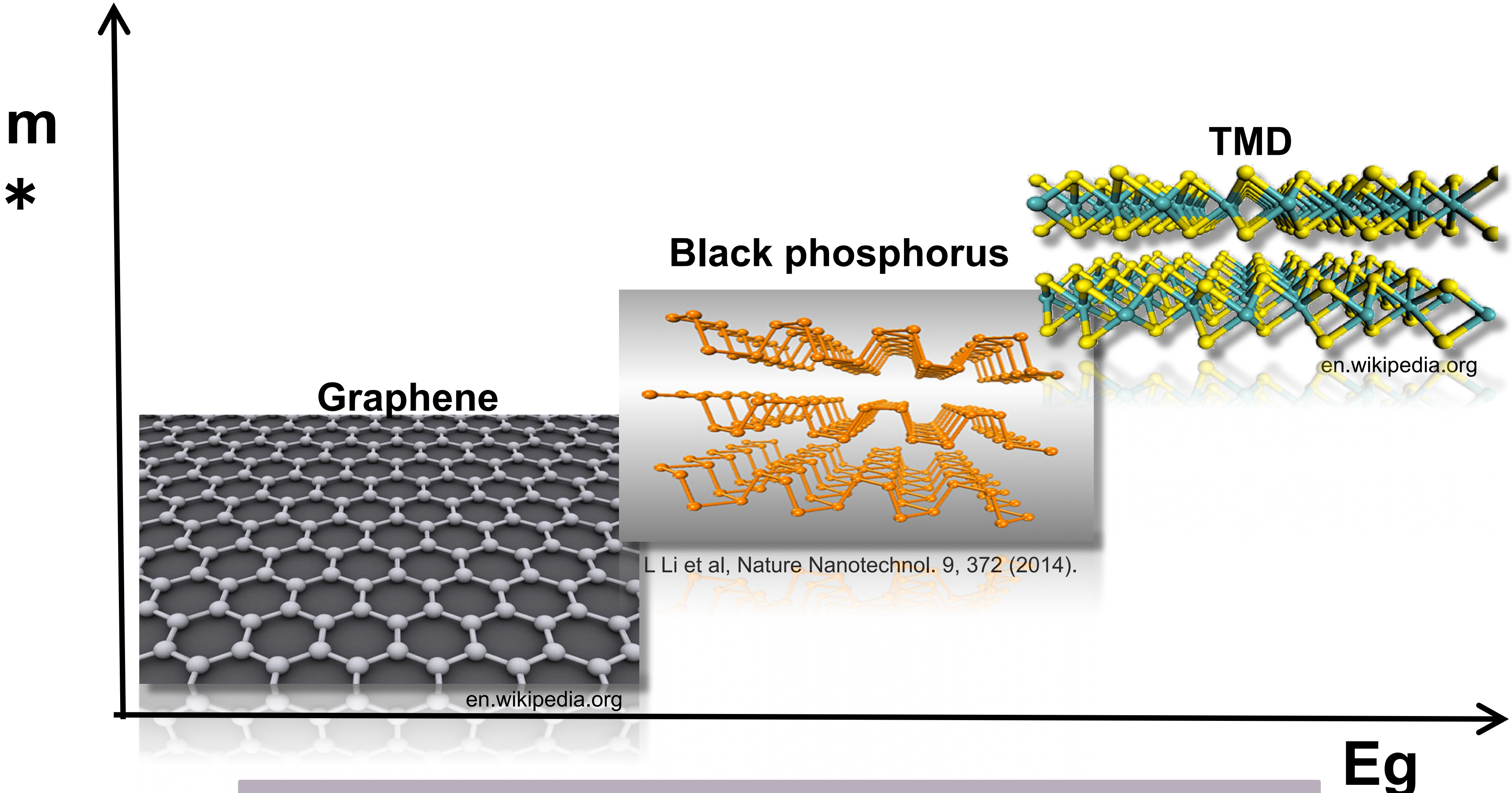


$\lambda_{thick} > \lambda_{thin}$

Thin Channel has smaller tunnel distance λ → High ON

2D Material Reduces Tunnel Distance

$I_{ON}\uparrow \rightarrow Trans\uparrow \rightarrow \lambda\downarrow \rightarrow t_{ch}\downarrow$



2D Material reduces tunnel distance λ

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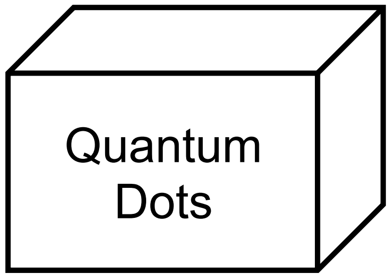
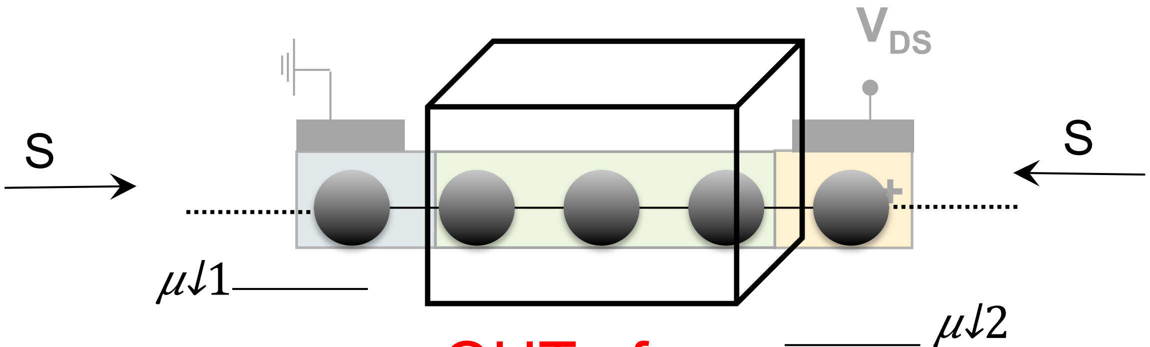
Closed Equilibrium



Well Defined Fermi Level μ_0

Open Boundary Non-Equilibrium

1. Injection S from contacts
2. Open Boundry
3. Channel is out of equilibrium



OUT of Equilibrium

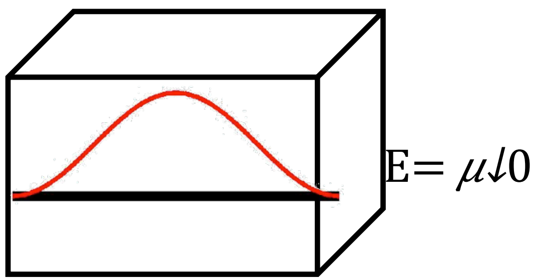
Transport in device requires non-equilibrium, open boundary Method

Non-equilibrium Open Boundary Method

Closed Equilibrium

$E\psi = H\psi$

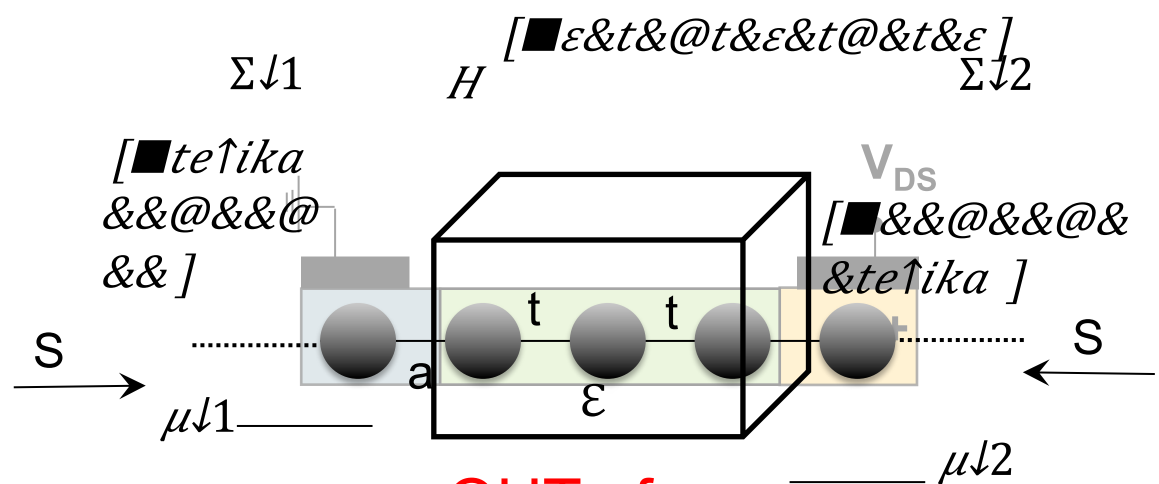
Schrodinger's Equation



Well Defined Fermi Level μ_0

Open Boundary Non-Equilibrium

$(E - H - \Sigma_1 - \Sigma_2)\psi = S$

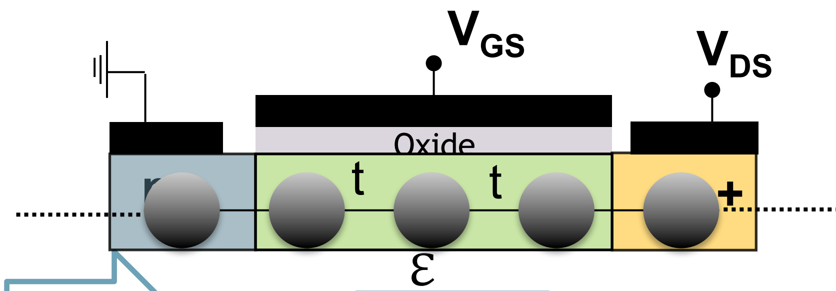


OUT of Equilibrium

Non-equilibrium, Open boundary Method Capture the required Physics

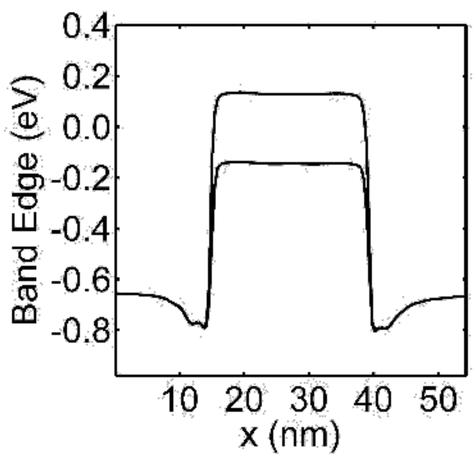
Self Consistent calculation

$\nabla(\epsilon \nabla \phi(x)) = -(p(x) - n(x) + Nd - Na)$



$\phi(x)$

H= [■ε−eϕ1&t&■& @t&ε−eϕ2&■t& @■@ &■t@ &■■⋱@t &■t@ε−eϕN]



$p(x) - n(x)$

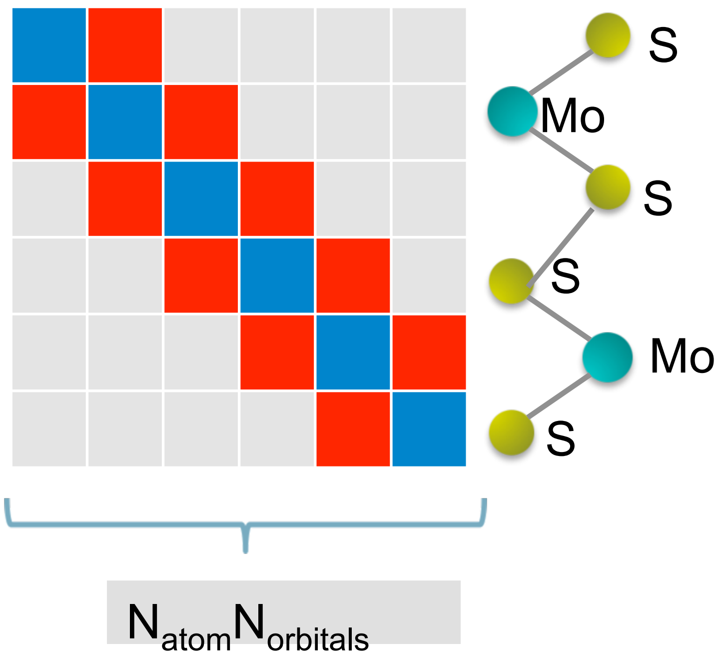
$S = (EI - H - \Sigma_1 - \Sigma_2)\psi$
$(p(x) - n(x)) \sim \psi \cdot \psi^{\dagger}$

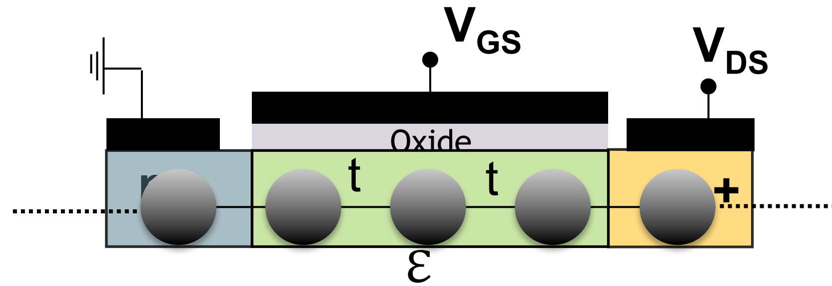
self-consistent calculation is performed for electrostatics

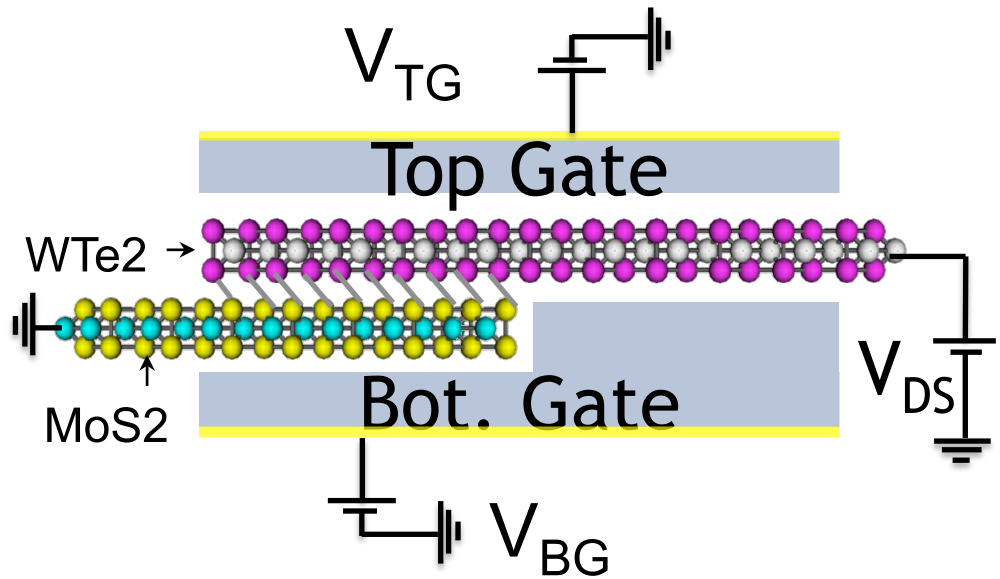
Hamiltonian based on atoms

- **Materials parameters**

Onsite ■ **Coupling** ■







The material parameters need to be obtained.

Device Modeling Simulator: NEMO5

Single layer MoS_2 band structure

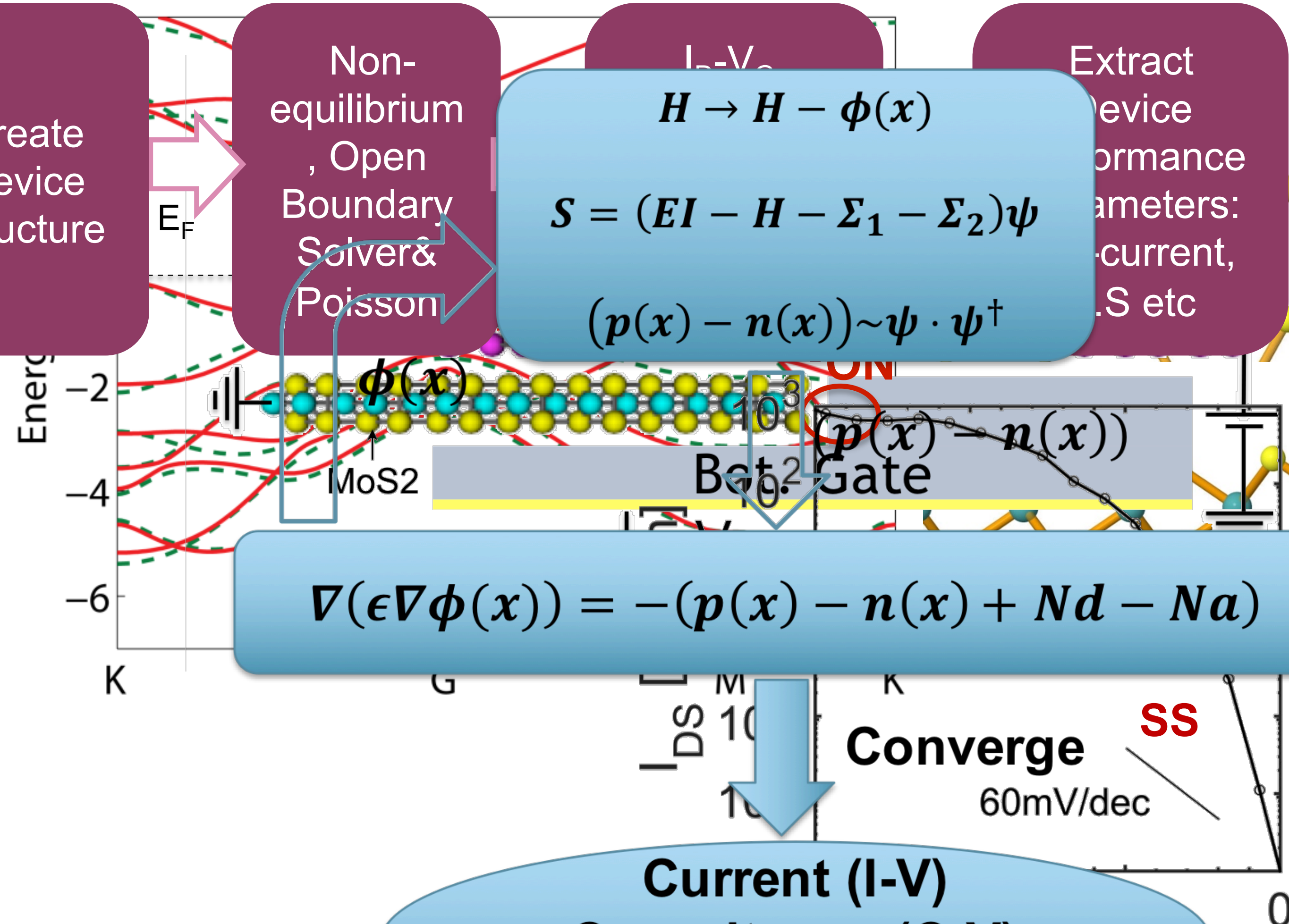
Obtain Parameters	Input	Self-consistent calculation	Output	Post Processing
Material Parameters such from DFT or literature	Create Device Structure	Non-equilibrium, Open Boundary Solver& Poisson	I_D-V_G	Extract Device Performance Parameters: current, SS etc

$$H \rightarrow H - \phi(x)$$

$$S = (EI - H - \Sigma_1 - \Sigma_2)\psi$$

$$(p(x) - n(x)) \sim \psi \cdot \psi^{\dagger}$$

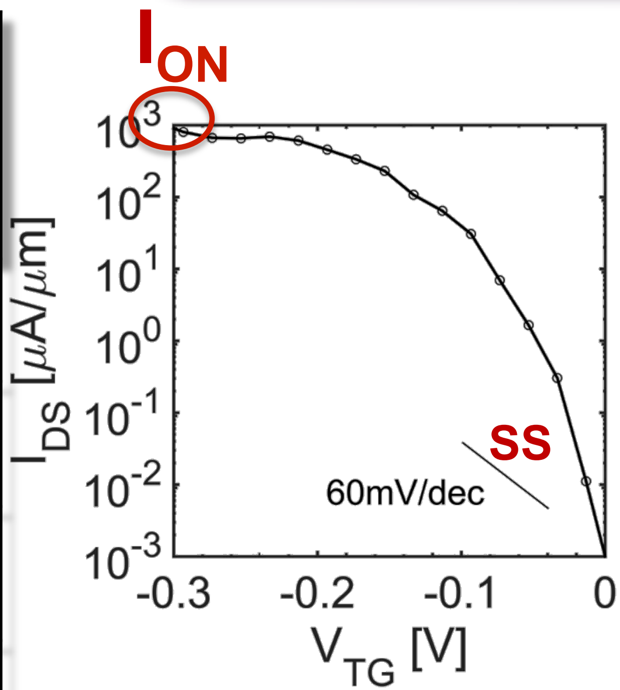
$$\nabla(\epsilon \nabla \phi(x)) = -(p(x) - n(x) + Nd - Na)$$

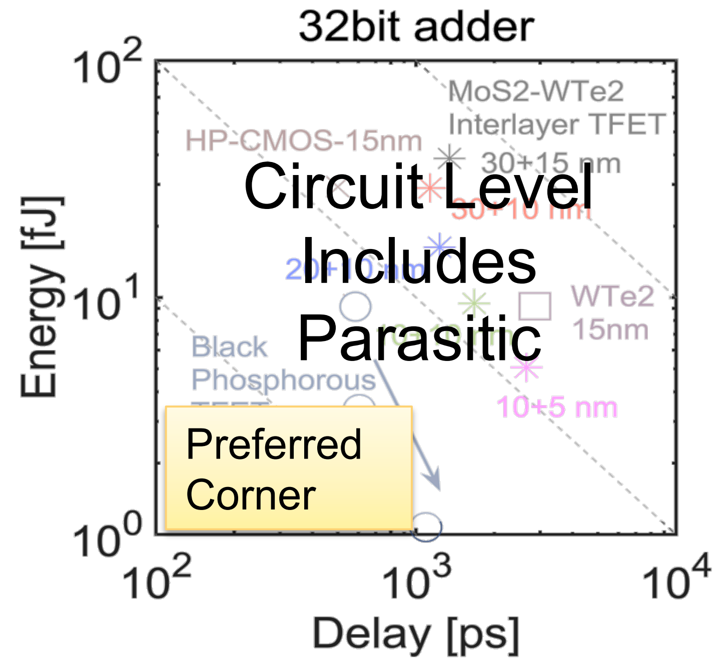


Converge

Current (I-V)
Capacitance (C-V)
Potential, Density

Device
VDD (V)
ION (uA/um)
SS (mV/dec)
Energy Delay Product
Scalability
Comments





Device Evaluation includes:
Vdd, ON, SS, Energy and Delay (circuit), Scalability and fabrication

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Motivation	• Power Dissipation Limit → TFET → Low ON → 2D
Method	• Open Boundary, Self-consistent and ballistic Calculation
Bilayer Graphene	• Experimental Benchmark • Electrostatically Doped Tunnel FET proposal
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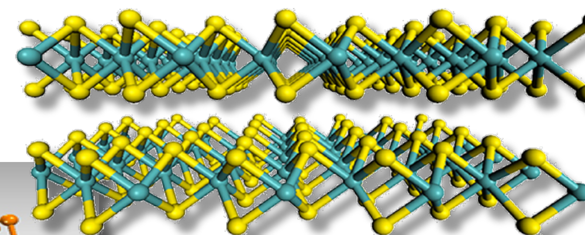
Choice of channel material for homojunction TFET

$$I_{ON}\uparrow \rightarrow Trans\uparrow \rightarrow \lambda\downarrow \rightarrow t_{ch}\downarrow$$

$$Trans \propto \exp(-\lambda \cdot \sqrt{m^*} \cdot E_g)$$

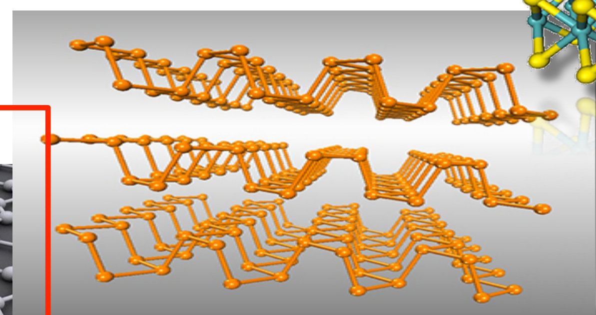
m*

TMD



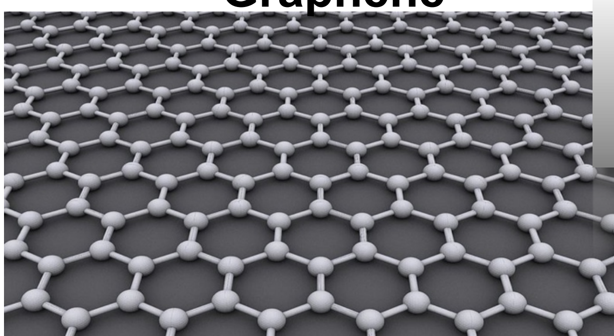
en.wikipedia.org

Black phosphorus



L Li et al, Nature Nanotechnol. 9, 372 (2014).

Graphene



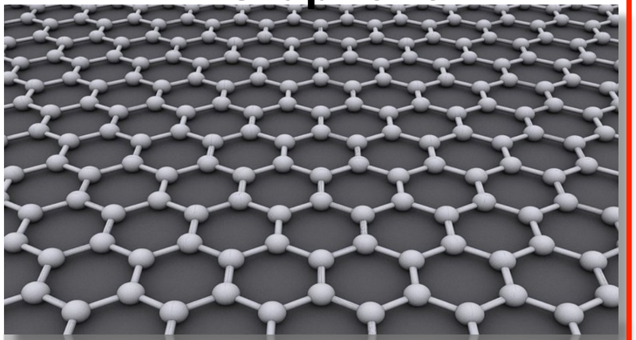
en.wikipedia.org

Eg

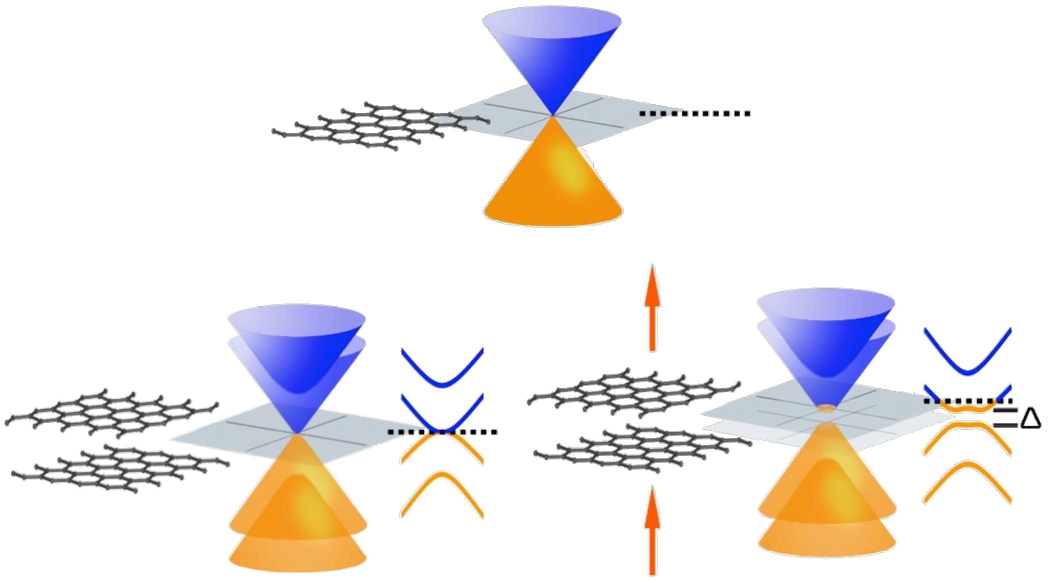
Graphene has the smallest combination m* and Eg for homojunction TFET

Bilayer Graphene: Tunable Eg

Graphene



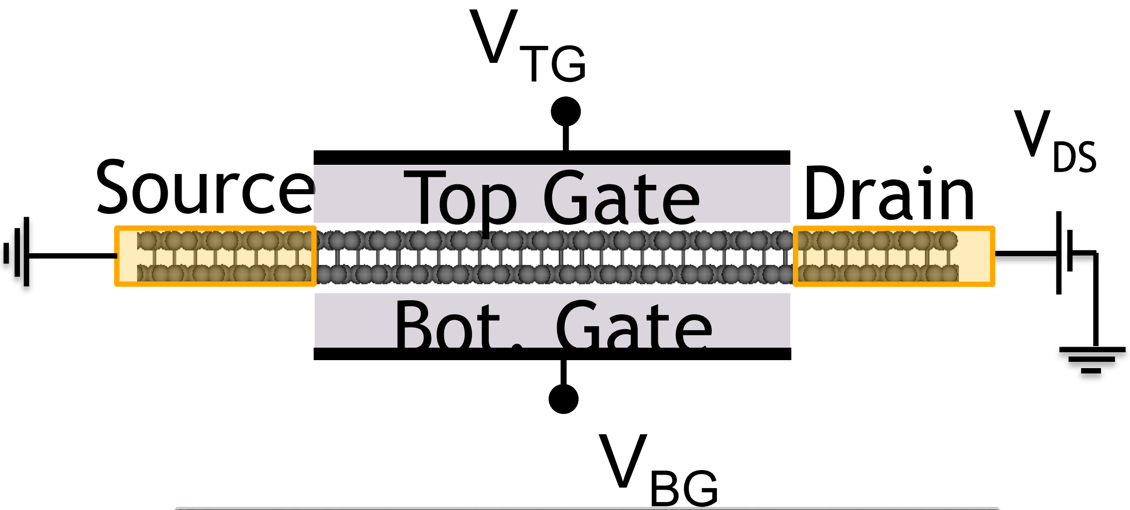
en.wikipedia.org

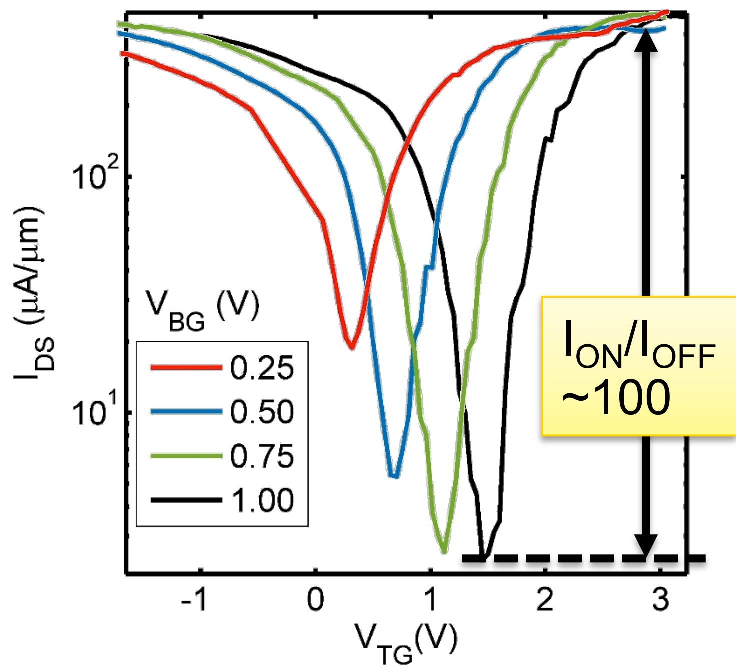


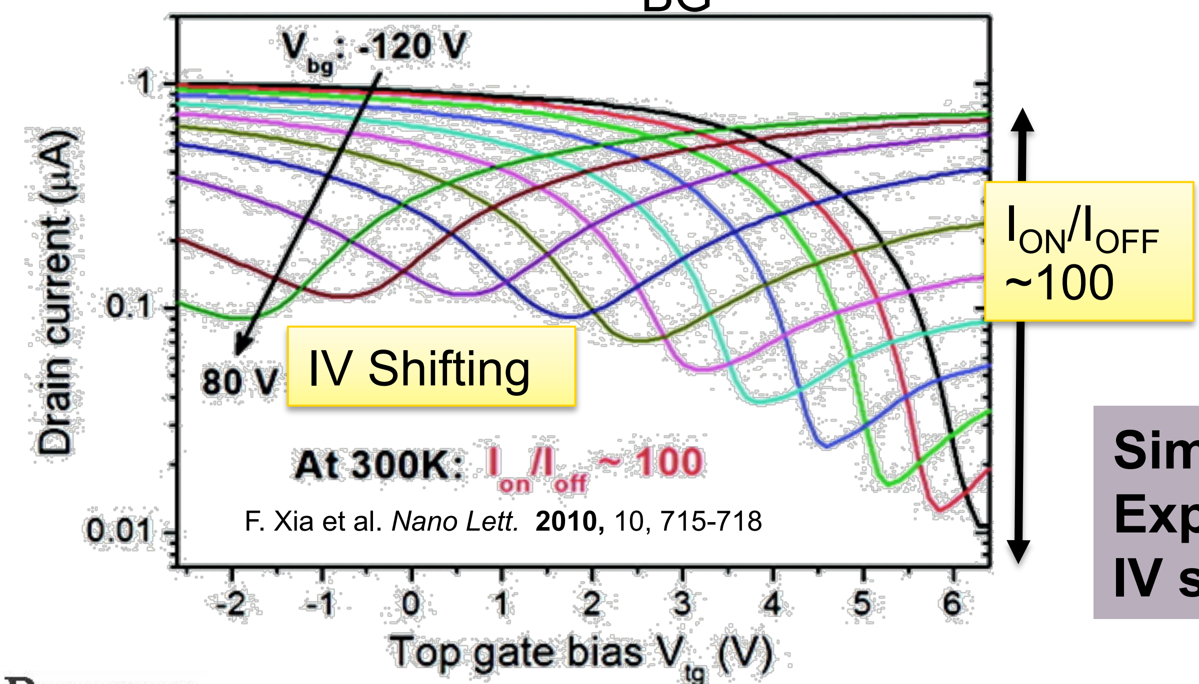
http://newscenter.lbl.gov/

Bilayer Graphene TFET:
Small Achievable Eg,
Small effective mass

Bilayer Graphene double gate FET Simulation and Experiment



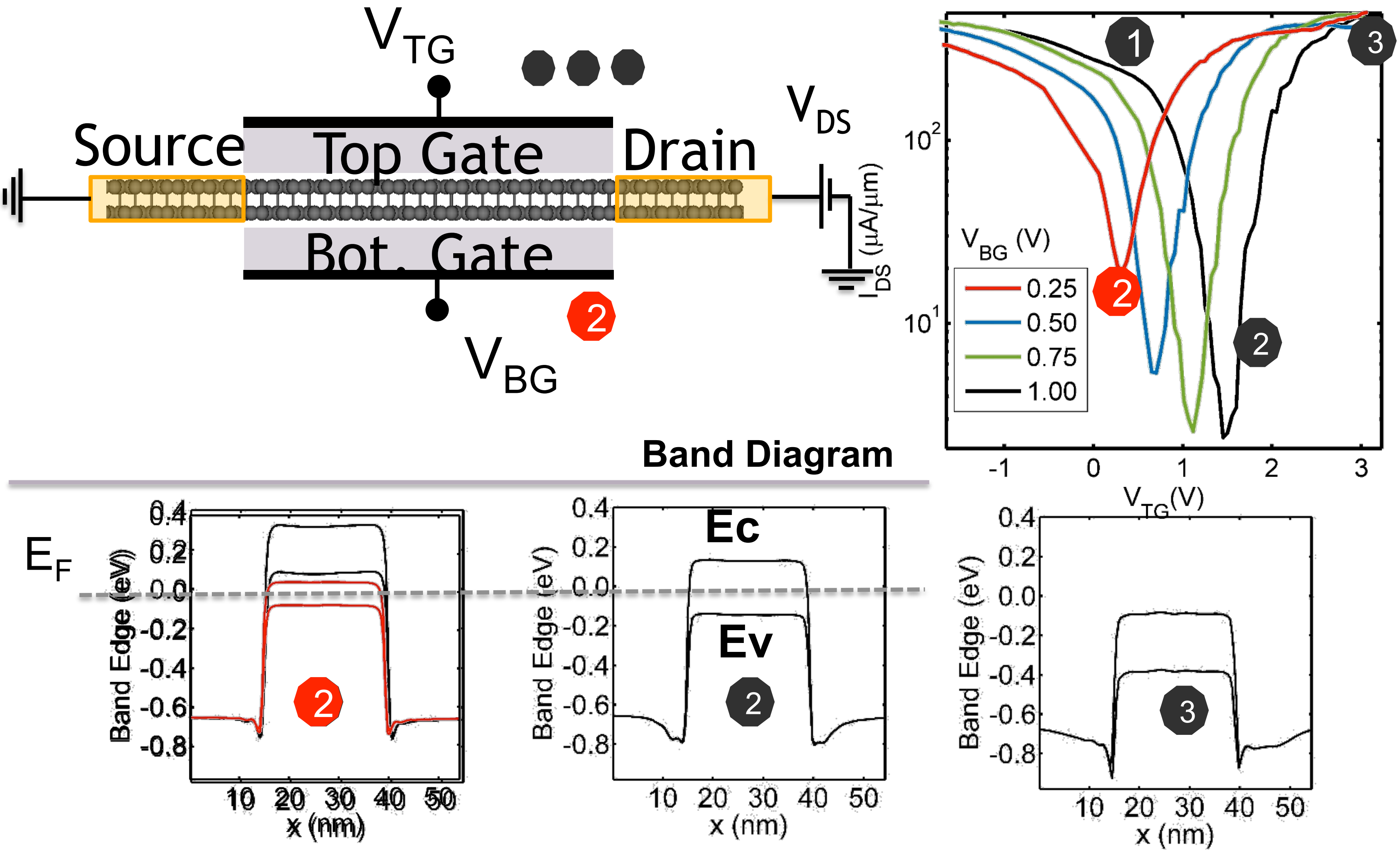




F. Xia et al. *Nano Lett.* **2010,** 10, 715-718

Simulation Matches Experiment:
IV shifting and I_{ON}/I_{OFF}

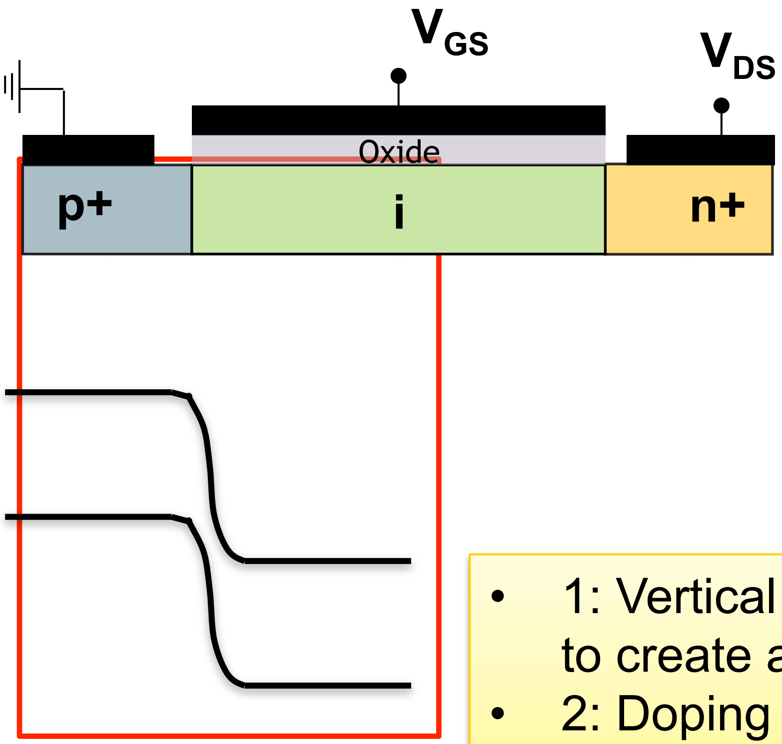
IV Shifting in Bilayer Graphene Double Gate FET



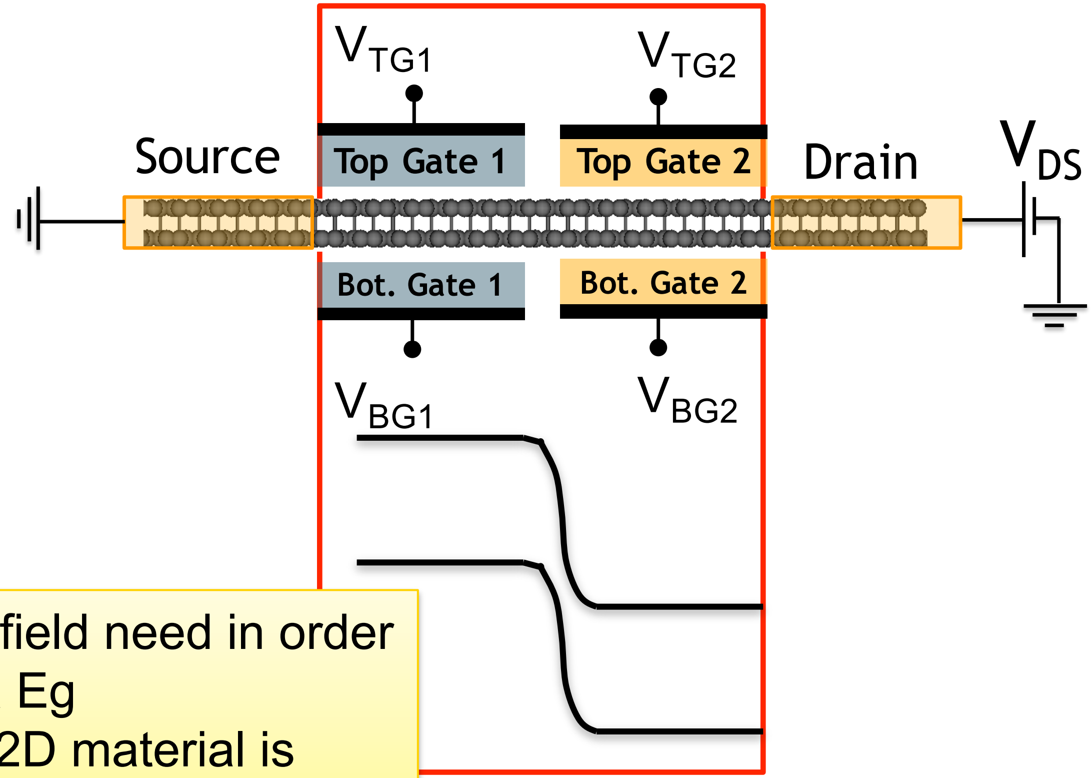
IV Shifting result from tunable band gap

Electrical Doped Bilayer Graphene Junction

Chemical Doping



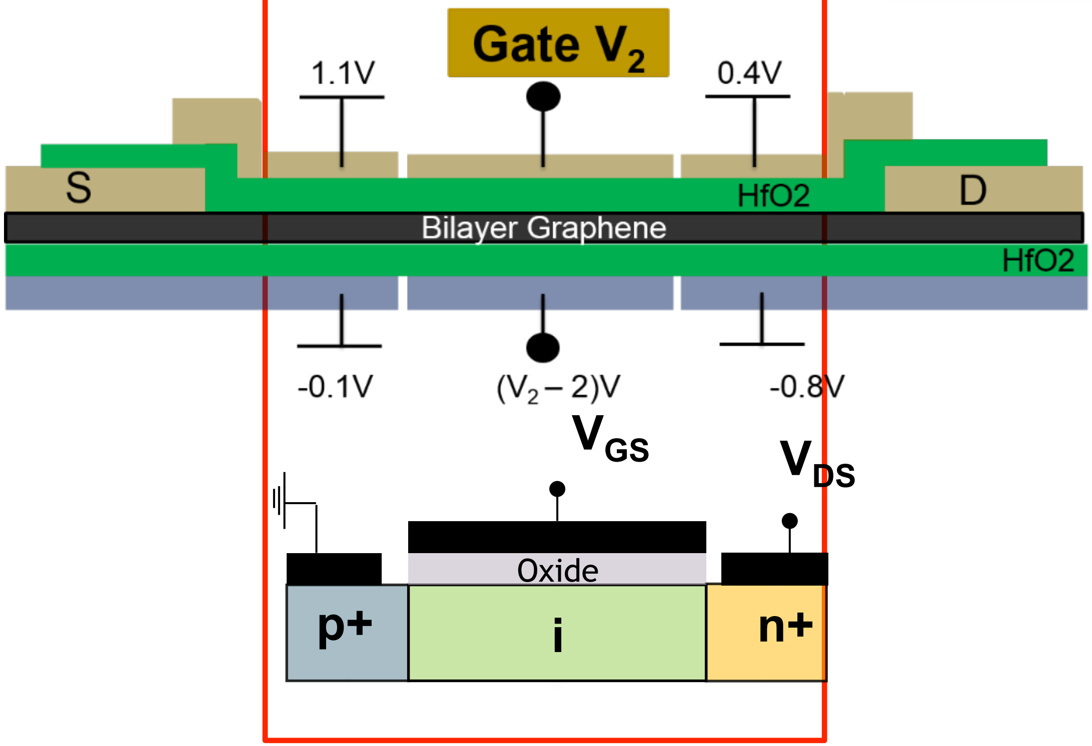
Electrical Doping

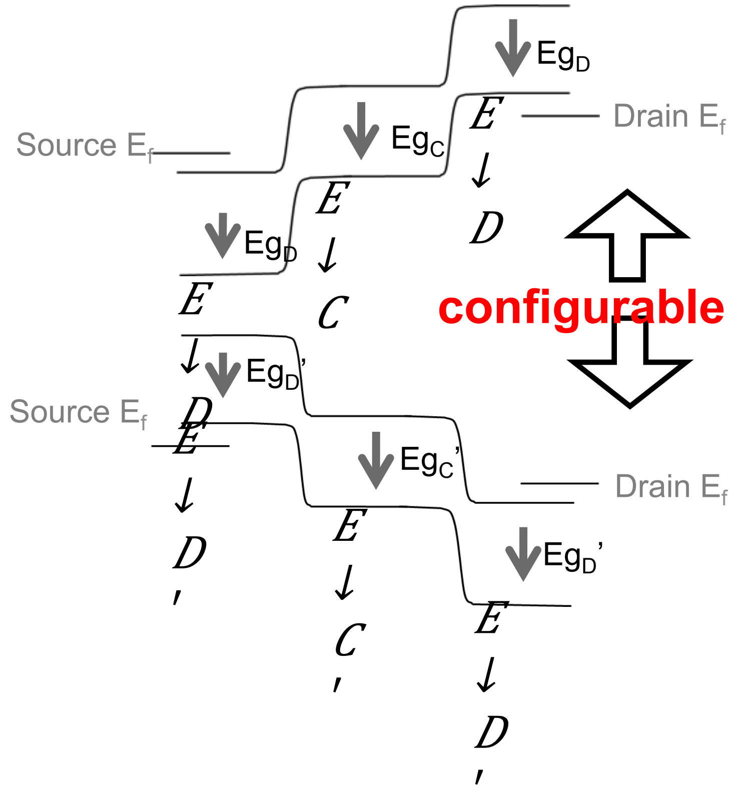


- 1: Vertical field need in order to create a Eg
- 2: Doping 2D material is challenging

Electrical Doping in bilayer graphene creates tunnel junction

Proposed Bilayer Graphene TFET



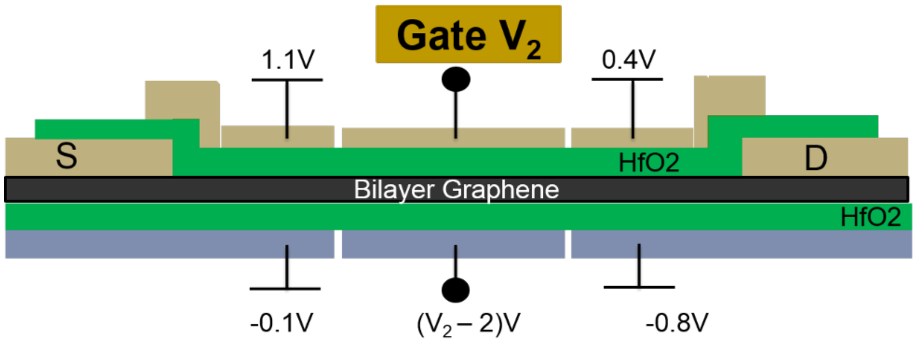


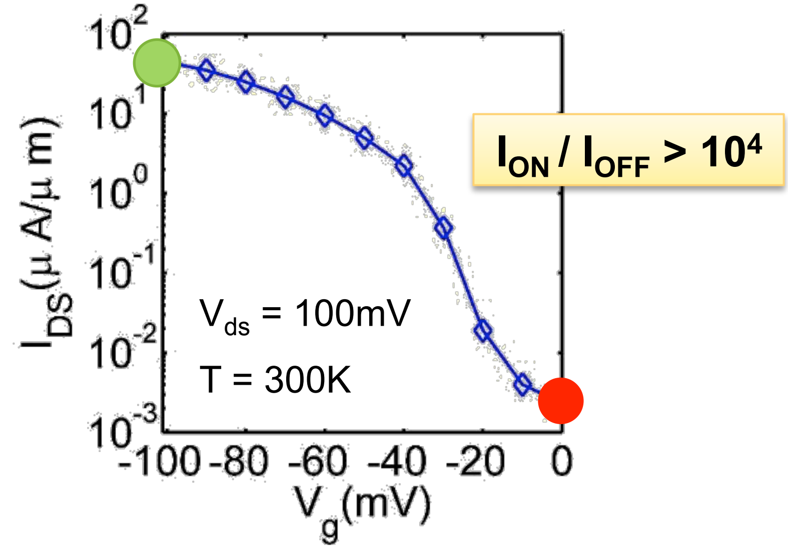
Advantages

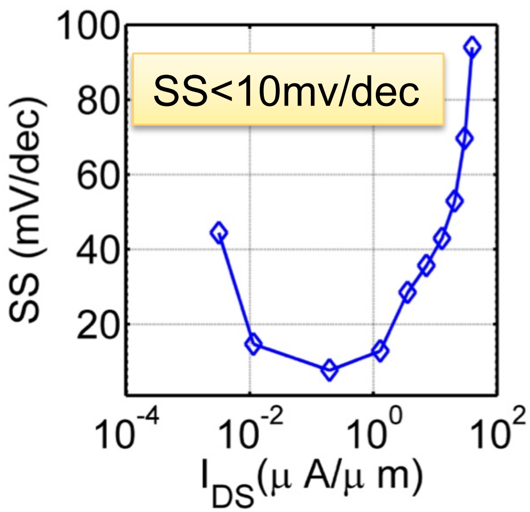
Configurable post after fabrication between pin and nip

No dopant states within bandgap → good OFF-state performance

Bilayer Graphene TFET: ON and SS







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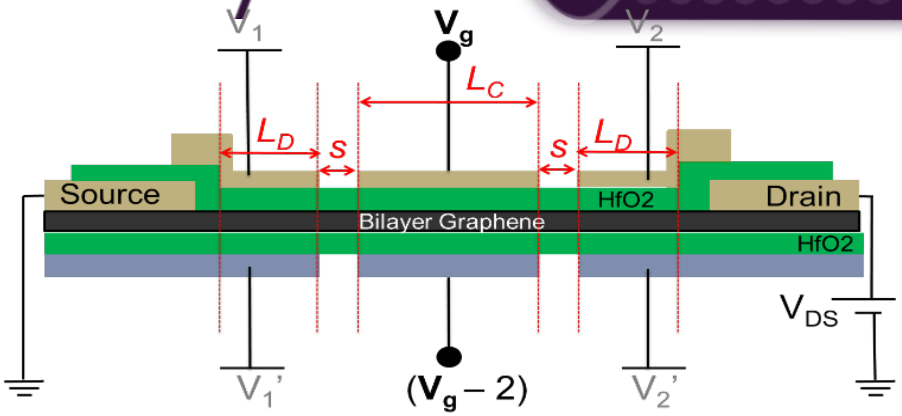
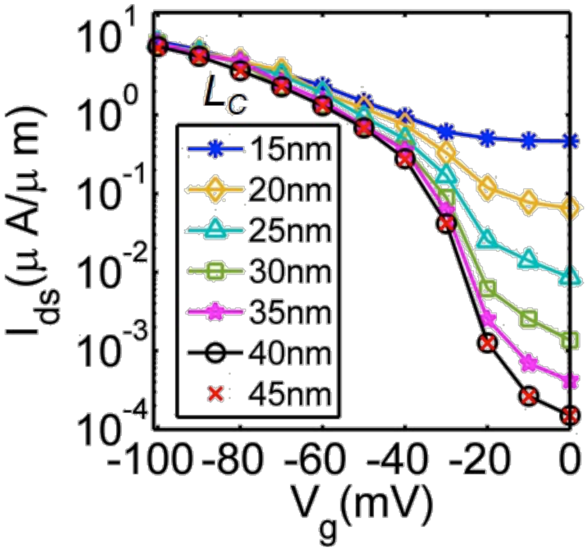
Configurable Electrostatically Doped High Performance Bilayer Graphene Tunnel FET

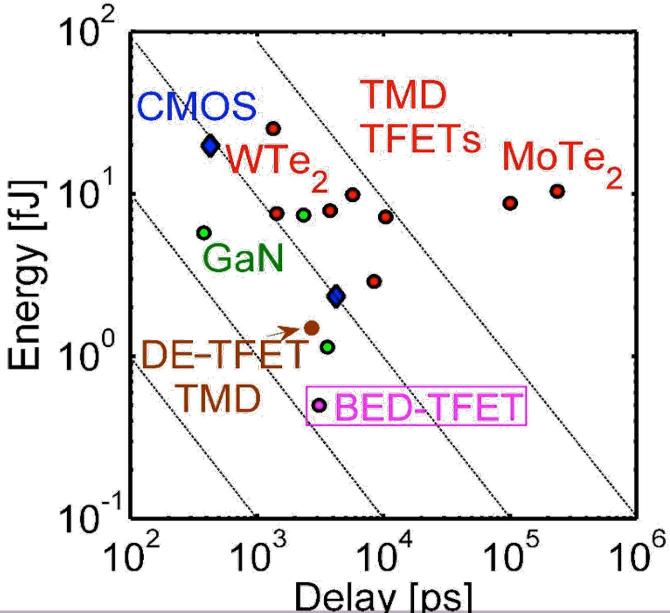
FAN W. CHEN[1], HESAMEDDIN ILATIKHAMENEH[2], GERHARD KLIMECK[2] (Fellow, IEEE), ZHIHONG CHEN[3], AND RAJIB RAHMAN[2]

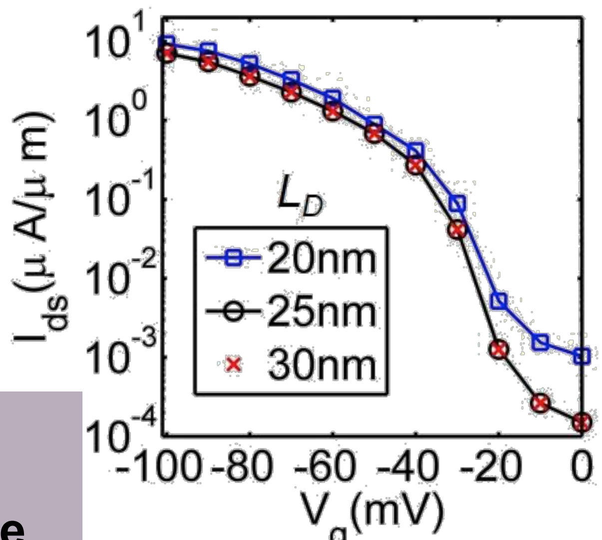
BLG TFET can operate at 0.1V with 100uA/um ON current

Bilayer Graphene TFET: Scalability and EDP



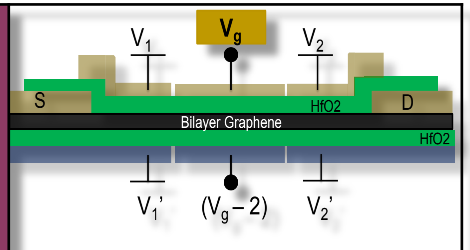






- **Good Energy Delay Product**
- **Larger foot print → not a good alternative**

Summary Evaluation of Bilayer Graphene TFET



Device	
VDD (V)	0.1
ION (uA/um)	100
SS (mV/dec)	8
Energy Delay Product	Energy ↓ Delay ↓
Scalability	90nm
Comments	Difficult Gate Alignment

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Further Reduce Tunnel Distance: Heterojunction TFET

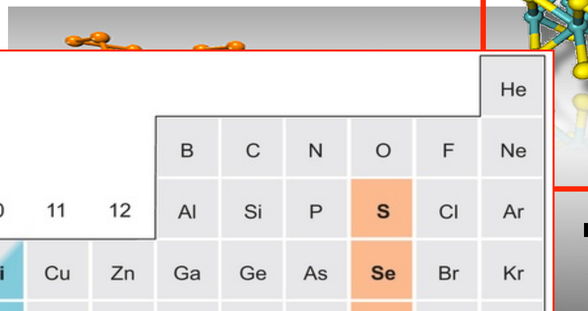
$I_{ON}\uparrow \rightarrow Trans\uparrow \rightarrow \lambda\downarrow \rightarrow t_{ch}\downarrow$

$Trans \propto \exp(-\lambda\cdot\sqrt{m^*}\cdot E_g)$

m*

Chemical formula: MX_2
MoS_2, WSe_2

Black phosphorus



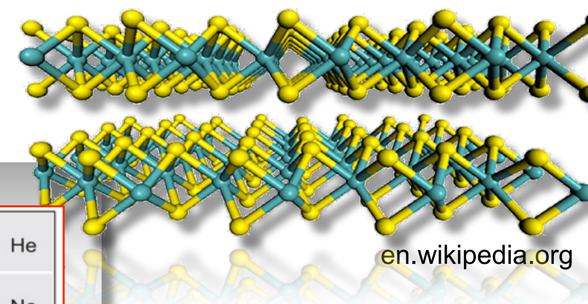
MX_2
M = Transition metal
X = Chalcogen

H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg	3	4	5	6	7	8	9	10	11	12	Al	Si	P	**S**	Cl	Ar
K	Ca	Sc	**Ti**	**V**	Cr	Mn	Fe	**Co**	**Ni**	Cu	Zn	Ga	Ge	As	**Se**	Br	Kr
Rb	Sr	Y	**Zr**	**Nb**	**Mo**	**Tc**	Ru	**Rh**	**Pd**	Ag	Cd	In	Sn	Sb	**Te**	I	Xe
Cs	Ba	La - Lu	**Hf**	**Ta**	**W**	**Re**	Os	**Ir**	**Pt**	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ac - Lr	Rf	Db	Sg	Bh	Hs	Mt	Ds	Rg	Cn	Uut	Fl	Uup	Lv	Uus	Uuo

Nature Chemistry 5, 263–275 (2013)

en.wikipedia.org

TMD



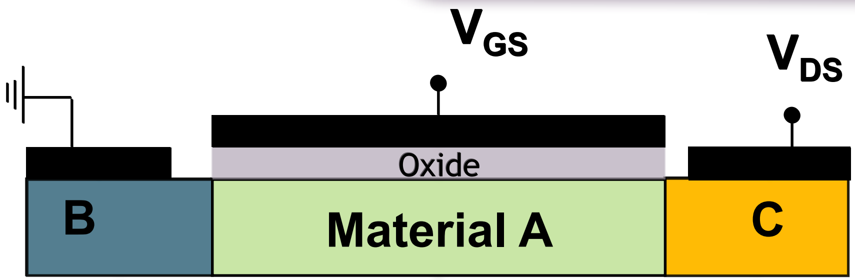
en.wikipedia.org

- Various materials ($MoS2$, $WTe2$, $WSe2$ ..)
- Eg: 1.0eV → 2.5eV

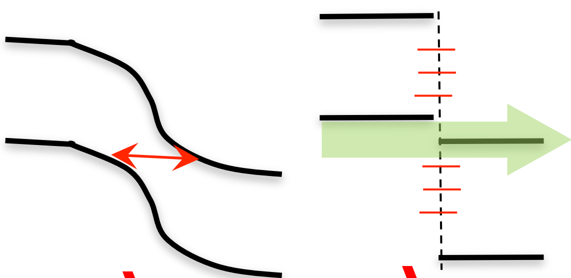
Eg

Various TMD materials are available for heterojunction TFET
→ Further reduce λ

A Common Problem for Heterojunction Tunnel FET

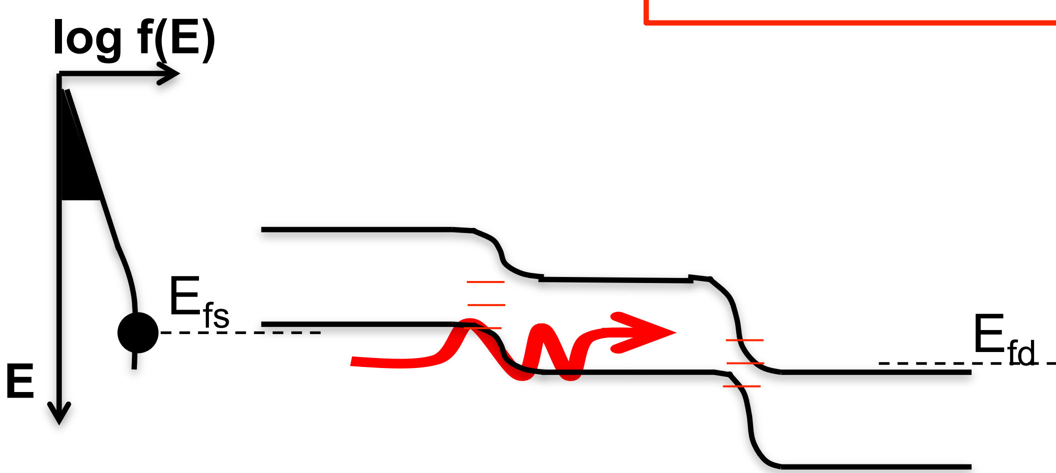


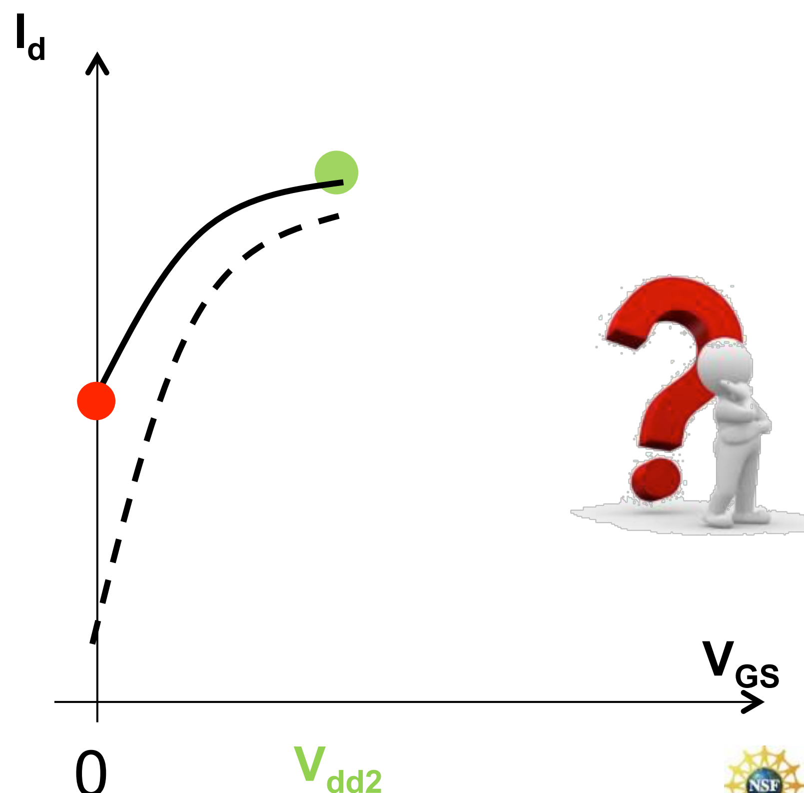
High Interface states degrades the OFF performance in heterojunction TFETs



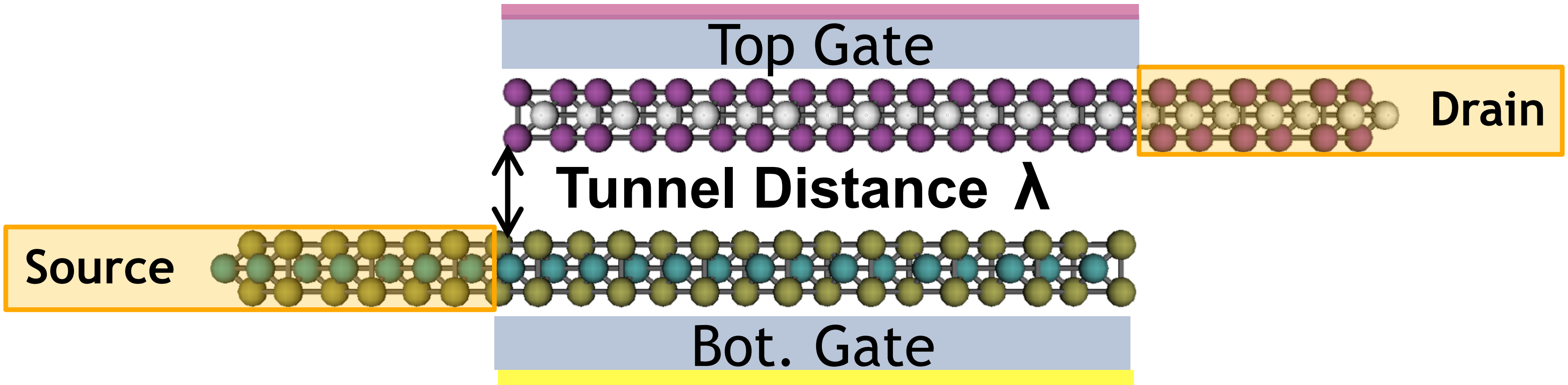
$\lambda_{homo} > \lambda_{hetero}$

Interface States!





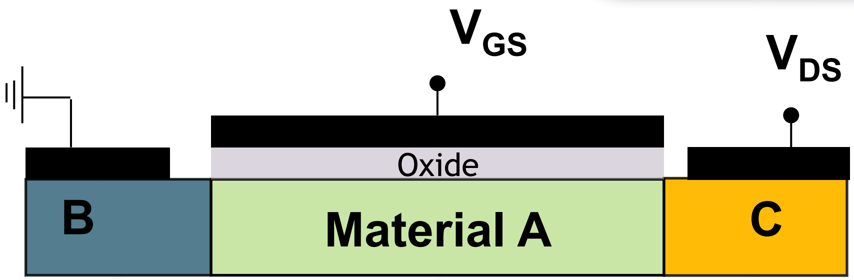
2D material interlayer TFET advantages

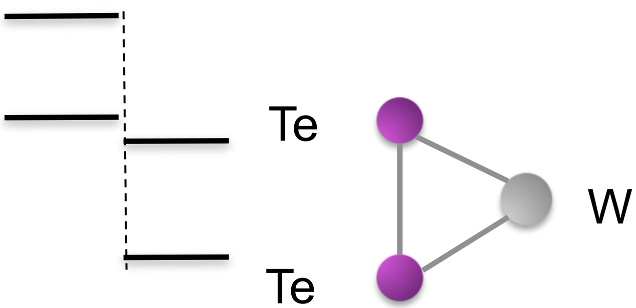


Surface promises low density of interface defects

Tunnel distance λ, is the sub-nanometer interlayer distance

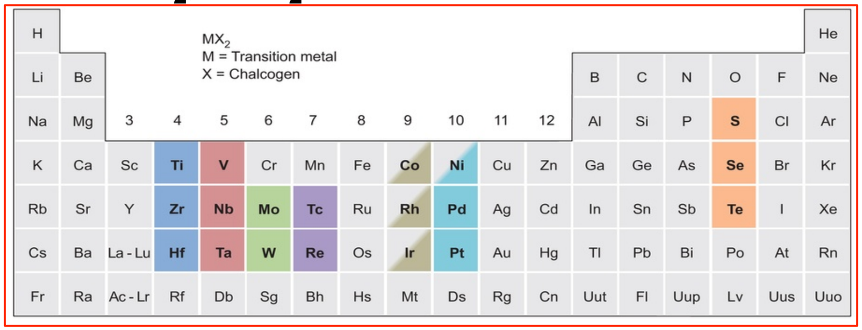
Interlayer TFETs: Choice of channel Material combination



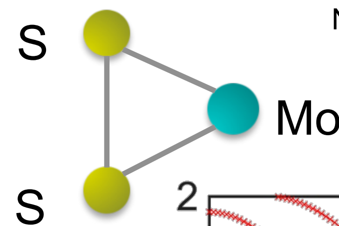


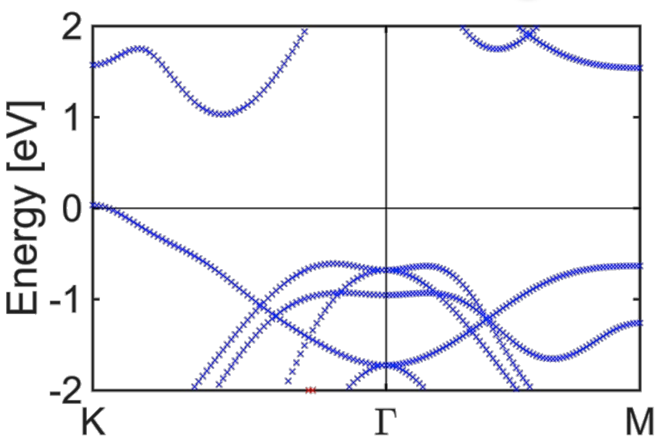
Chemical formula: MX_2

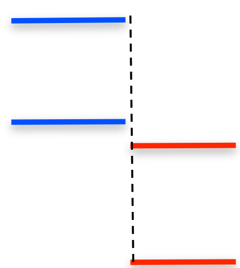
MoS_2, WSe_2

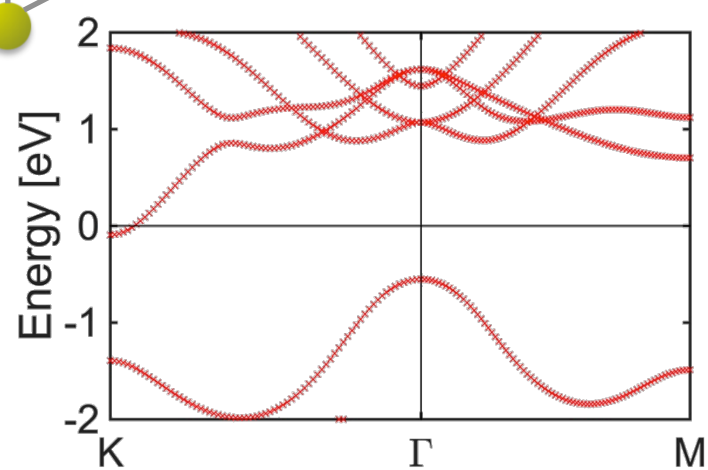


Nature Chemistry 5, 263–275 (2013)



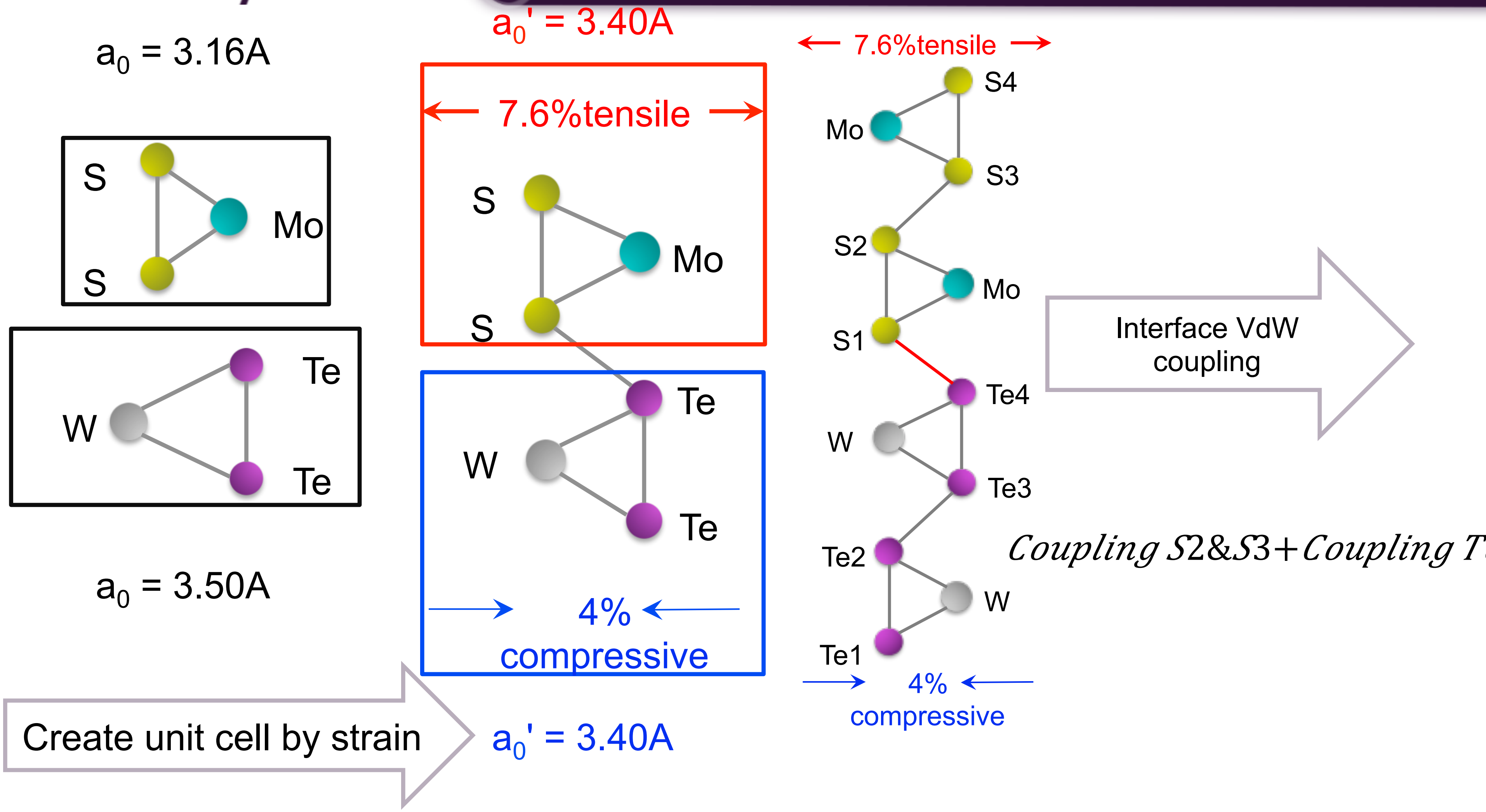






MoS2-WTe2 combination is chosen for broken band alignment

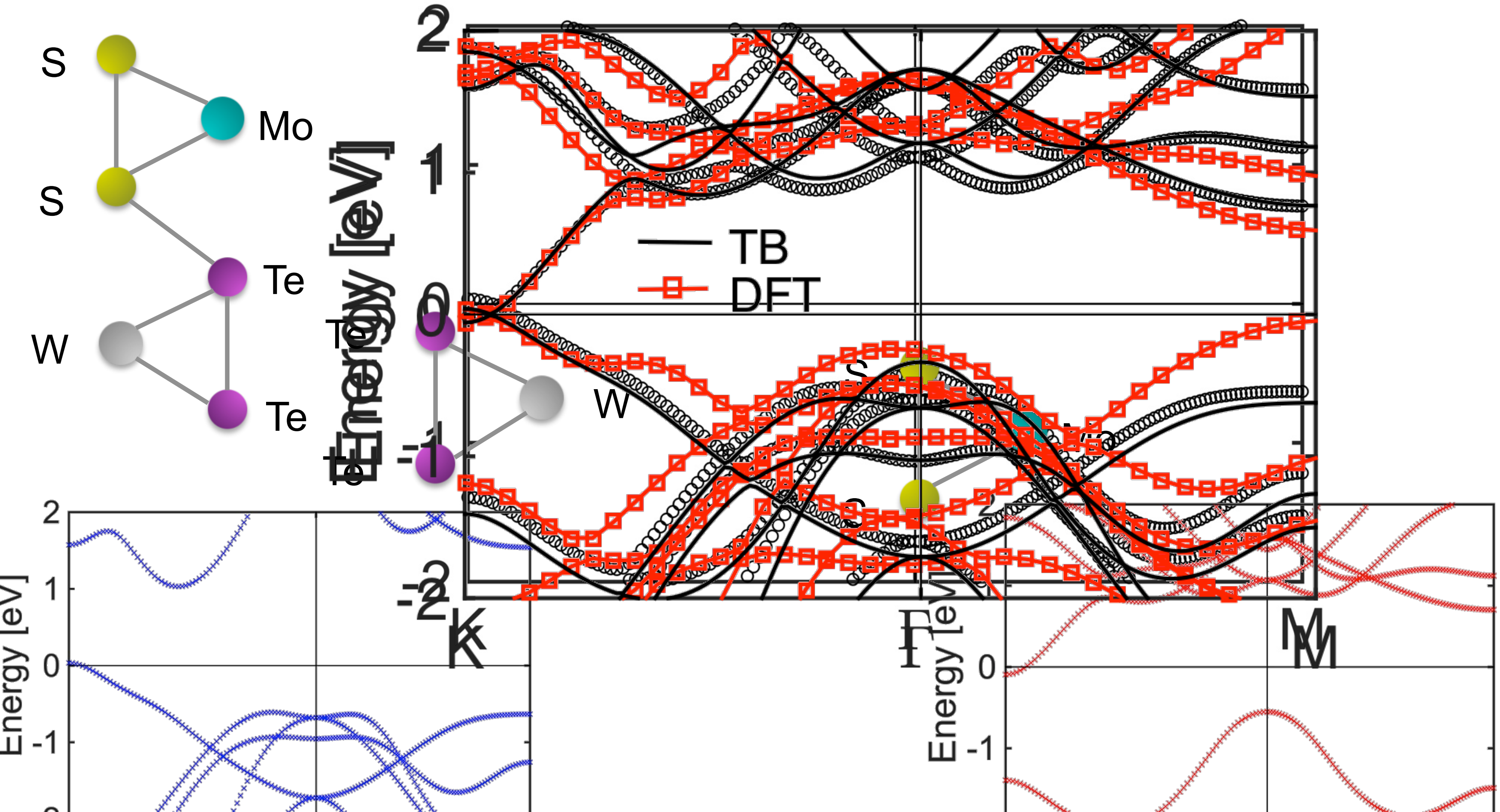
Hetero-junction Assumptions
Lattice Mismatch & Interface coupling



Assumption I : different layer has been strained to the same lattice constant to be registered

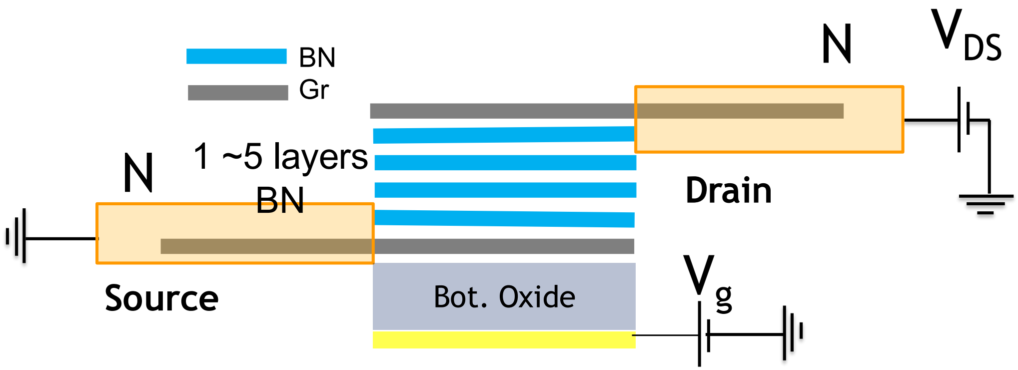
Assumption II : Interface VdW coupling is the average of the VdW of the two materials

Tight binding compared with DFT



TB matches well with DFT along the band edge at K point.
This is important for transport

Gr/BN/Gr vertical tunneling

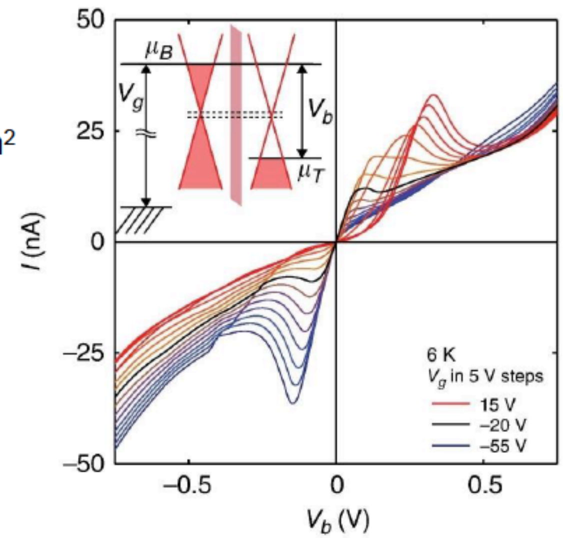


Gr/BN/Gr device structure is simulated to validate our model

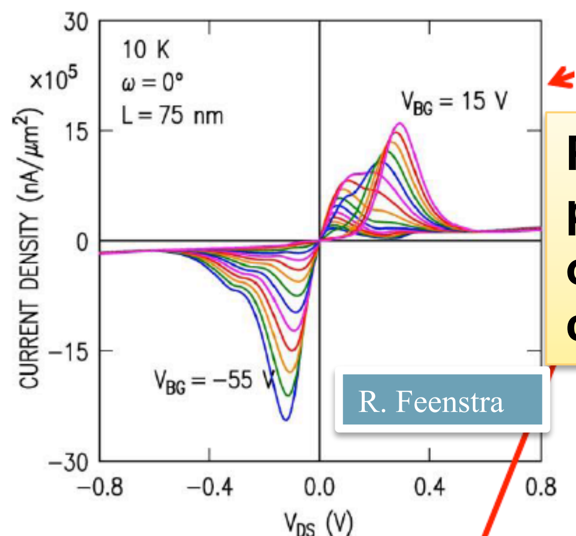
Assumption I & II are also applied to this simulation

Expt: Britnell et al., Nat. Comm. 4, 1794 (2013)

device area ≳ 1 μm²



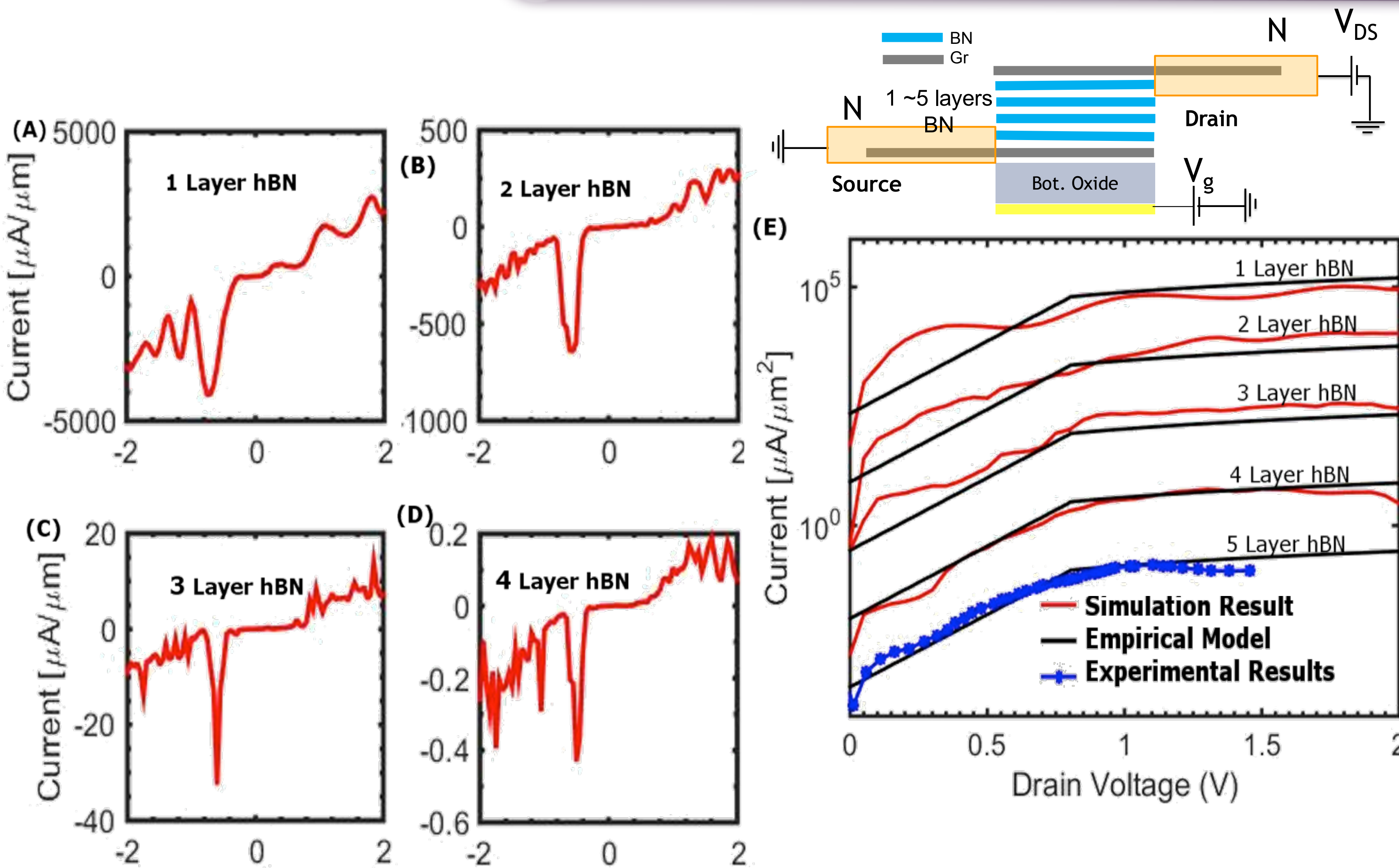
Theory: Plane-Wave Bardeen



Previous study predicts 2~3 orders of magnitude higher current

Gr/BN/Gr structure is simulated in order to Validate Model

Gr/BN/Gr: NEMO5 Current value matches experiment



NEMO5 results match experimental current value → Model Validated

Agenda

Motivation	• Power Dissipation Limit → TFET → Low ON → 2D
Method	• Open Boundary, Self-consistent and ballistic Calculation
Bilayer Graphene	•Pro: Low Power, Low Energy, Small Dealy •Con: too large to footprint, difficult gates aligning
Interlayer TFETs	• Gr/hBN/Gr Matching Experiments→ Validates Model • MoS2-WTe2 interlayer Tunnel FET Device physics &Performance
Black Phosphorous	• Thickness Engineered Tunnel FET proposal

NEMO5

A device switching Mechanism that is commonly believed

AIP Applied Physics Letters

Operating principles of vertical transistors based on mo
semiconductor heterojunctions

Kai Tak Lam, Gyungseon Seol, and Jing Guo

JOURNAL OF APPLIED PHYSICS **115**, 074508 (2014)

CrossMark

Single particle transport in two-dimensional heterojunction interlayer tunneling field effect transistor

Mingda (Oscar) Li,[1,a)] David Esseni,[2] Gregory Snider,[1] Debdeep Jena,[1] and Huili Grace Xing[1,b)]
[1]University of Notre Dame, Notre Dame, Indiana 46556, USA
[2]University of Udine, Udine, Italy

LETTER
doi:10.1038/nature15387

A subthermionic tunnel field-effect transistor with an atomically thin channel

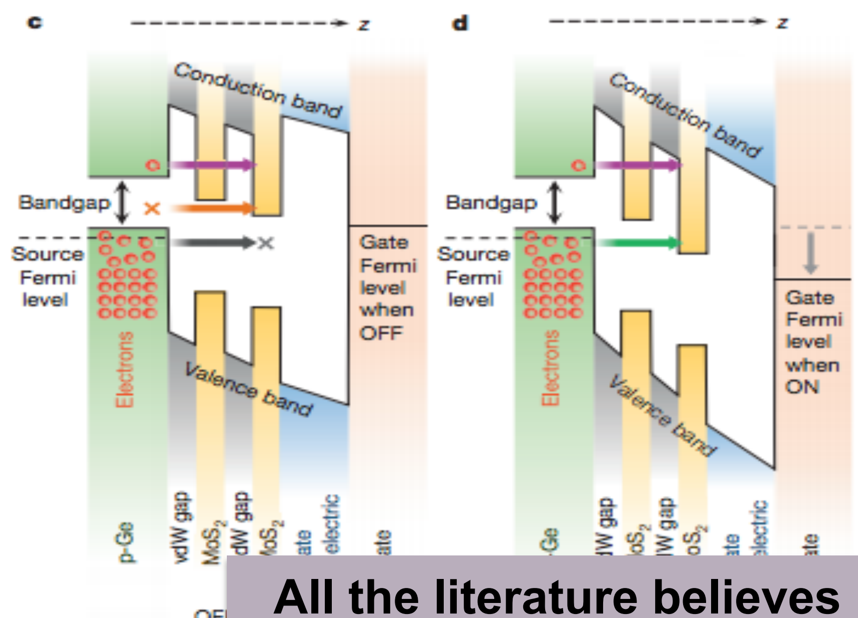
Deblina Sarkar[1], Xuejun Xie[1], Wei Liu[1], Wei Cao[1], Jiahao Kang[1], Yongji Gong[2], Stephan Kraemer[3], Pulickel M. Ajayan[2] & Kaustav Banerjee[1]

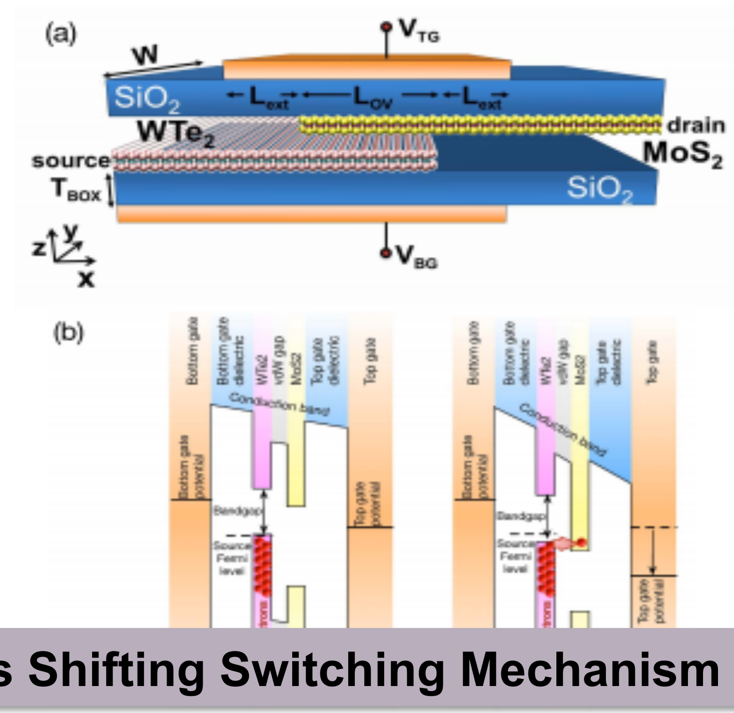
4388 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 63, NO. 11, NOVEMBER 2016

Operation and Design of van der Waals Tunnel Transistors: A 3-D Quantum Transport Study

Jiang Cao, *Student Member, IEEE*, Demetrio Logoteta, Sibel Özkaya, Blanca Biel, Alessandro Cresti, Marco G. Pala, *Member, IEEE*, and David Esseni, *Fellow, IEEE*

08 (2014)





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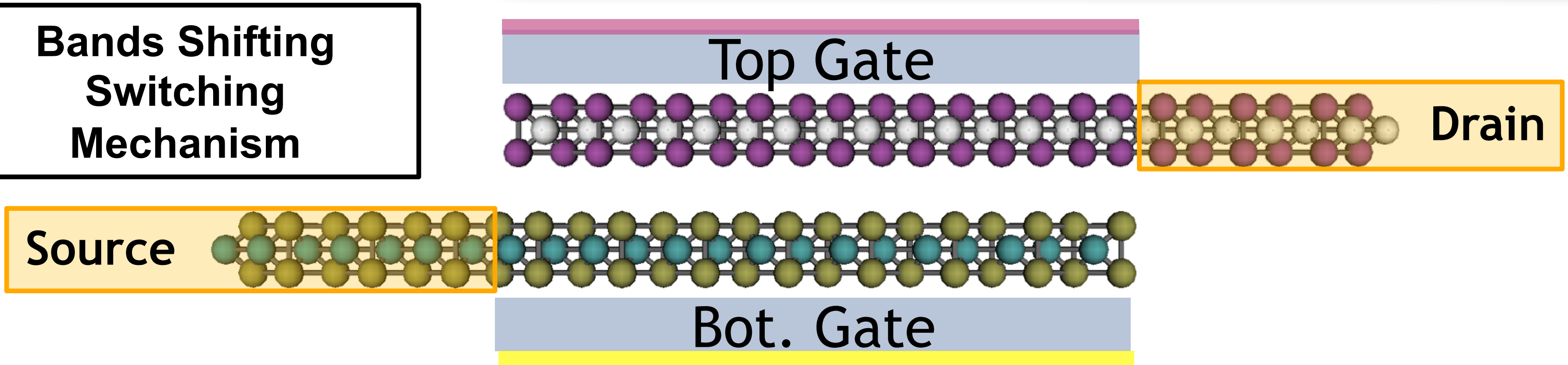
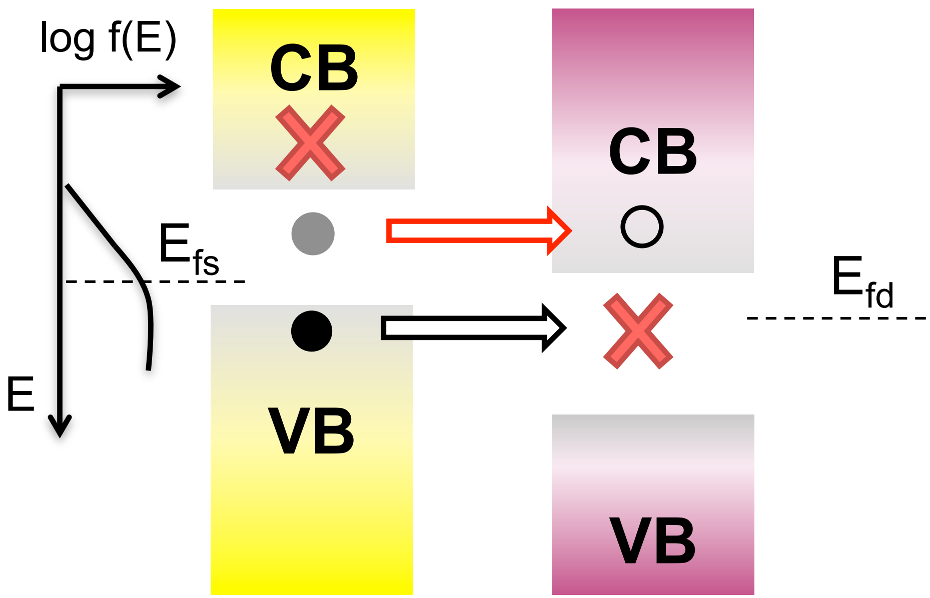
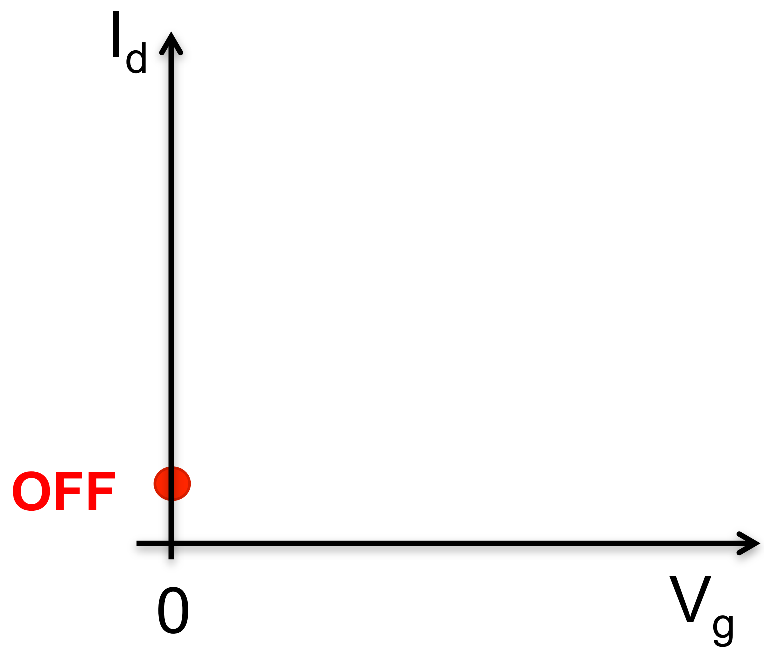
All the literature believes Bands Shifting Switching Mechanism

Interlayer TFET Bands Shifting Switching Mechanism: OFF

Bands Shifting Switching Mechanism

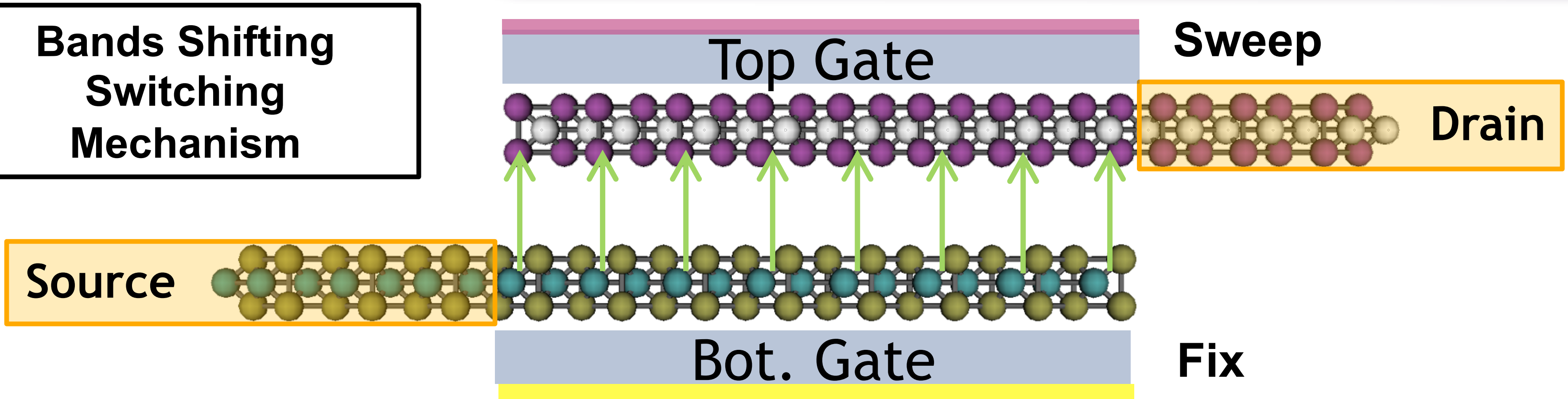


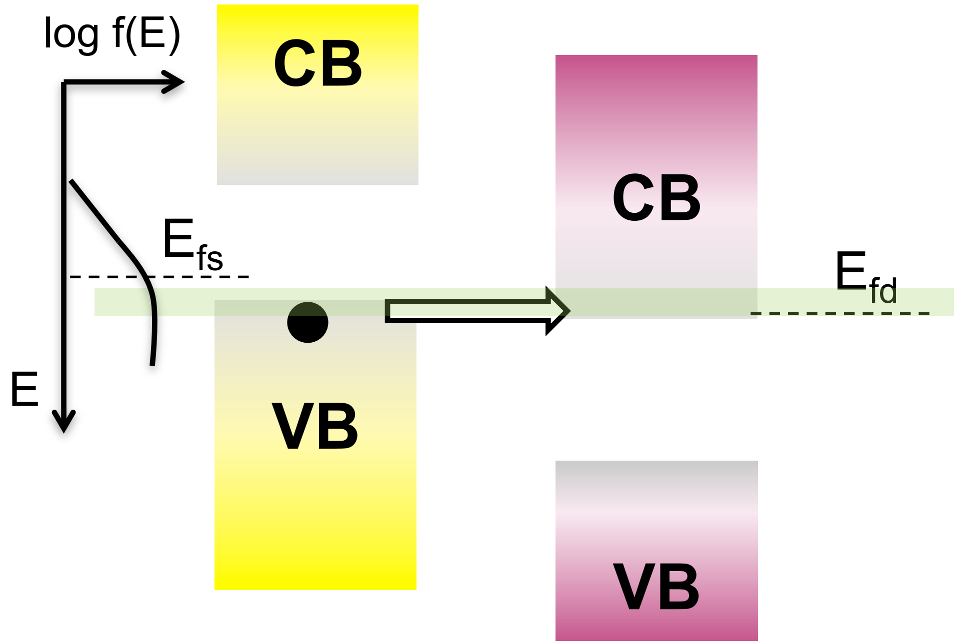


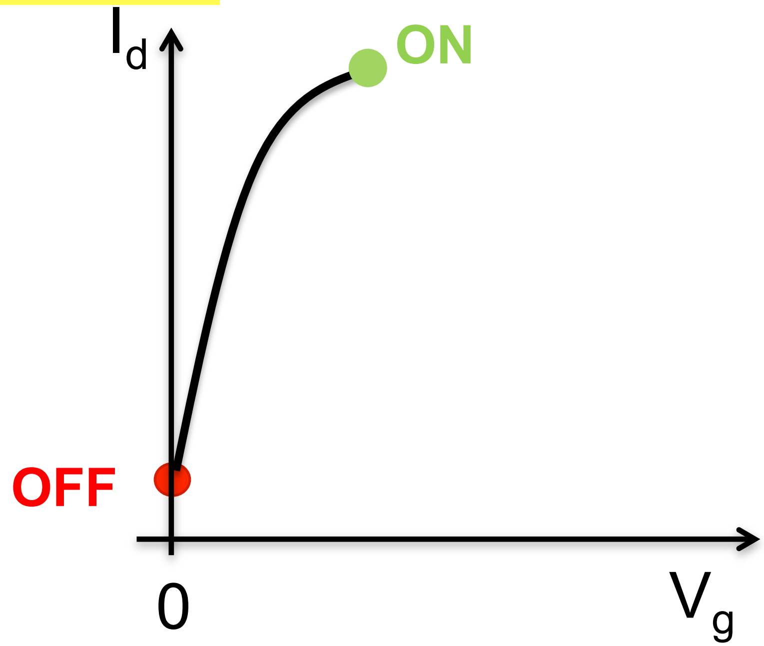


Interlayer TFET Bands Shifting Switching Mechanism: OFF

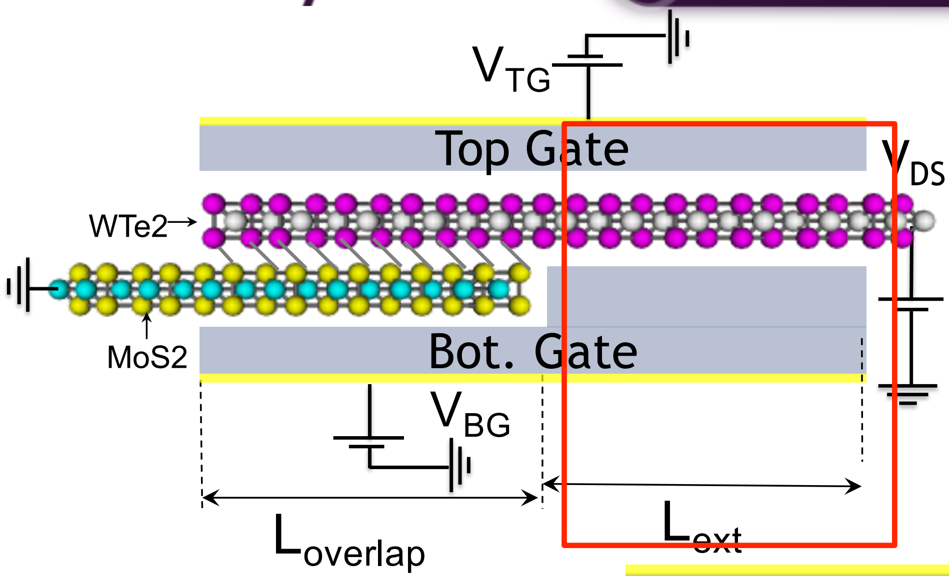
Bands Shifting Switching Mechanism



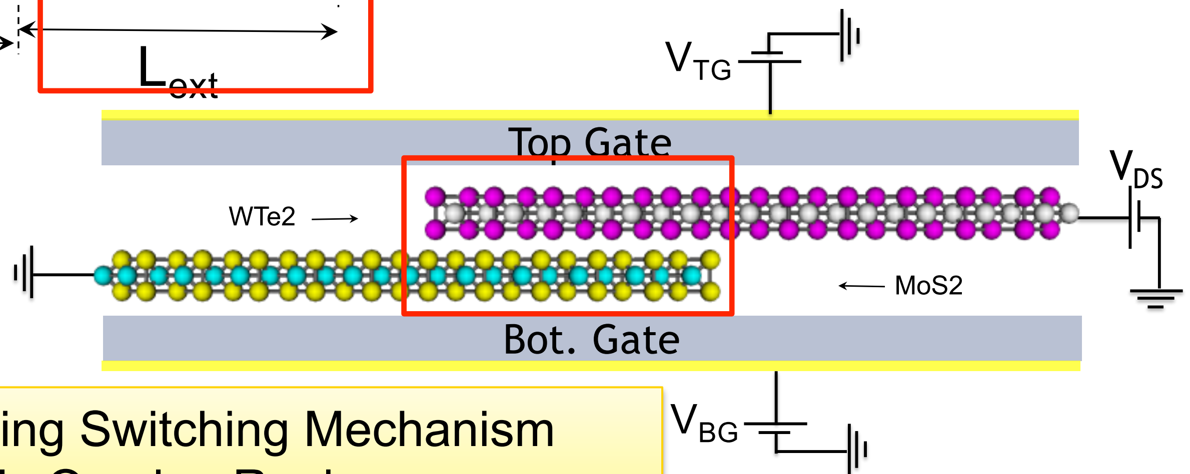




The Definition of Extension Region



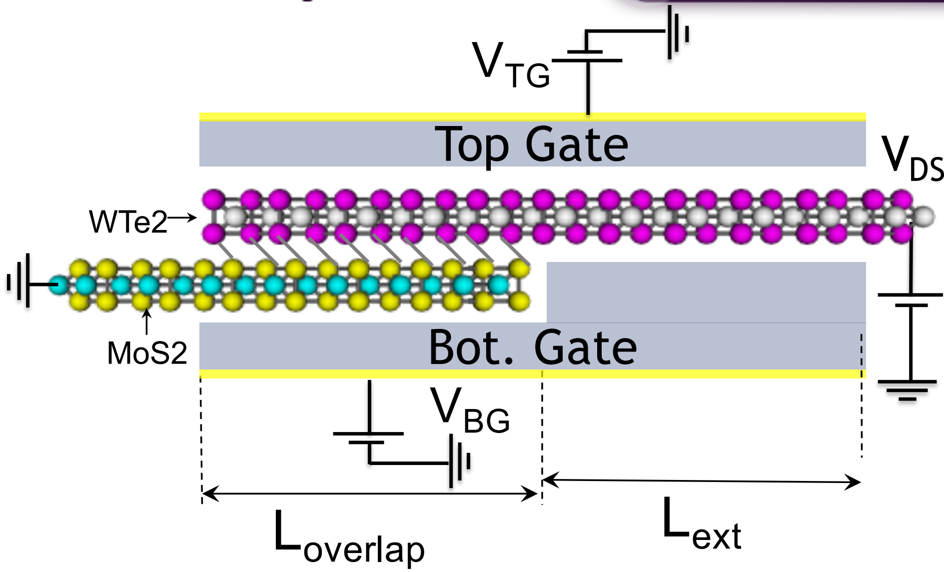
Extension Region

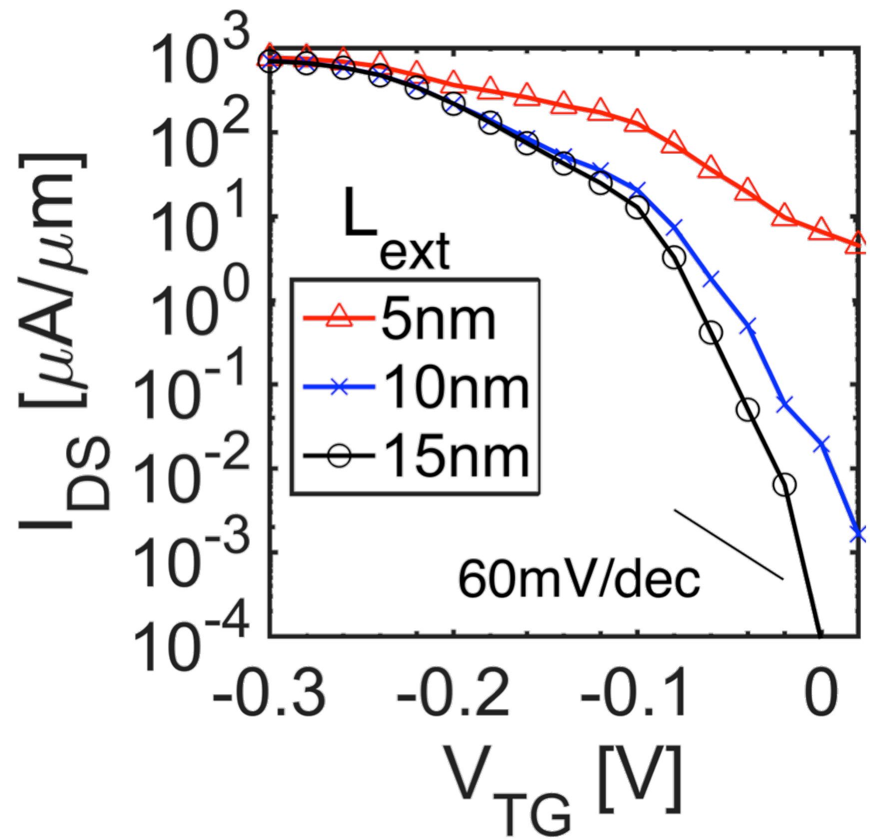


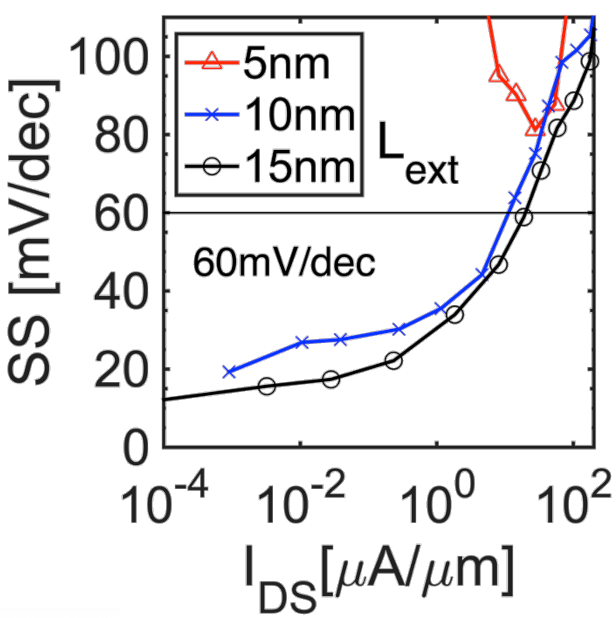
Device with Bands Shifting Switching Mechanism suggests device has only Overlap Region

Extension regions is defined as the region that has only one layer

The importance of extension region: OFF current and SS

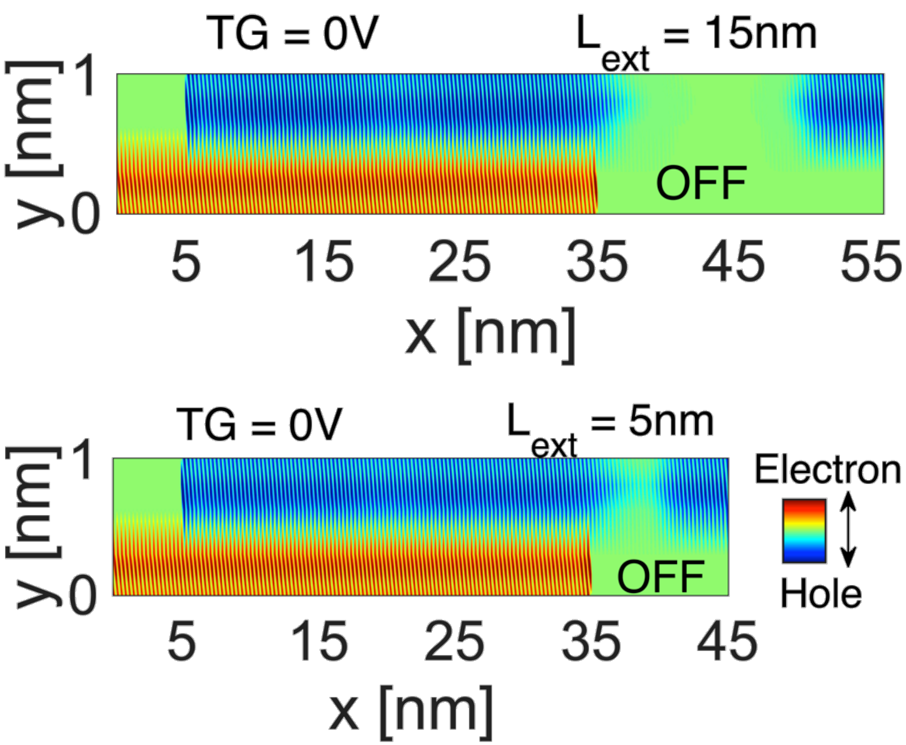


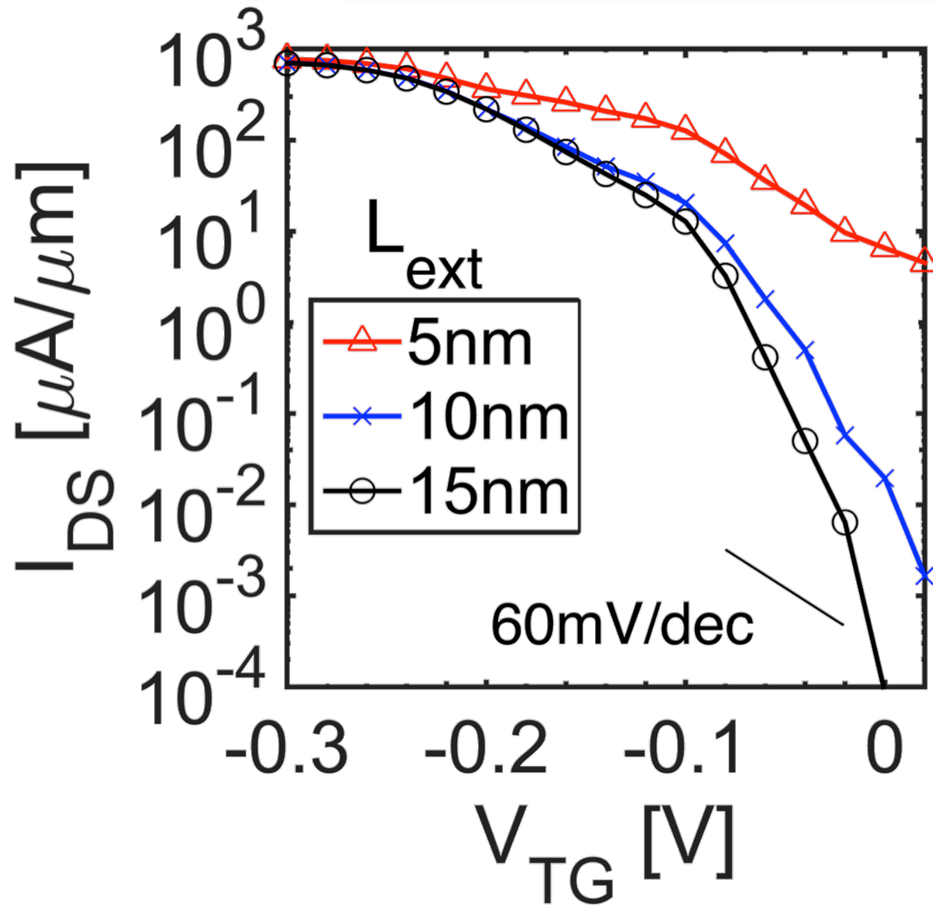




ON and SS are degraded with shorter extension region

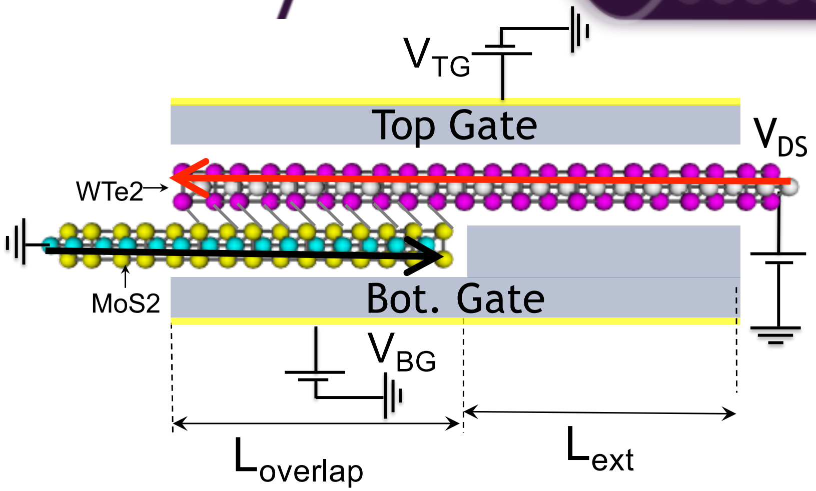
The importance of Extension Region Position Resolved Carrier Density

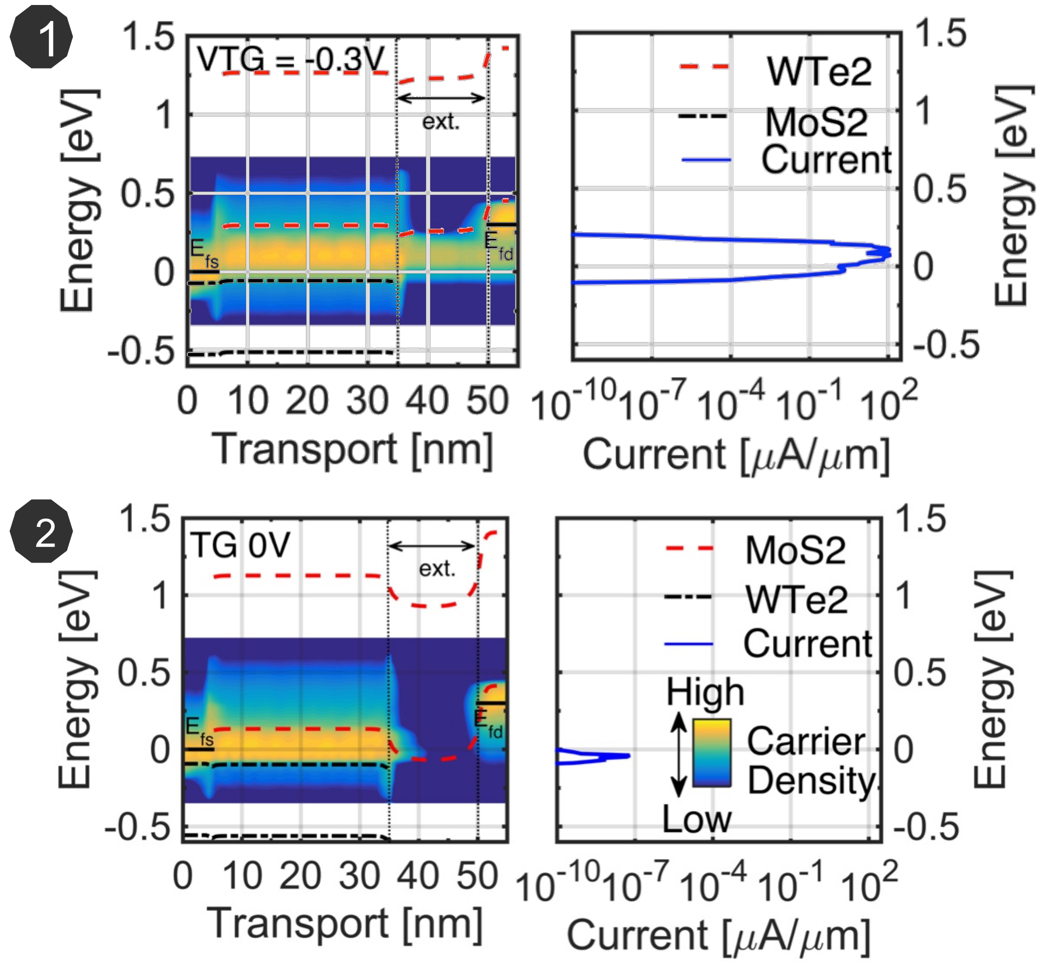


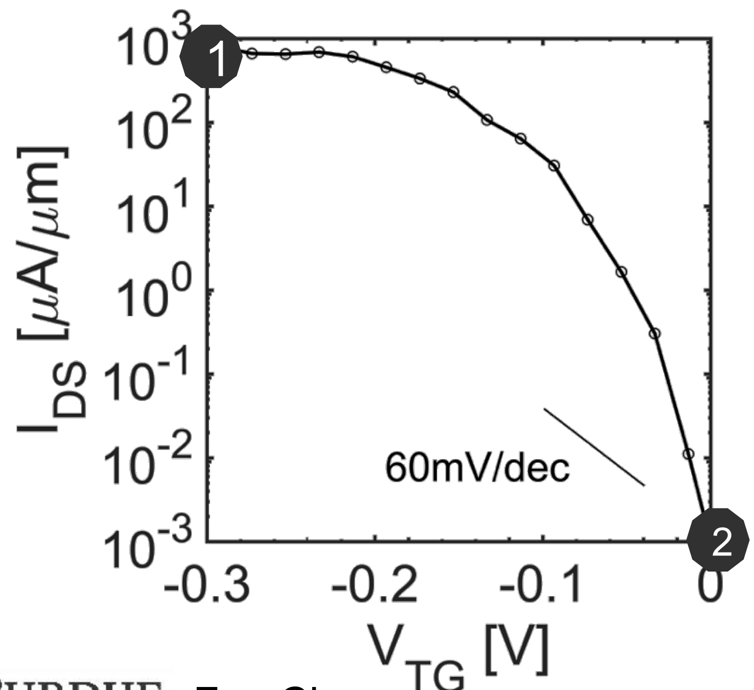


Both Top and Bottom Layer stay charged at the OFF state;
Long extension region blocks the leakage current.

The importance of extension region: band diagram & current

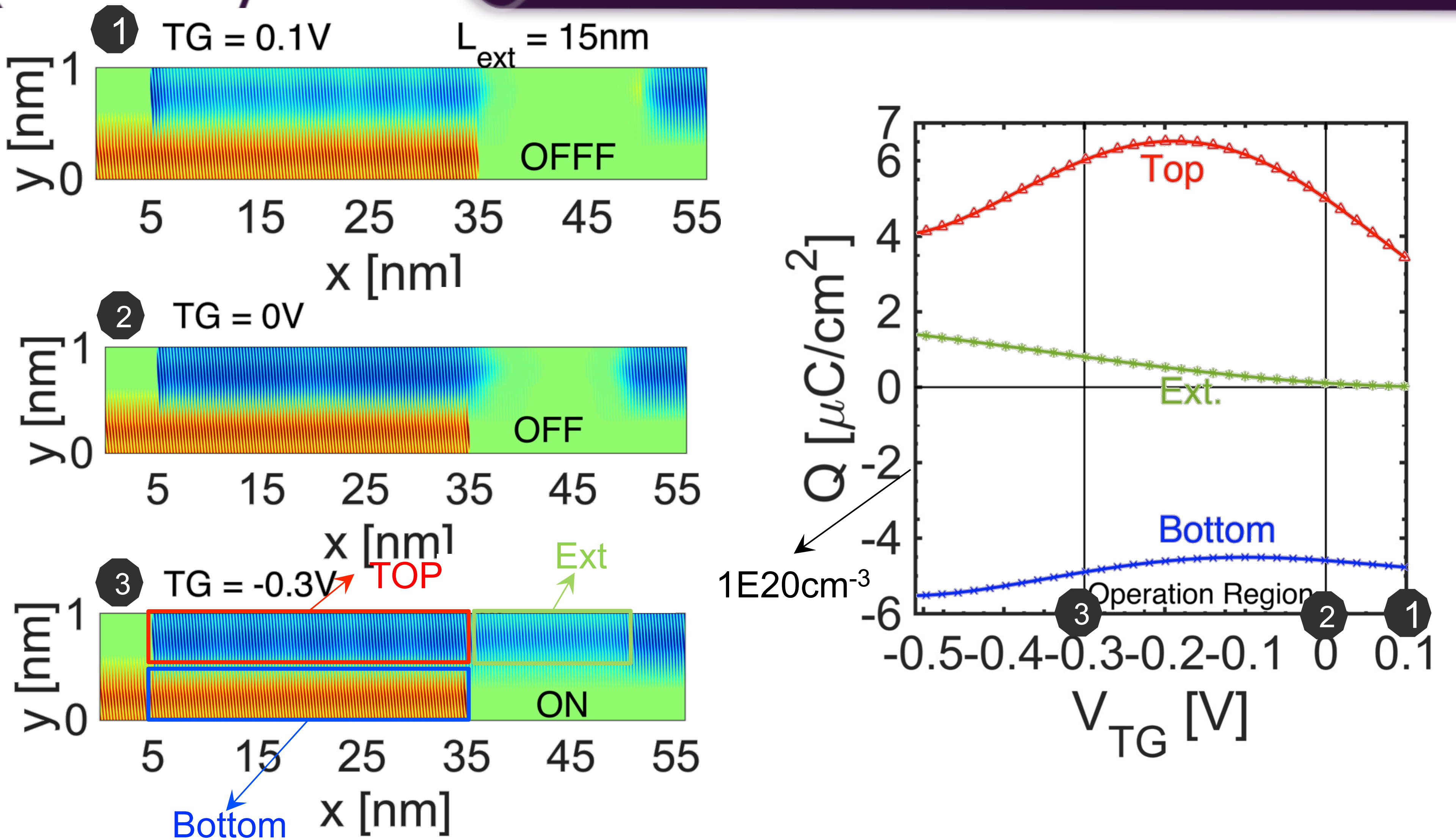






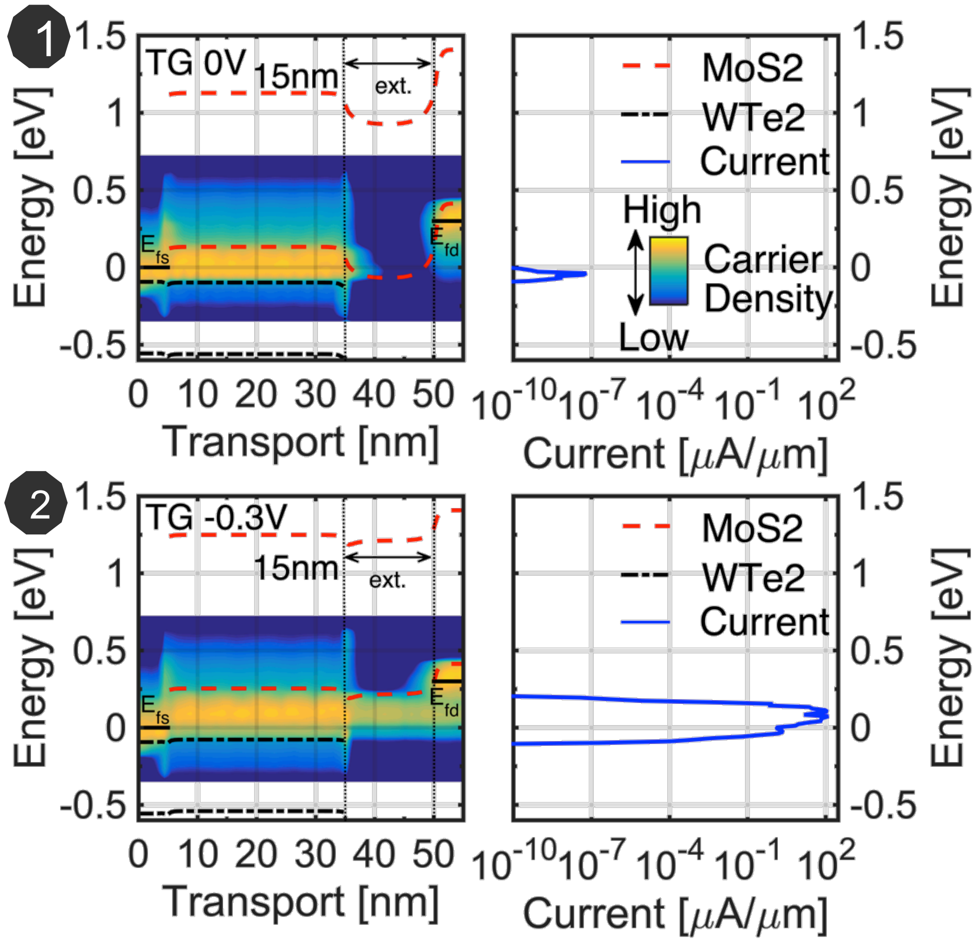
Overlap Region high density at OFF, Extension region turns off the device, Bands Shifting is Wrong

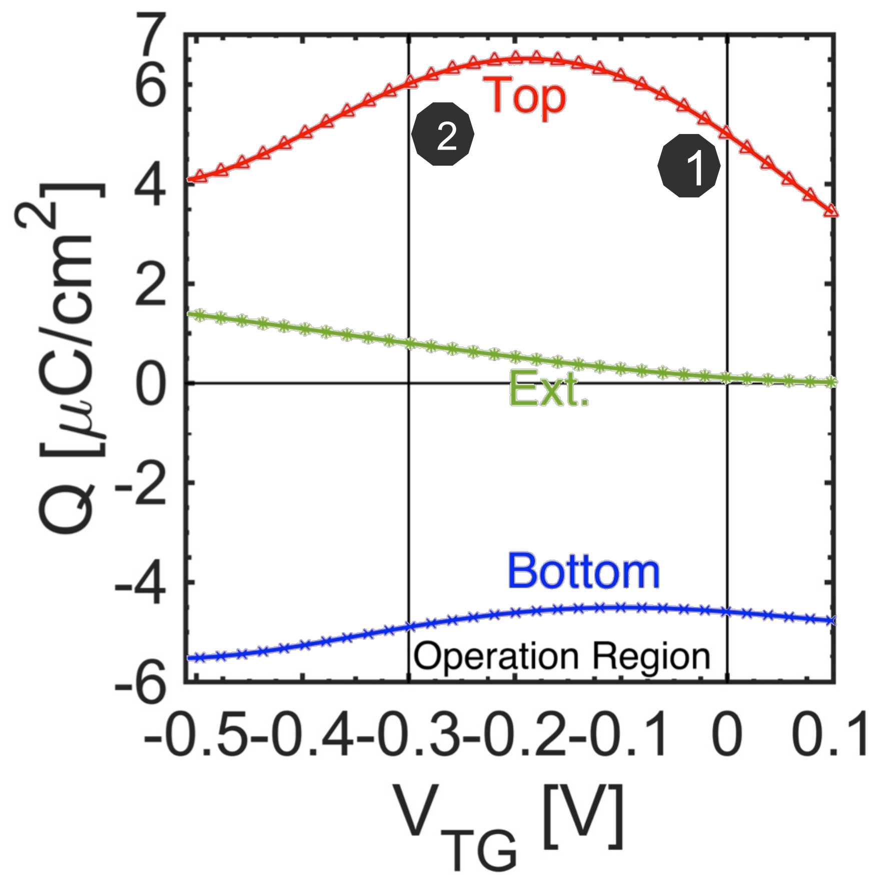
MoS2-WTe2 interlayer TFET: Highly Charge Device



Top and Bottom Layer stay highly Charged during both ON and OFF

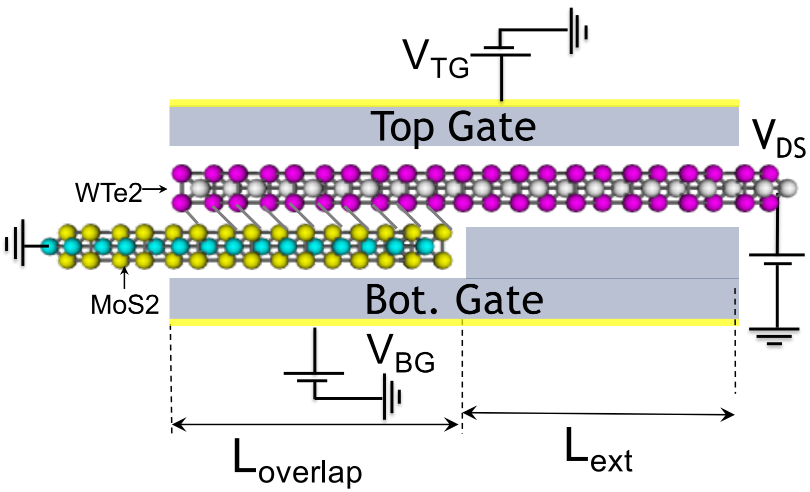
MoS2-WTe2 Interlayer TFET: Decrease in top layer charge

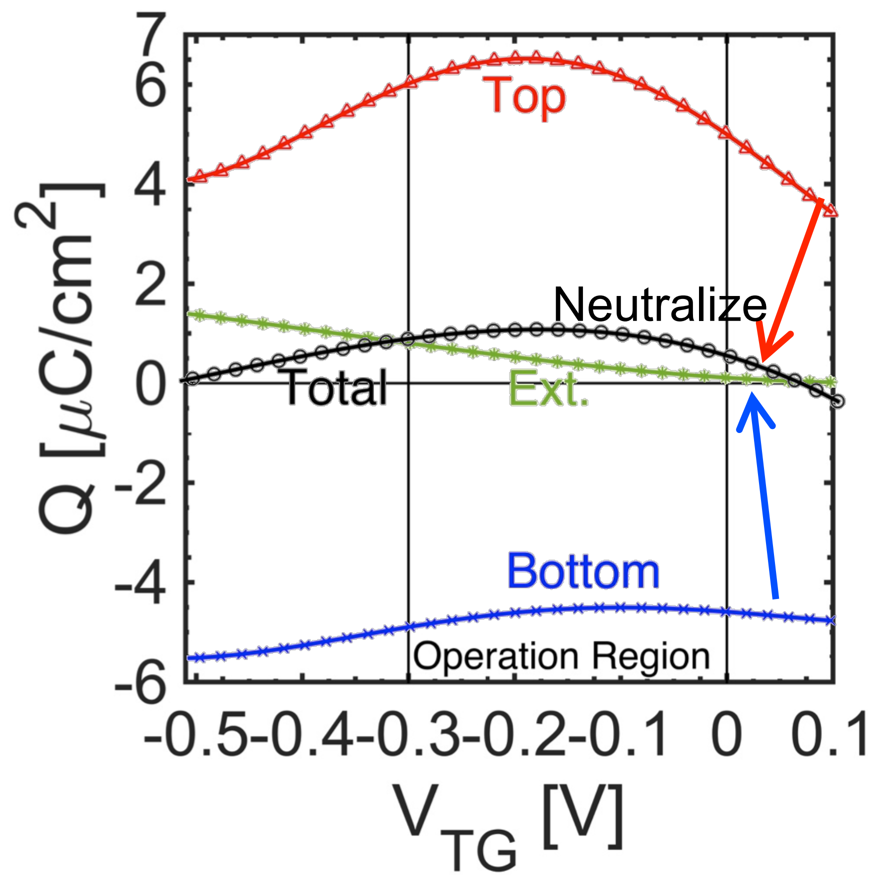




Decrease in top layer charge is due to current fllowing

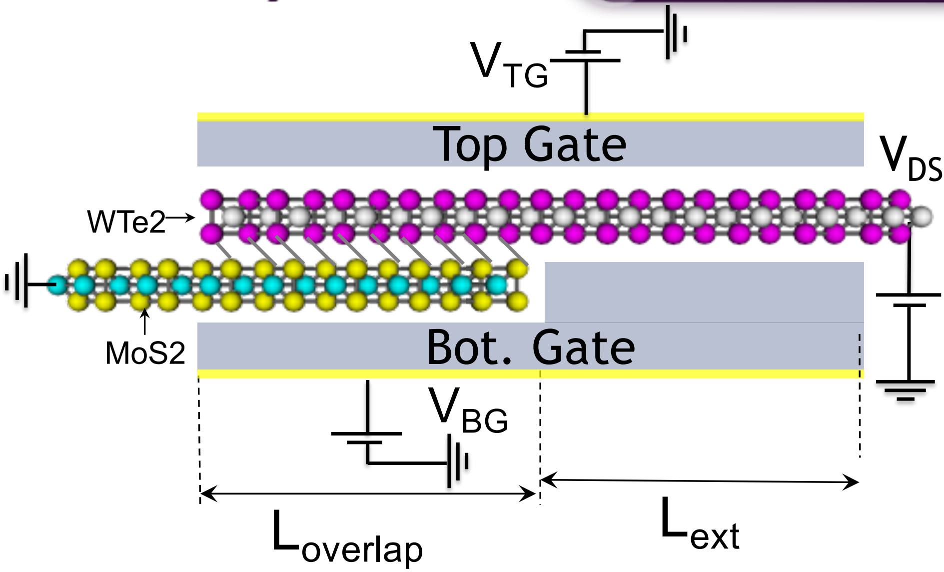
MoS2-WTe2 Interlayer TFET: Total Charge



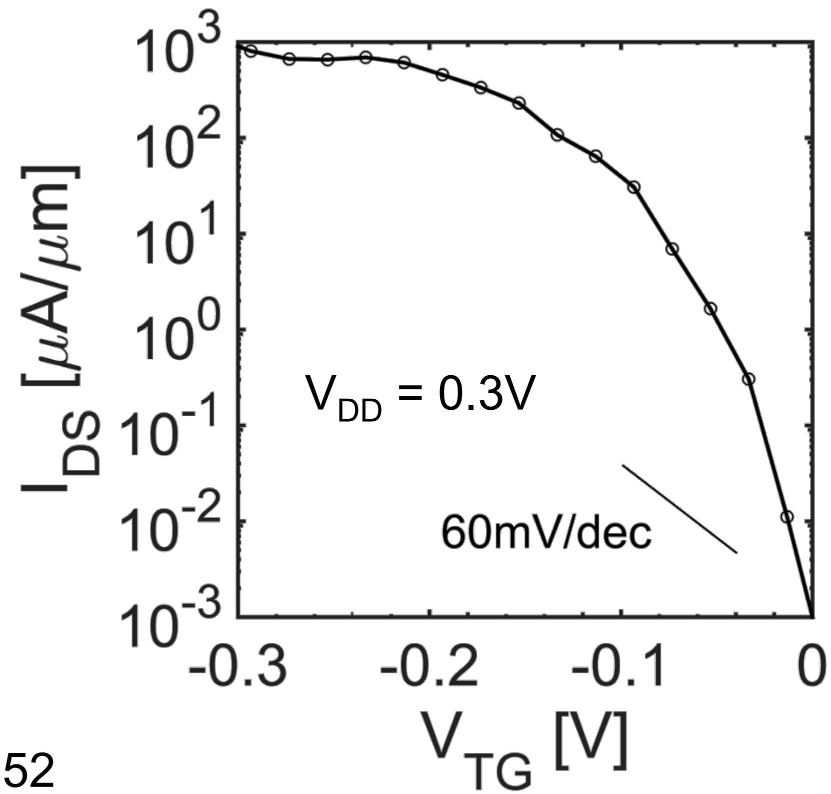


Though Device stays highly charged, total Charge is not huge due to neutralization

MoS2-WTe2 Interlayer TFET: ON and SS

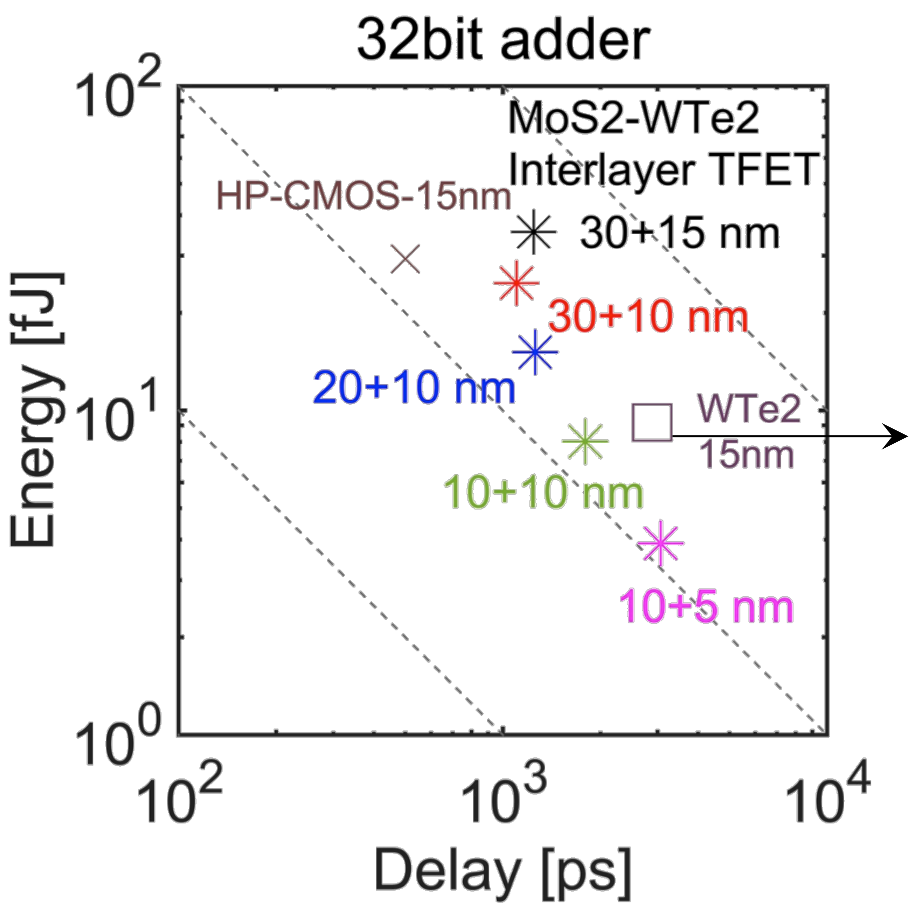


L_{ch} = 30nm
V_{DS} = -0.3V
V_{BG} = 0.5V
L_{ext} = 15nm
EOT = 0.5nm



WTe2-MoS2 Interlayer TFET demonstrates a smallest SS of 10mV/dec
ON current ~ 1000 uA/um

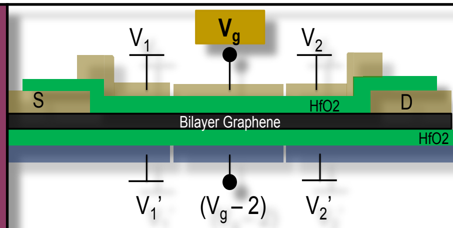
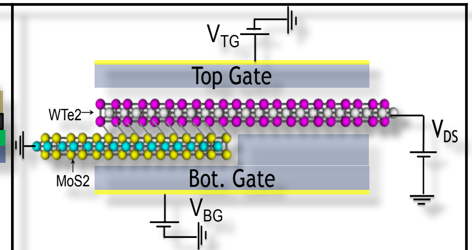
MoS2-WTe2 Interlayer TFET: Energy Delay Product



Best Performed homo-junction TFET based on TMD

MoS2-WTe2 interlayer TFETs does not show too much improvement in EDP

Evaluation of MoS2-WTe2 interlayer TFET

Device		
VDD (V)	0.1	0.3
ION (uA/um)	100	1000
SS (mV/dec)	8	10
Energy Delay Product	Energy ↓ Delay ↓	Energy ↓ Delay ↑
Scalability	90nm	15nm
Comments	Difficult Gate Alignment	Device Switching Mechanism

Agenda

Motivation	• Power Dissipation Limit → TFET → Low ON → 2D
Method	• Open Boundary, Self-consistent and ballistic Calculation
Bilayer Graphene	•Pro: Low Power, Low Energy, Small Dealy •Con: too large to footprint, difficult gates aligning
Interlayer TFETs	• Gr/hBN/Gr Matching Experiments→ Validates Model • MoS2-WTe2 interlayer TFET → Low Energy, Large Delay Different Switching Mechanism
Black Phosphorous	• Thickness Engineered Tunnel FET proposal

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Black Phosphorous	• Thickness Engineered Tunnel FET proposal

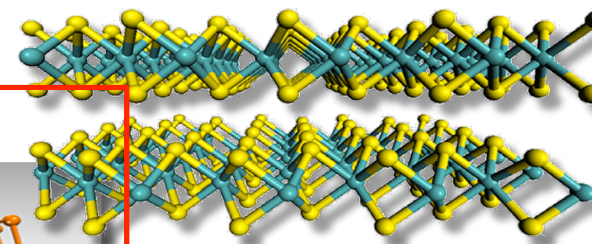
Further Reduce Tunnel Distance: Heterojunction TFET

$I_{ON}\uparrow \rightarrow Trans\uparrow \rightarrow \lambda\downarrow \rightarrow t_{ch}\downarrow$

$Trans \propto \exp(-\lambda \cdot \sqrt{m^*} \cdot E_g)$

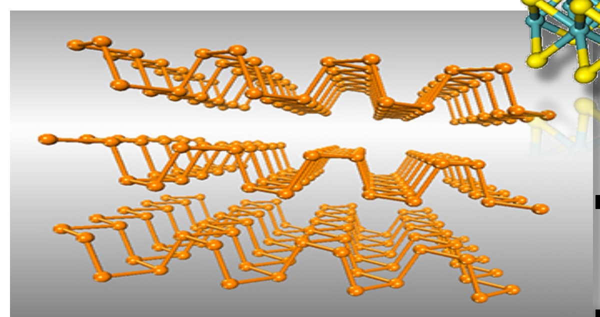
m*

TMD



en.wikipedia.org

Black phosphorus



L. Li et al. Nature Nanotechnol. 9, 372 (2014).

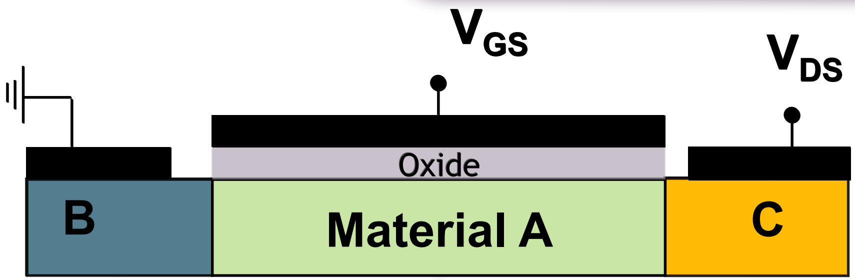
- Various materials (MoS_2, WTe_2, WSe_2 ..)
- Indirect Eg: 1.0eV → 2.5eV

Direct Eg ranging from 0.3 to 1.6eV

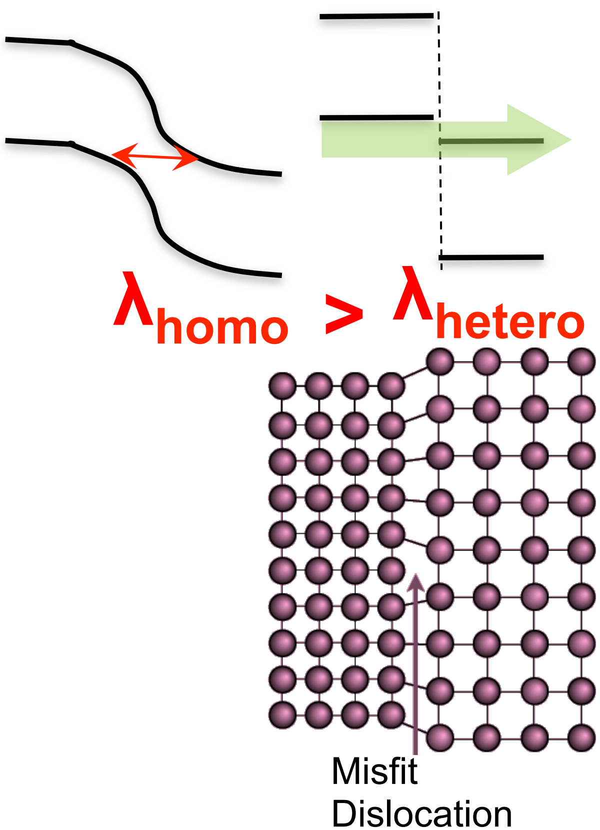
Eg

2D Material Reduces tunnel distance λ

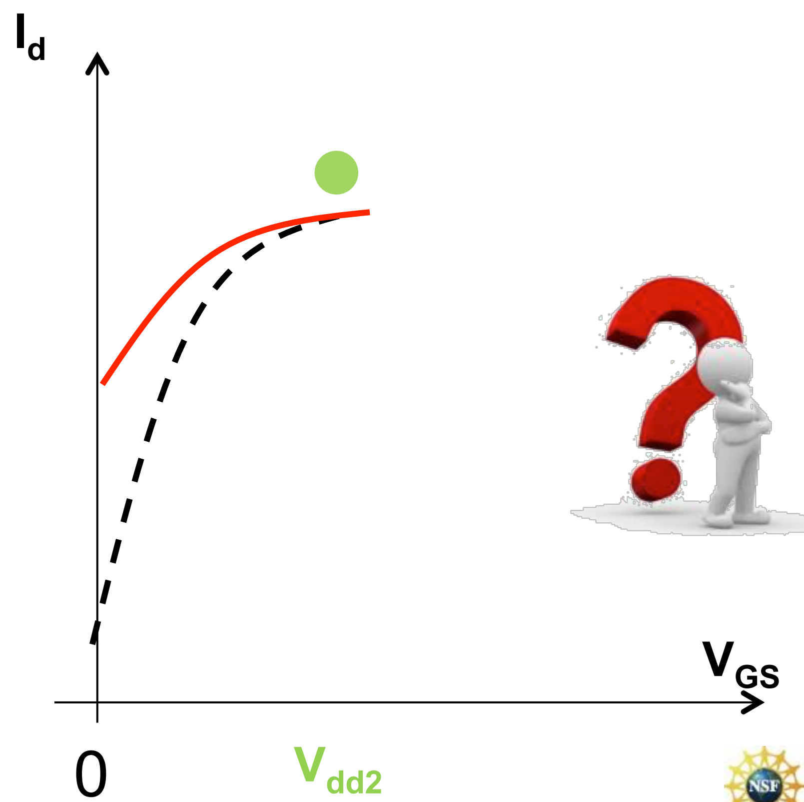
One Common Problem of Heterojunction Tunnel FET



Lattice mismatch degrades the performance of the hetero-junction TFETs



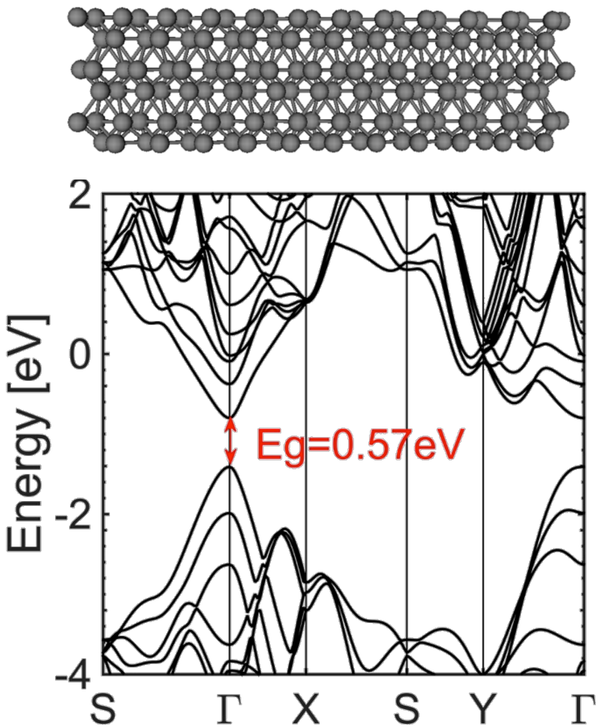
Lattice Mismatch prevents from achieving high quality interface



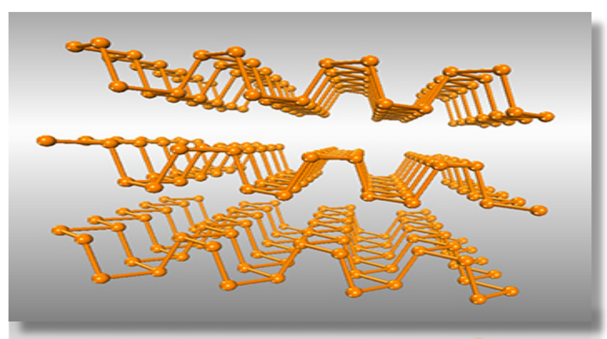
Heterojunction from Thickness Dependent Materials

$I_{ON}\uparrow \rightarrow Trans\uparrow \rightarrow \lambda\downarrow \rightarrow t_{ch}\downarrow$

$Trans \propto \exp(-\lambda \cdot \sqrt{m^*} \cdot E_g)$

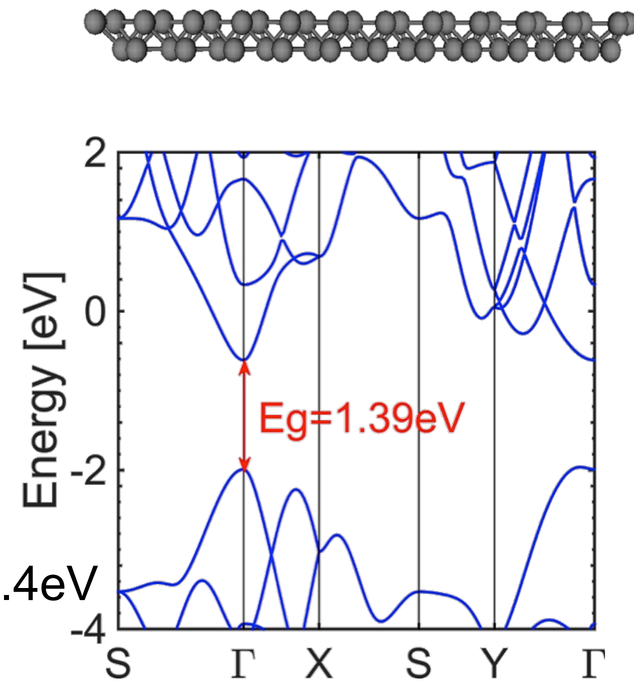


Black phosphorus



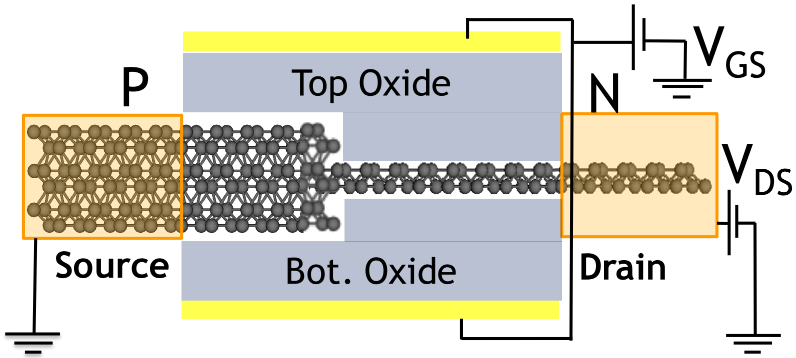
L Li et al, Nature Nanotechnol. 9, 372 (2014).

Direct Eg ranging from 0.3 to 1.4eV

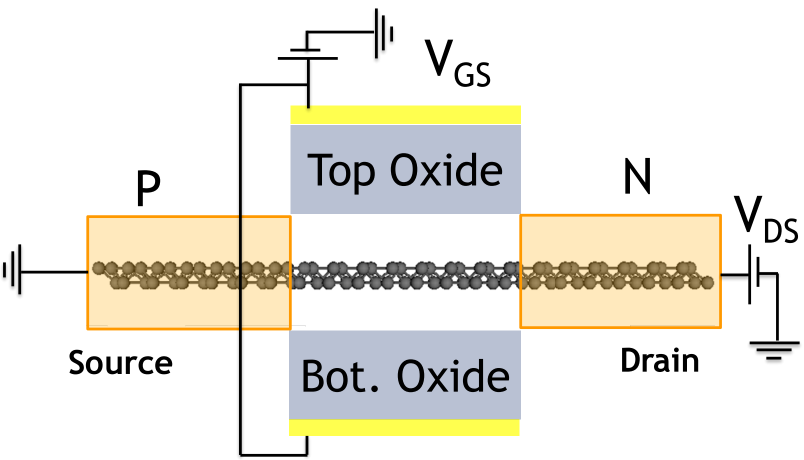


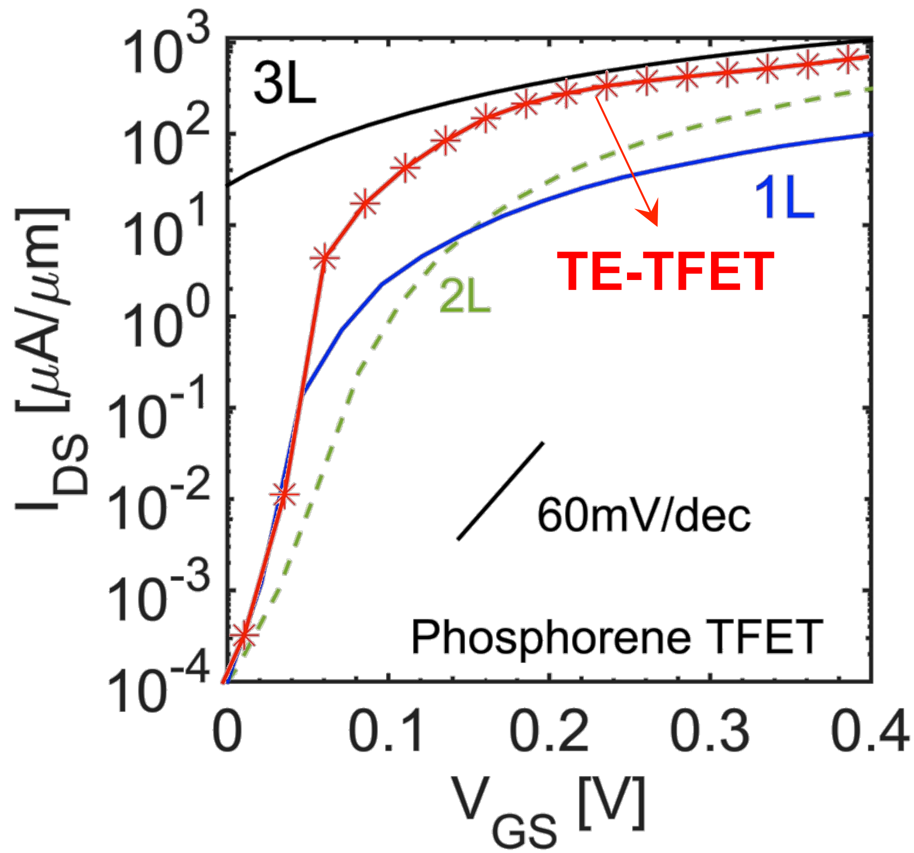
Using thickness dependent Eg to create an heterojunction TFET

Thickness Engineered TFET Performance

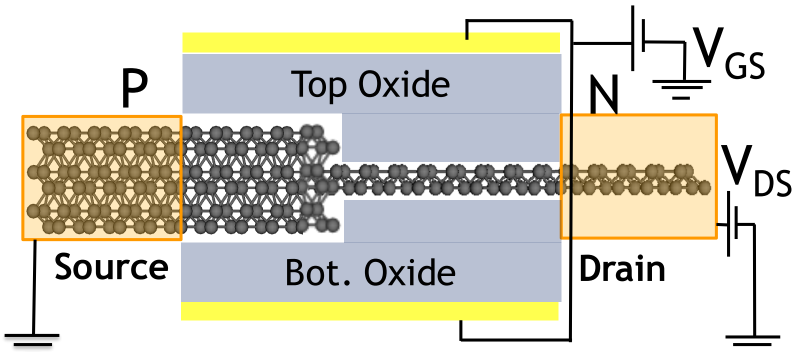


Thickness Engineered TFET → TE-TFET





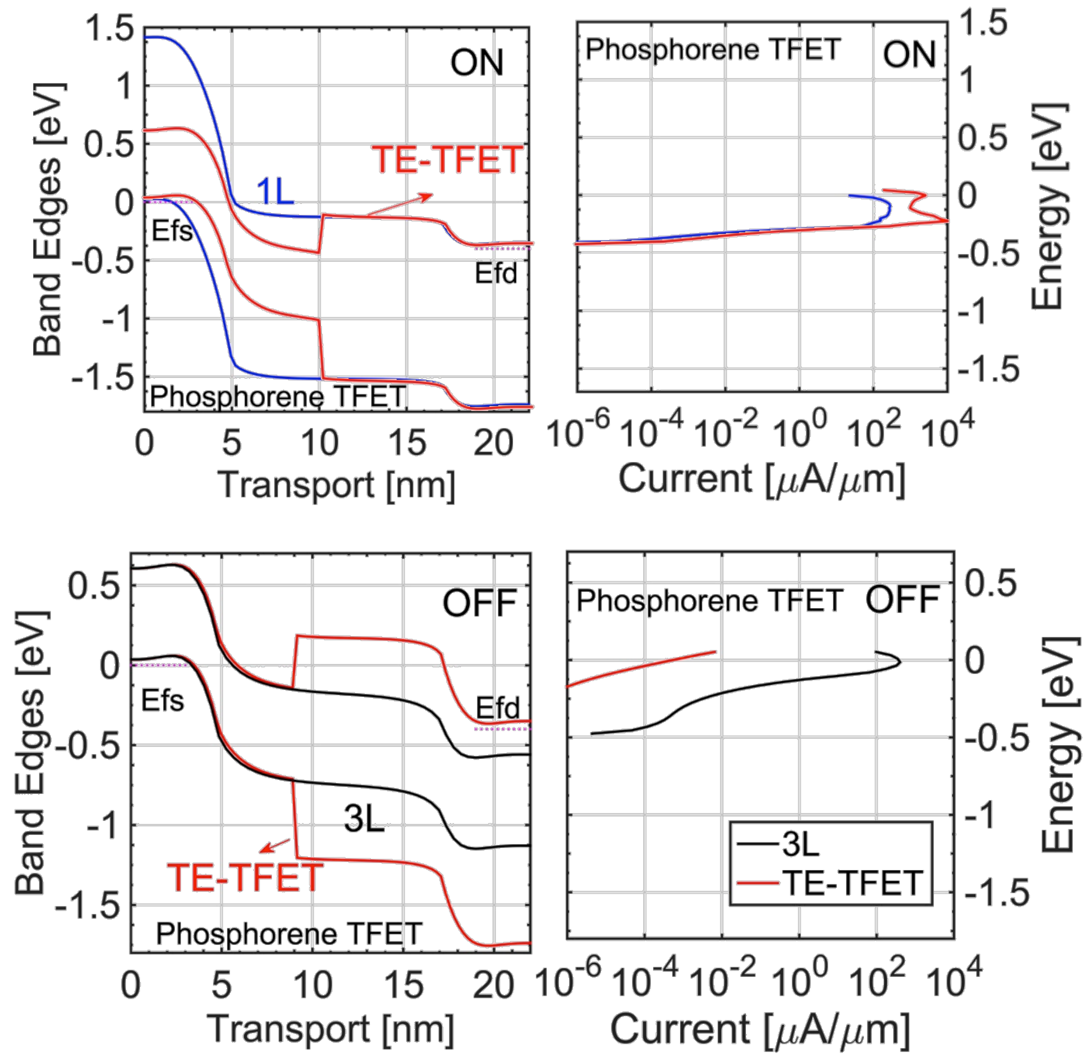
TE-TFET has a better ON, SS compared to homo-junction



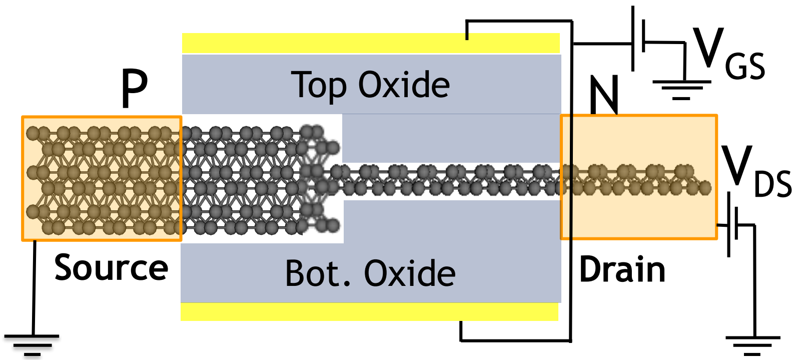
Thickness Engineered TFET →

TE-TFET

- **ON: small tunnel distance**
- **OFF: Large tunnel Barrier**



TE-TFET device scaling

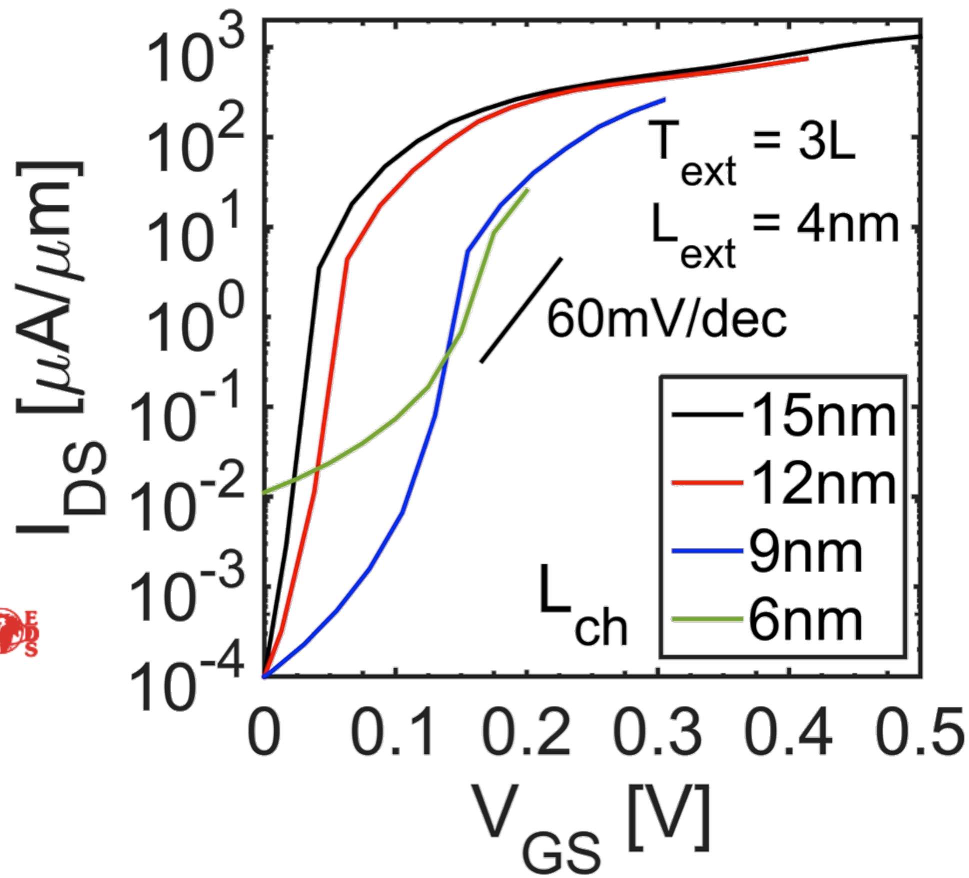


Thickness Engineered TFET → TE-TFET

130 IEEE ELECTRON DEVICE LETTERS, VOL. 38, NO. 1, JANUARY 2017

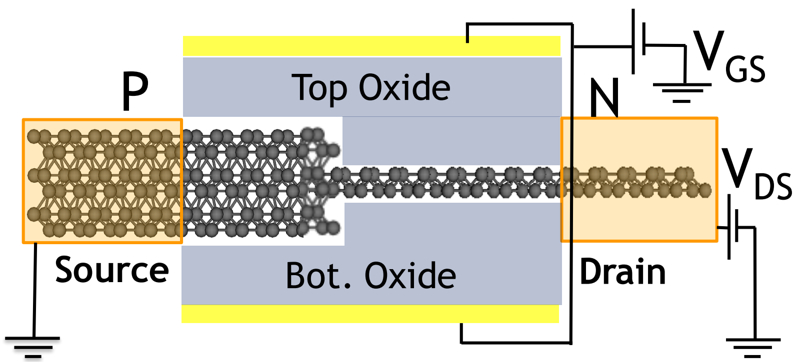
Thickness Engineered Tunnel Field-Effect Transistors Based on Phosphorene

Fan W. Chen, Hesameddin Ilatikhameneh, Tarek A. Ameen, Gerhard Klimeck, and Rajib Rahman

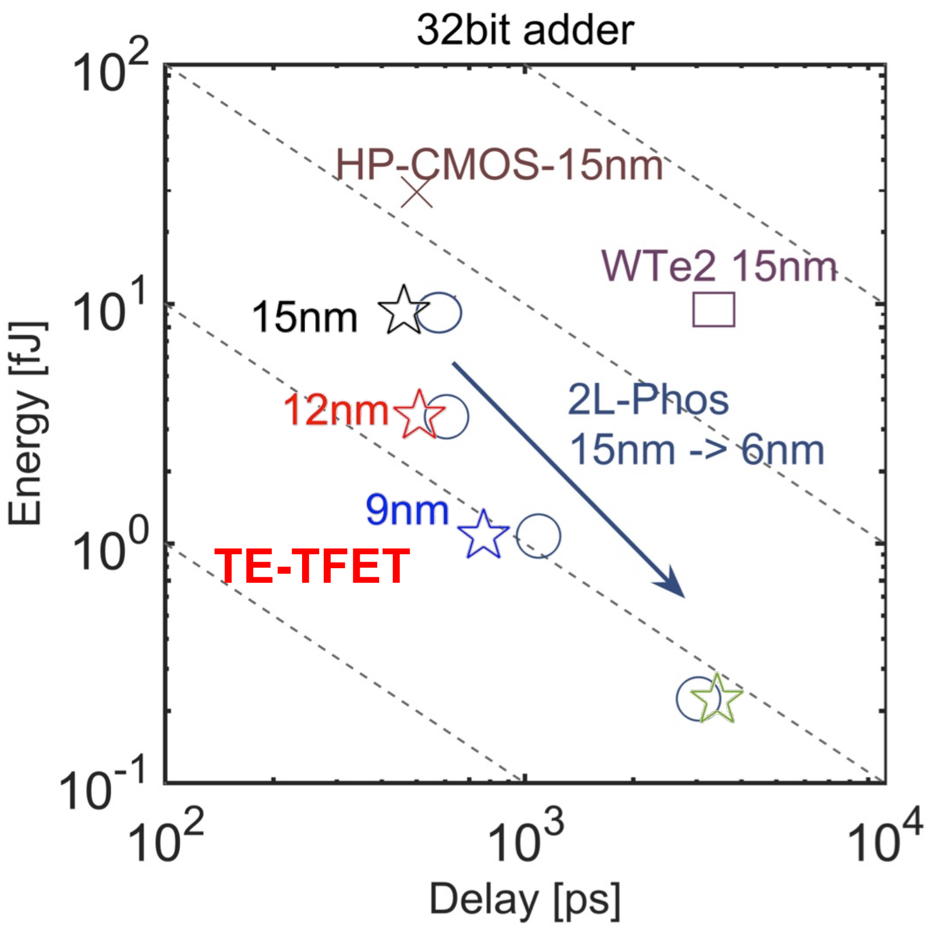


A scalability to 9nm channel length with constant field scaling

TE-TFET: Energy-Delay Product

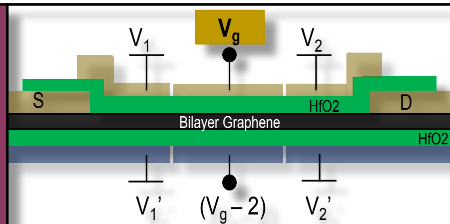
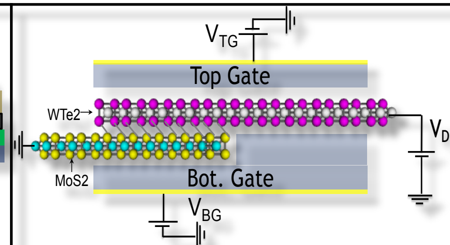
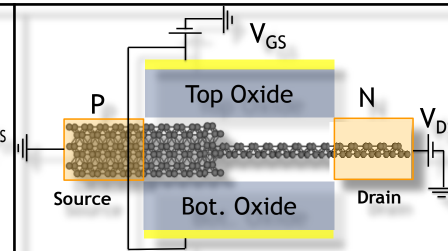


Thickness Engineered TFET → TE-TFET



Energy-Delay not much improvement compared to homo-junction BP TFET

Evaluation of TE-TFET based on phosphorene & Summary

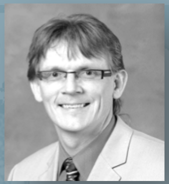
Device			
VDD (V)	0.1	0.3	0.4
ION (uA/um)	100	1000	1000
SS (mV/dec)	8	10	15
Energy Delay Product	Energy ↓ Delay ↓	Energy ↓ Delay ↑	Energy ↓ Delay ↓
Scalability	90nm	15nm	9nm
Comments	Difficult Gate Alignment	Device Switching Mechanism	Not much improved than homo BP, Difficult to fabricate

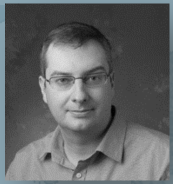
Agenda (Finished)

Motivation	• Power Dissipation Limit → TFET → Low ON → 2D
Method	• Open Boundary, Self-consistent and ballistic Calculation
Bilayer Graphene	• Pro: Low Power, Low Energy, Small Dealy • Con: too large to footprint, difficult gates aligning
Interlayer TFETs	• Gr/hBN/Gr Matching Experiments→ Validates Model • MoS2-WTe2 interlayer TFET → Low Energy, Large Delay Different Switching Mechanism
Black Phosphorous	• Pro: Scale down to 9nm, Low Energy, Small Delay • Con: Not much improvement compared to homo BP TFET, but more difficult to fabricate

Acknowledgements

PhD Committee


Gerhard Klimeck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Archana Tankasala


Yaohua Tan


Luis Jauregui

Thank you for your attention

Thank you!