Ph.D Defense
Low power transistors and Quantum Physics based on
Low Dimensional Materials

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# Agenda

## Motivation
- Why Tunnel FETs based on 2D materials

## Method
- Non-equilibrium, Open Boundary Simulator NEMO5

## Bilayer Graphene
- Experimental Benchmark
- Electrostatically Doped Tunnel FET proposal

## Interlayer TFETs
- Model Assumptions and Validation
- MoS2-WTe2 interlayer Tunnel FET Device physics & Performance

## Black Phosphorous
- Thickness Engineered Tunnel FET proposal
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More transistors, but not faster processors

Dual-Core Itanium 2

Pentium 4

Pentium

386

Power Consumption of transistors need to be reduced

Intel CPU Trends

(source: Intel, Wikipedia, K. Olukotun)
How to reduce the power consumption in a transistor?

Power Consumption $\downarrow \Rightarrow V_{dd} \downarrow$; it requires:
1. Keep Low $I_{OFF}$
2. Keep High $I_{ON}$
3. Small $SS$

$P \propto I_{OFF}$

$P = f \times C \times V_{dd}^2$

$\log I_d$ vs. $V_{dd}$

$V_{GS}$ vs. $V_{dd}$

Ideal

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Victor Moroz Berkeley Seminar 2011
Fundamental limitation of MOSFETs

Thermionic Emission:
Electron: $E >> E_f$, at Fermi Tail

MOSFET: Thermionic emission $\Rightarrow$ SS $> 60$ mV/dec
**Solution to Steep Transistor Tunnel FET (TFET)**

**TFET**

- **V<sub>GS</sub>**
- **V<sub>DS</sub>**
- **p+**
- **i**
- **n+**
- **Oxide**

**TFET → SS < 60 mV/dec → Vdd ↓ possible**

**Electron: E ~ E<sub>f</sub>, at Fermi level**

**ON State:** Small tunneling distance

**OFF State:** Large tunneling distance

**MOSFET**

- **SS < 60 mV/dec**

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Major Challenge in TFETs

- **MOSFET**: $I_{ON} \sim 1000 \, \text{uA/um}$
- **TFET**: $I_{ON} \sim 0.1-10 \, \text{uA/um}$

**Challenge for TFETs: Small $I_{ON}$**

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High ON requires small Tunnel Distance

WKB approximation:

$$\text{Trans} \propto \exp\left(-\lambda \sqrt{m^* E_{\downarrow g}}\right)$$

High ON needs Small $E_g$, small $m^*$, shorter tunnel distance $\lambda$
Thin Channel has Smaller Tunnel Distance

Thick channel

\[ V_{GS} \quad V_{DS} \]

\[
\begin{array}{c}
p+ \\
\uparrow \\
\text{Oxide} \\
\downarrow \\
n+ \\
\end{array}
\]

\[ \lambda_{\text{thick}} > \lambda_{\text{thin}} \]

Thin channel

\[ V_{GS} \quad V_{DS} \]

\[
\begin{array}{c}
p+ \\
\uparrow \\
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\downarrow \\
n+ \\
\end{array}
\]

\[ \lambda_{\text{thick}} > \lambda_{\text{thin}} \]

Thin Channel has smaller tunnel distance \( \lambda \rightarrow \) High ON
2D Material Reduces Tunnel Distance

Graphene

Black phosphorus

TMD


2D Material reduces tunnel distance \( \lambda \)
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Transport in device requires non-equilibrium, open boundary Method
Non-equilibrium, Open Boundary Method

Closed Equilibrium

\[ E\psi = H\psi \]

Schrodinger’s Equation

\[ E = \mu \downarrow 0 \]

Well Defined Fermi Level \( \mu \downarrow 0 \)

Open Boundary Non-Equilibrium

\[
(E - H - \Sigma \downarrow 1 - \Sigma \downarrow 2 )\psi = S
\]

Non-equilibrium, Open boundary Method Capture the required Physics

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Self Consistent calculation

\[ V(\varepsilon \nabla \phi(x)) = -(p(x) - n(x) + Nd - Na) \]

\[ H = [\varepsilon - \phi_1 - t \& \varepsilon - \phi_2 - t \& @ \varepsilon - \phi N ] \]

\[ S = (E_{1f} - H - \Sigma_{1f} - \Sigma_{2f} ) \psi (p(x) - n(x)) \sim \psi \psi \dagger \]

self-consistent calculation is performed for electrostatics
The material parameters need to be obtained.

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Obtain Parameters

Material Parameters such from DFT or literature

Create Device Structure

Self-consistent calculation

Single layer MoS$_2$ band structure

Output

Non-equilibrium, Open Boundary Solver & Poisson

Extract Device Performance Parameters: ON-current, S.S etc

$p(x) - n(x)$

$\nabla(\epsilon \nabla \phi(x)) = -(p(x) - n(x) + Nd - Na)$

Converge

Current (I-V)
Capacitance (C-V)
Potential, Density

$H \rightarrow H - \phi(x)$

$S = (EI - H - \Sigma_1 - \Sigma_2)\psi$

$(p(x) - n(x))\sim\psi \cdot \psi^*$

$60mV/dec$
Device Evaluation includes:

- Vdd
- ON
- SS
- Energy and Delay (circuit)
- Scalability
- Fabrication
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Graphene has the smallest combination $m^*$ and $E_g$ for homojunction TFET.
Bilayer Graphene: Tunable $E_g$

Bilayer Graphene TFET: Small Achievable $E_g$, Small effective mass

http://newscenter.lbl.gov/
Bilayer Graphene double gate FET
Simulation and Experiment

Simulation Matches Experiment:
IV shifting and $I_{\text{ON}}/I_{\text{OFF}}$

IV Shifting

At 300K: $I_{\text{on}}/I_{\text{off}} \sim 100$
F. Xia et al. Nano Lett. 2010, 10, 715-718

ON/OFF $\sim 100$
IV Shifting in Bilayer Graphene Double Gate FET

Band Diagram

IV Shifting result from tunable band gap

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Chemical Doping

- $V_{GS}$
- $V_{DS}$
- Oxide
- p+
- i
- n+

Electrical Doping

- $V_{TG1}$
- $V_{TG2}$
- Top Gate 1
- Top Gate 2
- $V_{BG1}$
- $V_{BG2}$
- Bot. Gate 1
- Bot. Gate 2
- Source
- Drain
- $V_{DS}$

• 1: Vertical field need in order to create a $E_g$
• 2: Doping 2D material is challenging

Electrical Doping in bilayer graphene creates tunnel junction

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Proposed Bilayer Graphene TFET

Advantages

Configurable post after fabrication between pin and nip

No dopant states within bandgap → good OFF-state performance

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BLG TFET can operate at 0.1V with 100uA/um ON current
Bilayer Graphene TFET: Scalability and EDP

- Good Energy Delay Product
- Larger foot print → not a good alternative
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<td>Energy Delay</td>
<td>Energy ↓</td>
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<tr>
<td>Product</td>
<td>Delay ↓</td>
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<td>90nm</td>
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<td>Comments</td>
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  - Pro: Low Power, Low Energy, Small Dealy
  - Con: too large to footprint, difficult gates aligning

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  - MoS2-WTe2 interlayer Tunnel FET Device physics & Performance

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Further Reduce Tunnel Distance: Heterojunction TFET

Trans $\propto \exp(-\lambda \sqrt{m^* E_{\text{tg}}})$

Various materials (MoS$_2$, WTe$_2$, WSe$_2$ ..)

$E_g$: 1.0eV $\rightarrow$ 2.5eV

Chemical formula: MX$_2$
MoS$_2$, WSe$_2$

Various TMD materials are available for heterojunction TFET
$\Rightarrow$ Further reduce $\lambda$
A Common Problem for Heterojunction Tunnel FET

High Interface states degrades the OFF performance in heterojunction TFETs

\[ \lambda_{\text{homo}} > \lambda_{\text{hetero}} \]

Interface States!

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Surface promises low density of interface defects

Tunnel distance $\lambda$, is the sub-nanometer interlayer distance
MoS2-WTe2 combination is chosen for broken band alignment
Assumption I: different layer has been strained to the same lattice constant to be registered

Assumption II: Interface VdW coupling is the average of the VdW of the two materials
Tight binding compared with DFT

TB matches well with DFT along the band edge at K point. This is important for transport.
Gr/BN/Gr vertical tunneling

Gr/BN/Gr device structure is simulated to validate our model

Assumption I & II are also applied to this simulation

Previous study predicts 2~3 orders of magnitude higher current

Gr/BN/Gr structure is simulated in order to Validate Model
Gr/BN/Gr: NEMO5 Current value matches experiment

NEMO5 results match experimental current value → Model Validated
Motivation: Power Dissipation Limit → TFET → Low ON → 2D

Method: Open Boundary, Self-consistent and ballistic Calculation

Bilayer Graphene:
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Interlayer TFETs:
- Gr/hBN/Gr Matching Experiments → Validates Model
- MoS2-WTe2 interlayer Tunnel FET Device physics & Performance

Black Phosphorous: Thickness Engineered Tunnel FET proposal
All the literature believes Bands Shifting Switching Mechanism
Interlayer TFET Bands Shifting Switching Mechanism: OFF

Bands Shifting Switching Mechanism

Top Gate

Drain

Source

Bot. Gate

log f(E)

E

E_{fs}

E_{fd}

CB

VB

CB

VB

OFF

0

V_g

I_d
Interlayer TFET Bands Shifting Switching Mechanism: OFF

Bands Shifting Switching Mechanism

Source

Top Gate

Bot. Gate

Sweep

Drain

Fix

log f(E)

E

E_{fs}

E_{fd}

CB

VB

CB

VB

ON

OFF

I_d

V_g

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The Definition of Extension Region

Device with Bands Shifting Switching Mechanism suggests device has only Overlap Region

Extension regions is defined as the region that has only one layer
The importance of extension region: OFF current and SS

ON and SS are degraded with shorter extension region.
Both Top and Bottom Layer stay charged at the OFF state; Long extension region blocks the leakage current.
The importance of extension region: band diagram & current

Overlap Region high density at OFF, Extension region turns off the device, Bands Shifting is Wrong
MoS2-WTe2 interlayer TFET: Highly Charge Device

Top and Bottom Layer stay highly Charged during both ON and OFF
MoS2-WTe2 Interlayer TFET: Decrease in top layer charge

Decrease in top layer charge is due to current flowing
MoS2-WTe2 Interlayer TFET: Total Charge

Though Device stays highly charged, total Charge is not huge due to neutralization.
MoS2-WTe2 Interlayer TFET: ON and SS

L_{ch} = 30nm
V_{DS} = 0.3V
V_{BG} = 0.5V
L_{ext} = 15nm
EOT = 0.5nm

WTe2-MoS2 Interlayer TFET demonstrates a smallest SS of 10mV/dec
ON current ~ 1000 \mu A/\mu m
MoS2-WTe2 interlayer TFETs does not show too much improvement in EDP.
### Evaluation of MoS2-WTe2 interlayer TFET

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<th>SS (mV/dec)</th>
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<td>1000</td>
<td>10</td>
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<td>15nm</td>
<td>Device Switching Mechanism</td>
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  - Power Dissipation Limit ➔ TFET ➔ Low ON ➔ 2D

- **Method**
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- **Bilayer Graphene**
  - **Pro**: Low Power, Low Energy, Small Delay
  - **Con**: too large to footprint, difficult gates aligning

- **Interlayer TFETs**
  - Gr/hBN/Gr Matching Experiments ➔ Validates Model
  - MoS2-WTe2 interlayer TFET ➔ Low Energy, Large Delay
  - Different Switching Mechanism

- **Black Phosphorous**
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• MoS2-WTe2 interlayer TFET → Low Energy, Large Delay Different Switching Mechanism |
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Further Reduce Tunnel Distance: Heterojunction TFET

\[ I_{\downarrow\uparrow{ON}} \rightarrow Trans \rightarrow \lambda \rightarrow t\downarrow ch \downarrow \]

\[ Trans \propto \exp(-\lambda \cdot \sqrt{m^* \cdot E_{g}}) \]

2D Material Reduces tunnel distance \( \lambda \)

Direct \( E_g \) ranging from 0.3 to 1.6eV

Various materials (MoS2, WTe2, WSe2 ..)
Indirect \( E_g \): 1.0eV \( \rightarrow \) 2.5eV

Black phosphorus

Eg

m *
One Common Problem of Heterojunction Tunnel FET

Lattice mismatch degrades the performance of the heterojunction TFETs

Lattice Mismatch prevents from achieving high quality interface

\[ \lambda_{\text{homo}} > \lambda_{\text{hetero}} \]

\[ \text{Misfit Dislocation} \]
Using thickness dependent $E_g$ to create an heterojunction TFET
TE-TFET has a better ON, SS compared to homo-junction
Thickness Engineered TFET → TE-TFET

- **ON**: small tunnel distance
- **OFF**: Large tunnel Barrier
Thickness Engineered TFET → TE-TFET

A scalability to 9nm channel length with constant field scaling
TE-TFET: Energy-Delay Product

Thickness Engineered TFET → TE-TFET

Energy-Delay not much improvement compared to homo-junction BP TFET
### Evaluation of TE-TFET based on phosphorene & Summary

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- Con: too large to footprint, difficult gates aligning

**Interlayer TFETs**
- Gr/hBN/Gr Matching Experiments $\rightarrow$ Validates Model
- MoS2-WTe2 interlayer TFET $\rightarrow$ Low Energy, Large Delay
  Different Switching Mechanism

**Black Phosphorous**
- Pro: Scale down to 9nm, Low Energy, Small Delay
- Con: Not much improvement compared to homo BP TFET, but more difficult to fabricate
PhD Committee
Gerhard Klimeck
Michael Manfra
Zhihong Chen
Supriyo Datta
Yong Chen
John Peterson

Colleagues & Mentors:
Rajib Rahman
Tillmann Kubis
Hesameddin Ilatikhameneh
Archana Tankasala
Yaohua Tan
Luis Jauregui

Thank you for your attention
Thank you!