Steep Sub-threshold Swing Transistors

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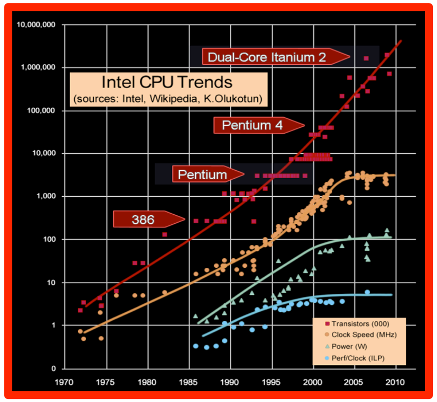
Outline

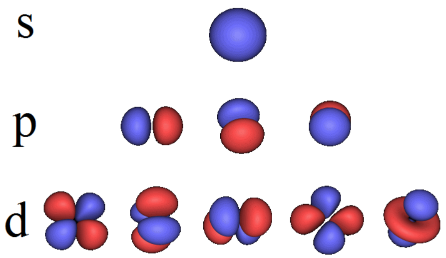
1) Motivation for steep transistors



Number of transistors

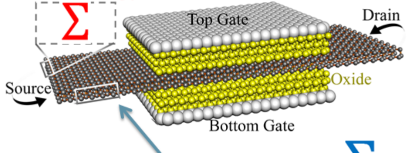
Frequency

2) Method: Atomistic transport simulation



- Inject carriers from contacts

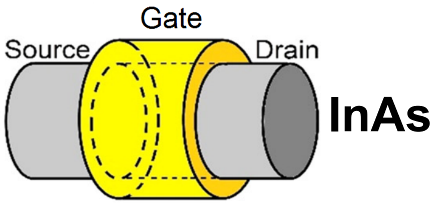
Self energy Σ



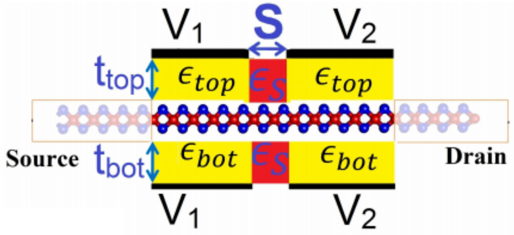
- Scattering processes Σ

3) Tunnel transistors

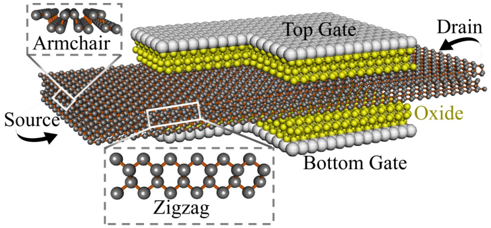
III-V



2D



Novel devices



Agenda

Introduction:

1) **Motivation for steep transistors**
2) Requirements for steep tunnel transistors

Atomistic quantum transport simulation

1) Benchmark with experiment
2) Verify and extend analytic models

Tunnel transistors

1) III-V materials
2) 2D materials
3) Best materials for scaling challenge

Motivation for steep transistors

Year	1995	2005	2015
CPU Freq.	100 MHz	1-2 GHz	2-4 GHz

GTA I

GTA IV

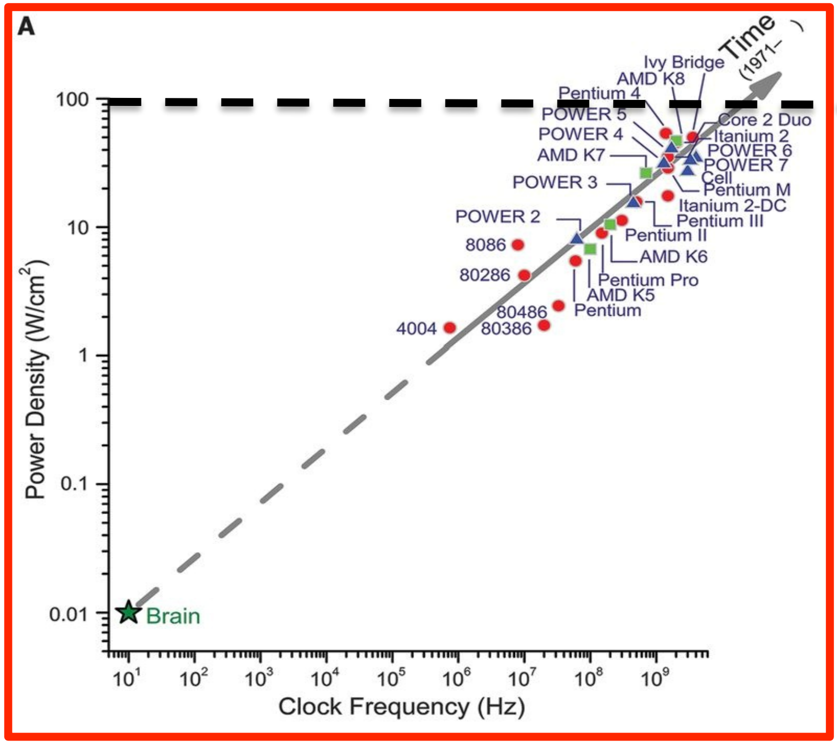
GTA VI

Freq. Boost ~10X ~2X

Motivation for steep transistors

Power dissipation is the main challenge of electronics.

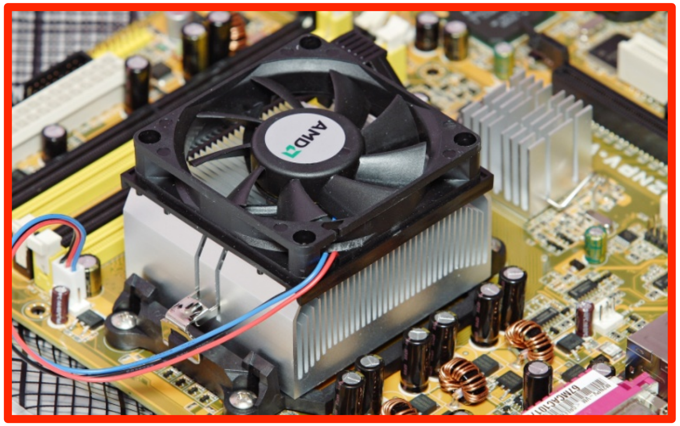
Power dissipation trend



Science 8 August 2014: Vol. 345 no. 6197 pp. 668-673

Cooling capability

Cooling limit

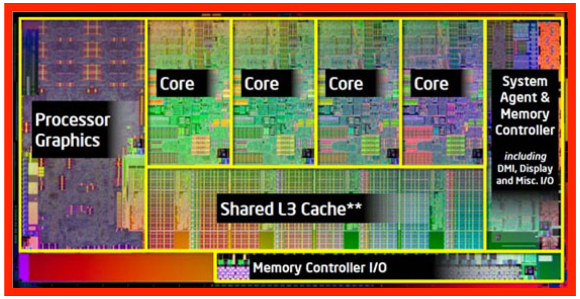


100 W/cm^2 is our cooling limit

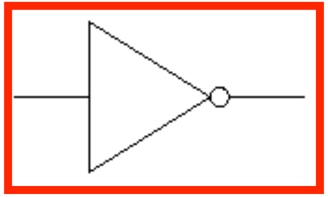
en.wikipedia.org

Origin of Power consumption

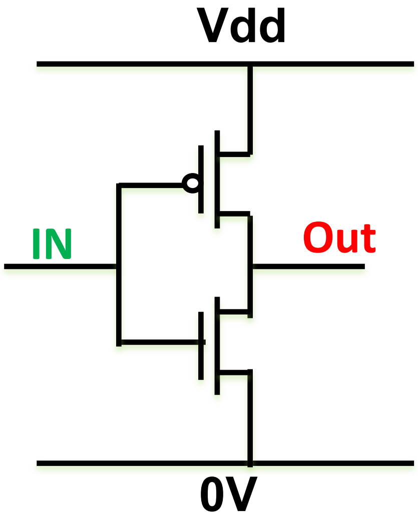
CPU   Logic blocks   Logic gates   Transistor



Not gate



Look into power dissipation at device level

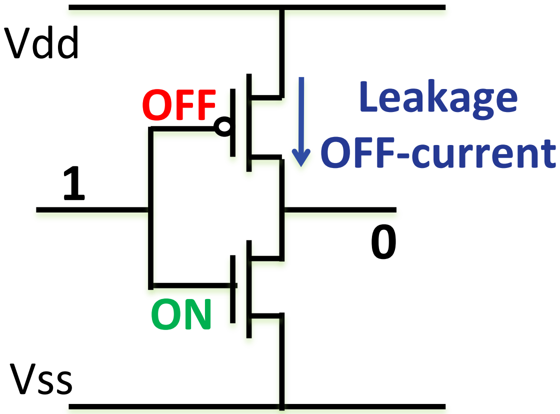


www.cpui5.com
www.anandtech.com

Origin of Power consumption

What is the origin of power consumption?

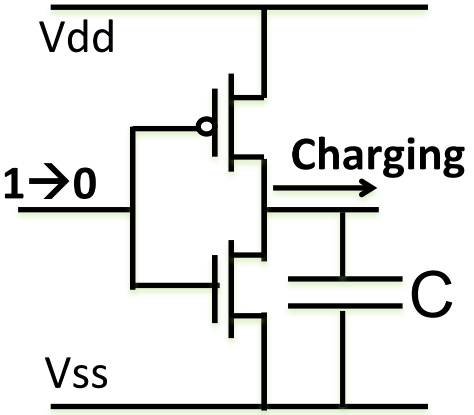
Static power



Ideal: $P = 0$

Reality: $\boxed{P \propto I_{OFF}}$

Dynamic power



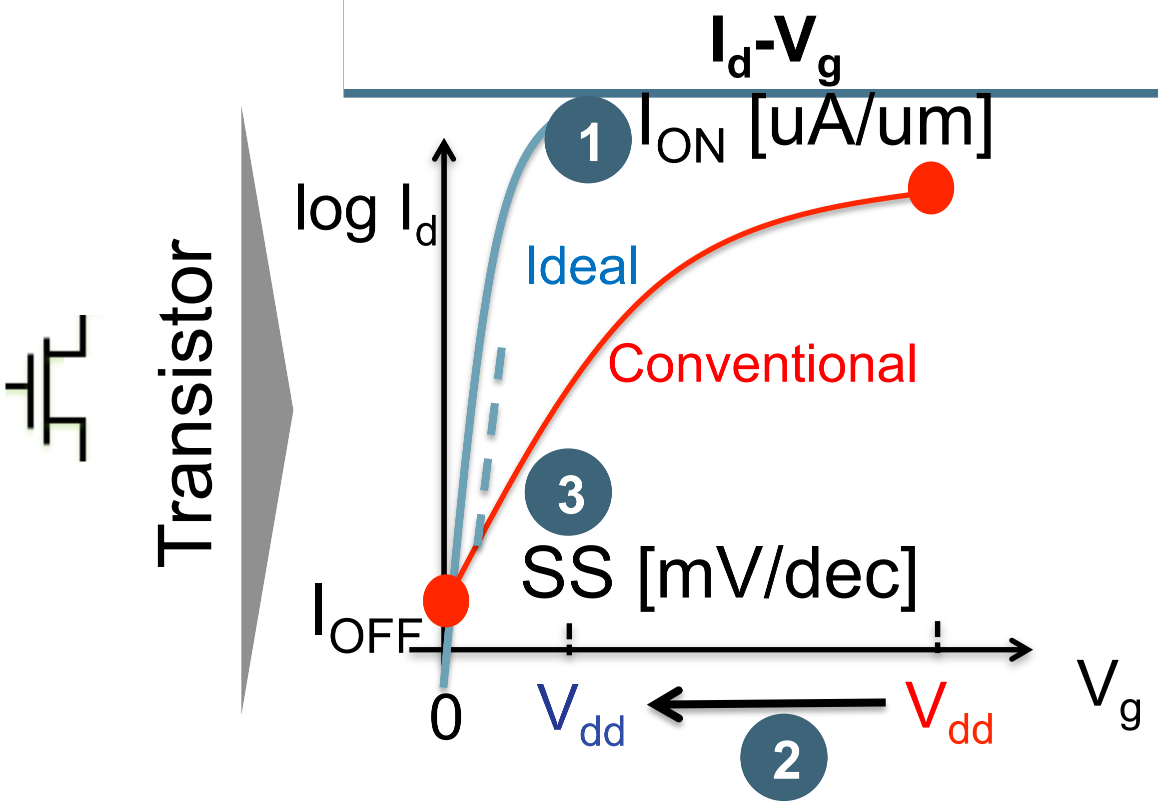
$$P = f \times C \times V_{dd}^2$$

$\downarrow P$ $\downarrow$ ✗ $\downarrow$ ✓ $\downarrow$

Major factors in power consumption: $\left\{\begin{array}{l} V_{dd} \\ I_{OFF} \end{array}\right.$

Ideal switch

What is the ideal transistor for low power application?



Ideal switch provides

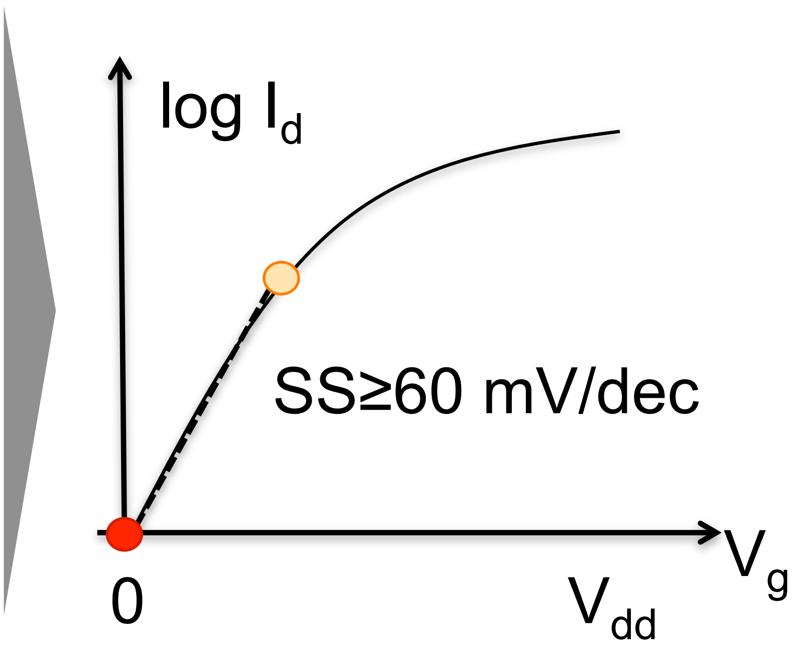
- **High I_{ON} (> 1000 uA/um)**
- **Low SS (< 60 mV/dec)**

Silicon MOSFETs

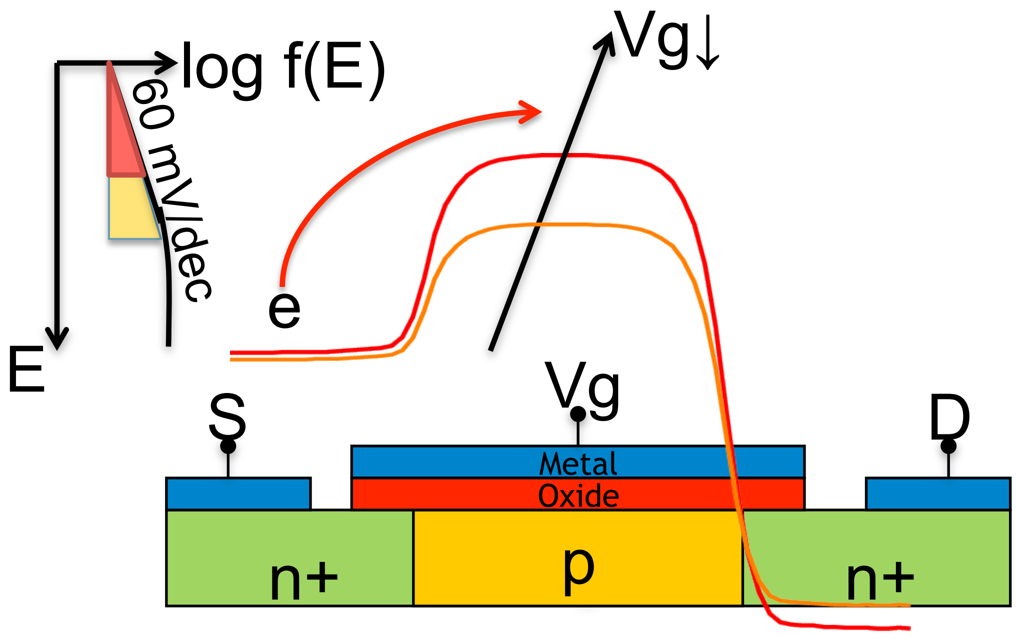
- SS in MOSFETs is limited to 60mV/dec
- Fermi-Dirac distribution has 60mV/dec slope at room temperature.

I_d-V_g

MOSFET



Operation

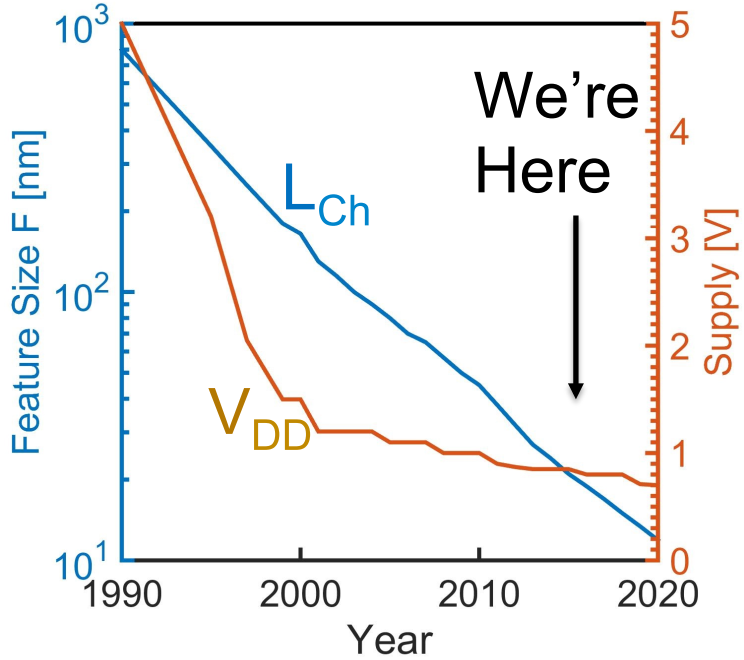


Thermionic emission → SS > 60 mV/dec

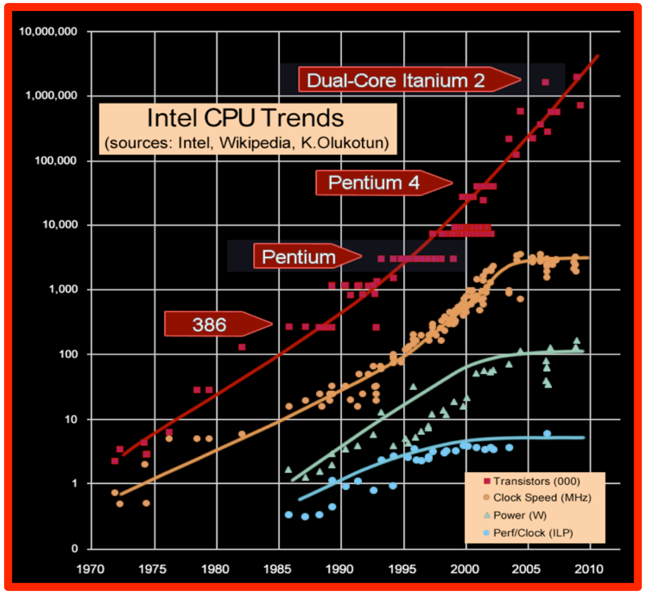
Challenge of MOSFETs

Scaling transistors are becoming more challenging

L_{ch} + V_{DD} scaling [ITRS]



Scaling consequence



2005: free lunch is over, updated 2009

Number of transistors

Frequency

Power

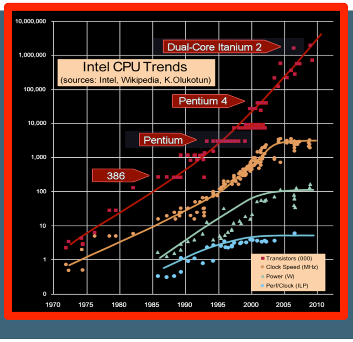
Agenda

Introduction:

1) Motivation for steep transistors

   Reduce power consumption

2) Requirements for steep transistors



Atomistic quantum transport simulation

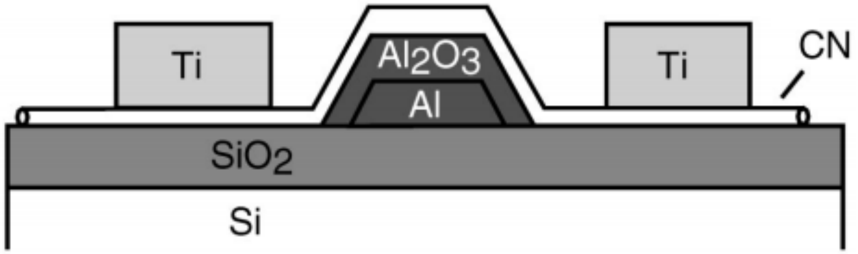
1) Benchmark with experiment
2) Verify and extend analytic models

Tunnel transistors

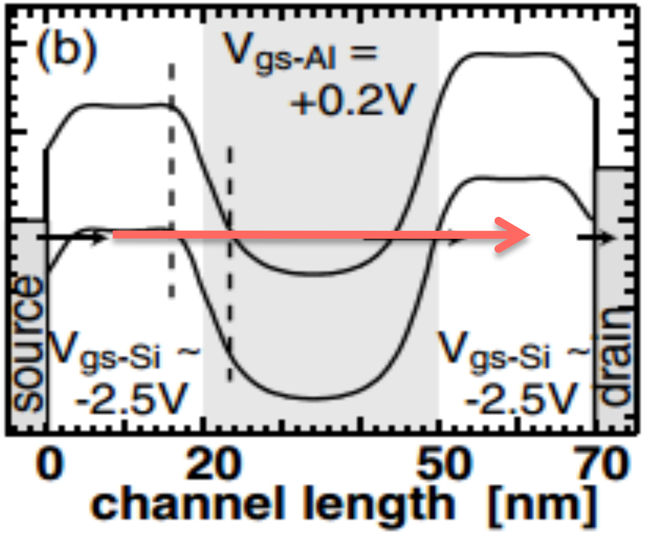
1) III-V materials
2) 2D materials
3) Best materials for scaling challenge

The first steep transistor (SS < 60 mV/dec) : Tunneling transistor based on CNT

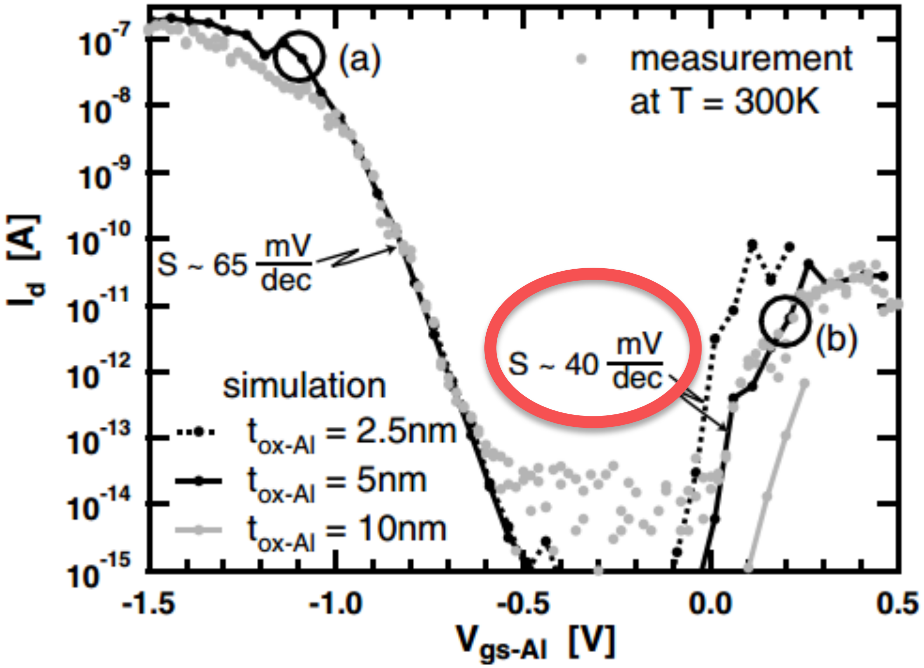
Device structure



Band diagram



I-V



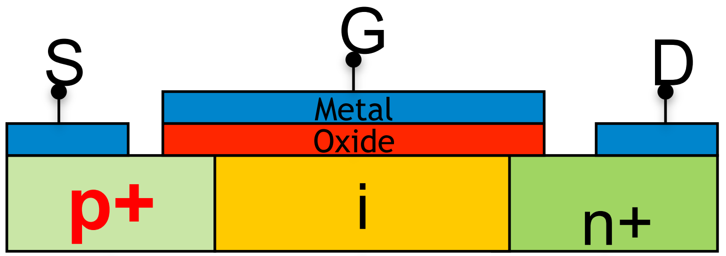
Band to band tunneling

Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors

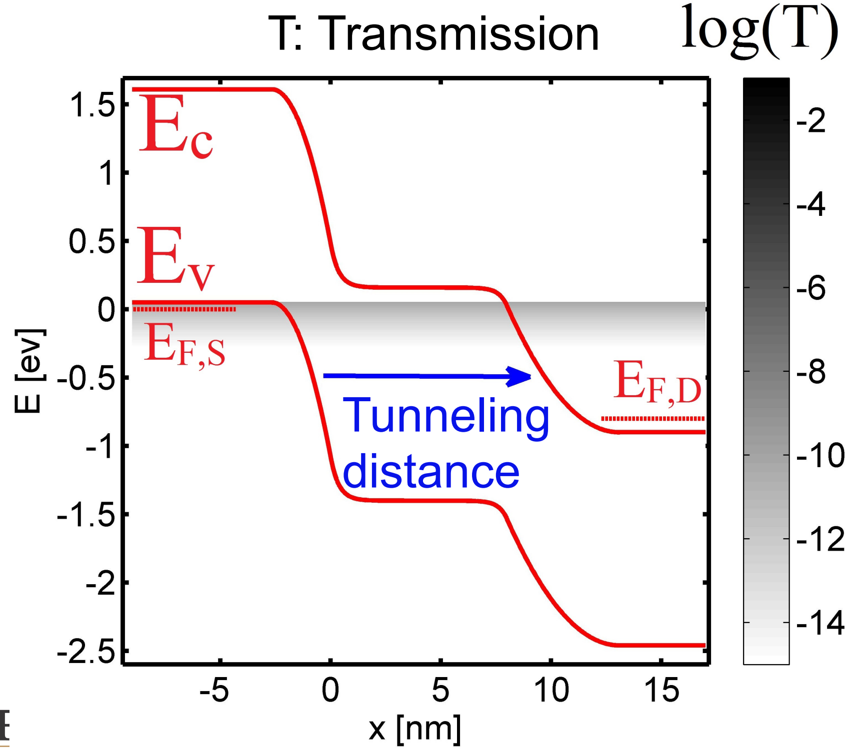
J. Appenzeller,[1] Y.-M. Lin,[1] J. Knoch,[2] and Ph. Avouris[1]

How do Tunnel FETs (TFETs) work?

Device structure

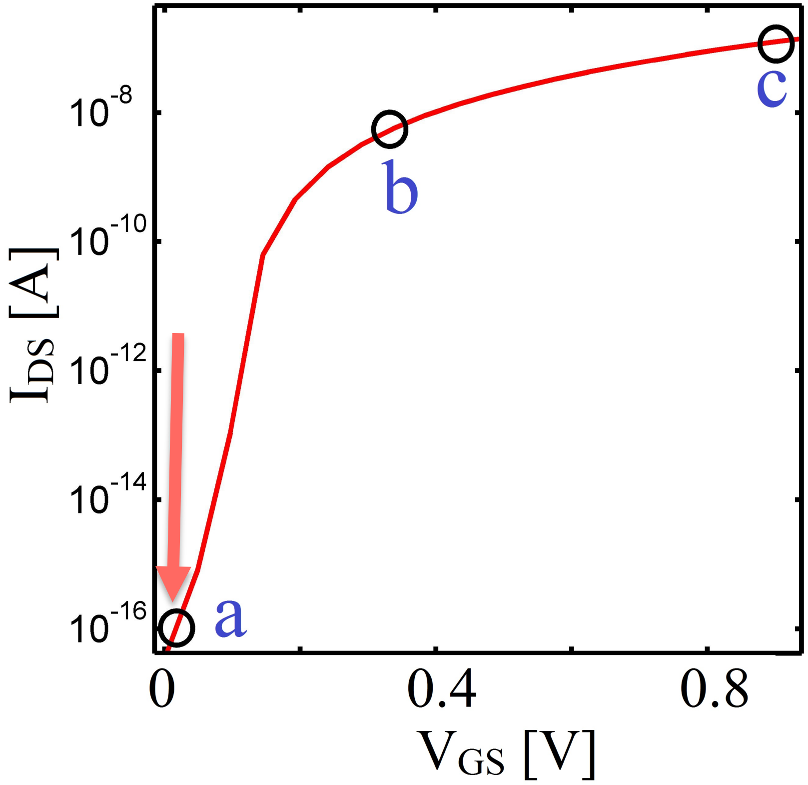


T: Transmission



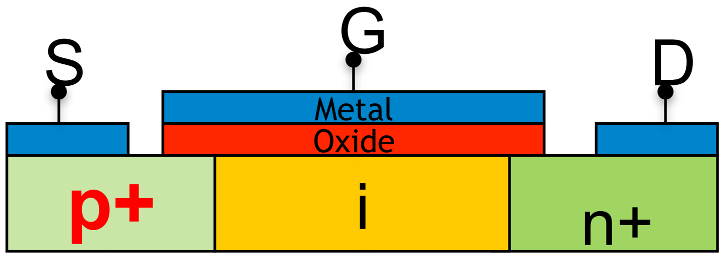
I-V

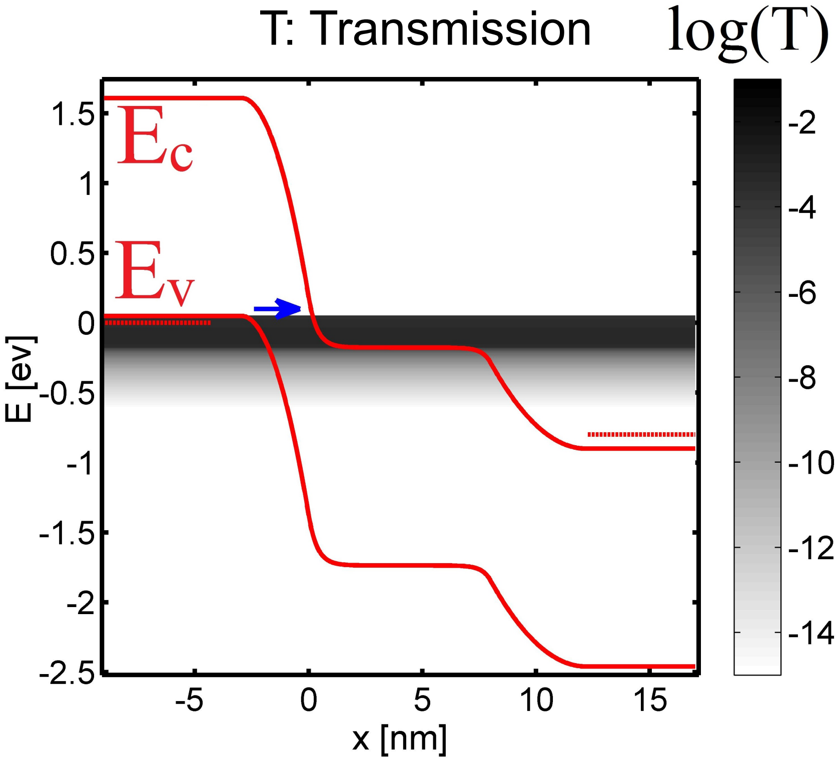
OFF-state



How do Tunnel FETs (TFETs) work?

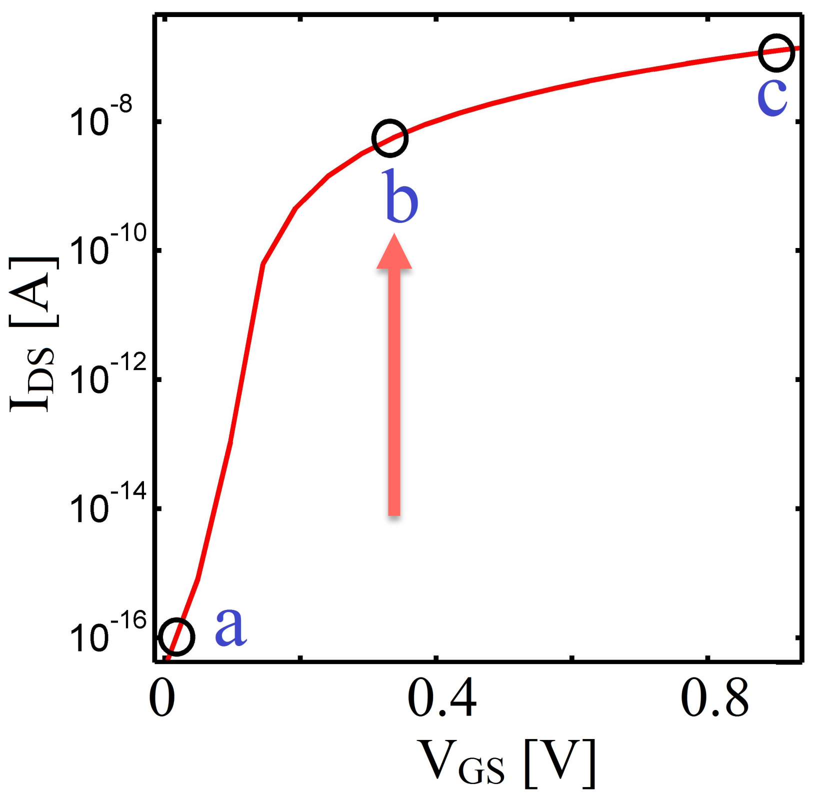
Device structure





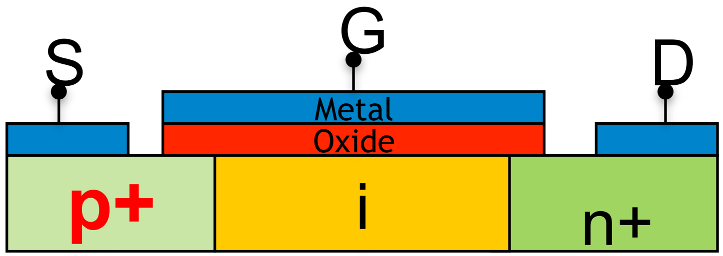
I-V

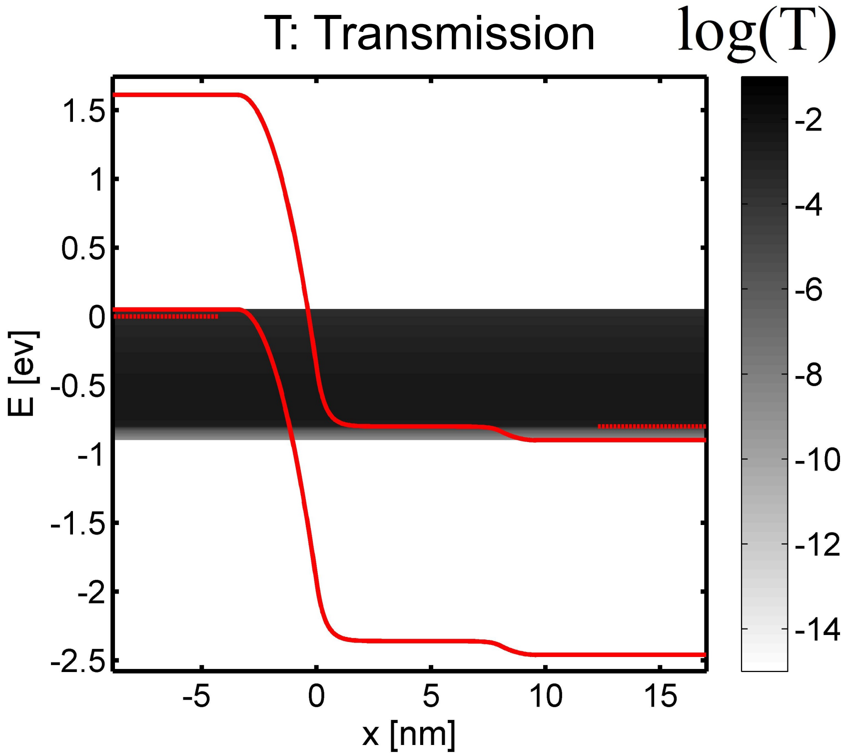
OFF-to-ON transition



How do Tunnel FETs (TFETs) work?

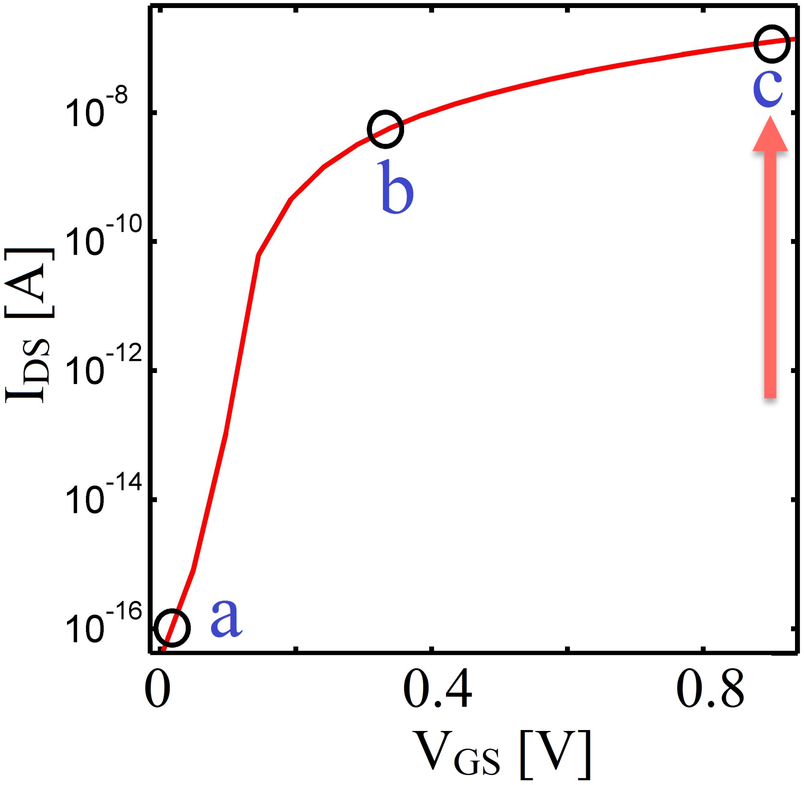
Device structure



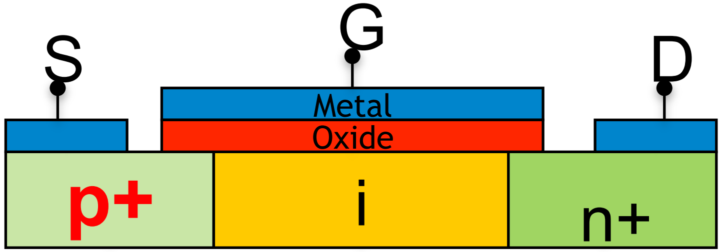


I-V

ON-state



P-i-N transistor → SS < 60 mV/dec ?



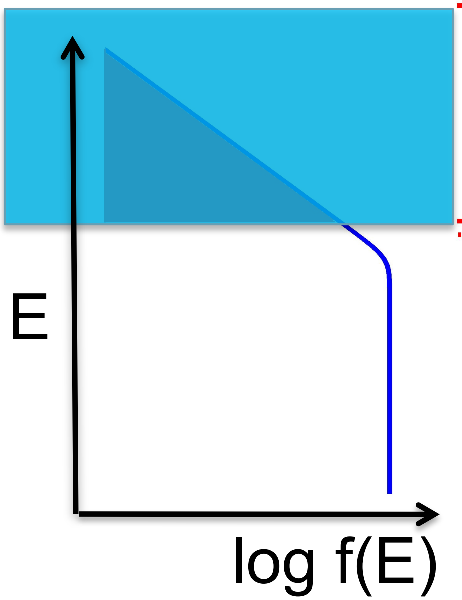
No

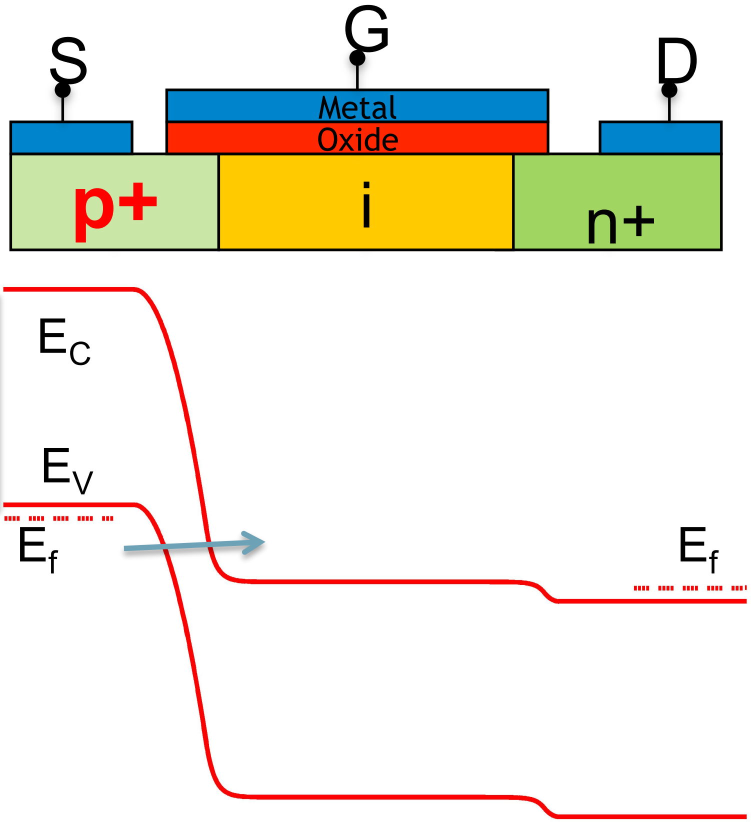
There are 3 requirements for steep device.

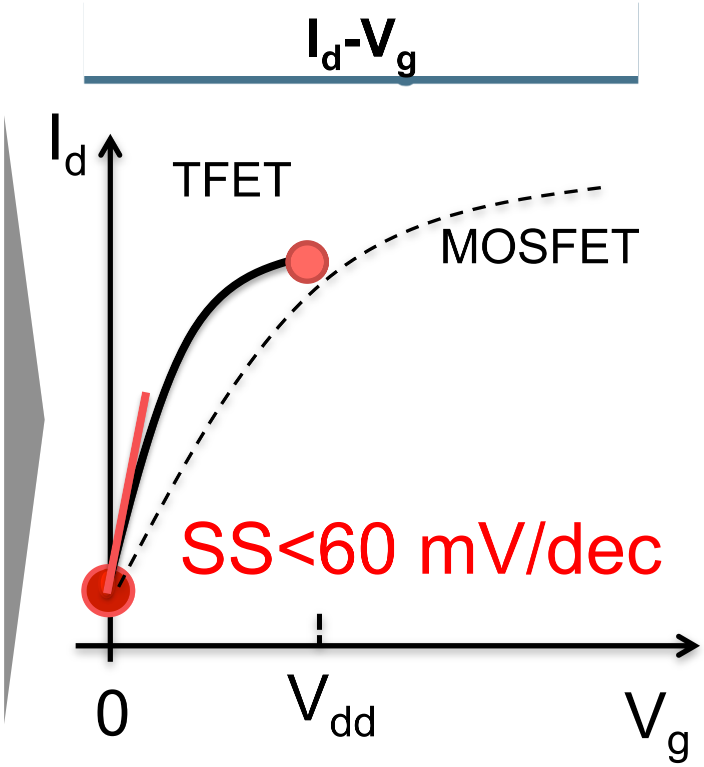
Steep switching requirements

How SS < 60 mV/dec can be achieved?

Hot carriers are filtered out by Semiconductor bandgap





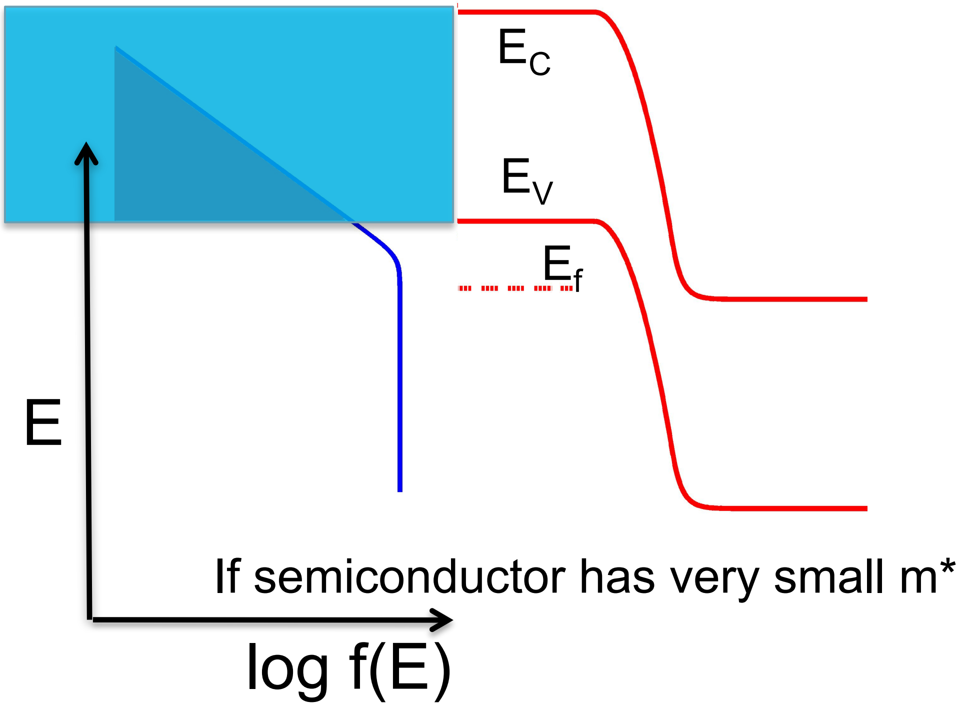


Filtering out hot carriers.

Steep switching requirements

Requirements for SS < 60 mV/dec

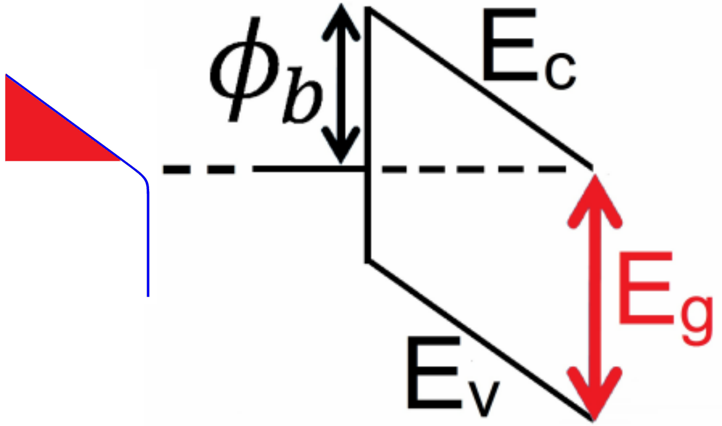
1) Effective energy filtering



If semiconductor has very small m*

Example

Schottky barrier is a tunneling device:
→ No energy filtering
→ SS > 60 mV/dec

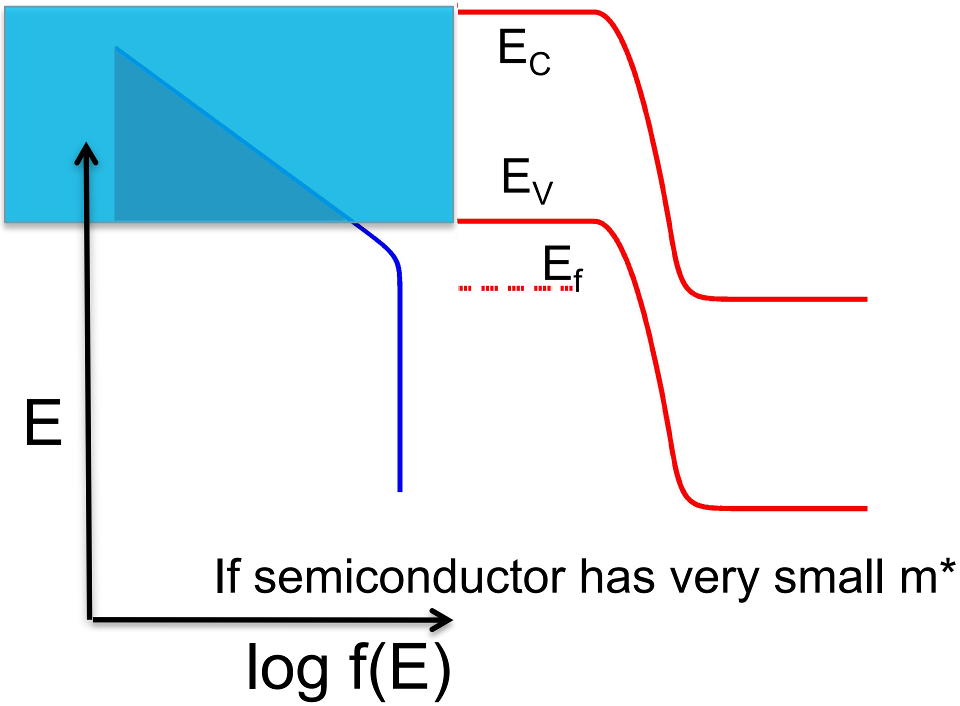


Optimized source doping level is required.

Steep switching requirements

Requirements for SS < 60 mV/dec

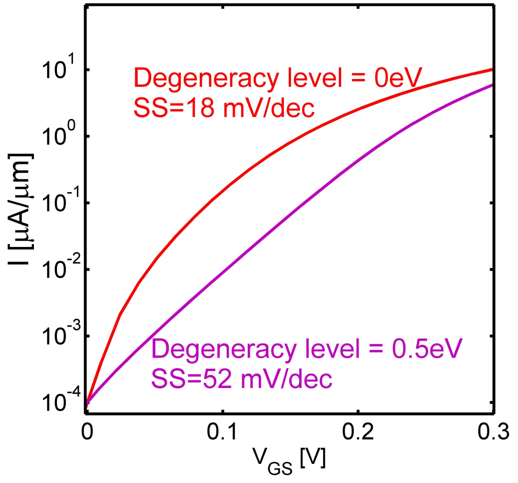
1) Effective energy filtering



If semiconductor has very small m*

Example

Increasing degeneracy
→ Redcued energy filtering
→ SS ~ 60 mV/dec

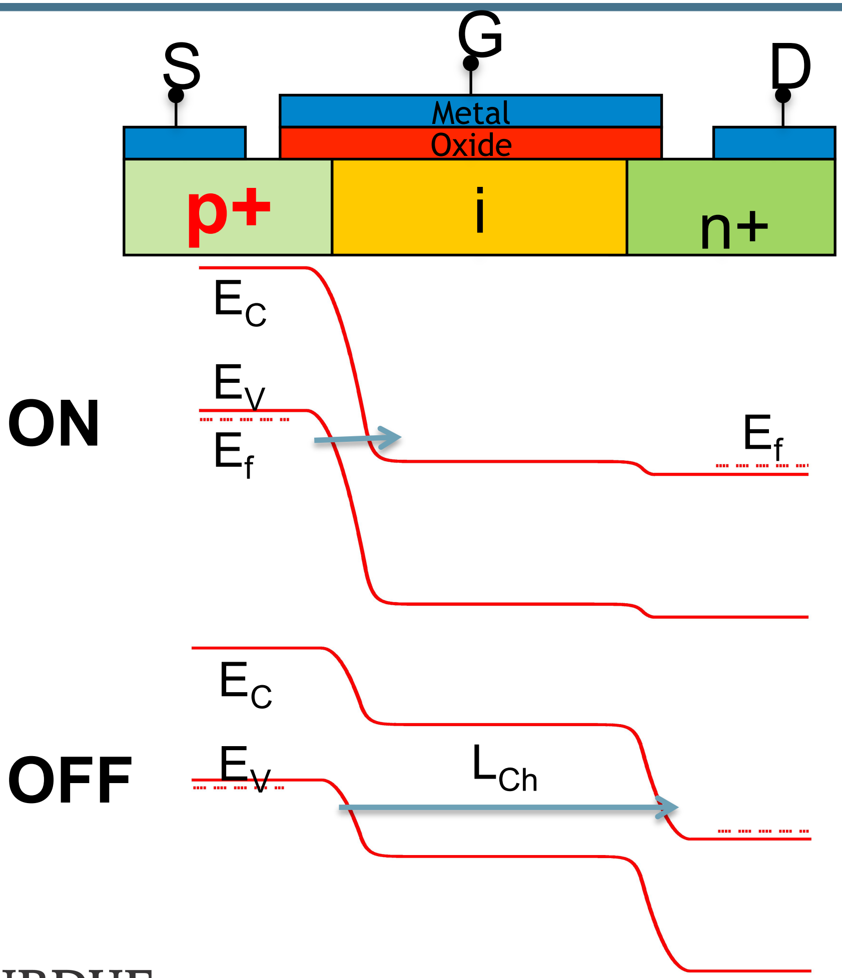


Optimized source doping level is required.

Steep switching requirements

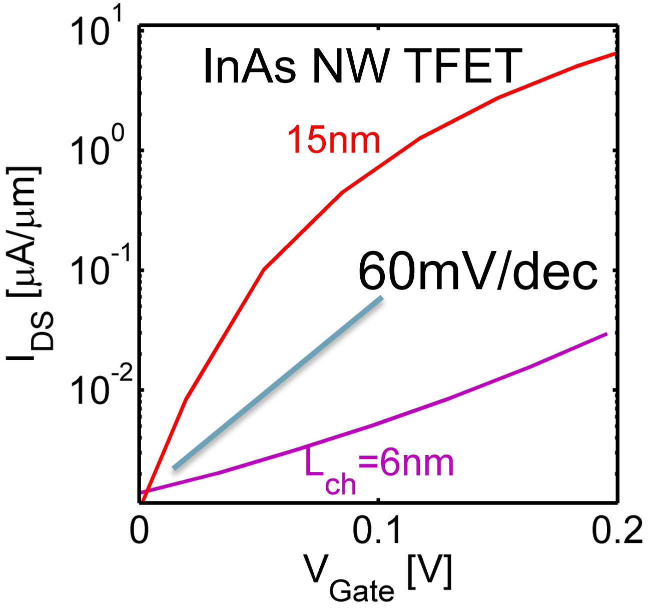
Requirements for SS < 60 mV/dec

2) Strong tunneling distance modulation



Example

Reduce channel length from 15nm → 6nm



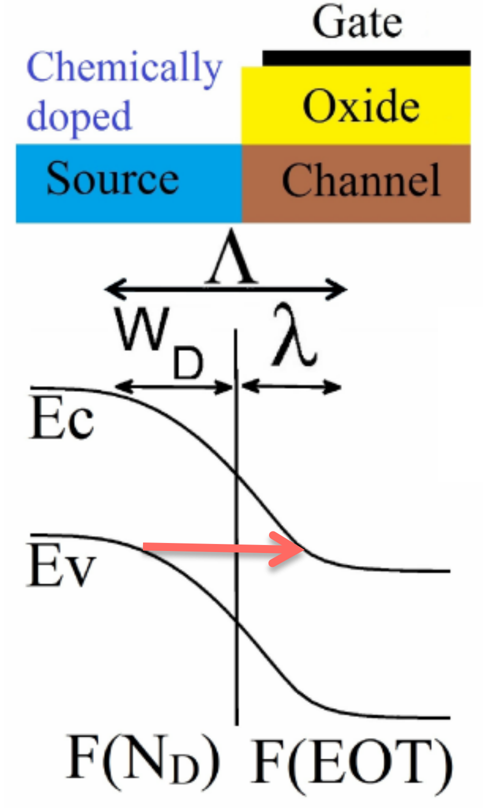
Vdd = 0.2V

Steep switching requirements

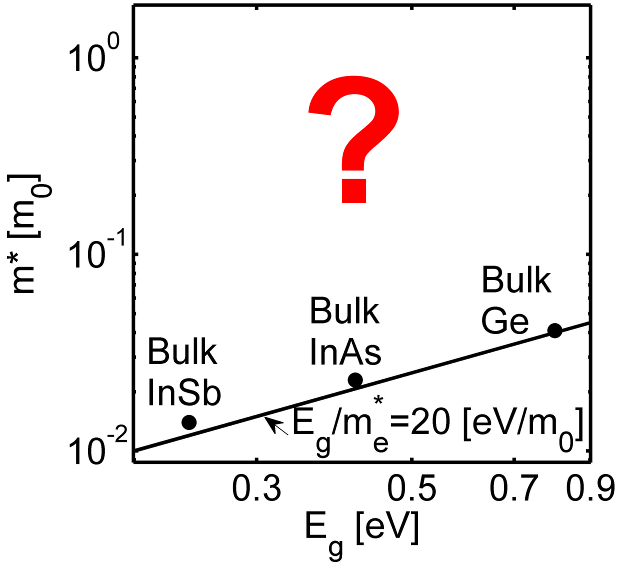
Requirements for SS < 60 mV/dec

3) High ON-current

1) Electrostatic: Small tunneling distance in ON-state



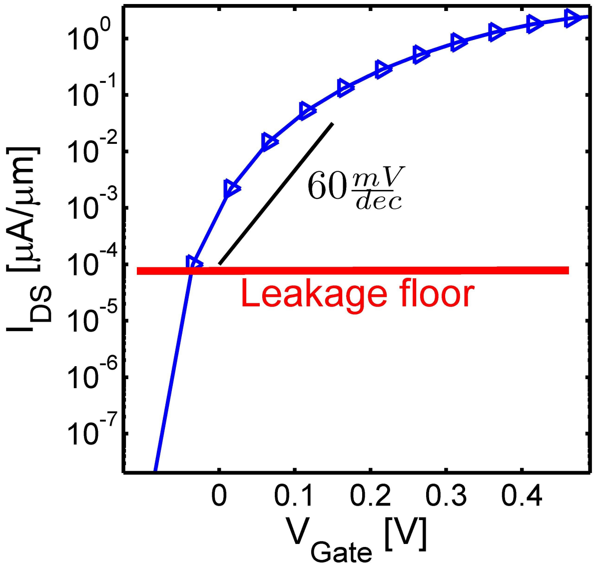
2) Optimum channel material



Device optimization

Example

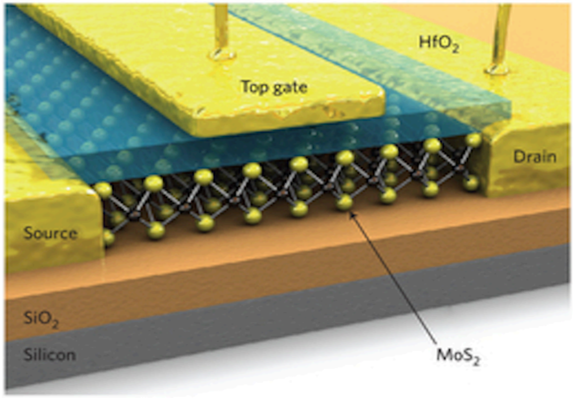
Small ON-current levels avoids observation of SS<60mV/dec



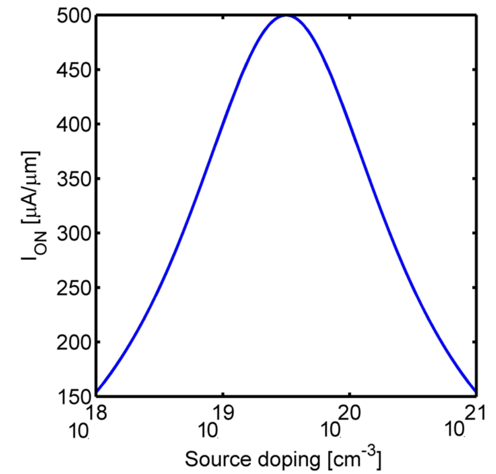
Many devices, many materials, many variables

How to find solutions to satisfy these requirements efficiently?

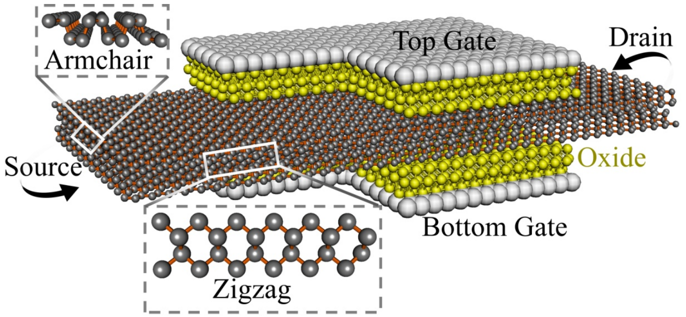
Performance of new materials?	Optimized device parameters?	Performance of novel designs



2D Material



Optimum doping

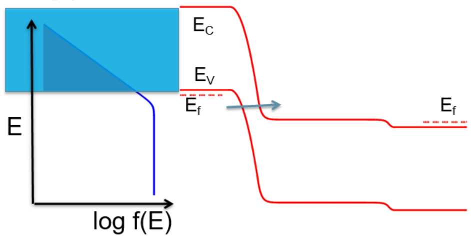


Phosphorene L-shaped TFET

Atomistic quantum transport simulations

Introduction:

1) Motivation for steep transistors
2) Requirements for steep tunnel transistors
    Energy filtering, High I_{ON}
    Tunneling distance modulation



Atomistic quantum transport simulation

1) Benchmark with experiment
2) Verify and extend analytic models

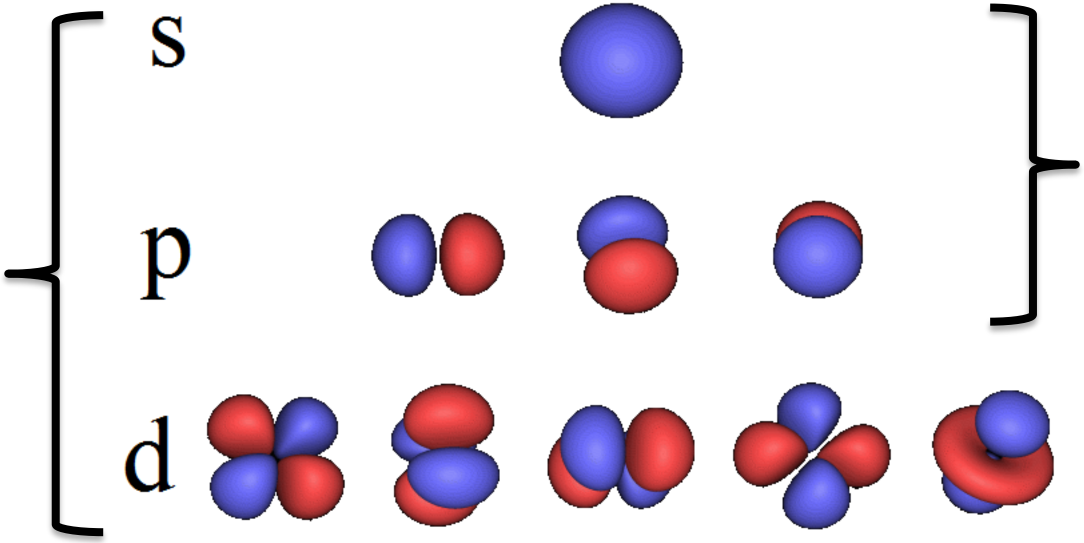
Tunnel transistors

1) III-V materials
2) 2D materials
3) Best materials for scaling challenge

Why Atomistic Modeling?

Atomistic simulation captures 2 important aspects of materials

1) Atomic orbital contributions

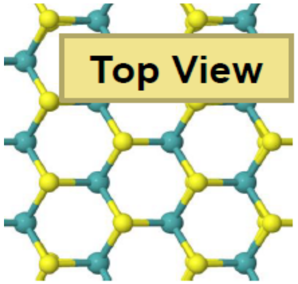


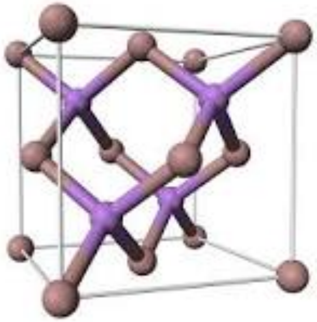
2D TMDs
MoS_2
WSe_2

Group IV and III-V

2) Crystal structure

2D TMDs
Hexagonal





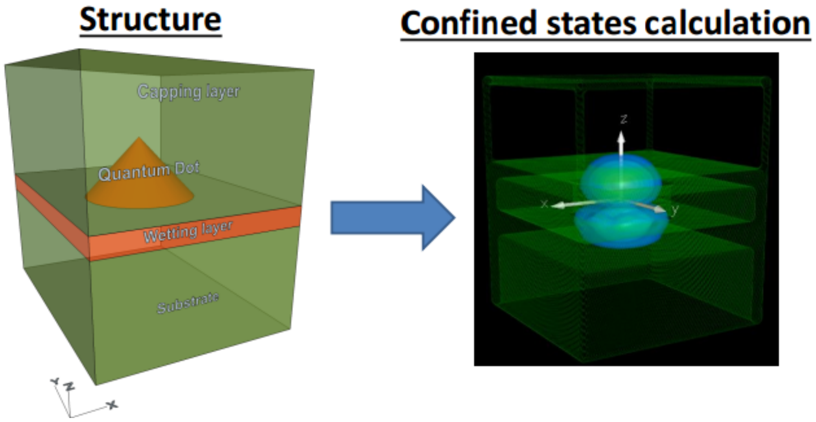
III-V
Zincblende

Why quantum transport?

Equilibrium

Schrodinger equation

$$\mathcal{H}\psi = E\psi$$



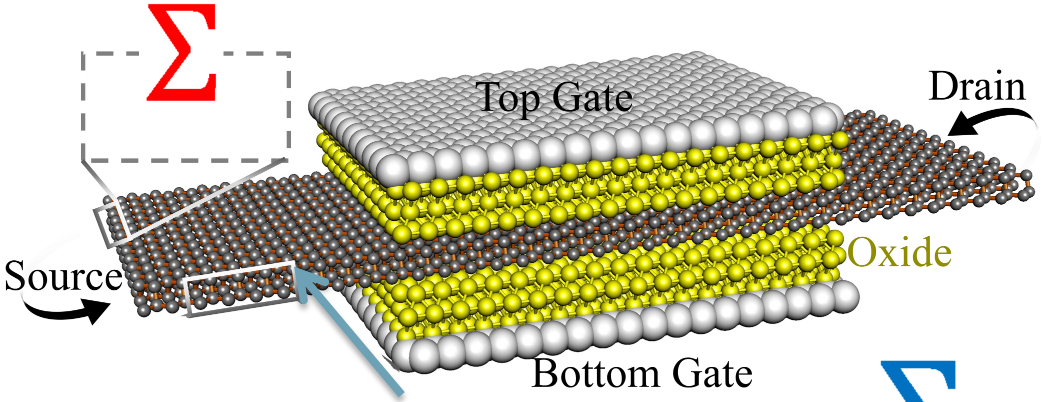
Non-equilibrium

Contacting Schrodinger: NEGF

$$(E - H - \boxed{\Sigma})G = 1$$

- Inject carriers from contacts

Self energy



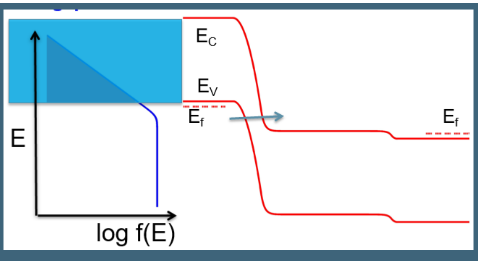
- Scattering processes Σ

NEGF can explain physics of the device out of equilibrium.

Agenda

Introduction

1) Motivation for steep transistors
2) Requirements for steep tunnel transistors



Atomistic quantum transport simulation

1) Benchmark with experiment
2) Verify and extend analytic models

Tunnel transistors

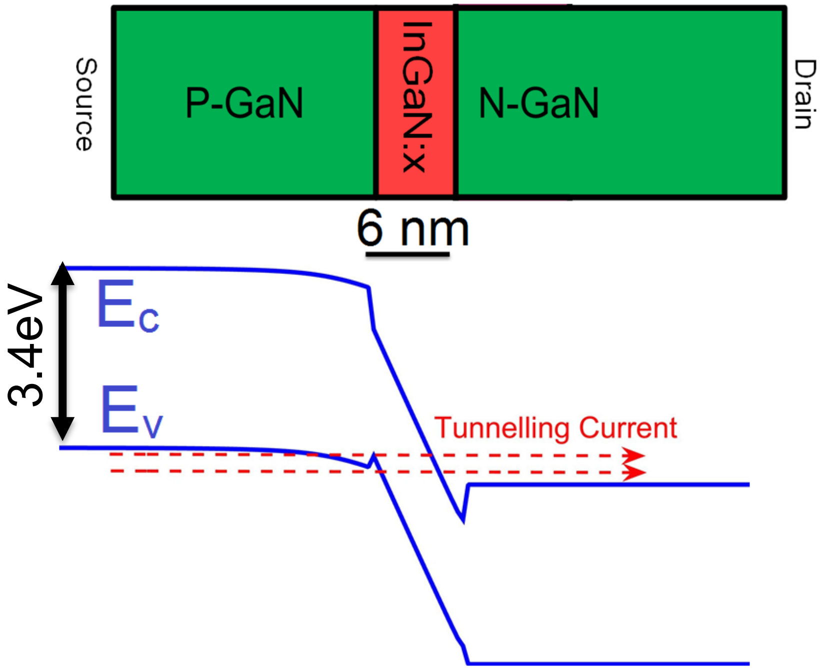
1) III-V materials
2) 2D materials
3) Best materials for scaling challenge

Quantum transport: Benchmark

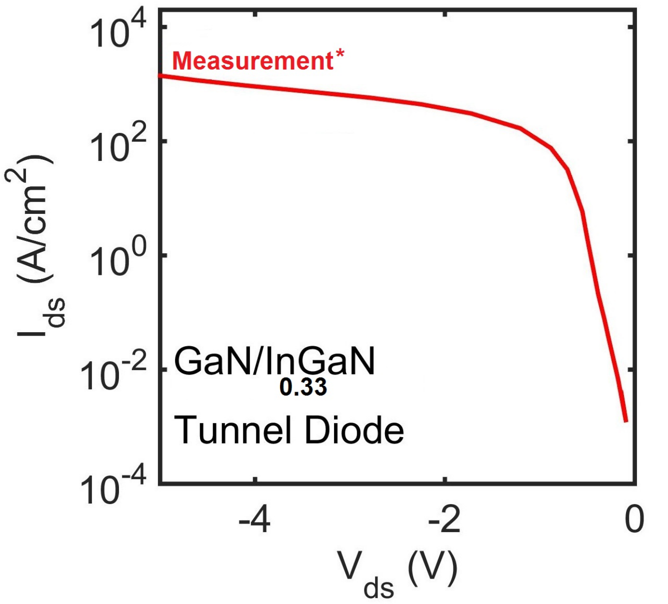
Benchmarking NEGF model with experiment

Nitride Tunnel Diode

Device structure – band diagram



I-V from Experiment



Appl. Phys. Lett. 97, 203502 2010

1) Motivation

a) High E-field (1V/nm)
b) Small gap at tunnel junction

→ High tunneling current

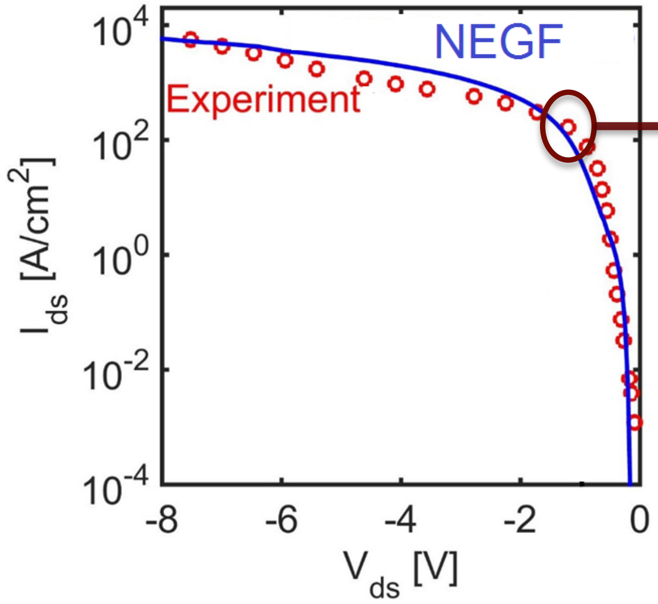
2) Origin of E-field

Large lattice mismatch
High piezoelectric coef

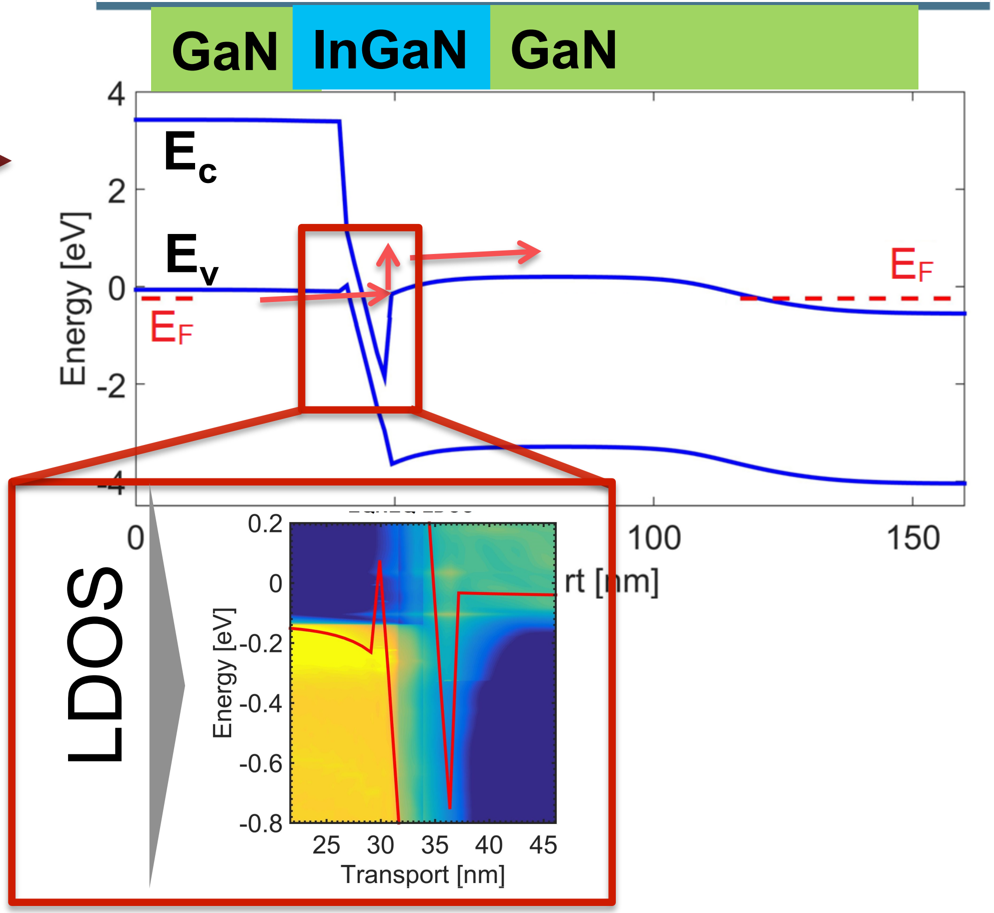
Quantum transport: Benchmark

Why does scattering matter in heterojunction tunneling devices?

NEGF vs Experiment



Underlying physics



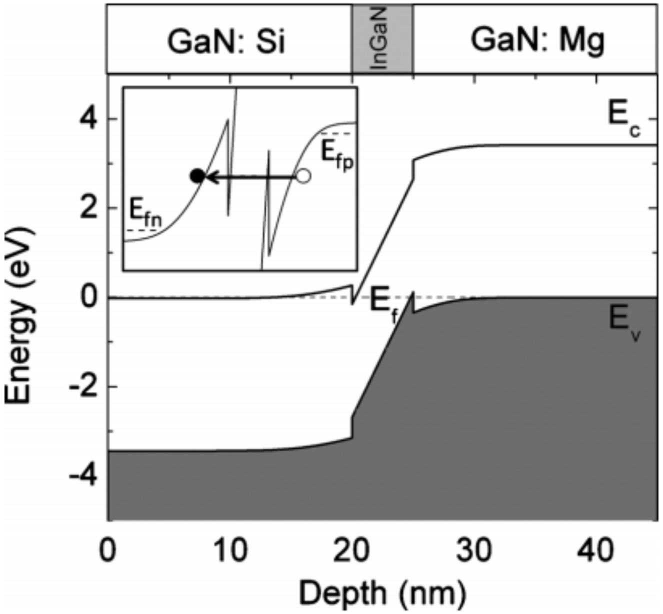
NEGF can capture physics of tunneling devices

Quantum transport: Benchmark

Benchmarking NEGF model with experiment

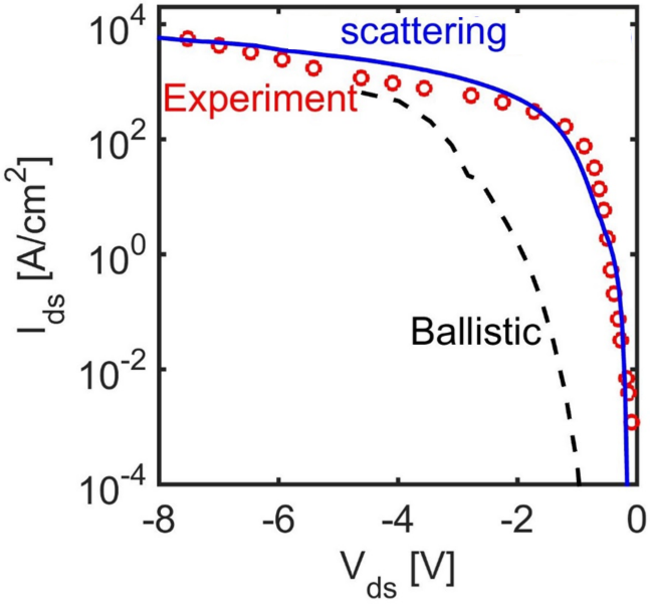
Nitride Tunnel Diode

Device structure – band diagram



Appl. Phys. Lett. 97, 203502 2010

Output

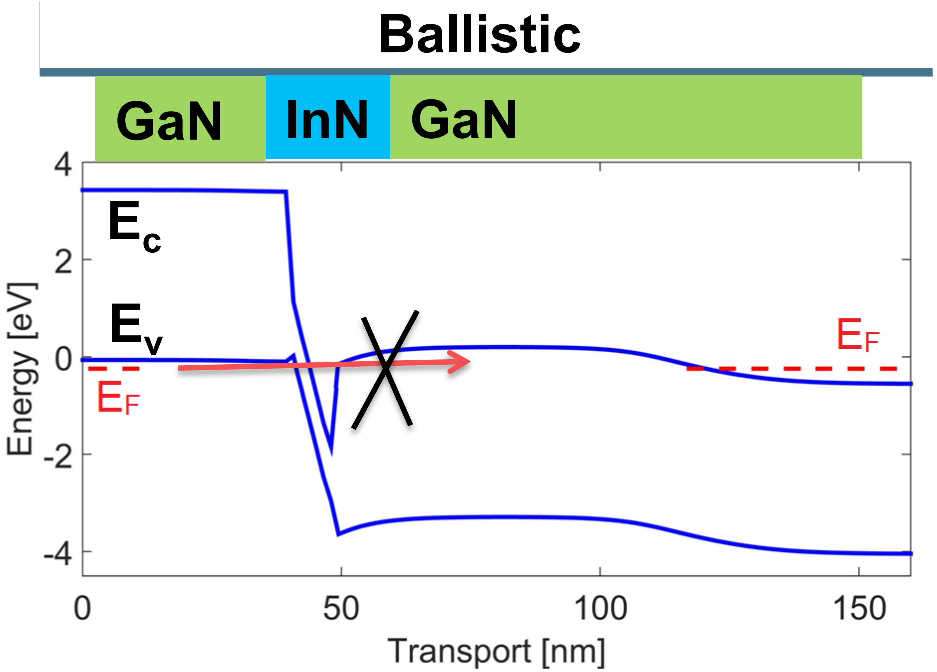


‘Impact of scatterinfg on heterostructure tunnel junctions’ to be published.

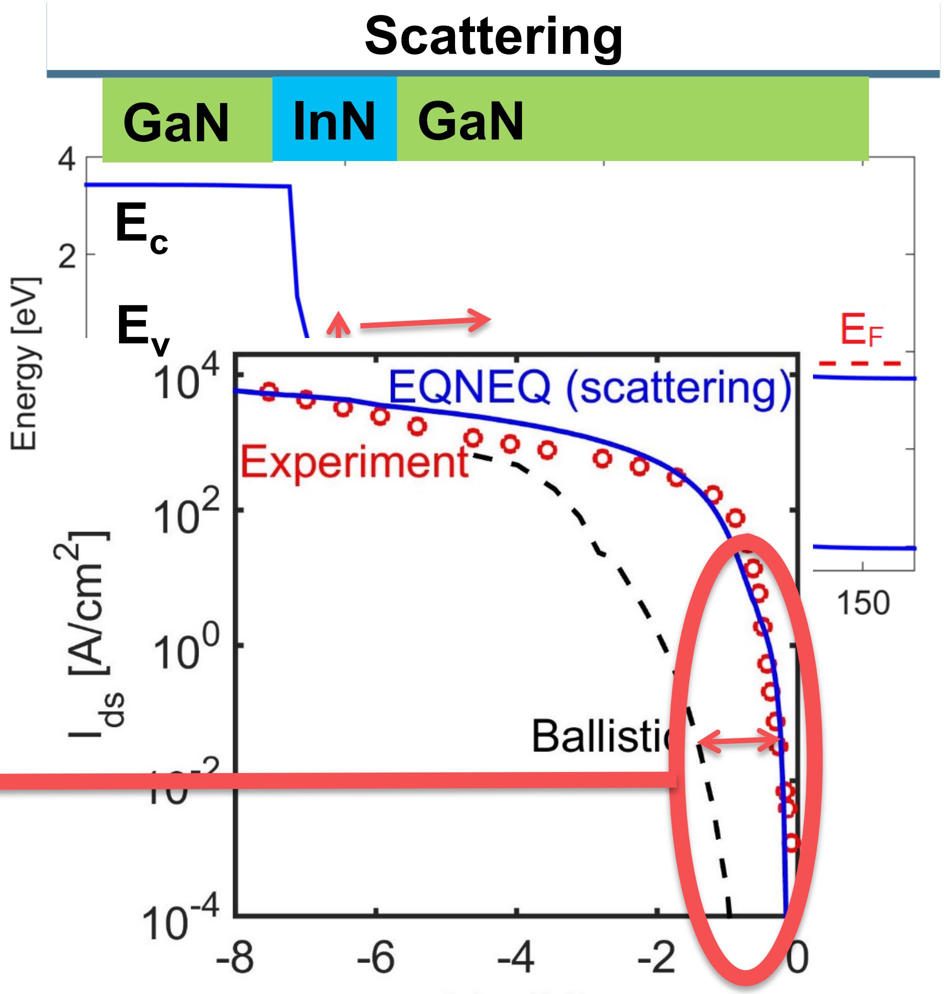
Scattering is important in heterojunction tunneling devices.

Quantum transport: Benchmark

Why does scattering matter in heterojunction tunneling devices?



Ballistic



Scattering

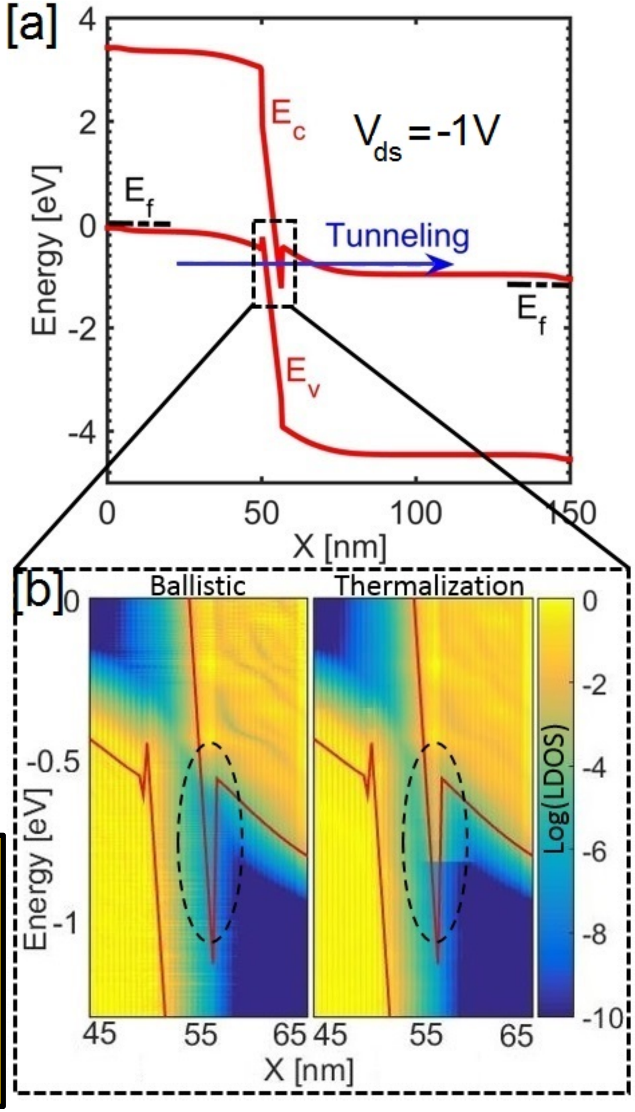
With scattering turn on occurs in lower voltages.

NEGF + scattering can capture physics of tunneling devices

Density of states with & without scattering

Band diagram

DOS



Ballistic case:
No States in the triangular well

With scattering:
States available in the triangular well

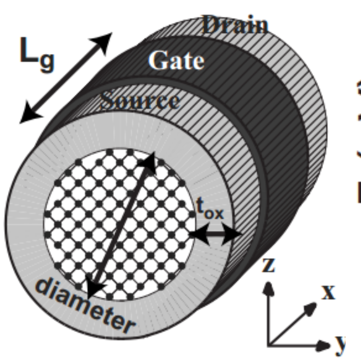
Quantum transport: Homojunction TFET

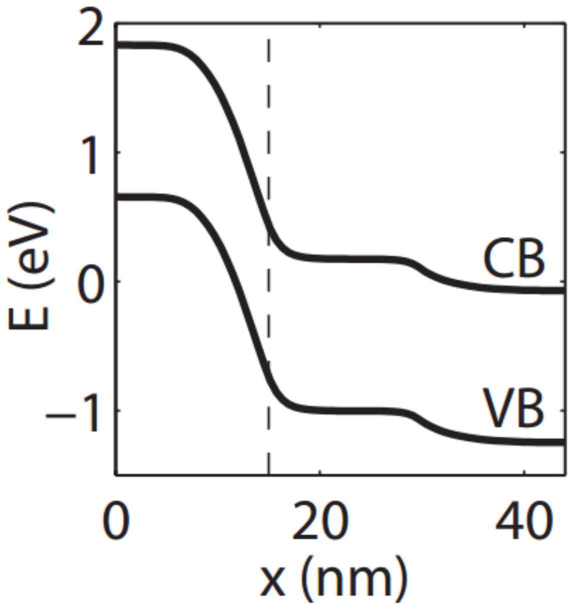
Question: Does scattering affect the performance of homojunction TFET?

Homojunction TFET

Device structure – band diagram

InAs Nanowire





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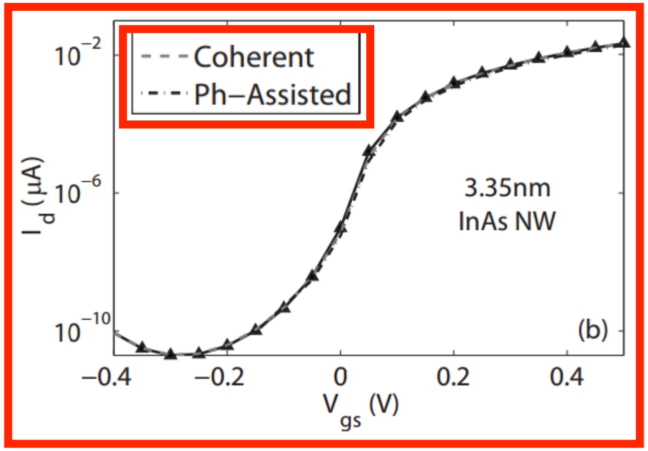


For homojunction TFETs:
Scattering does NOT impact the results

JOURNAL OF APPLIED PHYSICS **107**, 084507 (2010)

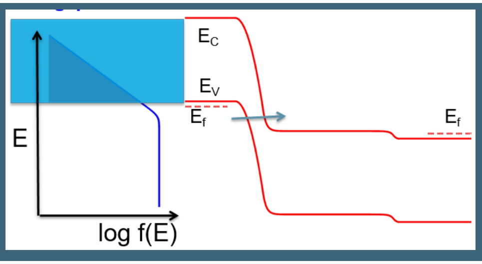
Simulation of nanowire tunneling transistors: From the Wentzel–Kramers–Brillouin approximation to full-band phonon-assisted tunneling

Mathieu Luisier[a] and Gerhard Klimeck

Agenda

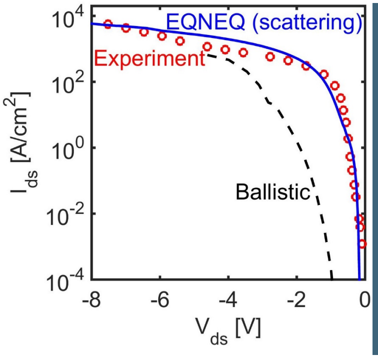
Introduction

1) Motivation for steep transistors
2) Requirements for steep tunnel transistors



Atomistic quantum transport simulation

1) Benchmark
NEGF → match experiment
2) Verify and extend analytic models



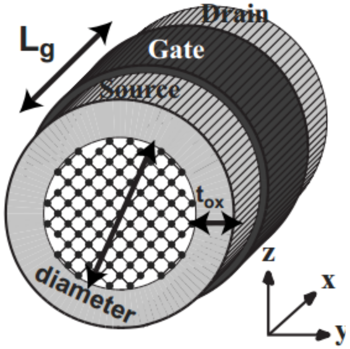
Tunnel transistors

1) III-V materials
2) 2D materials
3) Best materials for scaling challenge

Why do we care about analytic models?

Atomistic NEGF is accurate however …

1) Small dimensions (Diameter < 5nm)
2) Time + resources



Analytic models are fast and intuitive however …

1) Less accuracy

MoS$_2$ TFET: I_{ON} (Analytic) > 10^3 I_{ON} (NEGF)

DOI: 10.1063/1.4878515

WKB

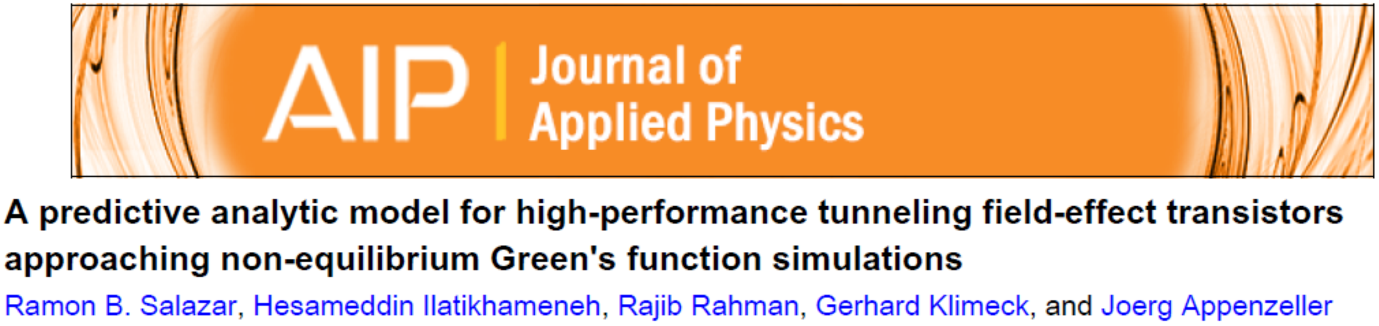
$$\boxed{T(E) = \exp\left[-2\int \mathrm{d}x\,\kappa(x)\right]}$$

NEGF → Correct and guide analytic models

Modeling approaches

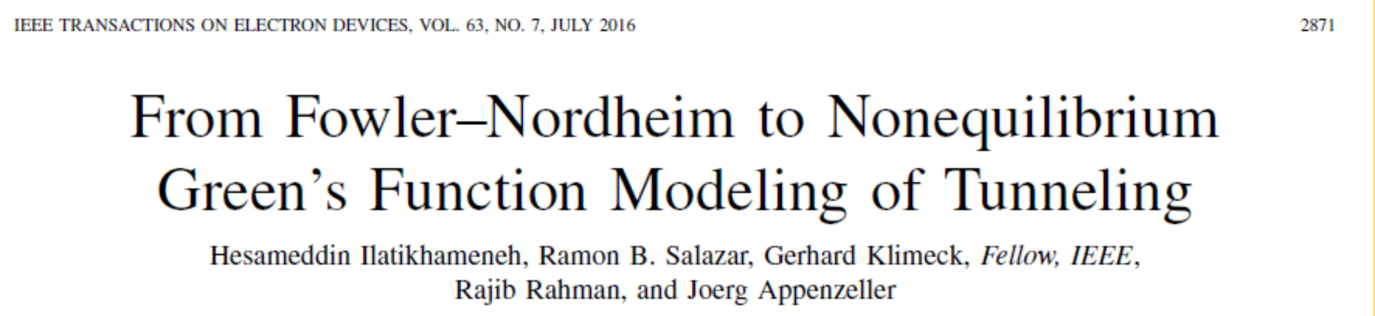
NEGF→ Correction and extension of analytic modeling approaches

	Transport: tunneling		Electrostatic
Rigorous	NEGF	+	3D Poisson
1D Integral			
Analytical			



A predictive analytic model for high-performance tunneling field-effect transistors approaching non-equilibrium Green's function simulations

Ramon B. Salazar, Hesameddin Ilatikhameneh, Rajib Rahman, Gerhard Klimeck, and Joerg Appenzeller



IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 63, NO. 7, JULY 2016 2871

From Fowler–Nordheim to Nonequilibrium Green's Function Modeling of Tunneling

Hesameddin Ilatikhameneh, Ramon B. Salazar, Gerhard Klimeck, *Fellow, IEEE*, Rajib Rahman, and Joerg Appenzeller

$T^{FN} = \exp\Big(- \quad qF \quad 3\hbar \Big)$

$qF \quad 2\hbar \Big)$

Analytic view of TFET

Analytic analysis of tunneling in nutshell

WKB, Kane, FN

Band-to-band-tunneling transmission:

$$T_{BTBT} = exp\left(-C \overbrace{\sqrt{m_t^* E_g}}^{\text{Material properties}} \overset{\text{Electrostatic}}{\Lambda}\right)$$

Tunneling mass $m \approx 0.7 m_r^*$ ①

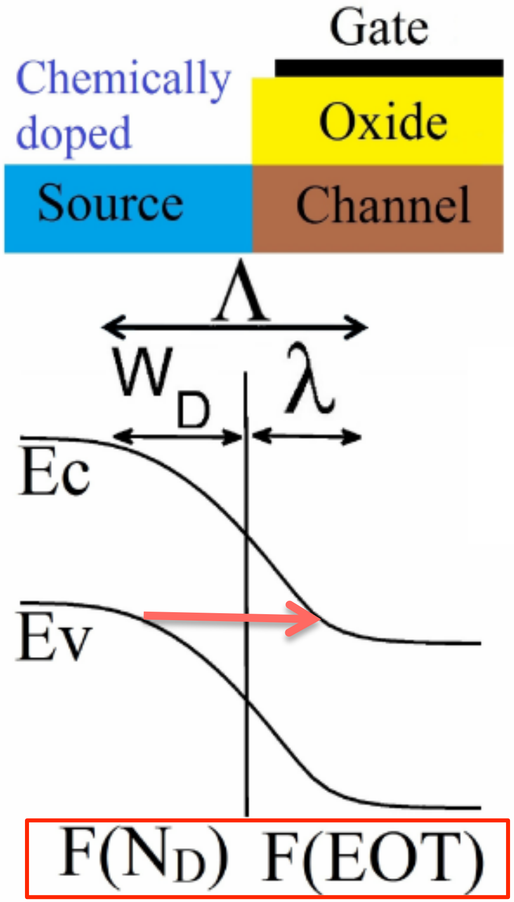
Confined bandgap ②

Tunneling distance ③

$$m_r^* = \frac{m_e m_h}{m_e + m_h}$$

Electrostatic

$$\Lambda = W_D + \lambda$$

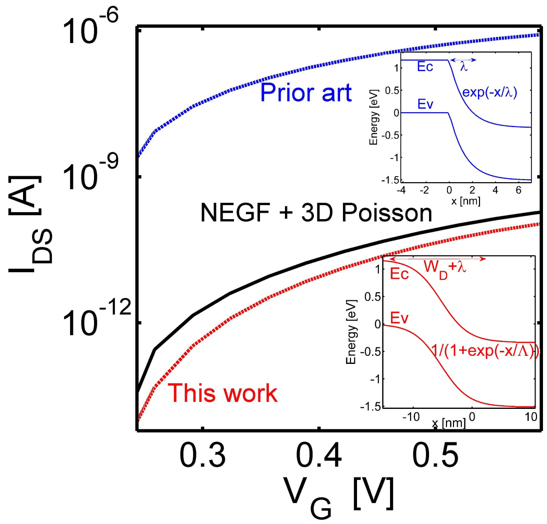


Quantum transport: 3) analytic models

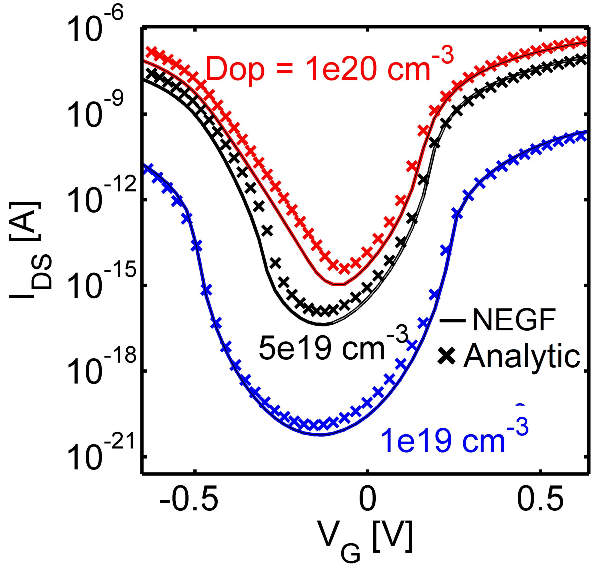
How to make WKB provide results matching atomistic simulations?

WKB

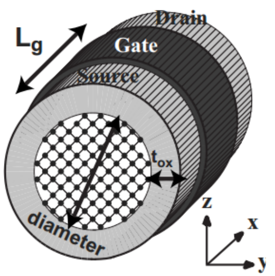
Our analytic model vs old model



Our analytic vs NEGF



InAs NW



Our new analytic model provides results close to NEGF.

JOURNAL OF APPLIED PHYSICS **118**, 164305 (2015)

A predictive analytic model for high-performance tunneling field-effect transistors approaching non-equilibrium Green's function simulations

Quantum transport: 3) analytic models

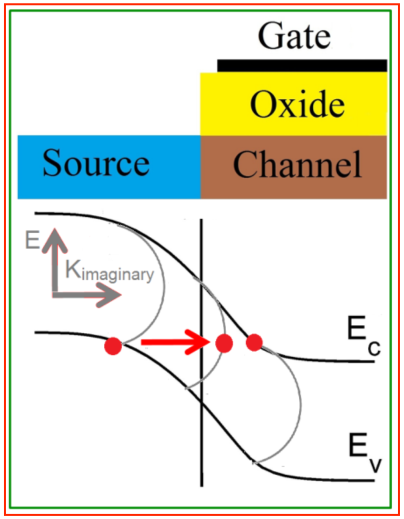
How to make WKB provide results matching atomistic simulations?

WKB

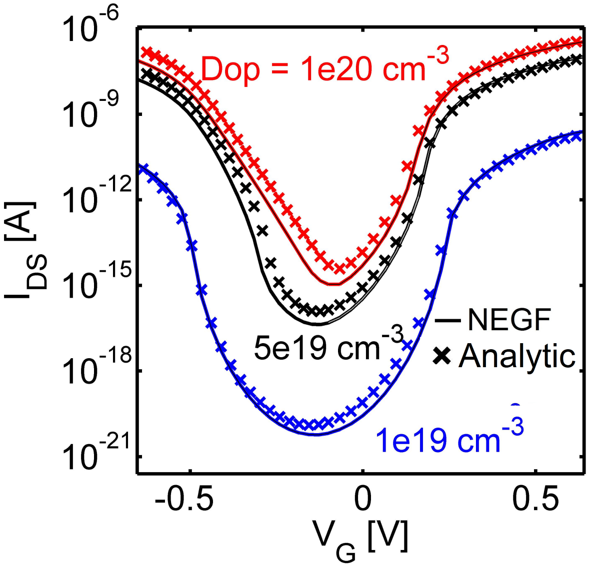
Inputs

1) Complex EK

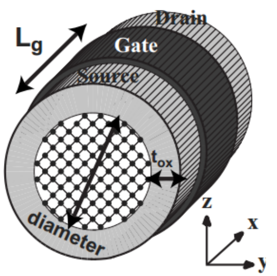
2) Potential Φ(x)



Output



InAs NW



Propose analytic potential → WKB provides close results to NEGF.

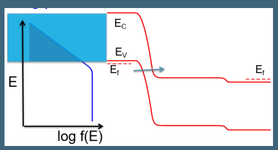
JOURNAL OF APPLIED PHYSICS **118**, 164305 (2015)

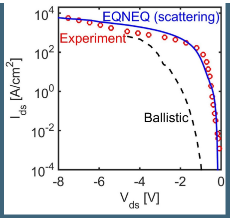
A predictive analytic model for high-performance tunneling field-effect transistors approaching non-equilibrium Green's function simulations

Agenda

Introduction

1) Motivation for steep transistors
2) Requirements for steep tunnel transistors

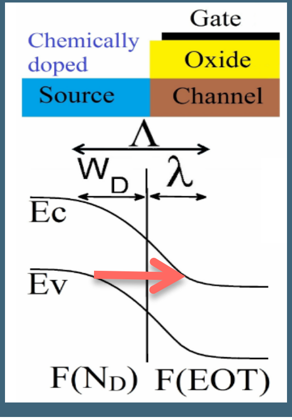




Atomistic quantum transport simulation

1) Benchmark
2) Analytic models

Simple and verified
way to analyze TFETs



Tunnel transistors

1) III-V materials
2) 2D materials
3) Best materials for scaling challenge

Why Atomistic Modeling?

Channel Materials

Group IV

- Si, Ge, SiGe
  Indirect gap → low I_{ON}

III-V

- InAs, GaAs, InN
  Eg ~ 0.2-4 eV
  Direct gap

2D

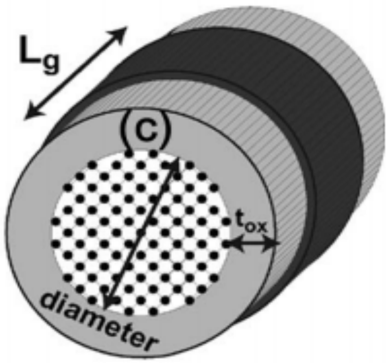
- TMDs: WSe_2, MoS_2
  Large direct gap
  Eg ~ 1eV
- Phosphorene
  Medium direct gap
  Eg ~ 0.4-1.4 eV
- Bilayer Graphene
  Small direct gap Eg
  Eg ~ 0.3eV

III-V Homojunction TFETs

Most promising device structure for III-V TFET? Gate-all-around nanowire

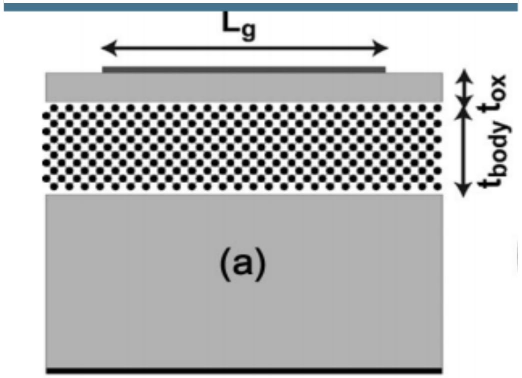
1) Best structure

Gate-all-around

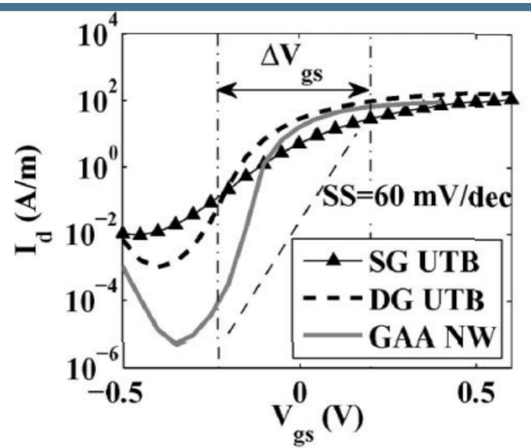


L_g=L_{ch}=40nm,
EOT=0.5nm,
Diameter=5nm

Ultra-thin bodies

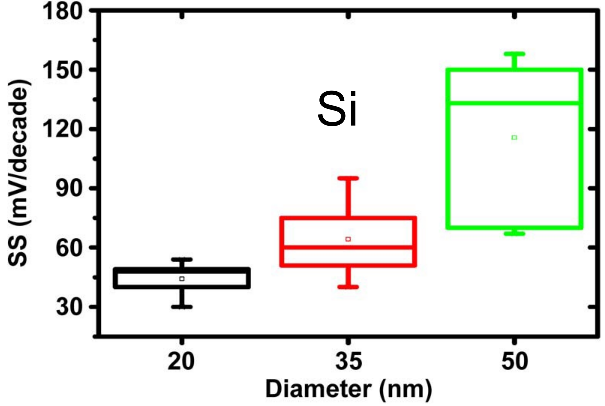


Simulation: GAA > UTB



2) Diameter

Experiment: t_{body} < 20nm is critical



Best candidate: Thin Gate-All-Around nanowire

Steep-slope Tunnel Field-Effect T

Katsuhiro Tomioka[1,2], Masatoshi Yoshimura and Takashi Fukui

Mathieu Luisier and Gerhard Klimeck

aAs Tunnel FETs

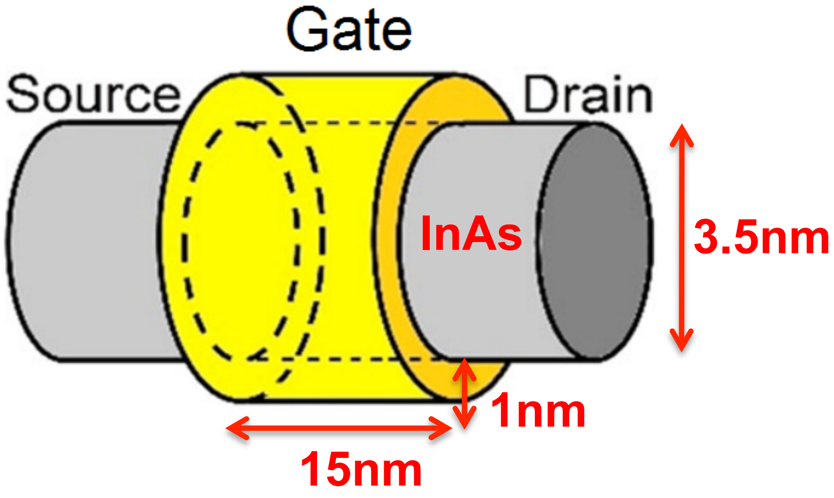
Osamu Ichikawa[2], Takenori Osada[2], Masahiko Hata[2], Mitsuru Takenaka[1], and Shinichi Takagi[1]

III-V Homojunction TFETs

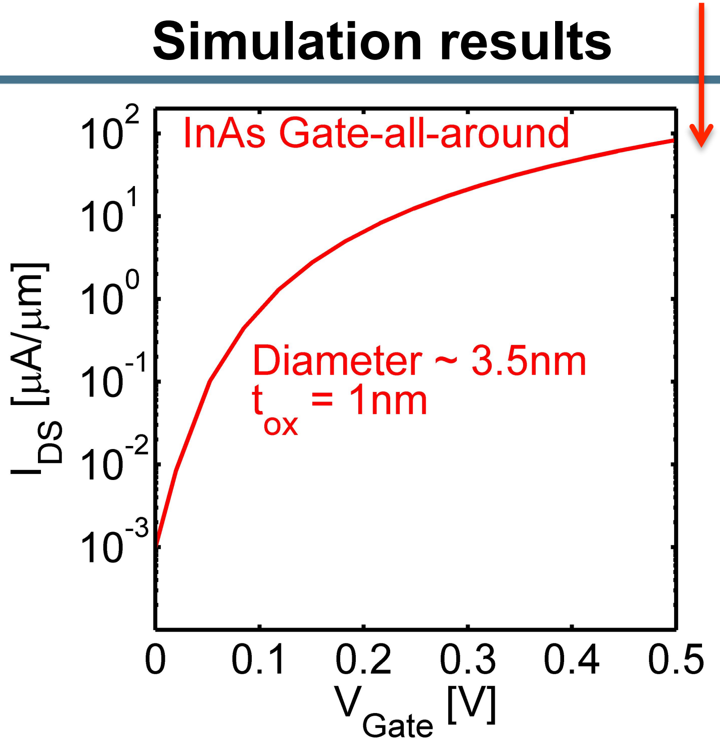
The upper limit of current level in III-V homojunction TFETs ~ 100 uA/um

Structure

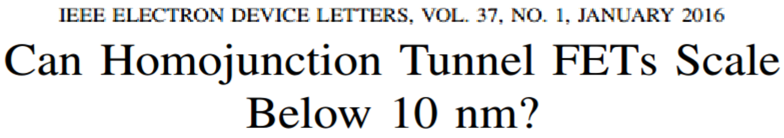
Excellent gate control:



Simulation results



Even with best gate control (Gate-all-around) → limited I_{ON}
Why?



IEEE ELECTRON DEVICE LETTERS, VOL. 37, NO. 1, JANUARY 2016

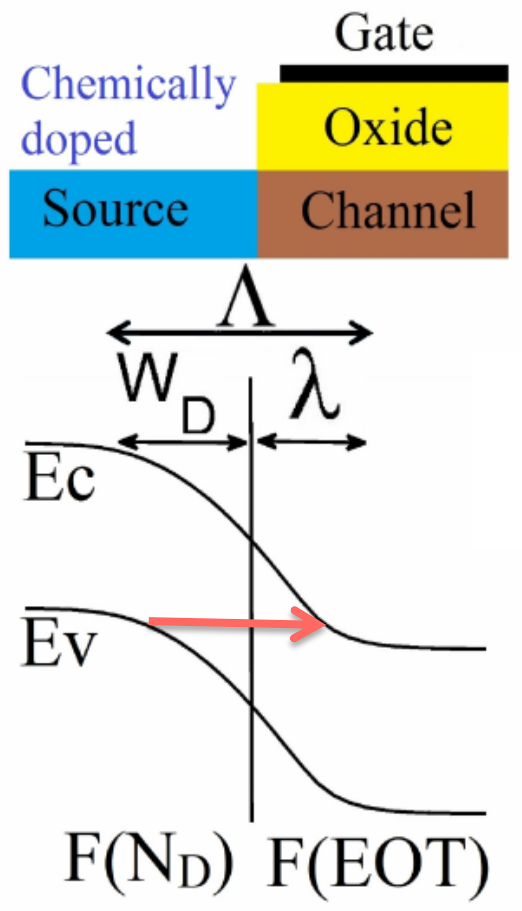
Can Homojunction Tunnel FETs Scale Below 10 nm?

III-V Homojunction TFETs

Why limited I_{ON} ?

Depletion width (W_D)

Scaling length (λ)



Pros:

1) High doping is feasible

Cons:

2) High ε of channel material

Cons:

1) Thick body

Simulation: Min(W_D) ~ 3nm

Experiments: W_D > 5nm

Simulation: Min(λ) ~ 1.5nm

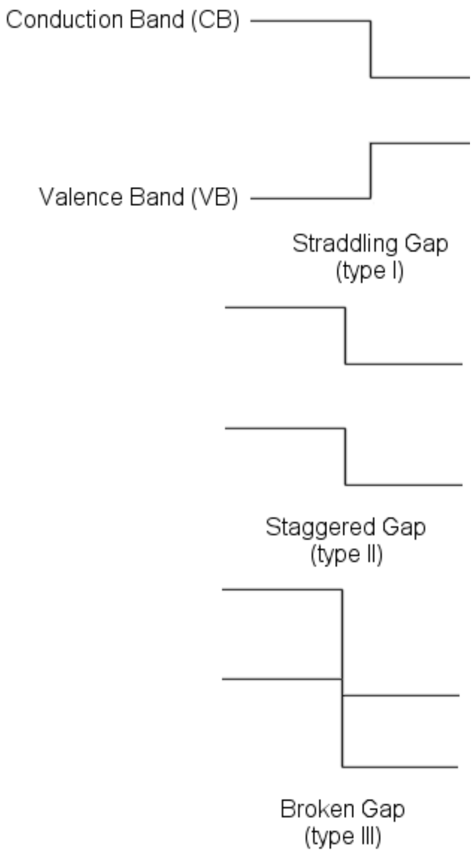
Experiments: λ > 5-10 nm

Large tunneling distance

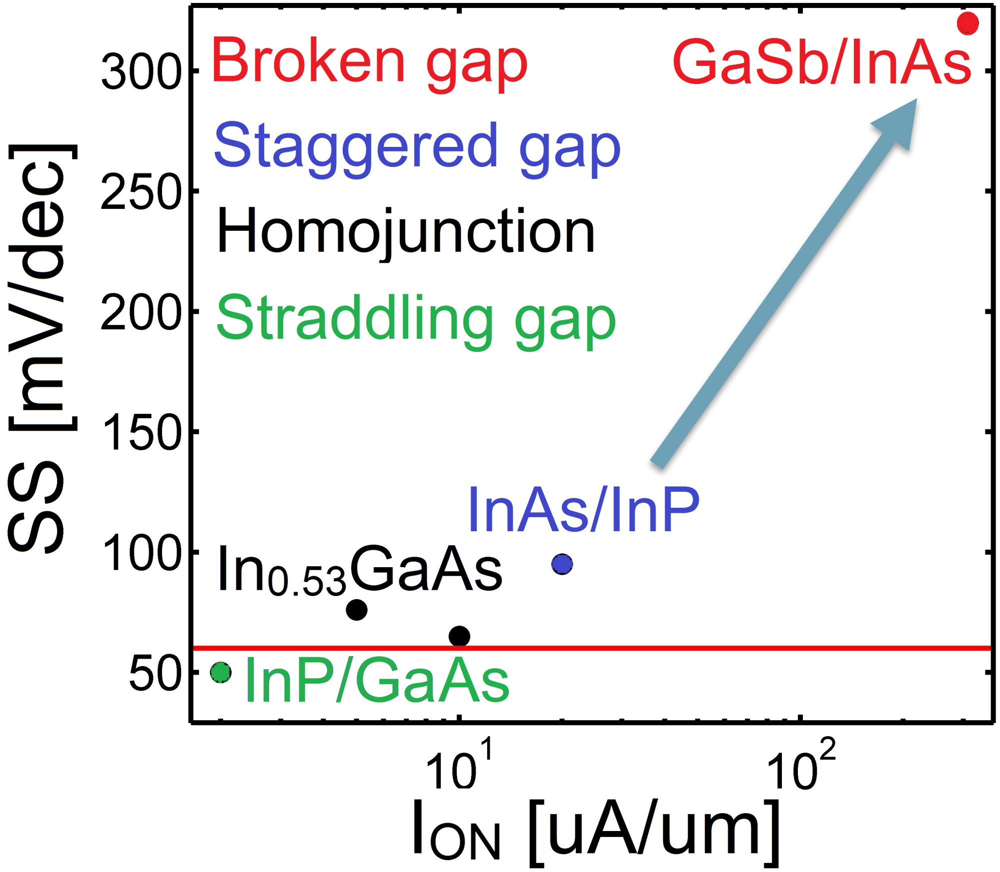
Solution: Broken gap III-V TFETs

High current levels → Broken gap III-V TFETs ~ 100-1000 uA/um

Band alignments



Experimental data



[InAs/InP] Zhou EDL 2011
[InGaAs] Nogouchi IEDM 2013

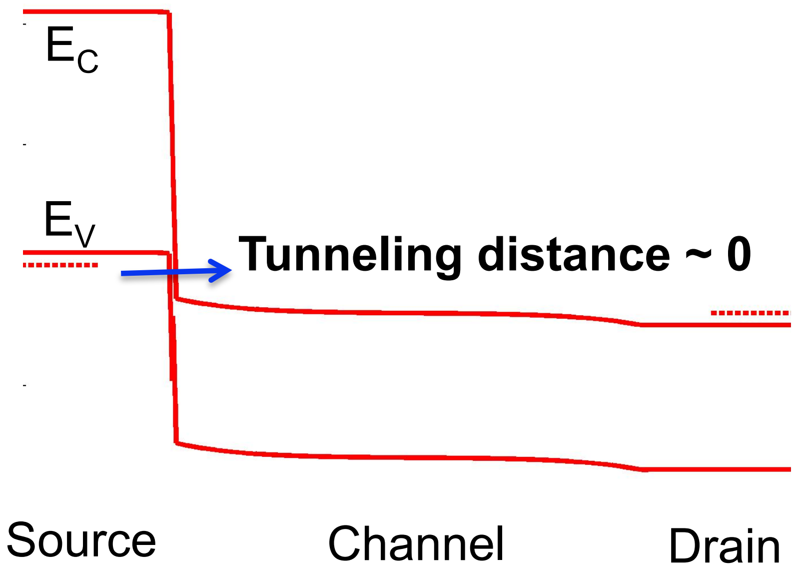
[InP/GaAs] Ganjipour ACS Nano, 2012

Solution: Broken gap III-V TFETs

High current levels → Broken gap III-V TFETs ~ 800 uA/um

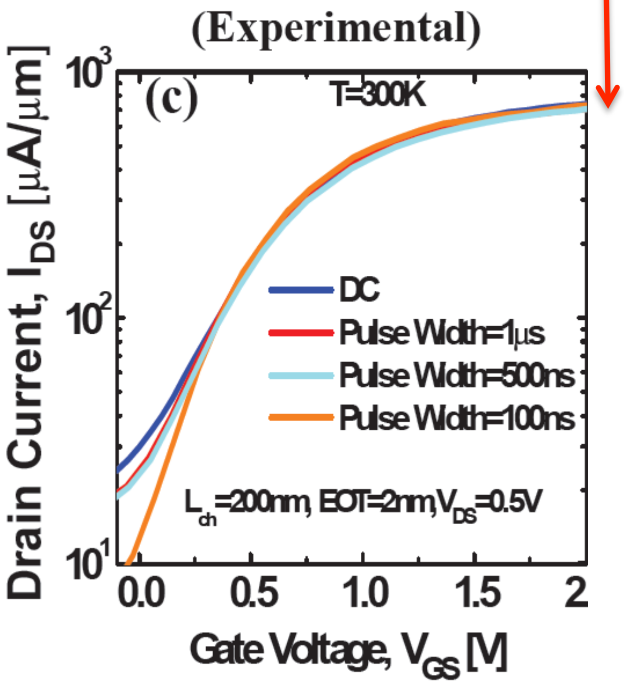
Band diagram

ON-state



ON-state:
Tunneling distance → 0
→ High I_{ON}

Results

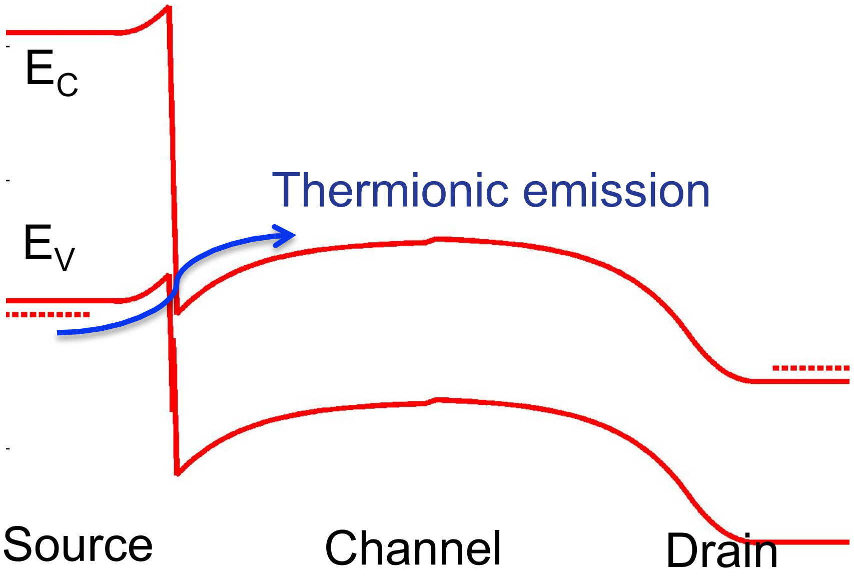


Demonstration of $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ Near Broken-gap Tunnel FET with I_{ON}=740μA/μm, G_M=700μS/μm and Gigahertz Switching Performance at V_{DS}=0.5V
R. Bijesh,[*] H. Liu, H. Madan, D. Mohata, W. Li[1], N. V. Nguyen[1], D. Gundlach[1], C.A. Richter[1], J. Maier, K. Wang, T. Clarke, J. M. Fastenau[2], D. Loubychev[2], W. K. Liu[2], V. Narayanan and S. Datta

Challenge of broken gap III-V TFETs

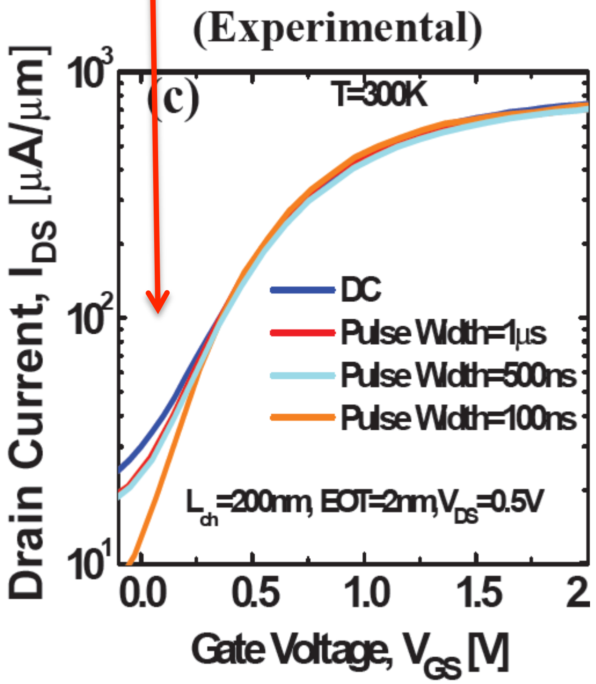
Problem of broken gap III-V TFETs ~ high SS

Band diagram



OFF-state

Results



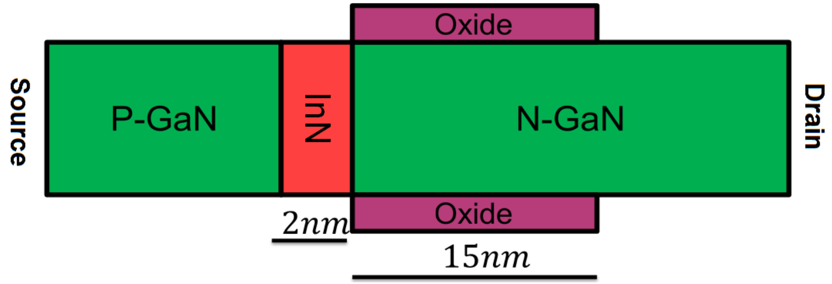
OFF-state:
A thermal path for current exists
→ Unsuccessful energy filtering

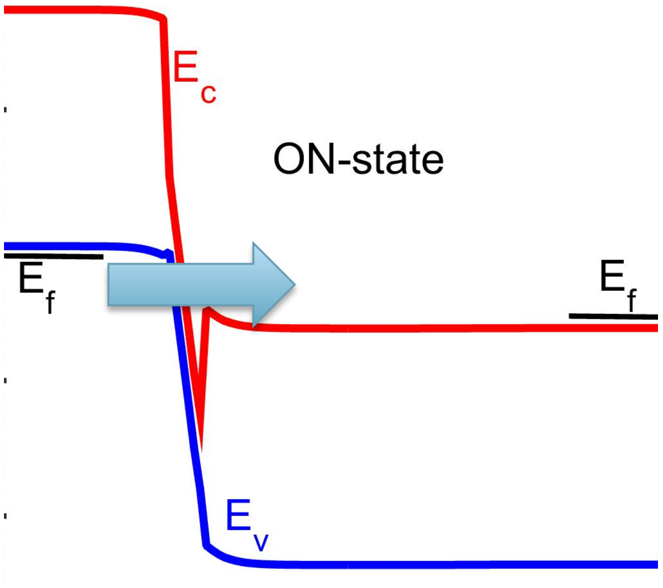
Demonstration of $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ Near Broken-gap Tunnel FET with I_{ON}=740µA/µm, G_M=700µS/µm and Gigahertz Switching Performance at V_{DS}=0.5V
R. Bijesh,* H. Liu, H. Madan, D. Mohata, W. Li[1], N. V. Nguyen[1], D. Gundlach[1] , C.A. Richter[1], J. Maier, K. Wang, T. Clarke, J. M. Fastenau[2], D. Loubychev[2], W. K. Liu[2], V. Narayanan and S. Datta

Challenge of broken gap III-V TFETs

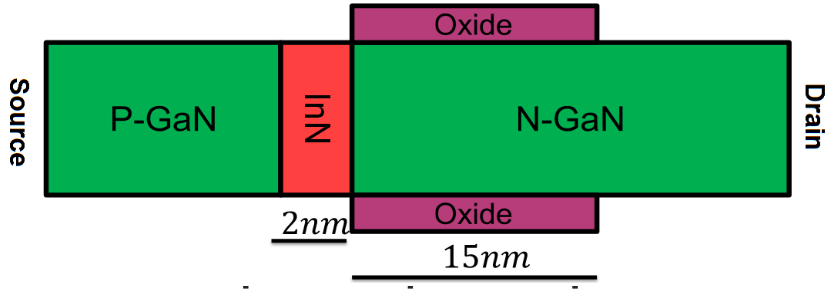
Solution: Nitride Hetero-structure

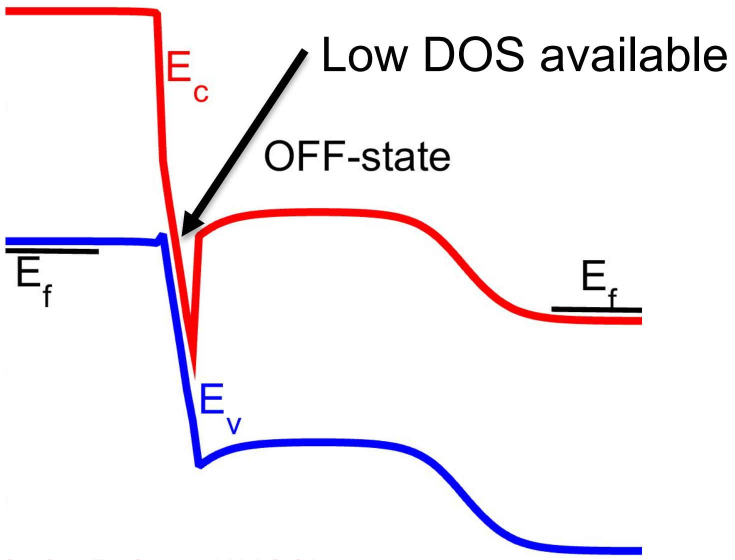
ON: Tunneling through small gap InN





OFF: Tunneling through large gap GaN





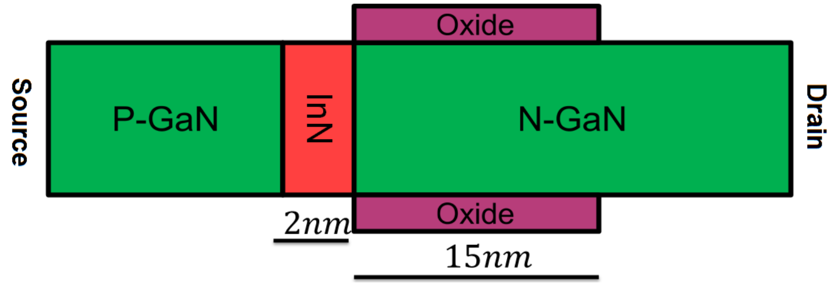
Polarization-Engineered III-Nitride Heterojunction Tunnel Field-Effect Transistors

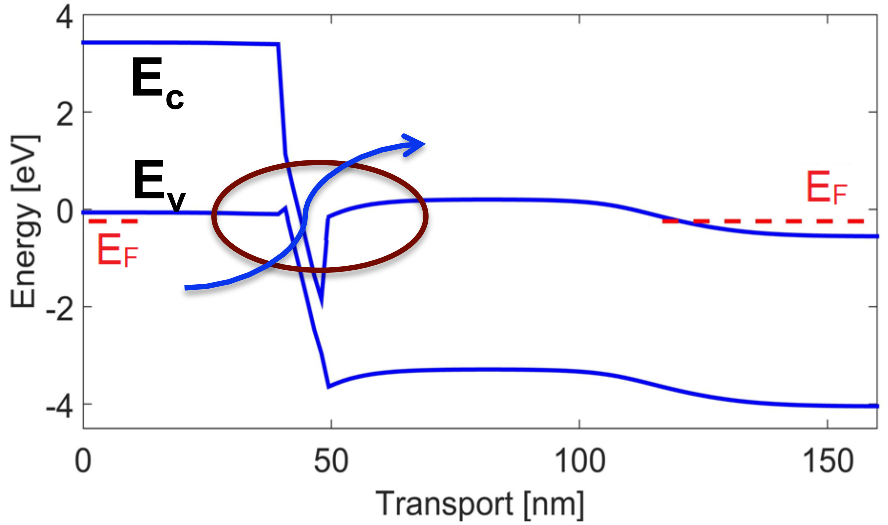
WENJUN LI[1], SAIMA SHARMIN[2], HESAMEDDIN ILATIKHAMENEH[2], RAJIB RAHMAN[2], YEQING LU[3], JINGSHAN WANG[1], XIAODONG YAN[1], ALAN SEABAUGH[1] (Fellow, IEEE), GERHARD KLIMECK[2] (Fellow, IEEE), DEBDEEP JENA[1] (Senior Member, IEEE), AND PATRICK FAY[1] (Senior Member, IEEE)

Solution: Nitride Heterostructure TFETs

Why SS < 60 mV/dec can be achieved in Nitride TFETs?

Device structure

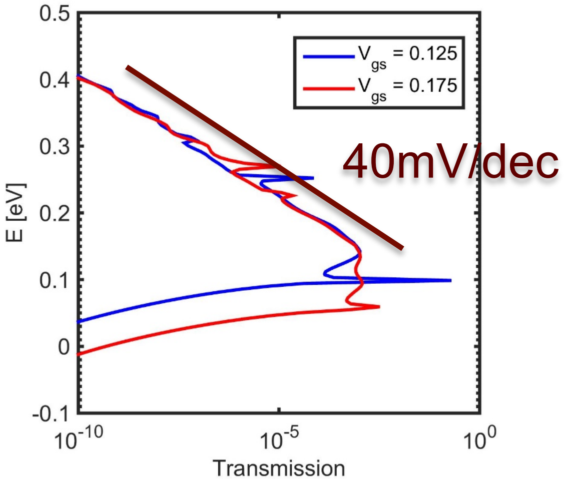




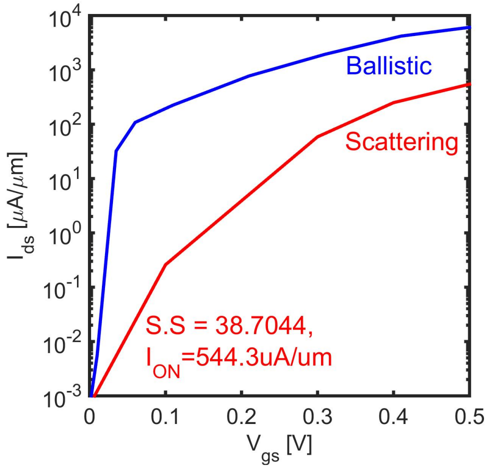
Reduced thermionic injection

Atomistic simulation results

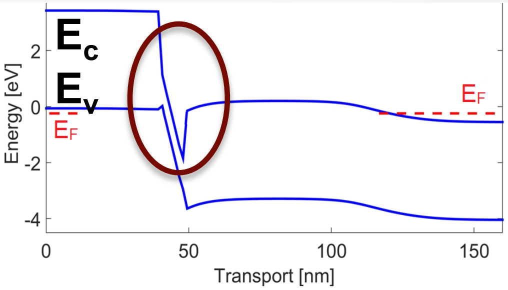
Transmission



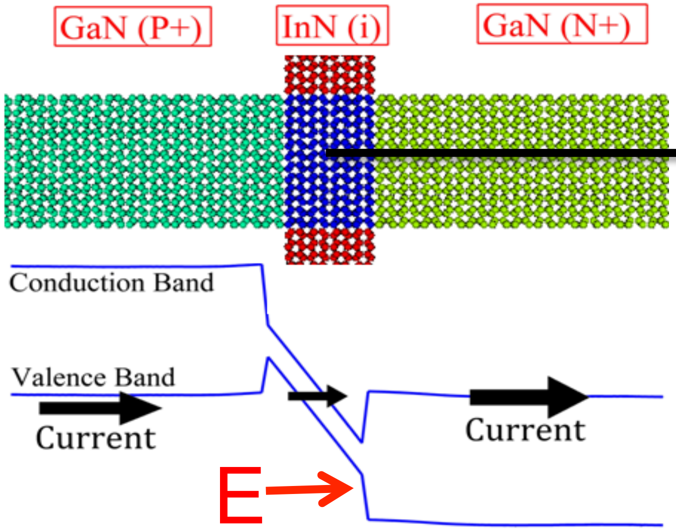
I-V



Why electric field in InN region is so high?

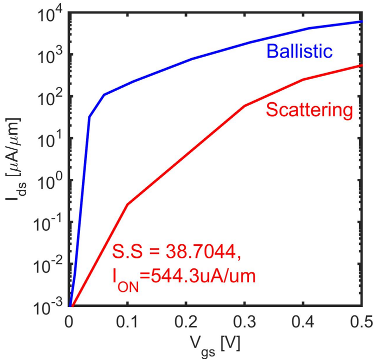


Structure



Band diagram

I-V



Lattice mismatch
Large strain (~10%)

↓

High piezoelectric coefficient

↓

High electric field

↓

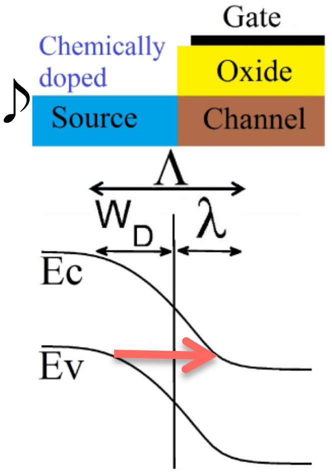
Small tunneling distance

High On-current

Summary of III-V TFETs

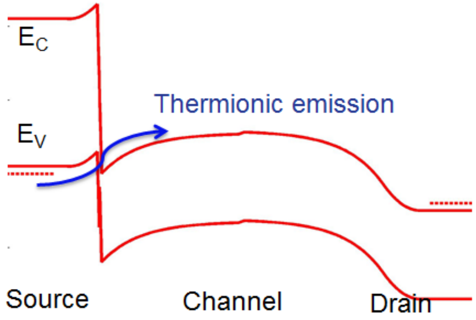
Homojunction TFETs

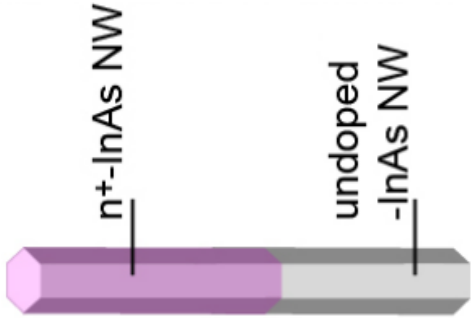
Challenge:♪
Large body thickness♪
→ Large λ♪
→ Small I_{ON}



Broken gapTFETs

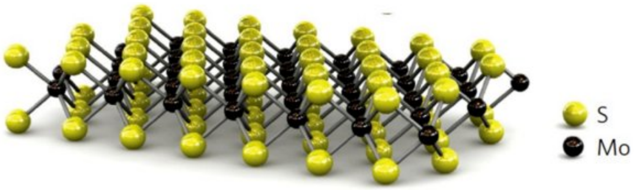
Challenge:♪
Thermionic emission in OFF state♪
→ High SS





30nm♪ 0.7nm♪

Channel thickness♪



Motivation for 2D TFETs

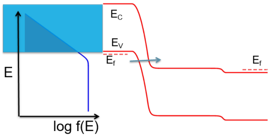
Steep-slope Tunnel Field-Effect Transistors using III-V Nanowire/Si Heterojunction

Katsuhiro Tomioka[1,2], Masatoshi Yoshimura[1] and Takashi Fukui[1]

Agenda

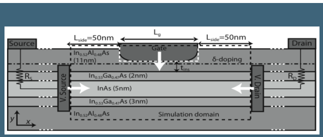
Introduction

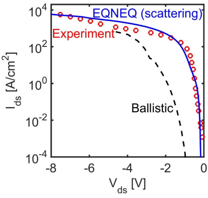
1) Motivation for steep transistors
2) Requirements for steep tunnel transistors

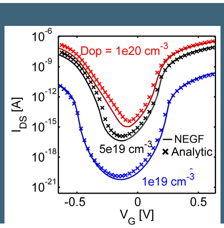


Atomistic quantum transport simulation

1) Device geometry optimization
2) Scattering impact
3) Verify and extend analytic models





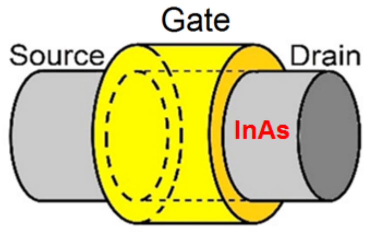


Tunnel transistors

1) III-V materials

Large body thickness → Large tunneling distance

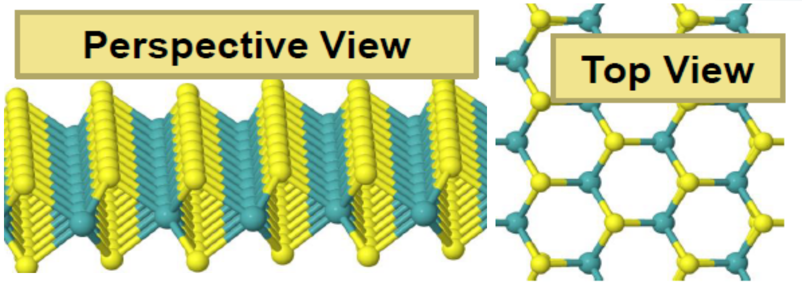
2) 2D materials
3) Best material for scaling challenge



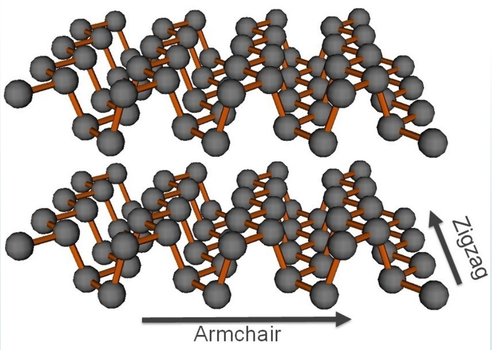
2D materials

Shortcut to end of channel thickness scaling

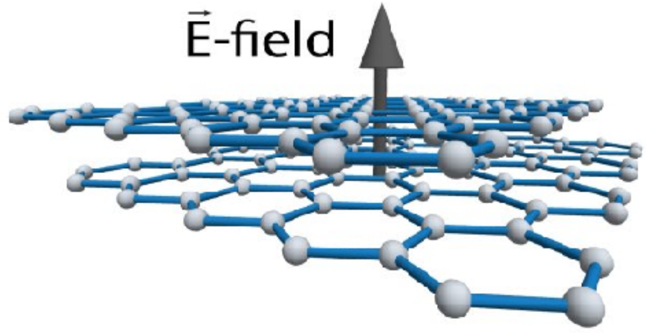
Transition metal dichalcogenides (TMD)



Phosphorene



Bilayer Graphene

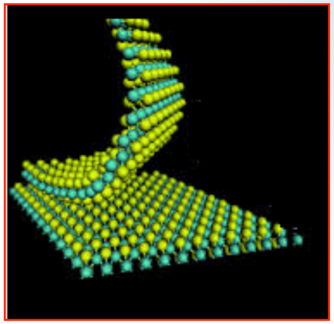


holographicgalaxy.blogspot.com

2D materials

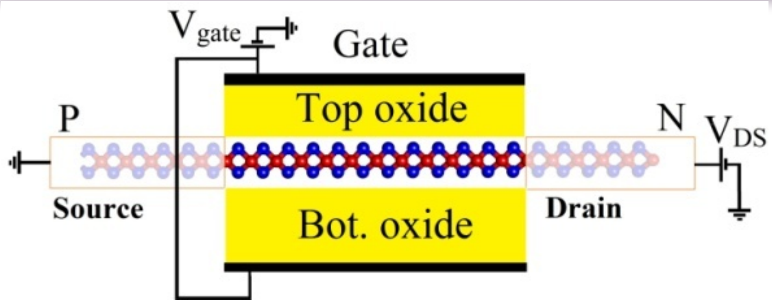
Fabrication technique

- Exfoliation (scotch tape)



Performance of 2D TFETs

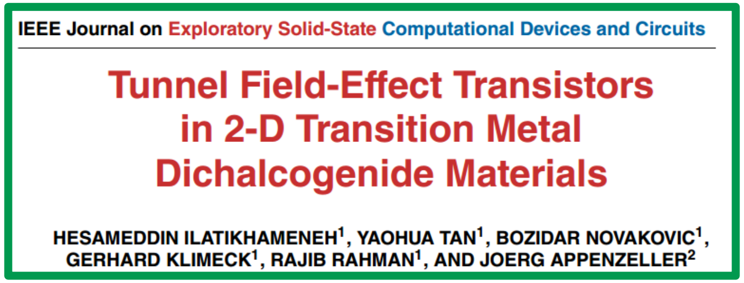
Performance of TMD TFETs



Atomistic simulation

Key messages:

- Thin channel is **NOT** enough for high I_{ON}
- Channel material **is** an important factor.



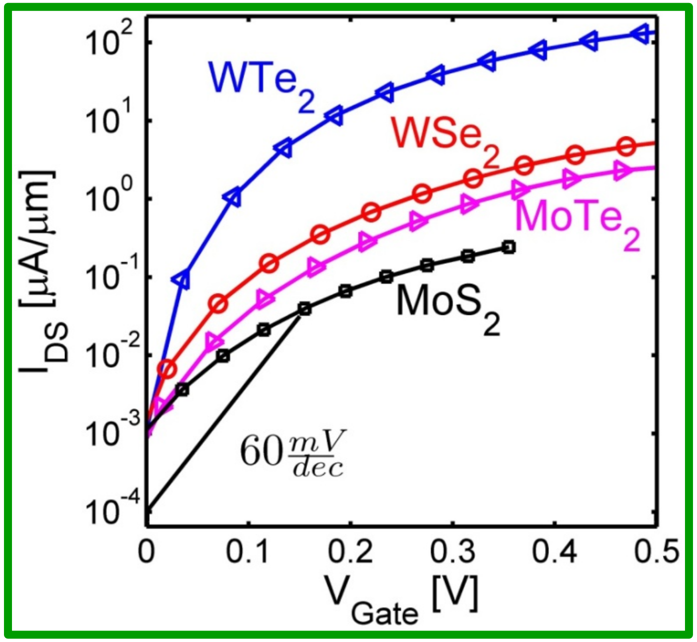
IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Tunnel Field-Effect Transistors in 2-D Transition Metal Dichalcogenide Materials

HESAMEDDIN ILATIKHAMENEH[1], YAOHUA TAN[1], BOZIDAR NOVAKOVIC[1], GERHARD KLIMECK[1], RAJIB RAHMAN[1], AND JOERG APPENZELLER[2]

Results

I_d-V_g of different TMDs

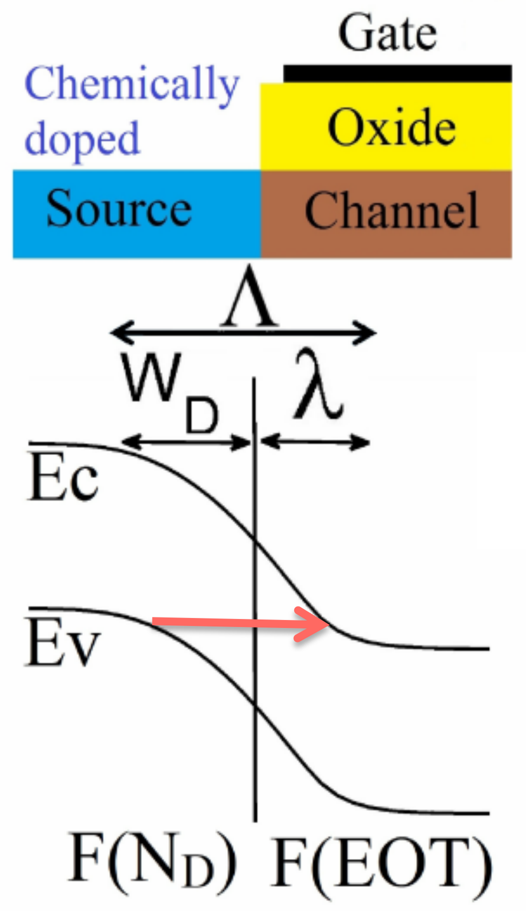


N_D = 1e20 cm^{-3} **V_{dd} = 0.5V**
EOT = 0.5nm **L_{ch} = 15nm**

Tunneling distance of TMD TFETs

2D materials have small tunneling distance

Depletion width (W_D)



Scaling length (λ)

Pros:
Low ε of channel material

Cons:
Chemical doping of 2D materials is in its infancy

N_D	W_D
1e20 cm^{-3}	2.5 nm
3e19 cm^{-3}	4.5 nm

Advantages:
1) Thin body

λ ~ 0.5nm

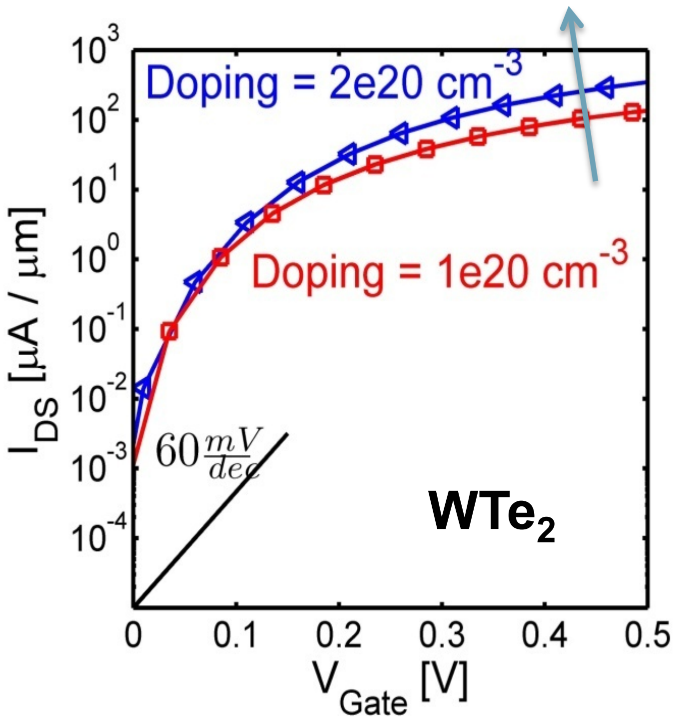
W_D is limiting factor

Challenges of TMD TFETs

Main challenges of TMDs

1) Large depletion width (W_D)

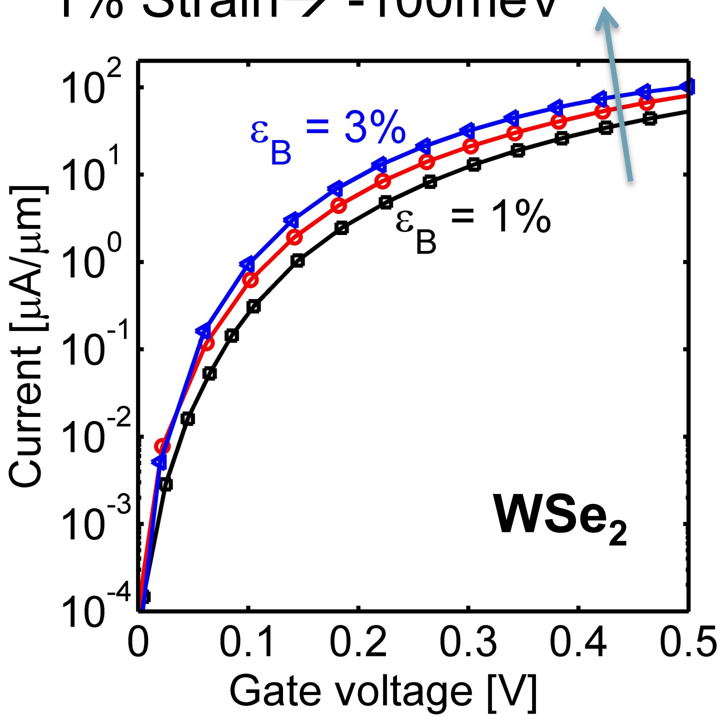
Source doping ↑→ W_D↓



2) Large bandgap (>1eV)

Tensile strain↑ → E_g↓

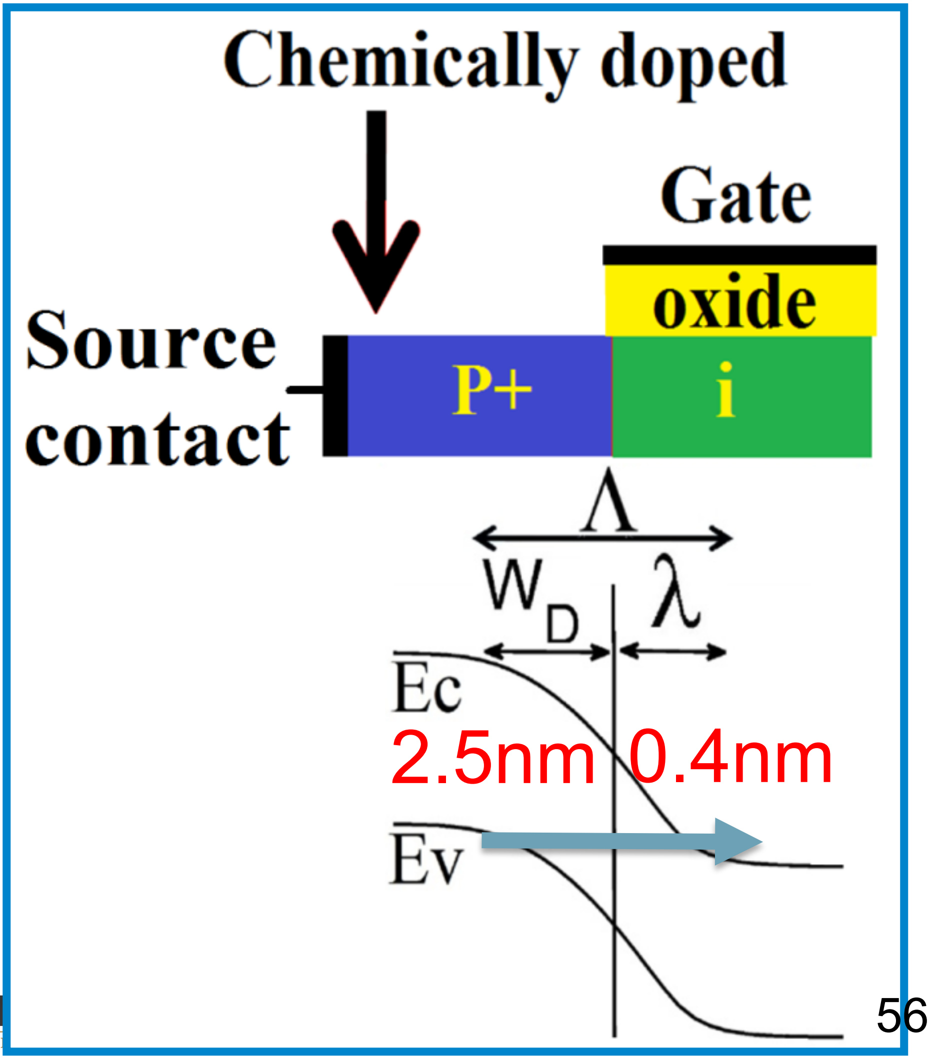
1% Strain→ -100meV



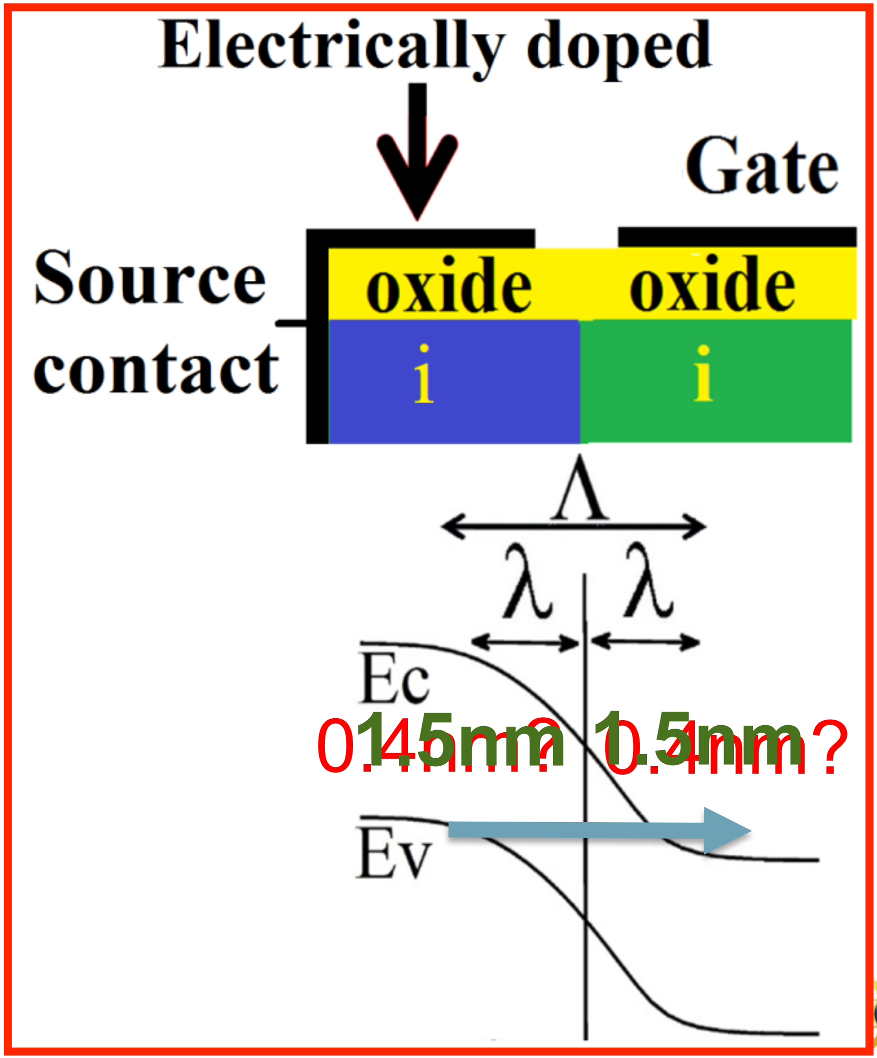
What avoids high I_{ON} in chemically doped TFET?

Is it possible to reduce tunneling distance more?

1) Chemical doping



2) Electrical doping



Electrically Doped TFET (ED-TFET)

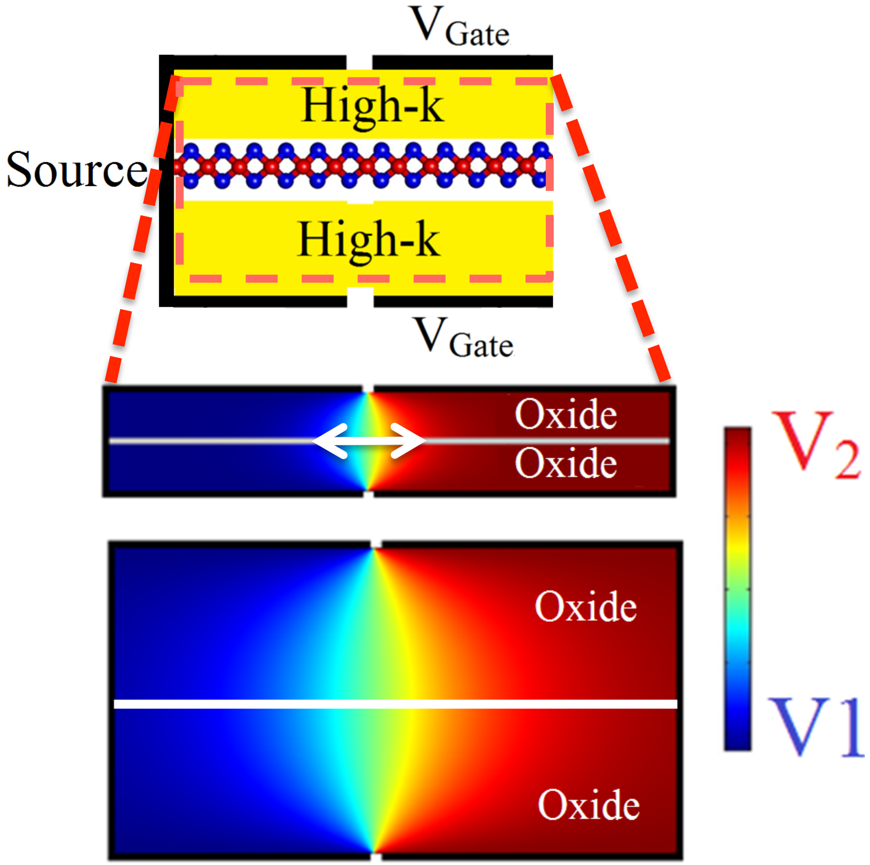
2D potential profile

Comment

Structure

Thin oxide

Thick oxide

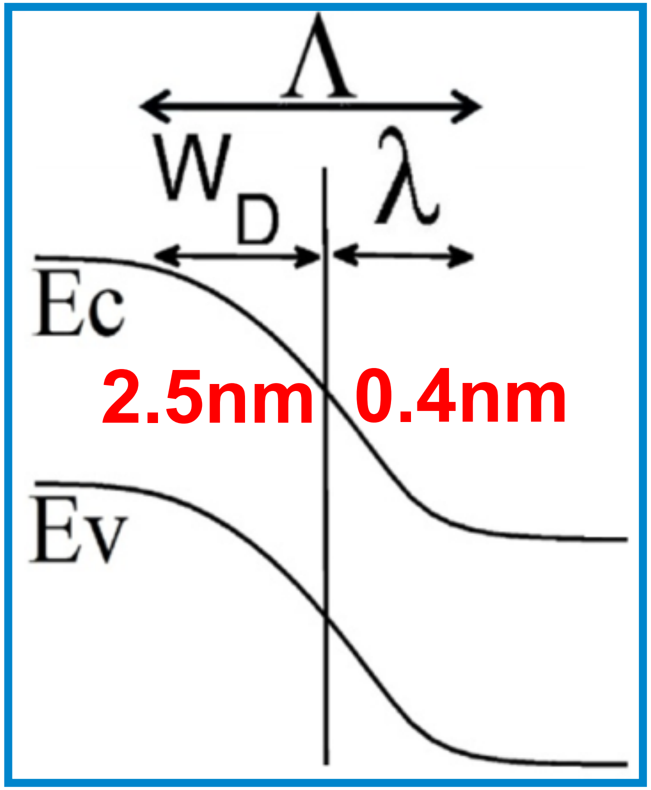


- **Presence of fringing fields**
- **Width of potential spread ~ T_{tot}**

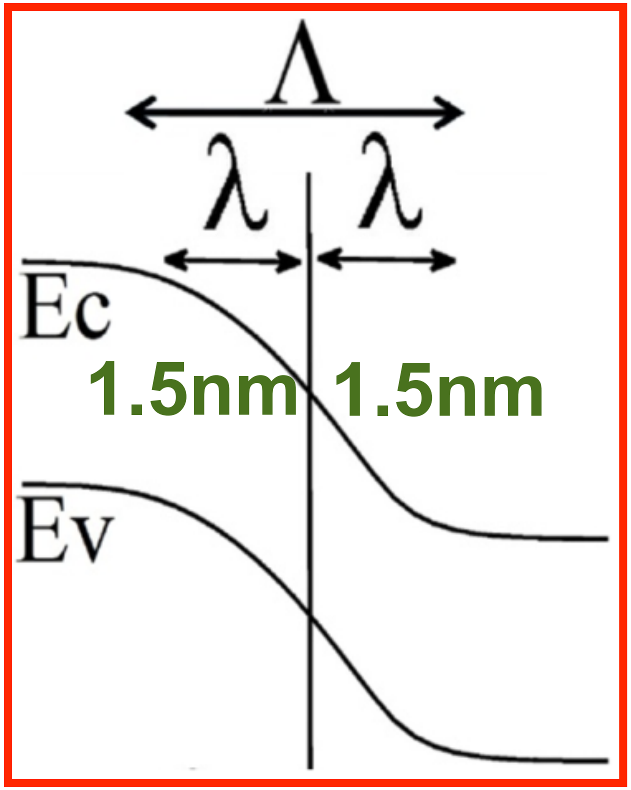
Oxide thickness is the major factor

I_{ON} challenge of electrically doped TFETs?

1) Chemical doping



2) Electrical doping



Is there a way to decrease tunneling distance?

I_{ON} challenge: Dielectric engineered TFET (DE-TFET)

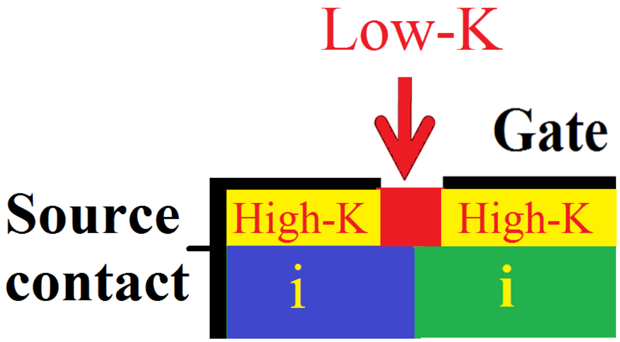
How to solve problem of electrically doped TFETs?

$$\lambda_{new} = f(t_{ox})$$

Answer: Dielectric engineering

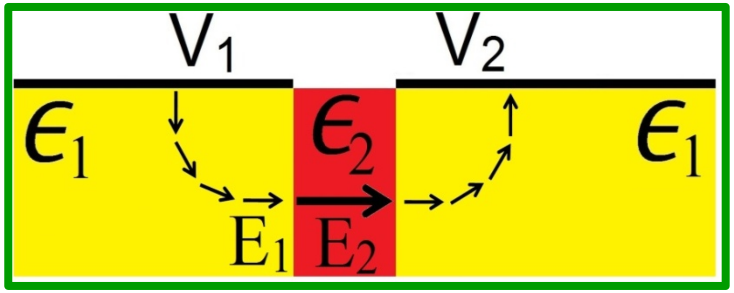
Illustration | **Comments**

Structure



- Combination of low-k and high-k dielectrics

Electric field amplification



$$\epsilon_1 E_1 = \epsilon_2 E_2$$

$$\epsilon_2 \ll \epsilon_1 \rightarrow E_2 \gg E_1$$

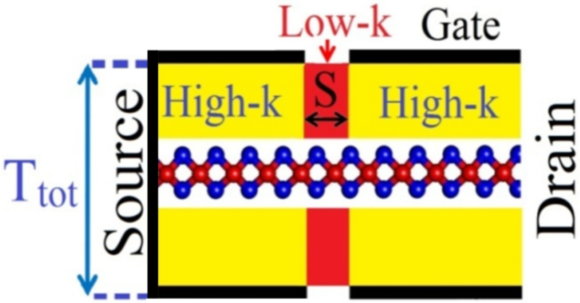
Electric field amplification → High I_{ON}

Dielectric Engineered TFET (DE-TFET): Performance

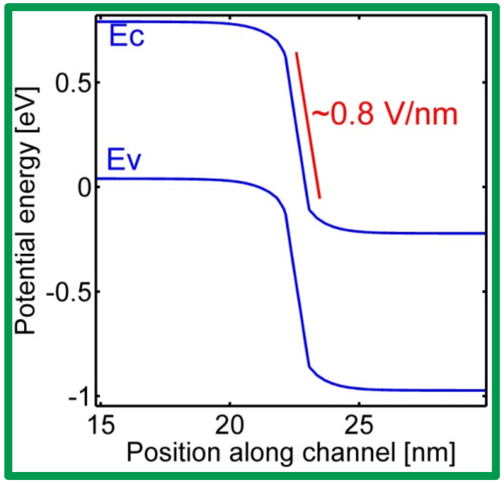
DE-TFET: High performance steep transistor

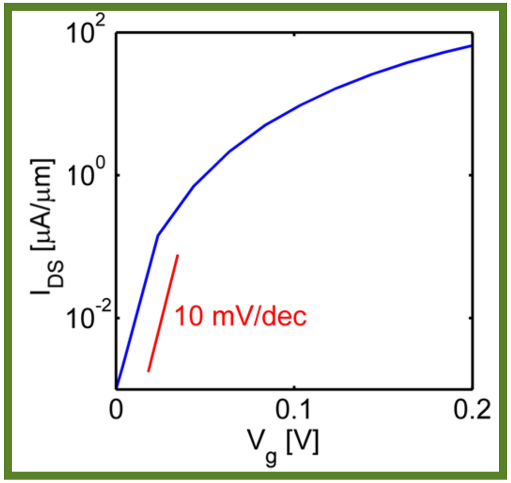
Structure

Atomistic simulation results



Vdd = 0.2V





- Monolayer WTe_2 channel
- Low-k = air gap
- High-k = HfO_2
- L_{ch} = 12nm

- I_{ON} DE-TFET >> I_{ON} of MOSFETs and SS = 10 mV/dec
- No chemical doping or heterostructure → No dopant or interface state

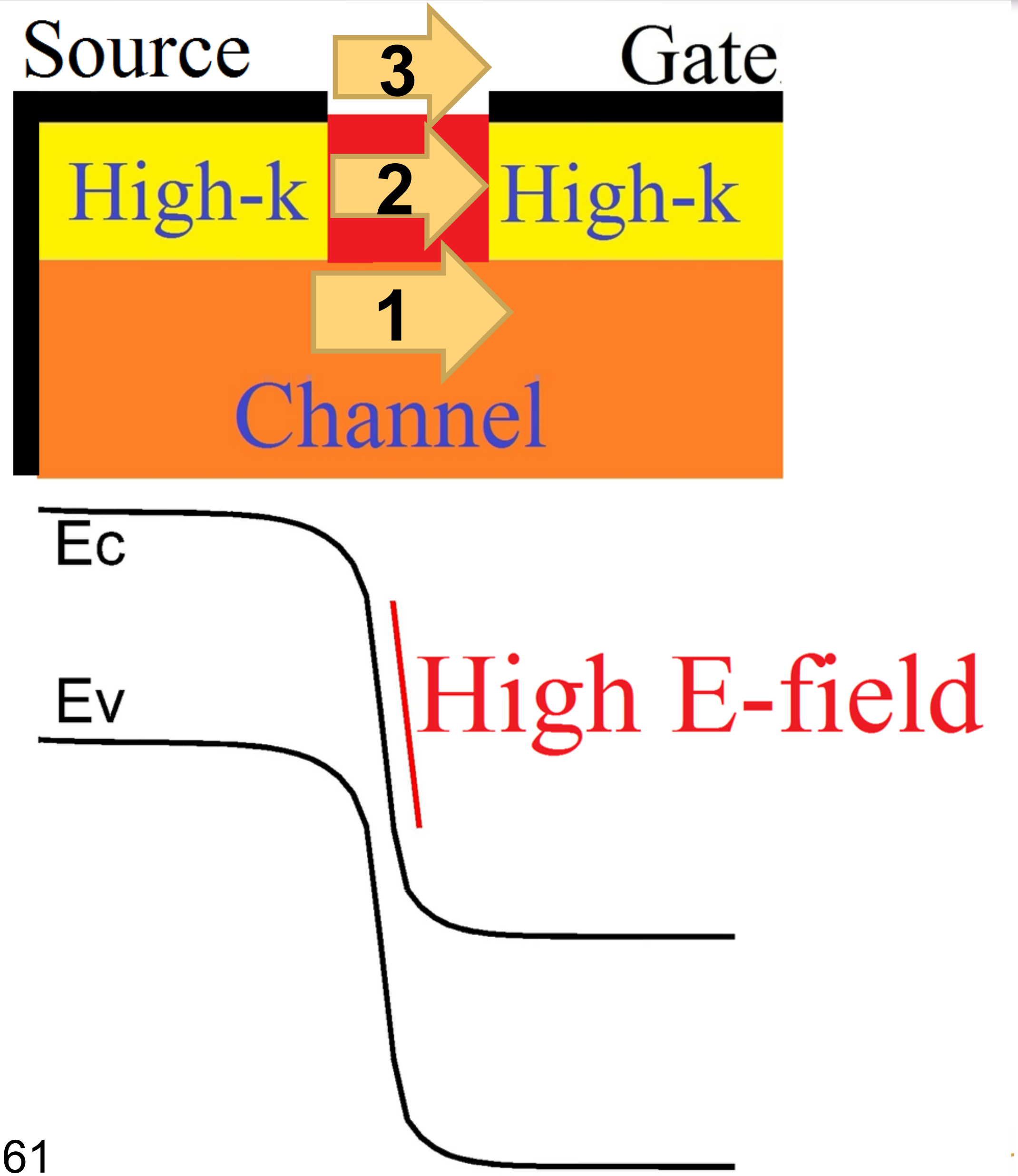
Patent application

Dielectric Engineered Tunnel Field-Effect Transistor

Hesameddin Ilatikhameneh, Tarek A. Ameen, Gerhard Klimeck, Joerg Appenzeller, and Rajib Rahman

DE-TFET Challenges

- Challenges:
- 1) E-field breakdown of channel
- 2) E-field breakdown of dielectrics
- 3) Gate leakage between contacts



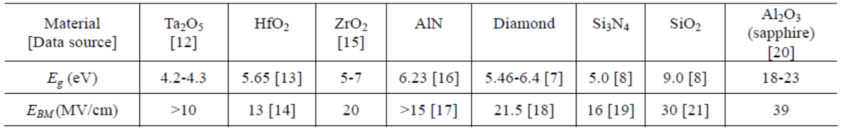
DE-TFET Challenges

- Challenges:
- 1 and 2) High E-field breakdown

Breakdown field

- Max E in semiconductors ~1V/nm
- Max E in dielectrics ~4V/nm

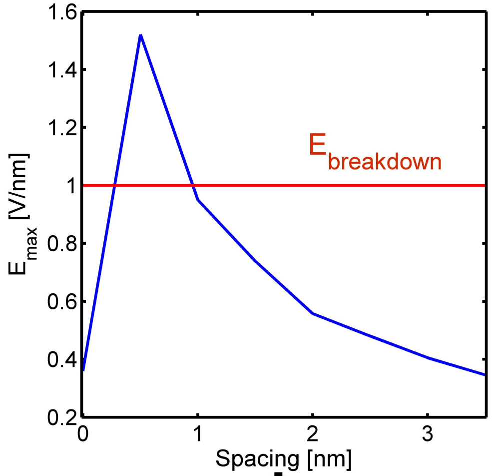
MAXIMUM BREAKDOWN FIELD E_{BM} AND BANDGAP E_G OF THE DIELECTRICS (INSULATORS) IN FIGURE 1 (T = 300 K)

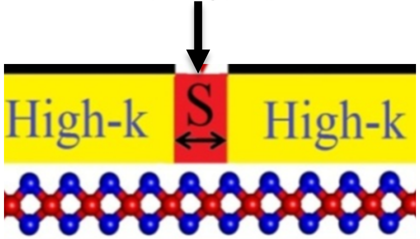


Material [Data source]	Ta_2O_5 [12]	HfO_2	ZrO_2 [15]	AlN	Diamond	Si_3N_4	SiO_2	Al_2O_3 (sapphire) [20]
E_g (eV)	4.2-4.3	5.65 [13]	5-7	6.23 [16]	5.46-6.4 [7]	5.0 [8]	9.0 [8]	18-23
E_{BM} (MV/cm)	>10	13 [14]	20	>15 [17]	21.5 [18]	16 [19]	30 [21]	39

DOI: 10.1109/ICMEL.2006.1651032

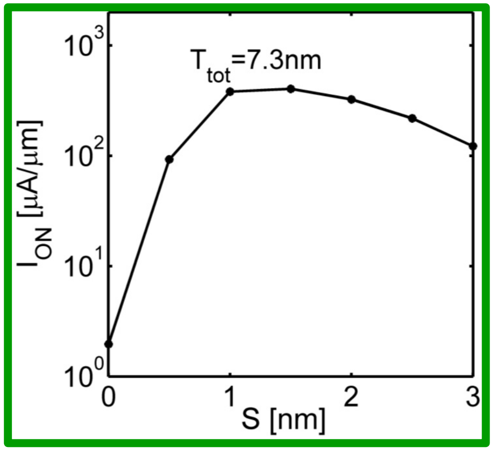
Max E

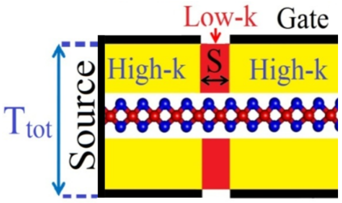




Adjust spacing for the required E-field

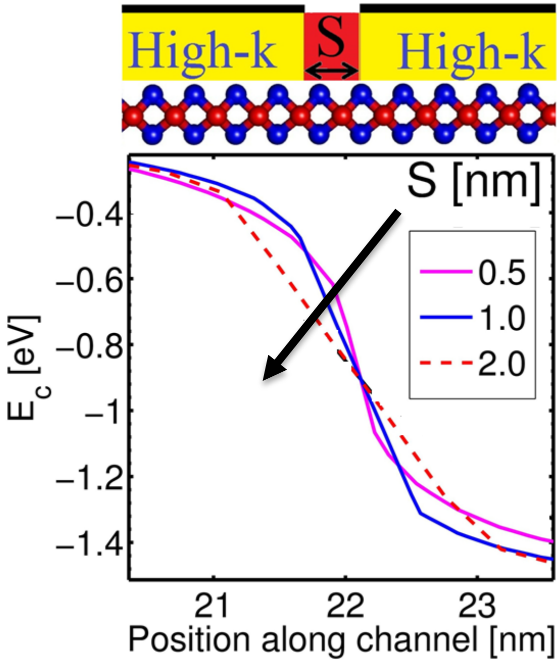
Insensitivity to E





Insensitivity to Spacing

- Why is I_{ON} insensitive to spacing in some range?



- Increasing S (above 0.5nm)
  - 1) $E_{max} \downarrow \rightarrow I_{on} \downarrow$
  - 2) tunneling window $\uparrow \rightarrow I_{on} \uparrow$

TFET Challenges

- Challenges:
- 2) Leakage between contacts

High transmission

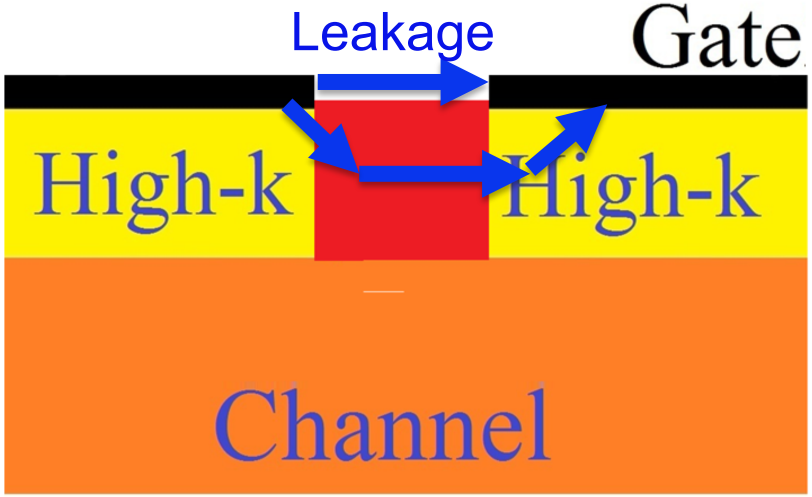
Small Λ → high transmission

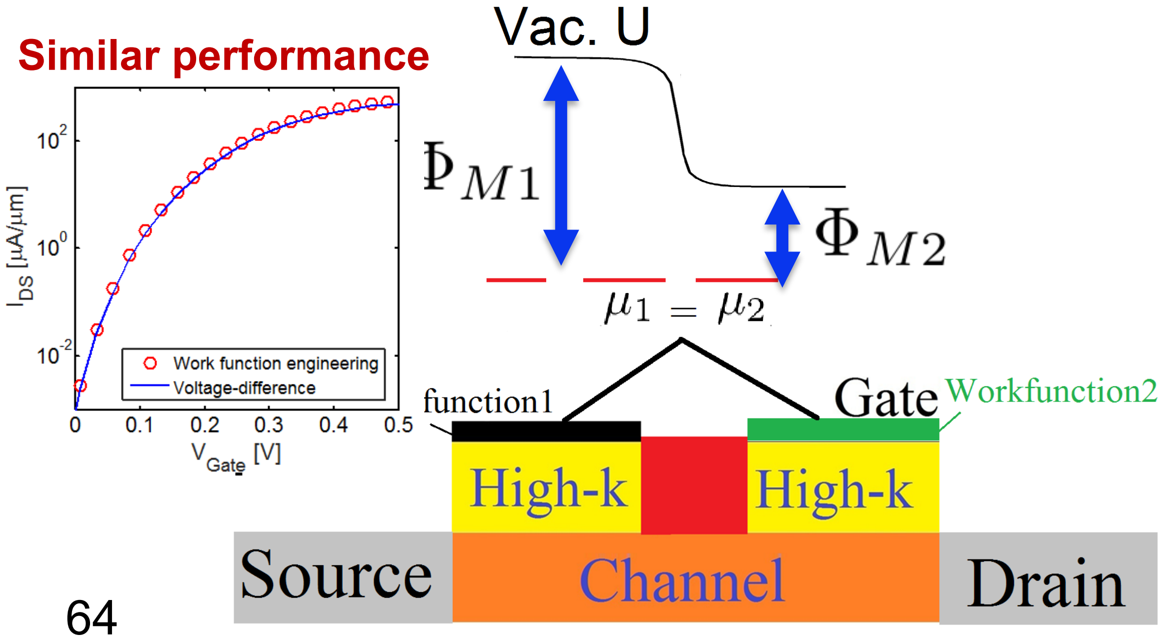
$$T_{BTBT} = exp\left(-C\,\sqrt{m_t^* E_g}\,\Lambda\right)$$

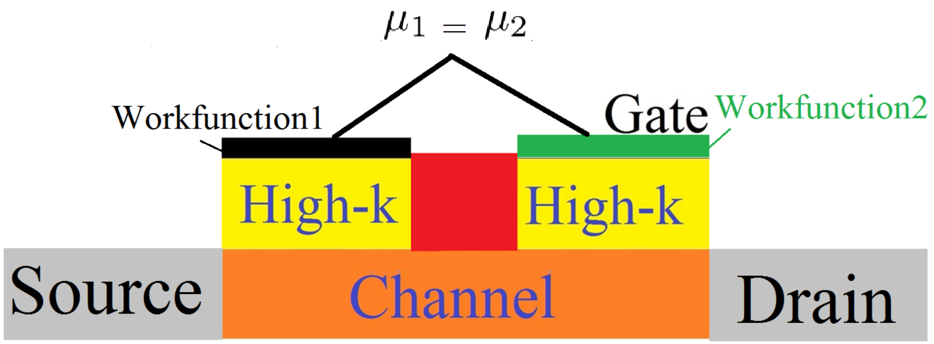
Solution

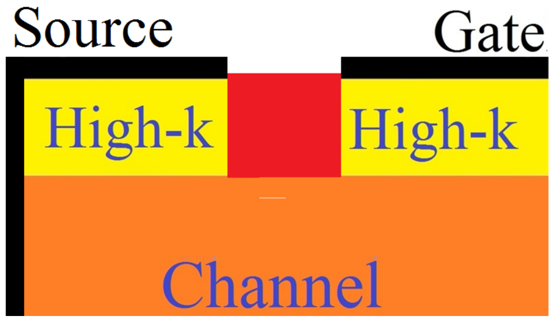
Landauer formula

$$I \propto T(\mu_1 - \mu_2)$$

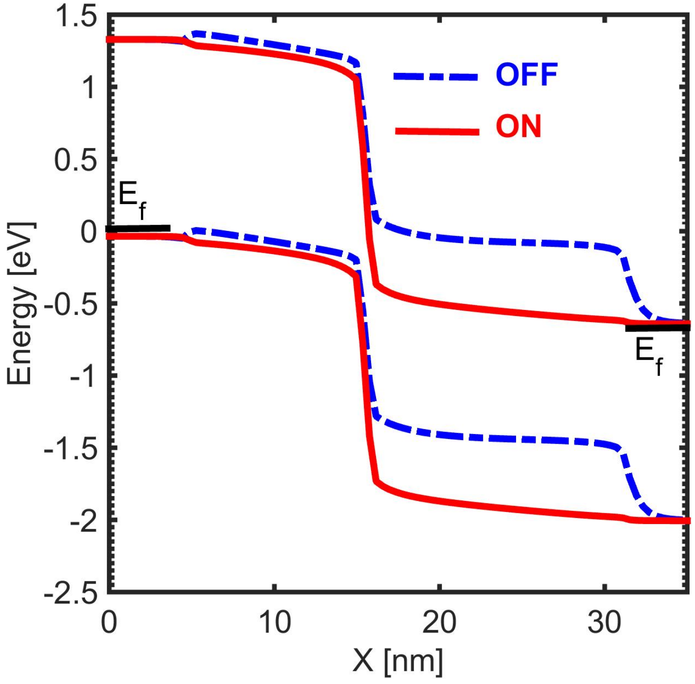




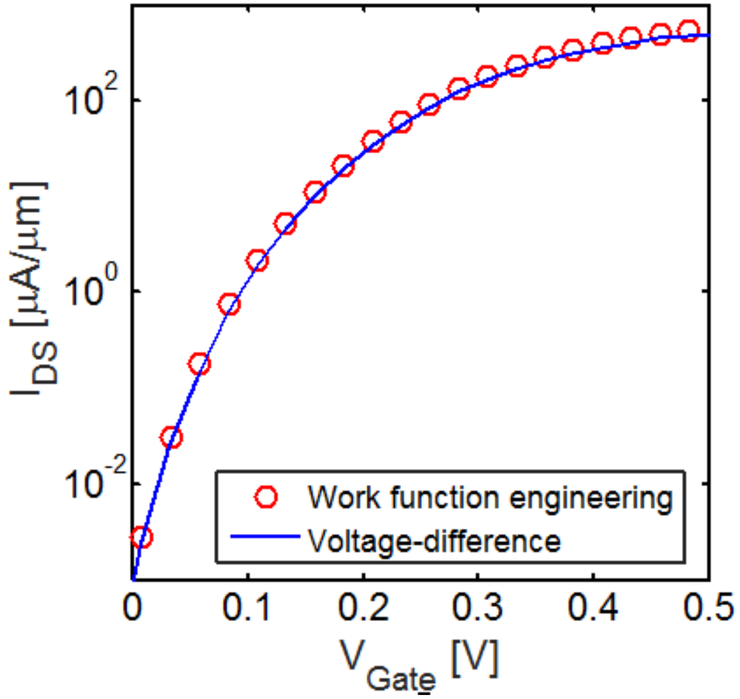




Band diagram

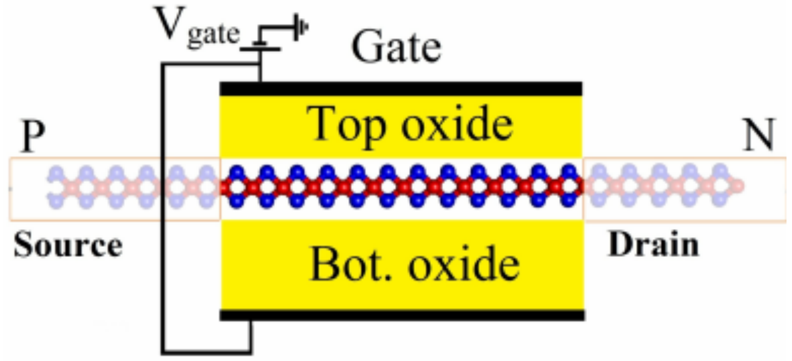


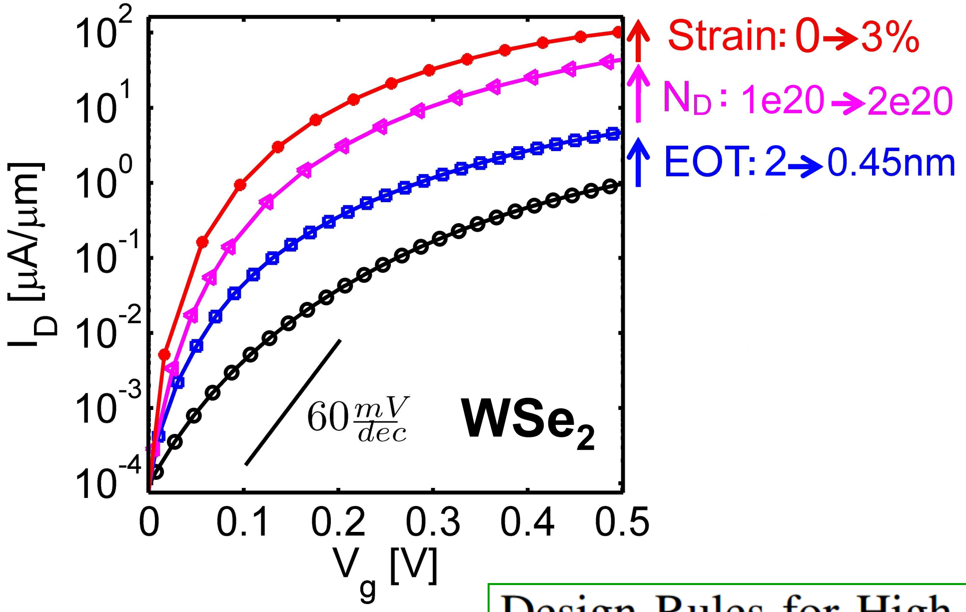
Similar performance



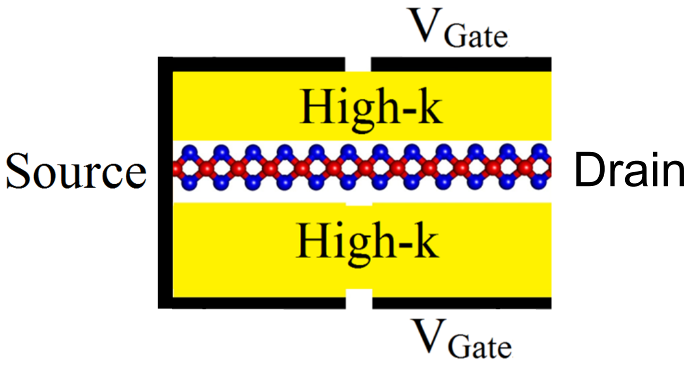
Performance boosters of TMD TFETs

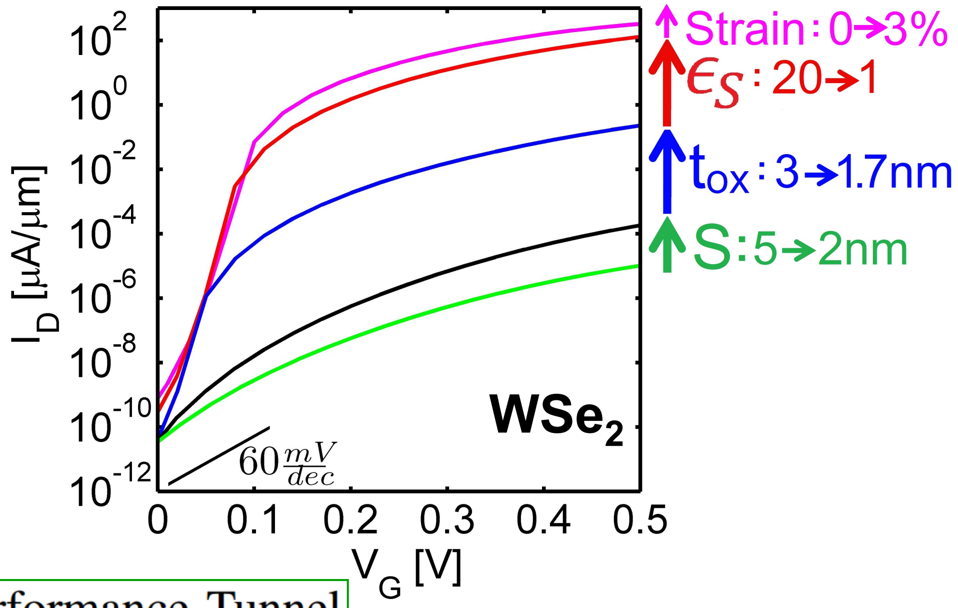
Chemically doped TFET





Electrically doped TFETs



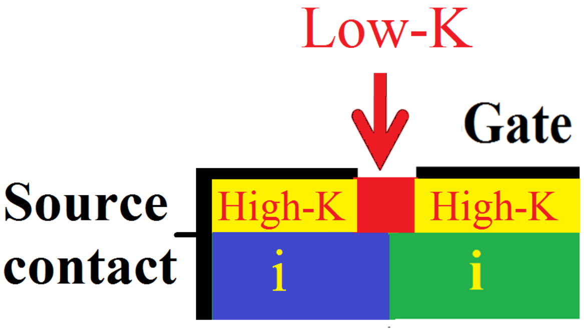


Design Rules for High Performance Tunnel Transistors from 2D Materials

Summary of TMD TFETs

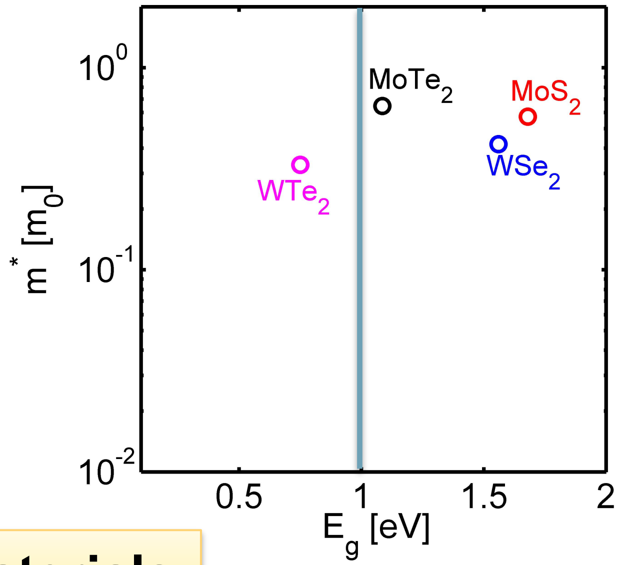
Tunneling distance

Dielectric engineering♪
→ Tunneling distance ~ 1nm



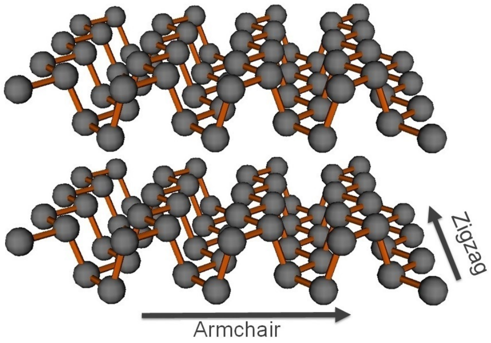
Material properties

Large E_g and m*♪
WTe_2 is not stable

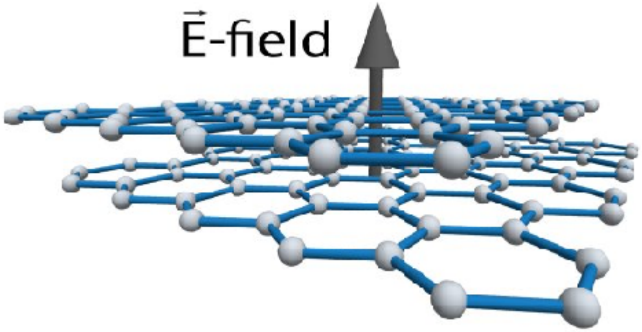


Motivation for low bandgap 2D materials

Phosphorene



Bilayer Graphene



Agenda

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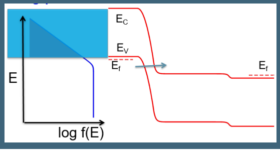
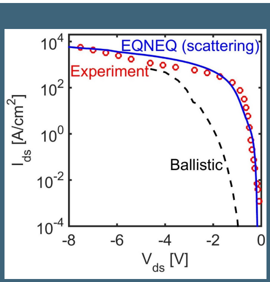
1) Motivation for steep transistors
2) Requirements for steep tunnel transistors



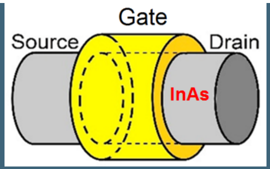
Atomistic quantum transport simulation

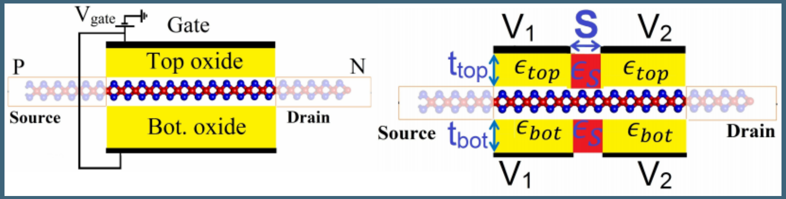
1) Device geometry optimization
2) Scattering impact
3) Verify and extend analytic models

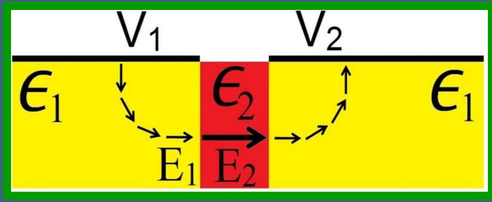


Tunnel transistors

1) III-V materials
2) 2D materials
    a) Chemical doping
    b) Electrical doping
    c) Dielectric engineering
3) Best materials for scaling challenge







Channel length scaling of TFETs

Steep devices → V_{DD} ↓

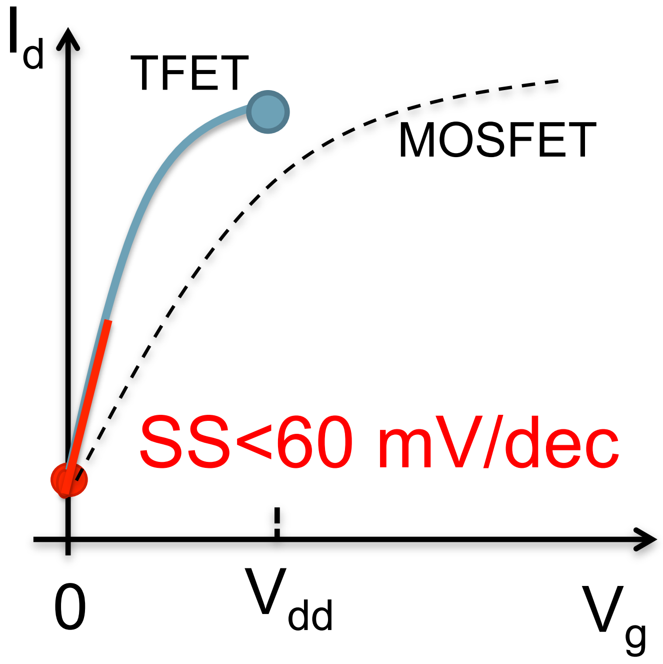
+

Scaled channels→ L_{Ch} ↓

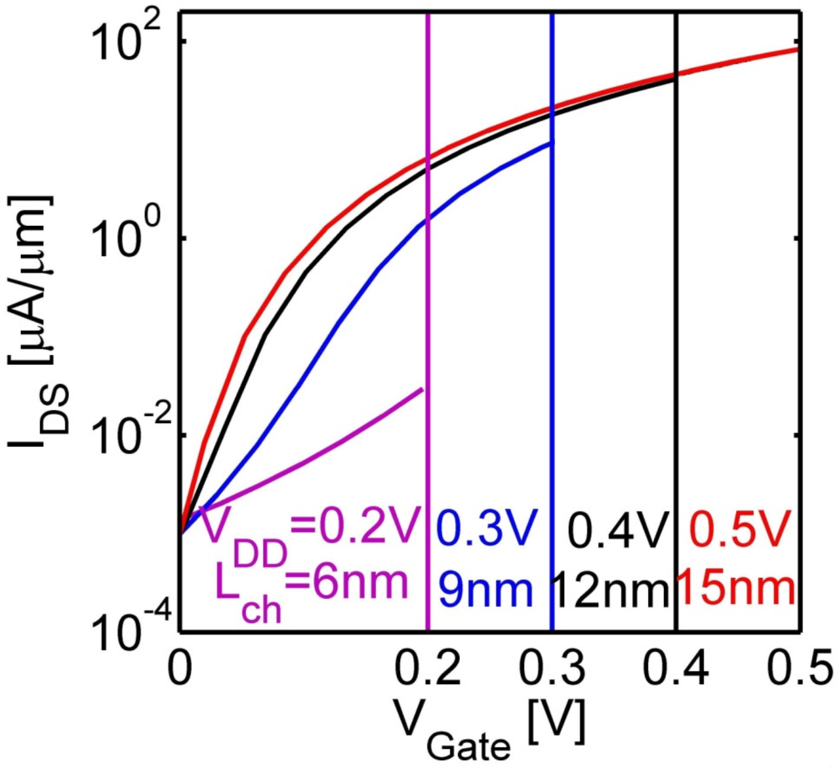
Scaling challenge of TFETs

Our target:

V_{dd} scaling + L_{ch} scaling



What happens in reality:

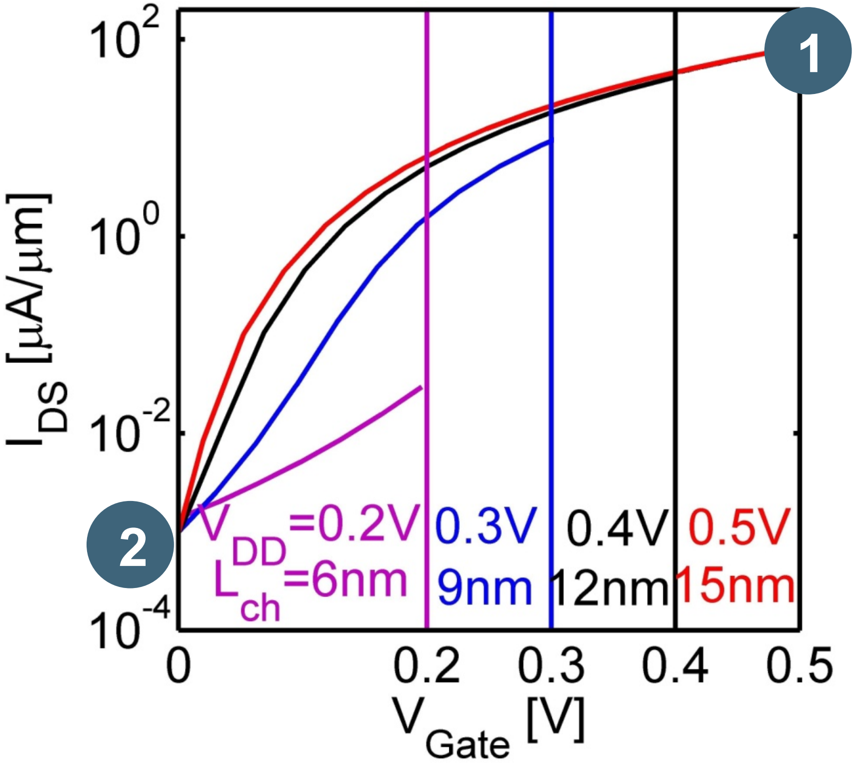


InAs gate-all-around (NEGF)

We scale V_{DD} down with L_{ch}: L_{ch}/V_{DD}=30 V/nm

Why L_{ch} and V_{DD} scaling degrades performance?

Scaling challenge



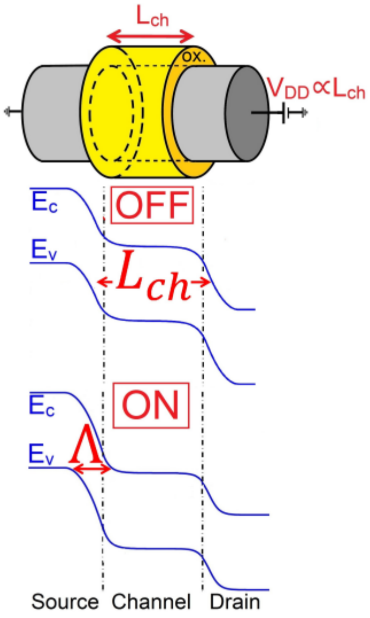
Scaling consequences

① V_{DD} ↓→Tunneling energy window ↓ →I_{ON}↓

② L_{ch} ↓ → I_{ON}/I_{OFF} ↓↓

$$T_{OFF} = exp\left(-C\ \sqrt{m_t^* E_g}\ L_{ch}\right)$$

$$T_{ON} = exp\left(-C\ \sqrt{m_t^* E_g}\ \Lambda\right)$$



Scaling L_{ch} → $L_{ch} \sim \Lambda$ → I_{ON} / I_{OFF} ↓

Scaling challenge of TFETs: Best material

1) Best material for ultra-scaled TFETs?

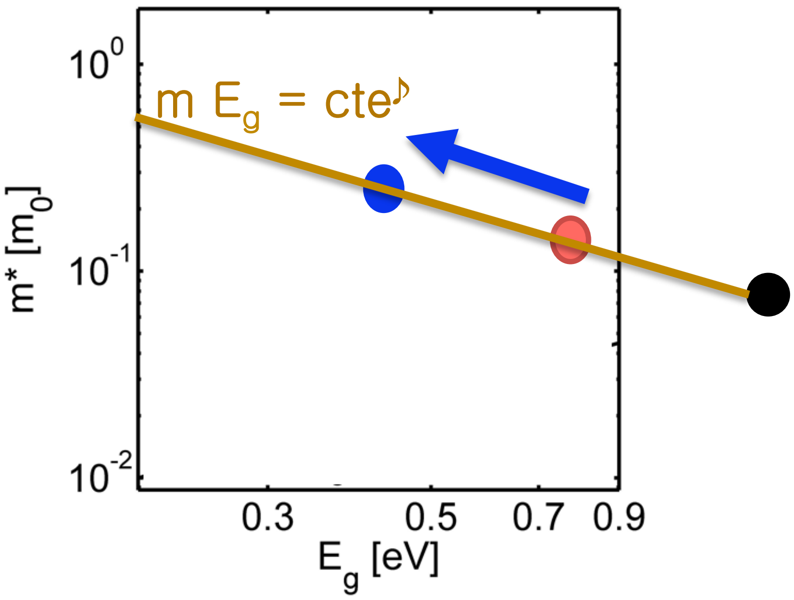
EOT: 0.5nm, N_D=1e20 cm^{-3}♪

$$T_{ON} = exp\left(-C\ \boxed{\sqrt{m_t^* E_g}}\ \Lambda\right)$$

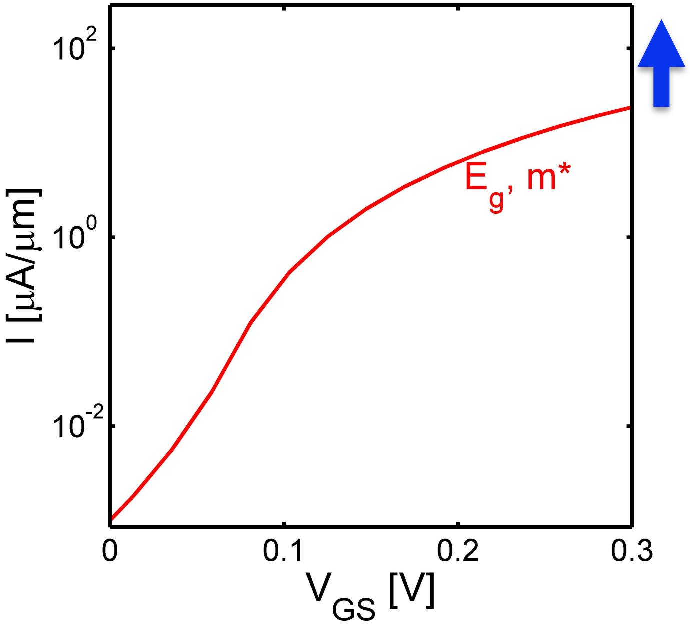
$$T_{OFF} = exp\left(-C\ \boxed{\sqrt{m_t^* E_g}}\ L_{ch}\right)$$

$m{*}E_g$ = cte → I_{ON} /I_{OFF} = cte (?)♪

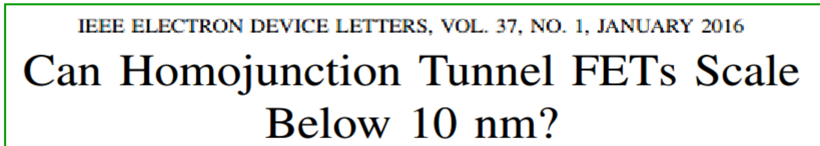
Material properties



I_D-V_G



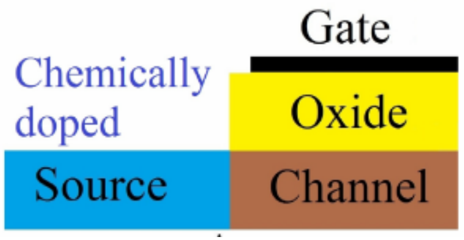
Lower Eg, higher m* → better performance


IEEE ELECTRON DEVICE LETTERS, VOL. 37, NO. 1, JANUARY 2016

Can Homojunction Tunnel FETs Scale Below 10 nm?

Why m* and Eg have different impact on performance?

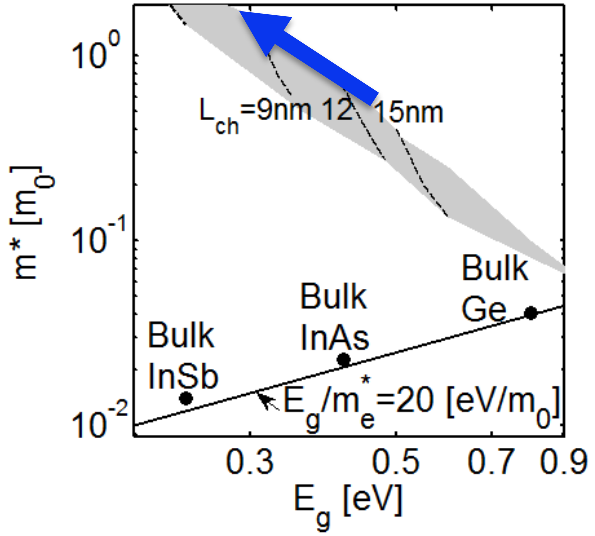
2) Why m* and Eg are not interchangeable?

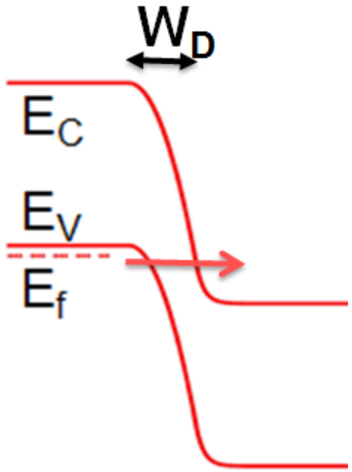


$$T_{ON} = exp\left(-C\ \sqrt{m_t^* E_g}\ \Lambda\right)$$

$$f\left(E_g\right)$$

m^*-E_g → best I_{ON}/I_{OFF} > 1e5



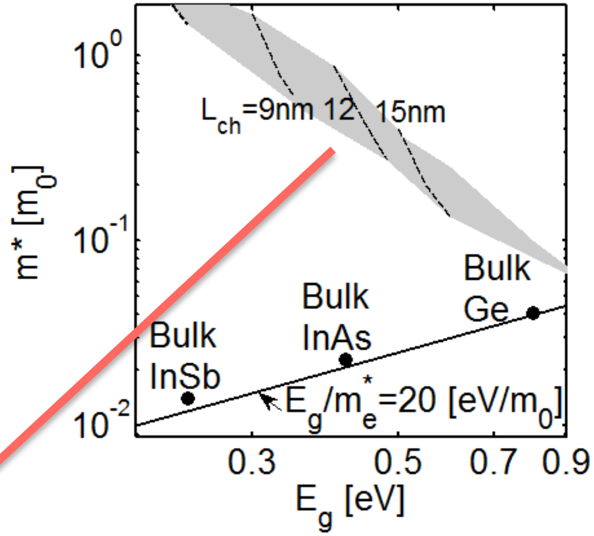


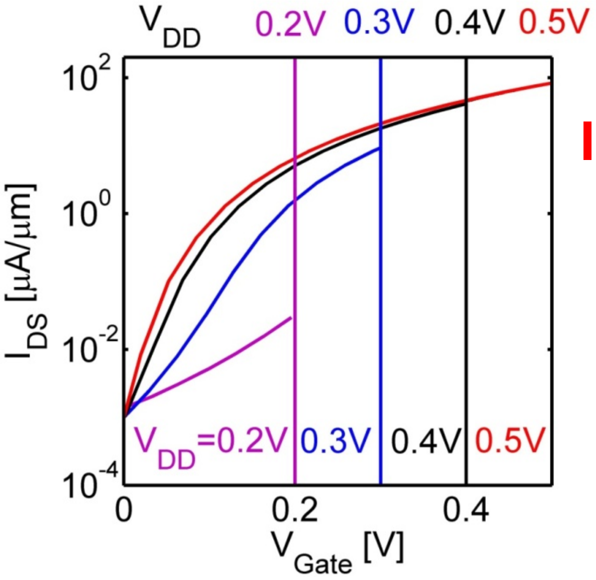
Larger E_g → Larger tunneling distance Λ → I_{ON} ↓

Best material choice for short channel TFETs

The solution of the scaling problem:

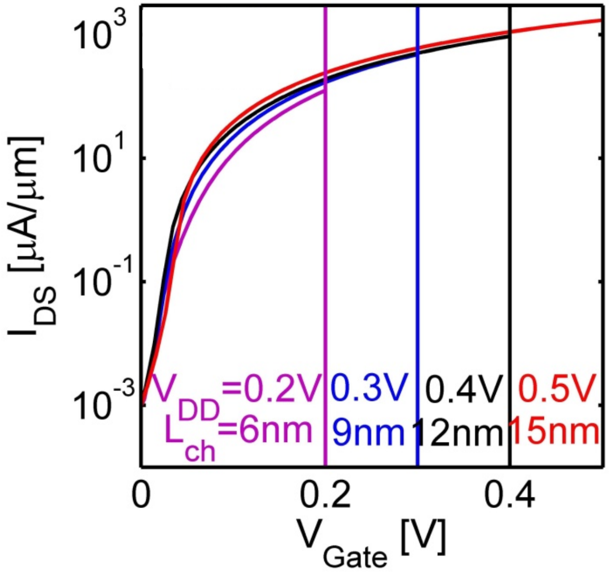
$$L_{ch}\downarrow \;\&\; V_{dd}\downarrow \begin{cases} E_g \downarrow \text{Opt: } 1.2qV_{DD}[eV] \\ m^* \uparrow \text{ Opt} \end{cases}$$





InAs

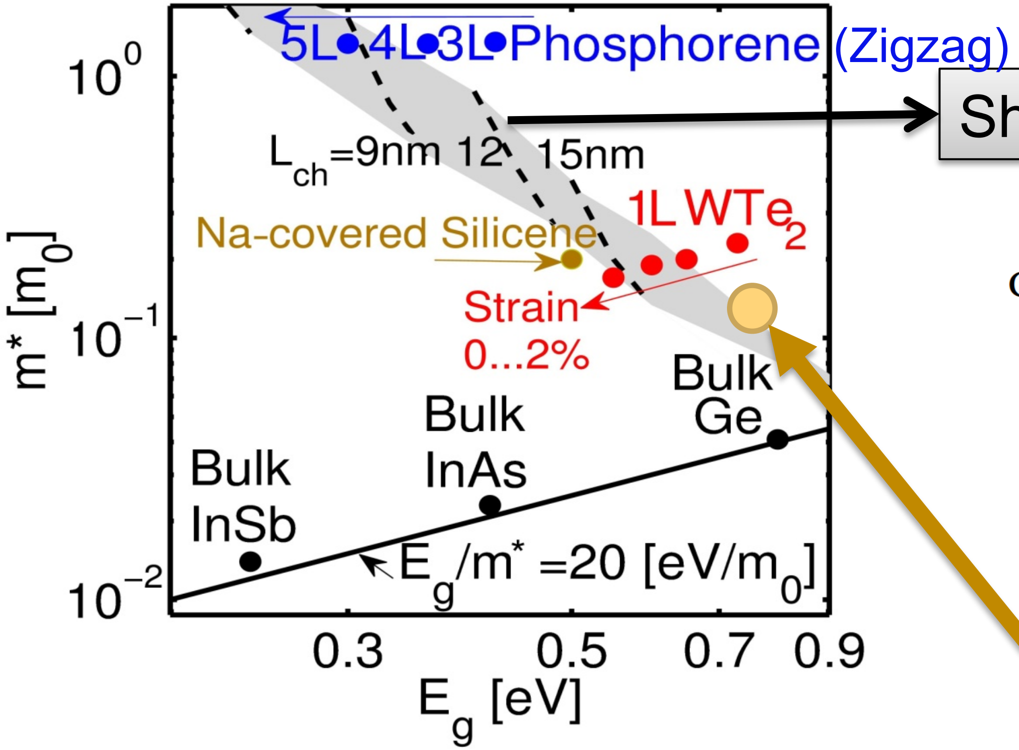
Optimum material for each node



Optimum channel material is necessary for ultra-scaled TFETs

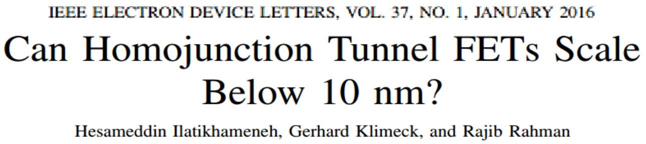
Sub 10nm TFETs

Best channel materials for TFET applications:
1) Low $E_g \sim 1.2\ V_{DD}$
2) High m*



Shaded region: $I_{ON}/I_{OFF} > 10^5$

2L Phosphorene (armchair)


IEEE ELECTRON DEVICE LETTERS, VOL. 37, NO. 1, JANUARY 2016

Can Homojunction Tunnel FETs Scale Below 10 nm?

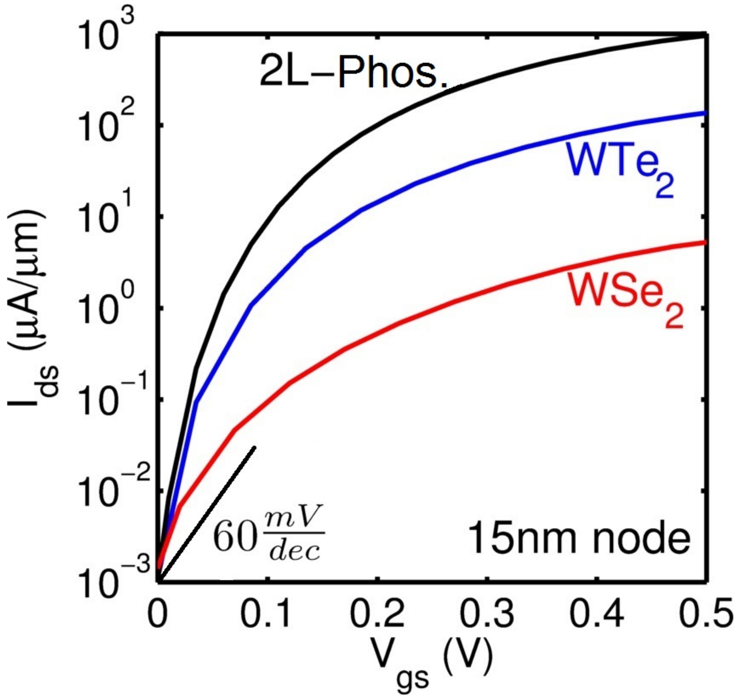
Hesameddin Ilatikhameneh, Gerhard Klimeck, and Rajib Rahman

2D materials outperform III-V TFETs in sub 10nm channel lengths.

Phosphorene TFET

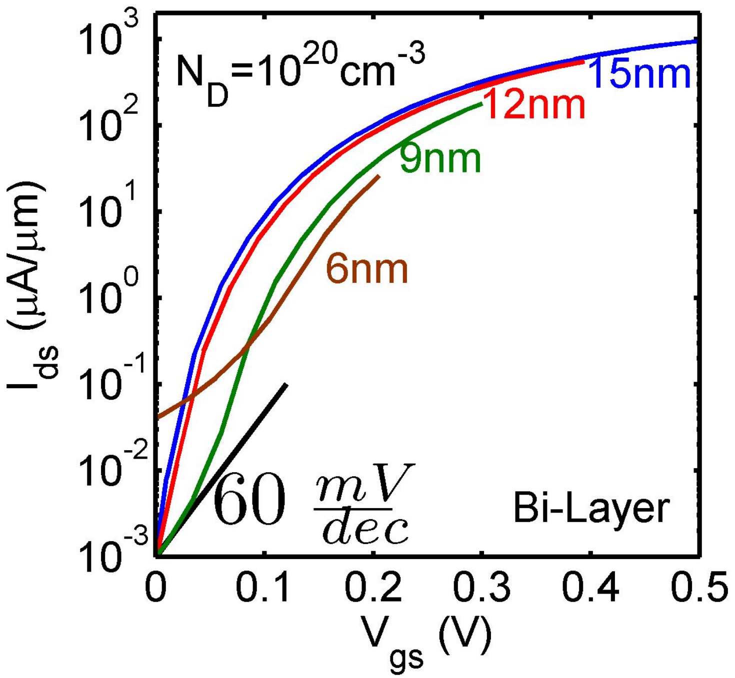
E_g of Bilayer Phosphorene ~ 0.8 eV = 1.3 V_{DD}

Phosphorene TFET



Phosphorene outperforms TMD TFETs
→ a proper bandgap

Scaling of Phosphorene TFET



Scales well for L_{ch} > 6nm

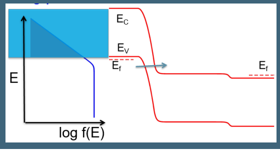
SCIENTIFIC REPORTS

OPEN Few-layer Phosphorene: An Ideal 2D Material For Tunnel Transistors

Agenda

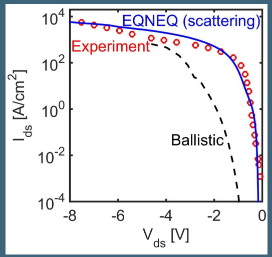
Introduction

1) Motivation for steep transistors
2) Requirements for steep tunnel transistors



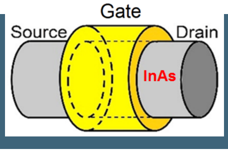
Atomistic quantum transport simulation

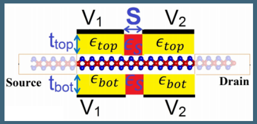
1) Device geometry optimization
2) Scattering impact
3) Verify and extend analytic models

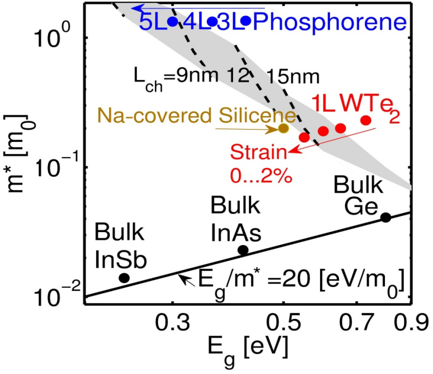


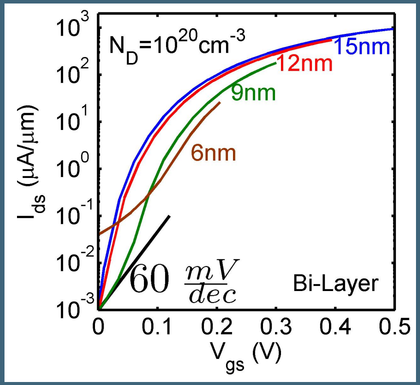
Tunnel transistors

1) III-V materials
2) 2D materials
3) Best materials for scaling challenge
4) What to do for L_{ch} < 9nm?



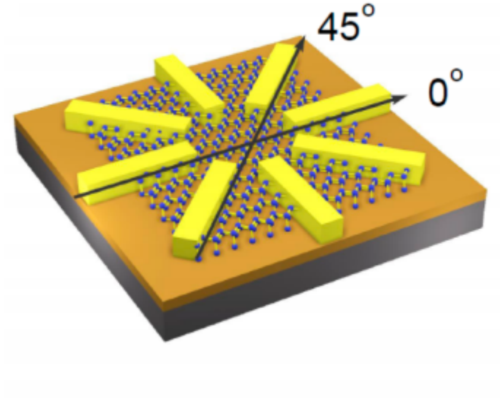


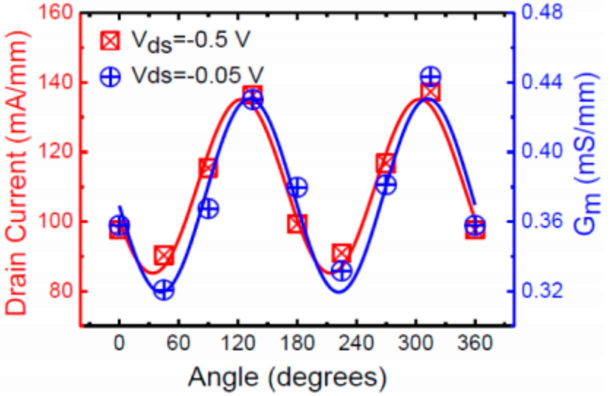


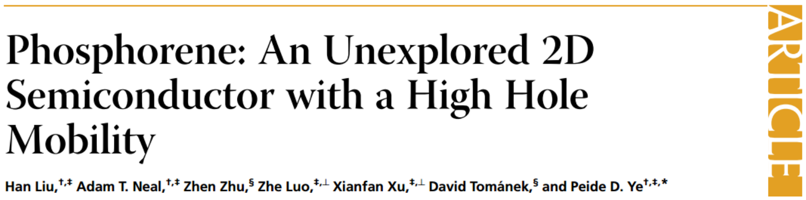


Anisotropic effective mass of Phosphorene

Effective mass of phosphorene is very anisotropic ($m^*_x/m^*_y >> 1$)





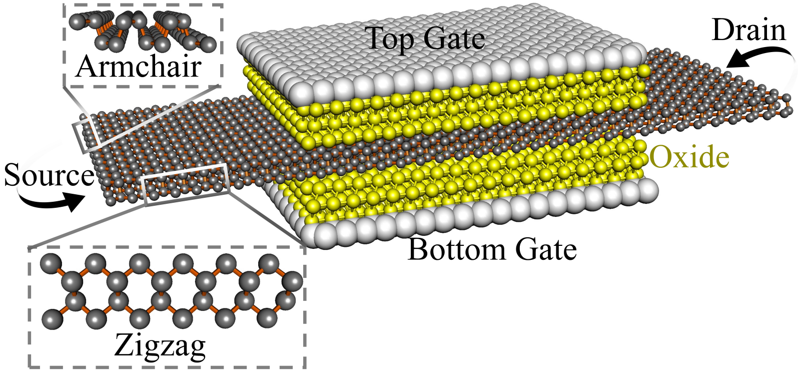


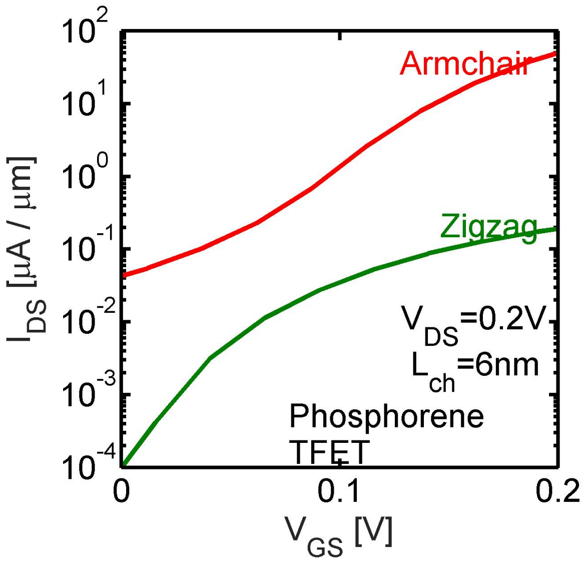
ARTICLE

Phosphorene: An Unexplored 2D Semiconductor with a High Hole Mobility

Han Liu,[†,‡] Adam T. Neal,[†,‡] Zhen Zhu,[§] Zhe Luo,[‡,⊥] Xianfan Xu,[‡,⊥] David Tománek,[§] and Peide D. Ye[†,‡,*]

Phosphorene Nanoribbon TFET

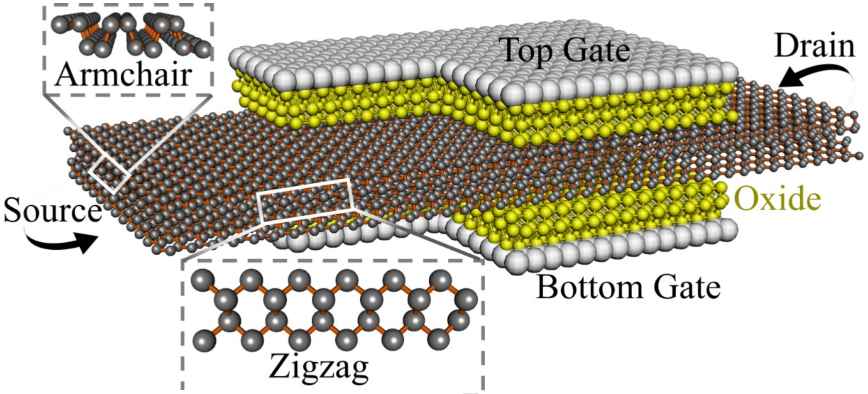




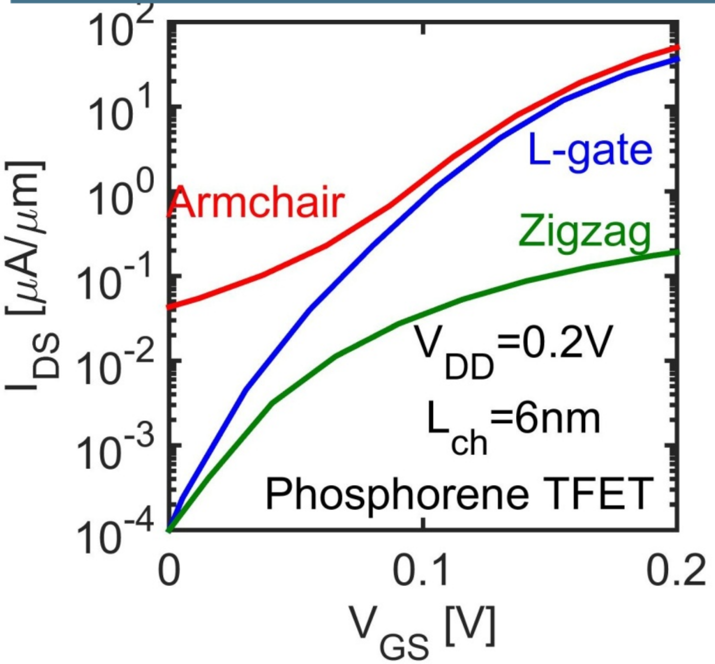
Is it possible to have benefits of both directions?

L-shaped phosphorene TFET

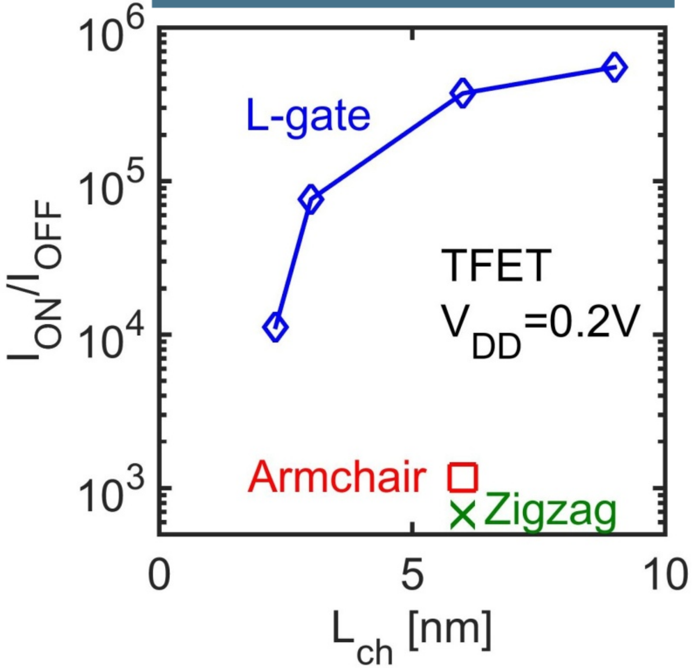
L-shaped TFET can perform even with L_{ch} of 2nm.



Benefits of both directions



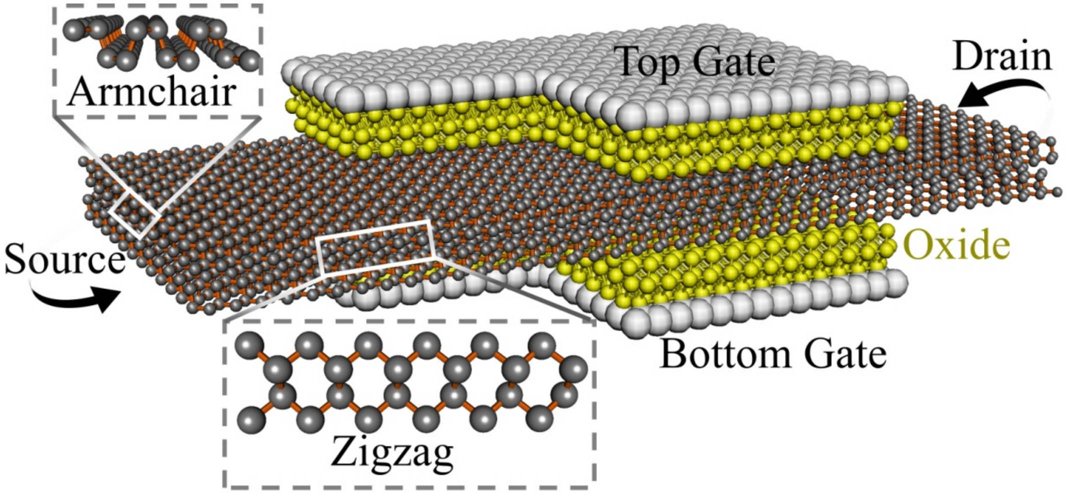
Successful scaling



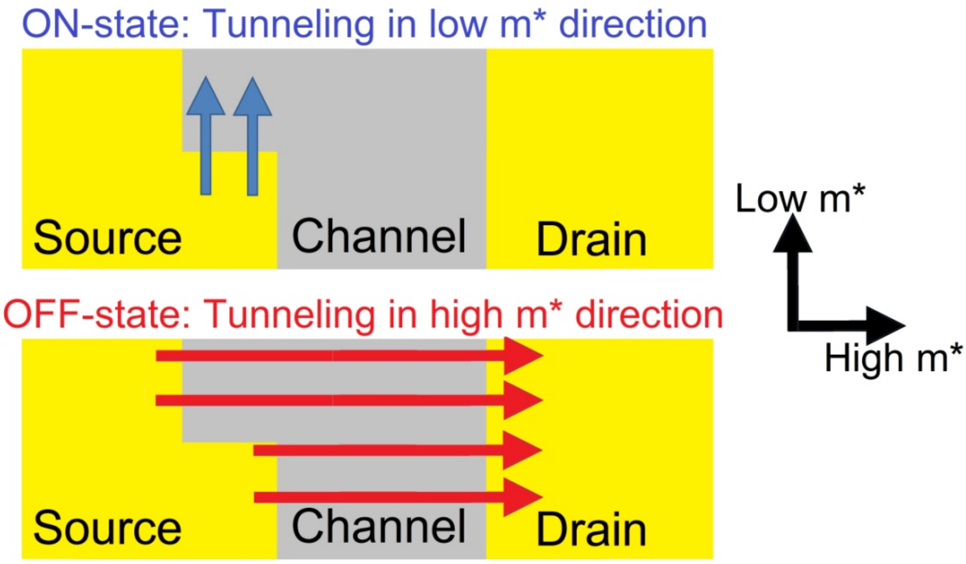
L-shaped phosphorene TFET

How does L-shaped TFET work?

Perspective view



Top view



$$T_{ON} = exp\left(-C\sqrt{m_t^* E_g}\;\Lambda\right)$$

$$T_{OFF} = exp\left(-C\sqrt{m_t^* E_g}\;L_{ch}\right)$$

→

1) Low m* for high I_{ON}
2) High m* for low I_{OFF}

Using a material with anisotropic m* and L-shaped gate have benefits of

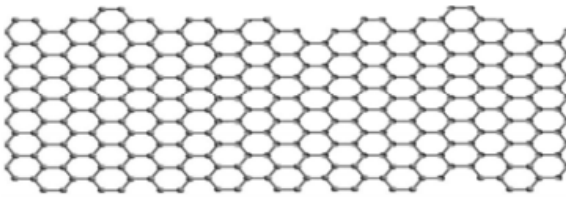
- High I_{ON} / I_{OFF}

SCIENTIFIC REPORTS

Edge roughness challenge

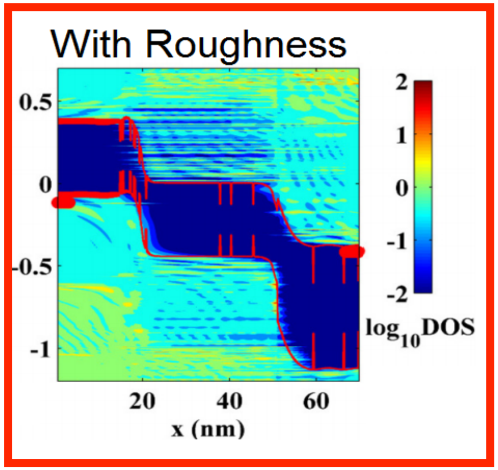
Nano-ribbons suffer from edge roughness

Graphene Nanoribbon



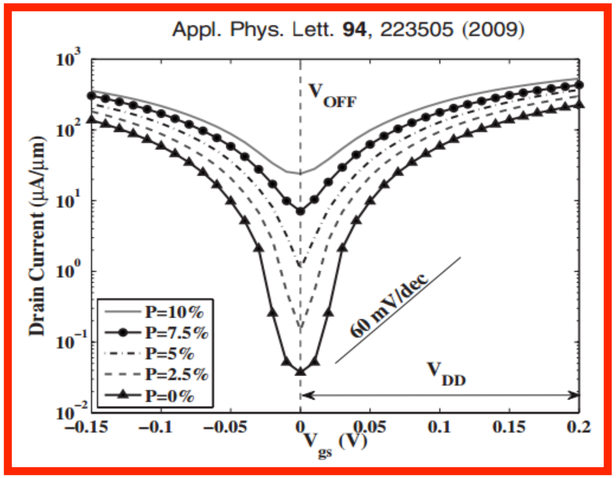
Appl. Phys. Lett. **104**, 243113 (2014)

LDOS

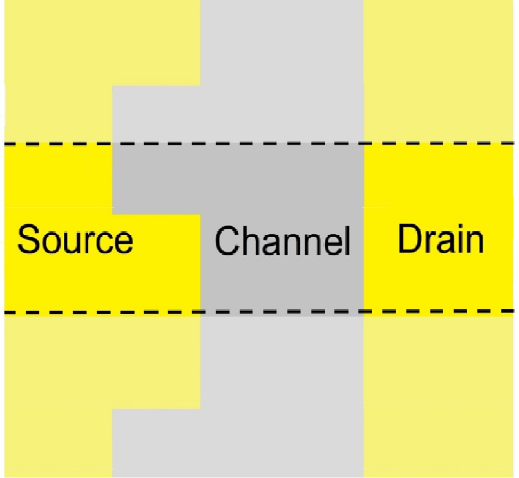


Sloppy IV

Appl. Phys. Lett. **94**, 223505 (2009)

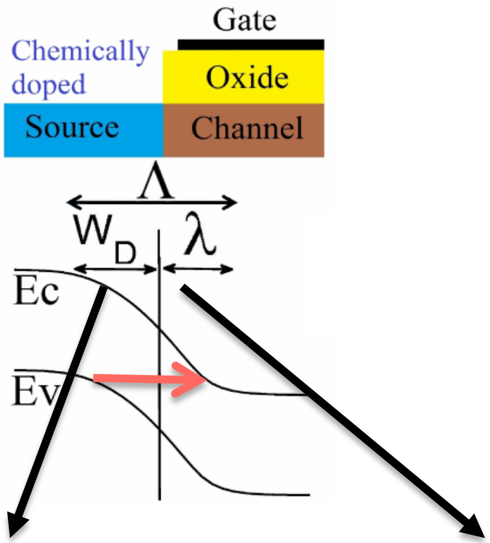


Solution: edge-less pattern



Summary

Tunneling distance

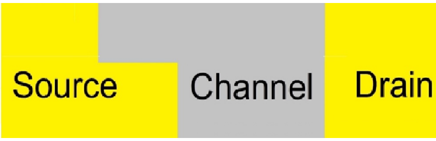


Challenge for 2D

Challenge for III–V

DE-TFET → V_{dd} scaling

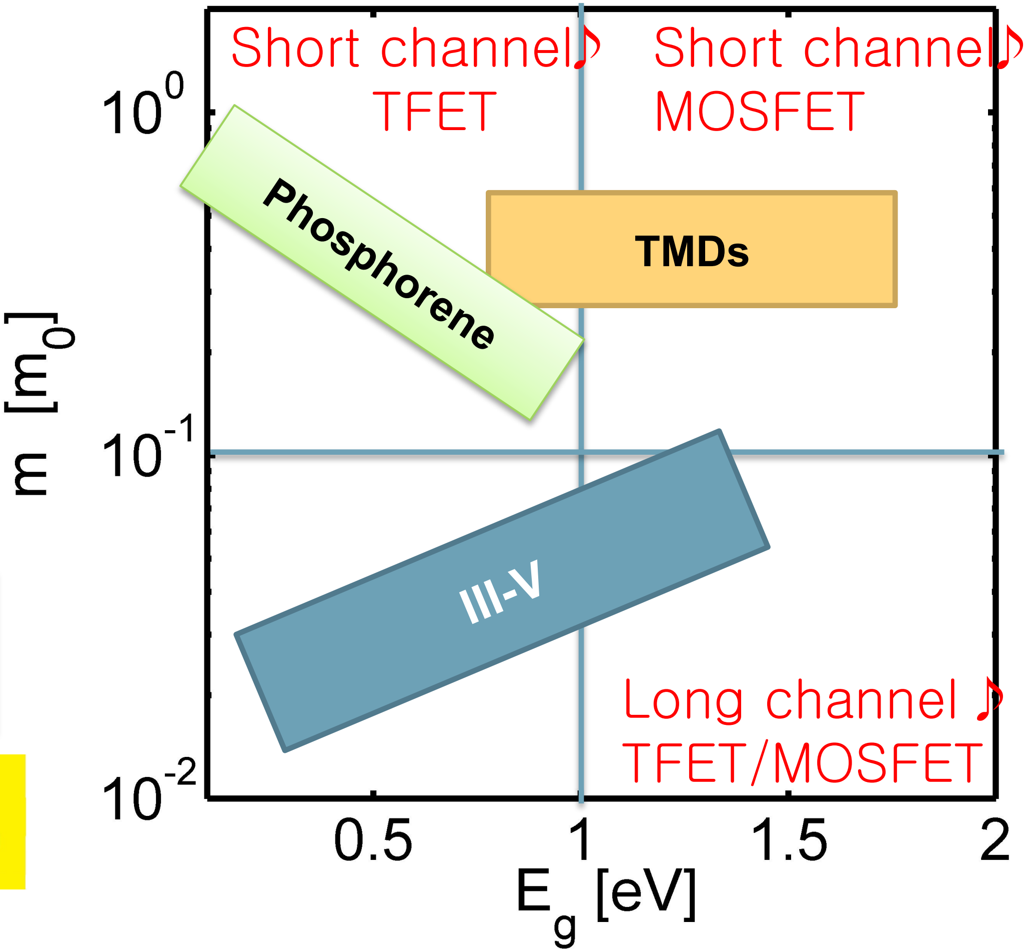
L-gate TFET → L_{ch} scaling



Material properties

L_{ch} determines optimum m*♪

V_{DD} determines optimum E_g♪



Outcome of research

2 patent applications:
DE-TFET and L-gate design

Coauthor of 21 Journal papers:
2 Scientific reports,1 Nano letter, 1 PRB, 11 IEEE, 1 JAP, 1 Phys. B, etc.

Coauthor of 25 conference presentations

Coauthor of 13 conference proceedings

Coauthor of 3 nanohub tools

1 invited talk

…

Acknowledgements

Special thanks to

Professors


Gerhard
Klimeck


Rajib
Rahman


Joerg
Appenzeller


Zhihong
Chen


Supriyo
Datta

Colleagues: Tarek Ameen , Mehdi Salmani, Fan Chen, Archana Tankasala, Saima Sharmin

Bozidar Novakovic, Jun Huang, Arvind Ajoy, Daniel Meija, NEMO5 team

Ramon Salazar, Abhijith Prakash, Tao Chu

Thank you for your attention

PhD Overview

Coding

- Mode-space
- Strain relaxation
- Quantum transport
- Phonon spectra & Unfolding …

Research

- Dielectric engineered TFET
- L-shaped gate TFET
- TMD-TFET
- Optimum material Sub-10nm TFET
- Phosphorene TFET
- Scaling theory of 2D materials
- BLG-TFET
- Analytic models for TFETs
- Nitride TFETs
- Dynamic bandgap FET
- Optimum high-K
- Phonon unfolding method
- Thickness engineered TFET
- Universal strain in quantum dots (QD)
- Optical spectra of self-assembled QDs

Back up slides

Mode-space approach for tight-binding Hamiltonian

J. Huang

I INTRODUCTION

- NEGF challenge → large device dimensions
- Motivation of mode-space approach is to reduce the size of Hamiltonian → speed
- Previously, mode-space approach have been used for effective mass Hamiltonians
- But previous method does not work w/ TB.

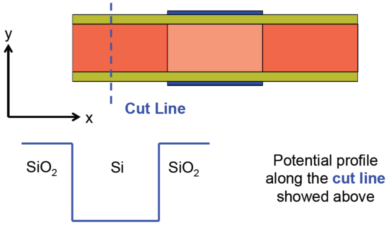
II ACHIVEMENTS

- Generic solver to reduce Hamiltonian size
- Applicable to both electrons and phonons

III RESULTS

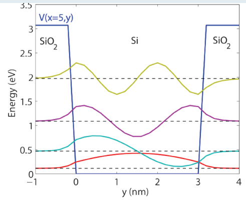
- Milnikov approach is implemented in a generic way.
- Good match between mode-space I-V and real space
- Speed up of 100-1000 were obtained in quantum calculation part.

1 Simulation domain

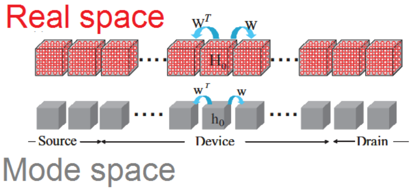


Potential profile along the cut line showed above

2 Propagating modes as basis

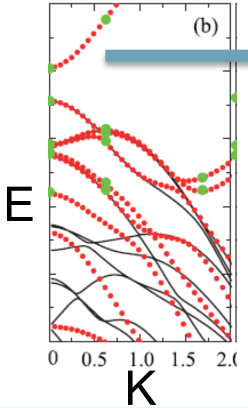


3 Reduce size of Hamiltonian [1]



4 Mode space in TB → Induce unphysical bands [1]

5 Optimization to remove unphysical bands[1]



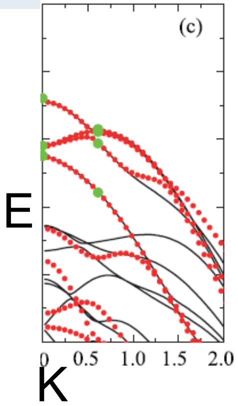
Optimization

1) Count # bands in bandgap

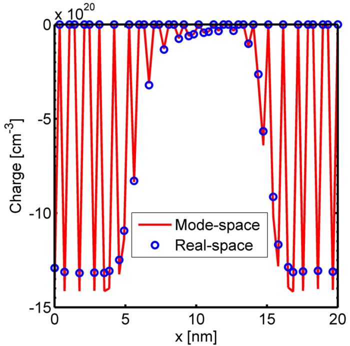
2) Enlarge basis such that # bands in bandgap decrease

Red dots: Mode-space

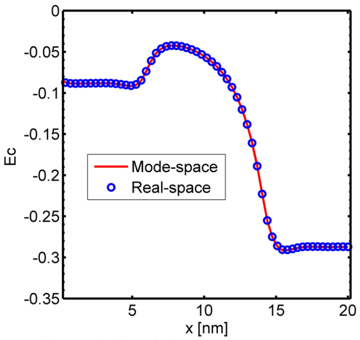
Black line: real-space



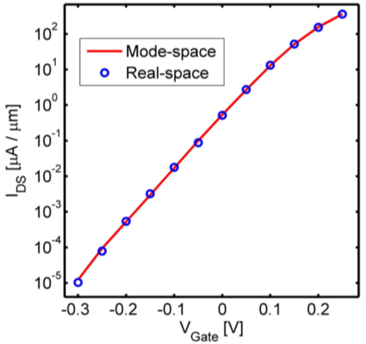
6 Charge



7 SCF potential (Ec)



8 IV



[1] Phys. Rev. B **85**, 035317

Universal Behavior in strain in quantum dots

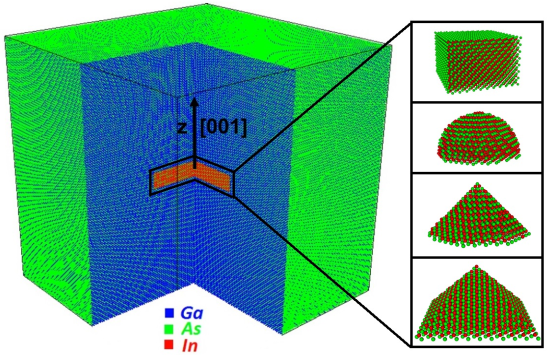
Device: self-assembled quantum dots

Problem:

- Strain distribution affects electronic properties significantly.
- Atomistic strain is too expensive to compute (~ 10M atom sim).
- Analytical strain is inaccurate and exist only for cuboid shape.

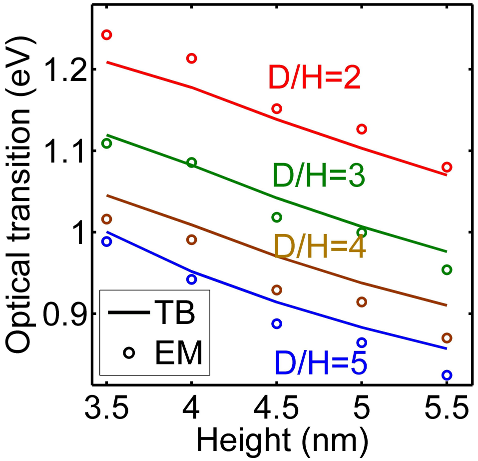
Objective:

- Significantly reduce computations.

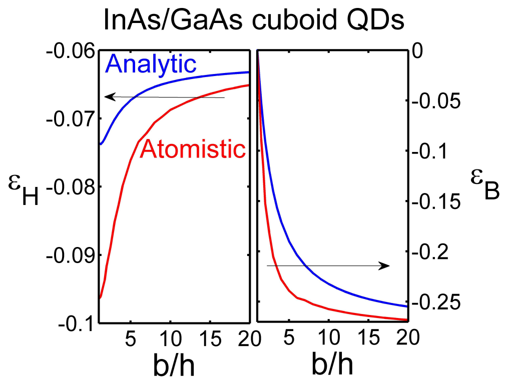


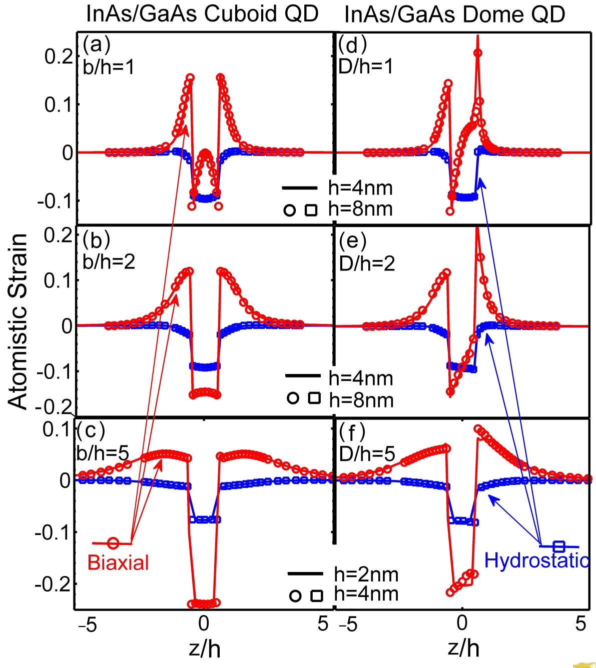
Results / Impact:

- Atomistic strain depends on aspect ratio and materials and not on individual dimensions.
- Fitted compact expressions that provide atomistic strain.
- Compact model (EM) that sacrifices 5% accuracy but cost 20K less computations.



Prior analytic model vs atomistic





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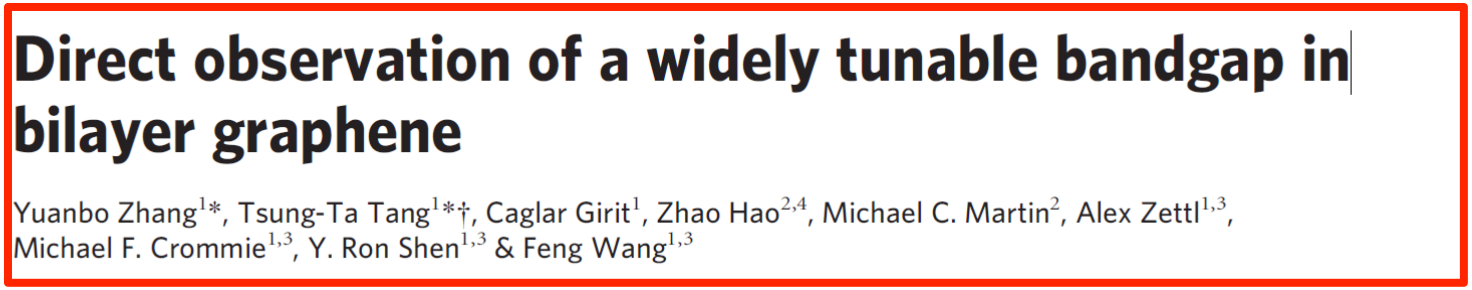
*Ilatikhameneh, H., Ameen, T., Klimeck, G., & Rahman, R. (2015). Universal Behavior of Strain in Quantum DotsIEEE JOURNAL OF QUANTUM ELECTRONICS, VOL. 52, NO. 7, JULY 2016.

Bilayer Graphene (BLG)

The bandgap of bilayer graphene can be tuned by vertical field.

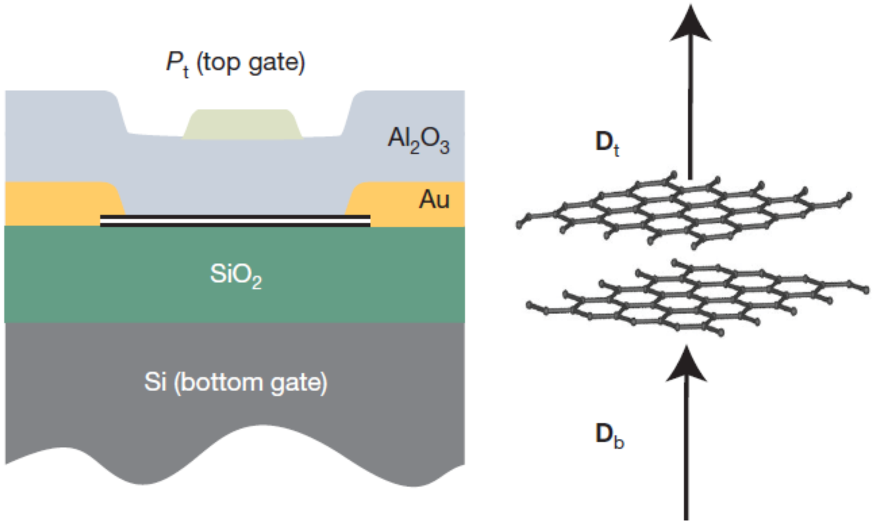
Electrical field determines both bandgap and doping in BLG.



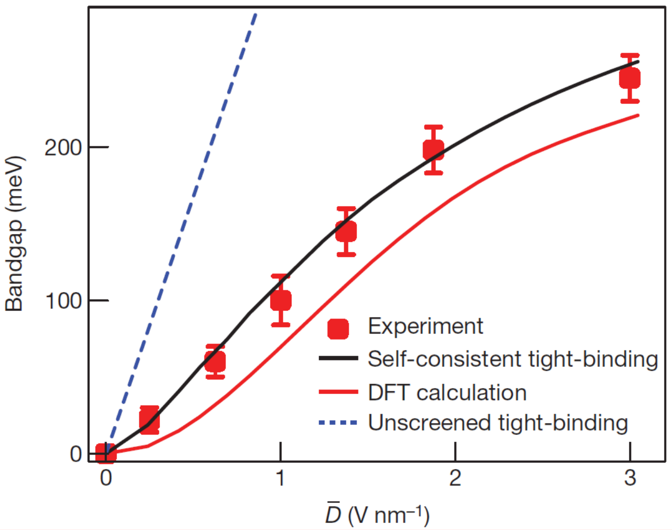
Direct observation of a widely tunable bandgap in bilayer graphene

Yuanbo Zhang[1]*, Tsung-Ta Tang[1]*†, Caglar Girit[1], Zhao Hao[2,4], Michael C. Martin[2], Alex Zettl[1,3], Michael F. Crommie[1,3], Y. Ron Shen[1,3] & Feng Wang[1,3]

Device structure to apply vertical field



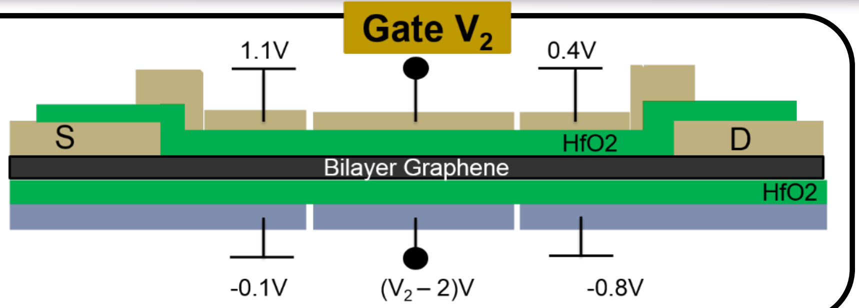
Field controlled bandgap



Bilayer Graphene Tunnel Field-Effect Transistor

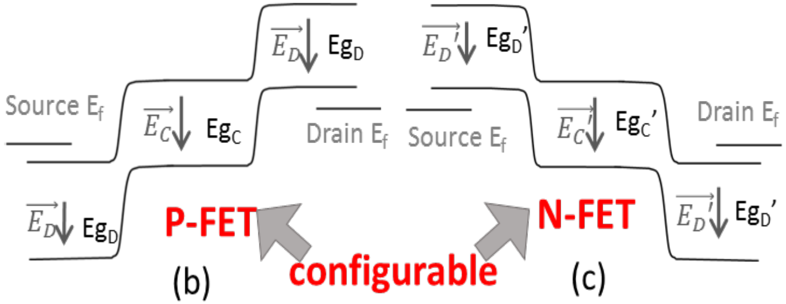
- **Device:**
  - Bilayer graphene Electrostatically Doped TFET (BED-TFET)
- **Target:**
  - Electrostatically Reconfigurable
  - Ultra-low power (VDD=0.1V)

BED-TFET



- **Main idea**
  - Small E_g tuned by electric field → I_{ON}↑
  - Reconfigurable between P- and N-TFET

Idea



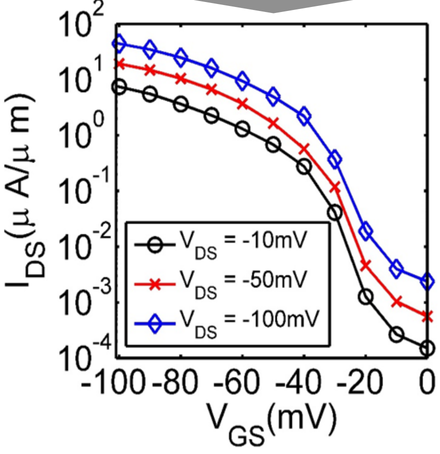
- **Outcome**
  - $I_{ON}/I_{OFF} > 10^4$ for V_{DD} of 0.1V
  - Subthreshold slope: ~8mV/dec
  - High I_{60} > 10 uA/um

[Online.] http://arxiv.org/abs/1509.03593

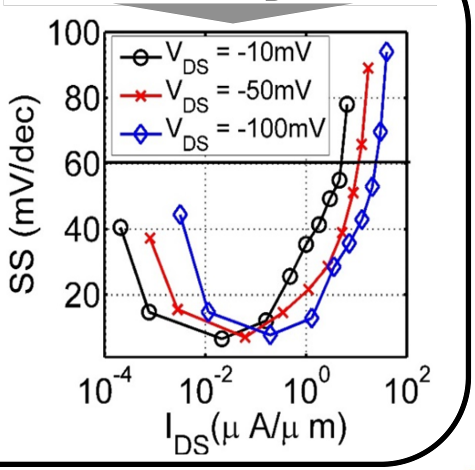
Configurable Electrostatically Doped High Performance Bilayer Graphene Tunnel FET

Fan W. Chen, Hesameddin Ilatikhameneh, Gerhard Klimeck, Zhihong Chen, Rajib Rahman

I_D-V_G



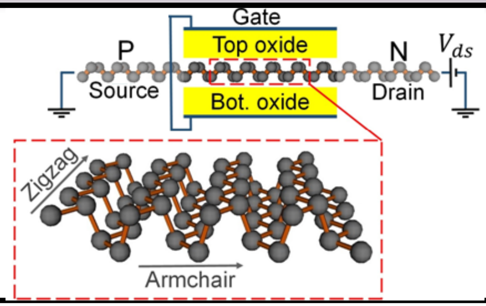
SS-I_D



Phosphorene Tunnel Field-Effect Transistor

- **Device:**
  - Phosphorene Tunnel FET (Ph-TFET)
  - Anisotropic effective mass
- **Target:**
  - High ON-current and small capacitance

Ph-TFET

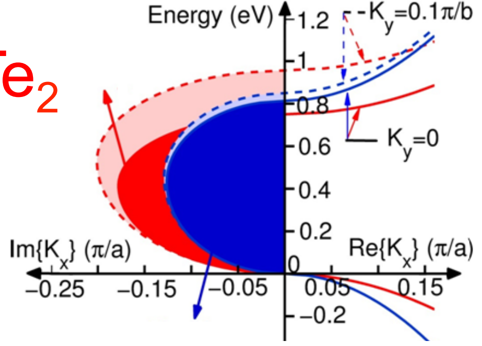


Anisotropic material

- **Main idea**
  - Small transport m* → High tunneling rate
  - large transverse m* → High DOS for injection
  - Tunable E_g from 1.4-0.4eV by flake thickness
- **Methodology**
  - Full band NEGF + 3D Poisson

Idea

WTe_2 vs. Ph



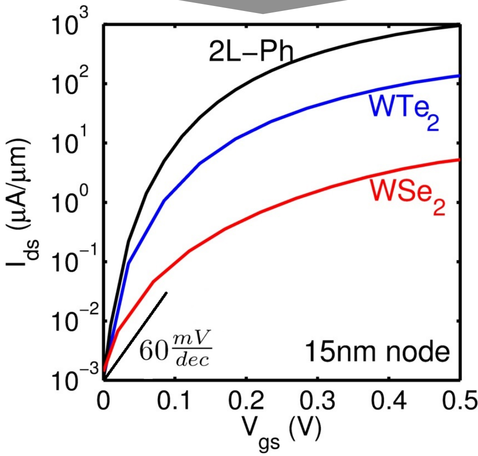
Complex EK

- **Outcome**
  - Max ON-current: ~1000 uA/um
  - Much lower capacitance than TMDs
  - Significant improvement in EDP over TMDs

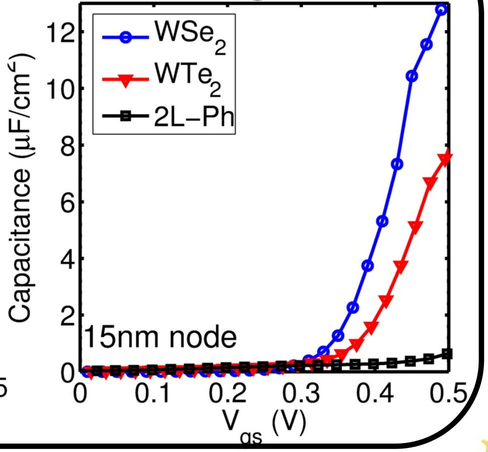
Few-layer Phosphorene: An Ideal 2D Material For Tunnel Transistors

Tarek A. Ameen, Hesameddin Ilatikhameneh, Gerhard Klimeck, Rajib Rahman

I_D-V_G



C-V_G



E-K Equilibrium-NonEQuilibrium Model (EK-EQNEQ)

Devices: Nitride Tunnel Hetero-structures

Problem:

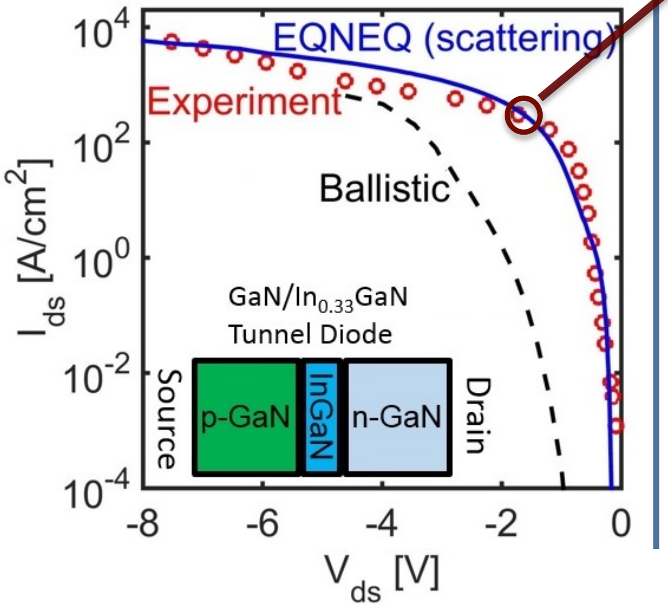
- Barrier is too long to transport ballistic
- Quasi-bound states are not filled ballistic

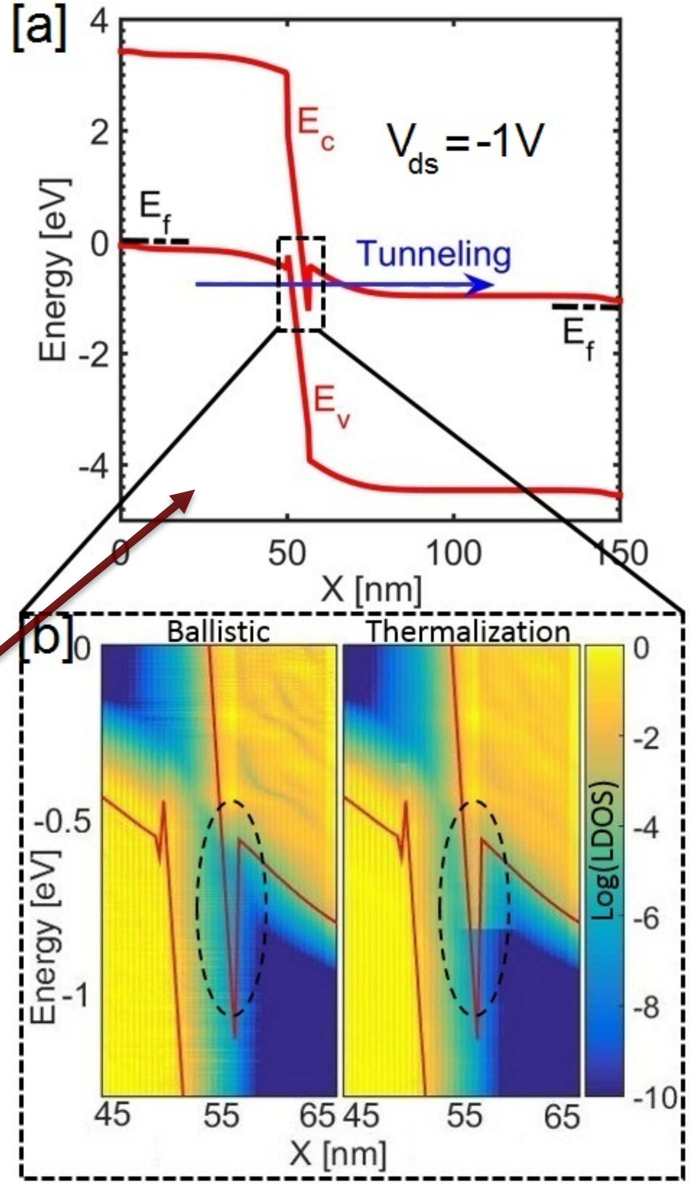
Approach:

- Divide device into two Equilibrium and one None-equilibrium regions.
- Region boundaries depend on E-K band diagrams

Results / Impact:

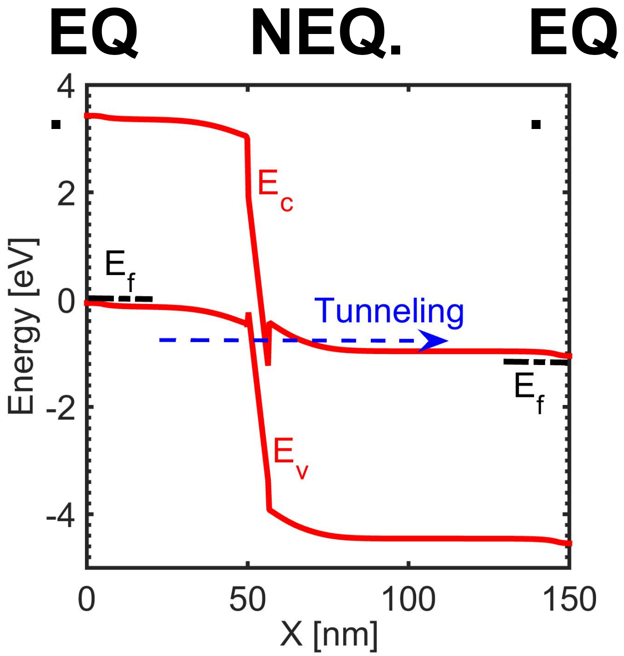
New EQ-NEQ model matches well with measurements of Nitride diodes (Succeeded where ballistic have failed).



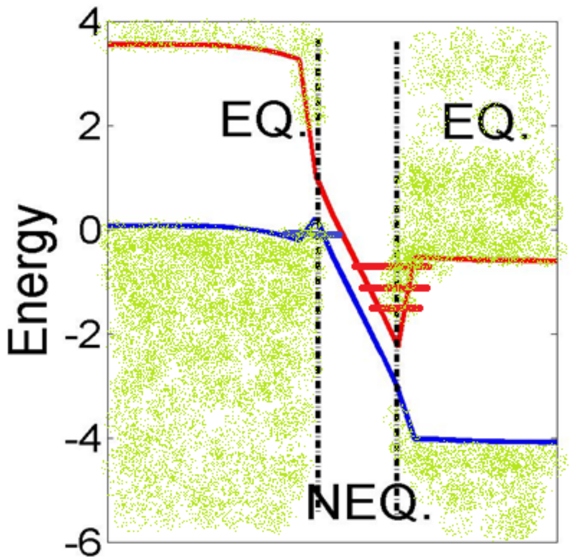


Scattering model

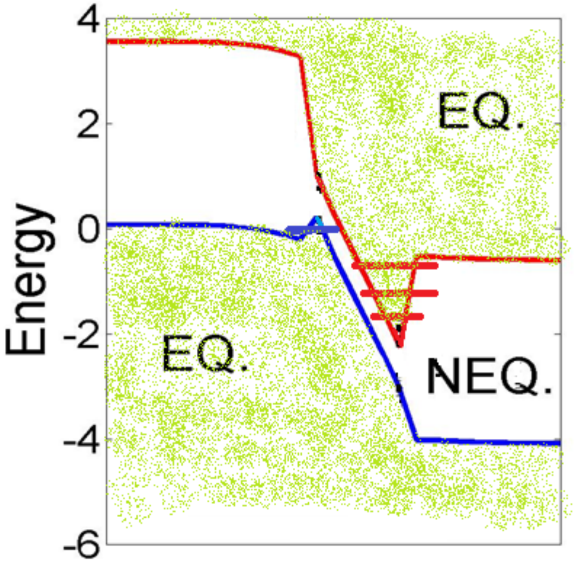
1) Conventional NEGF



2) Old EQ-NEQ model



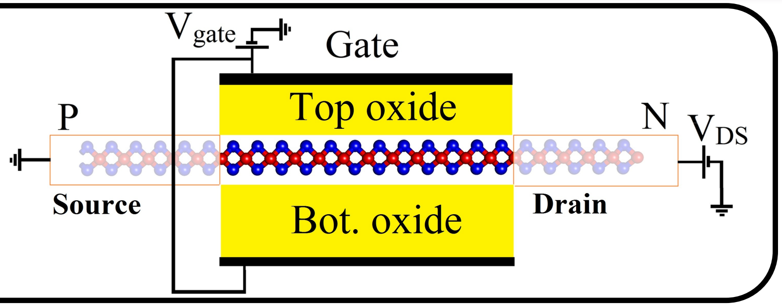
3) New EQ-NEQ model



TMD Tunnel Field-Effect Transistor

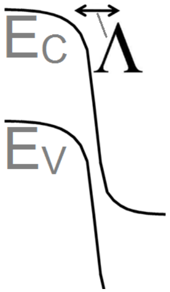
- **Device:**
  - ➢ Transistion Metal Dichalcogenide Tunnel FET (TMD-TFET)
- **Target:**
  - ➢ Higher ON-current and gate control

TMD-TFET



- **Main idea**
  - ➢ Thinner channel → smaller tunneling distance
- **Methodology**
  - ➢ Full band NEGF + 3D Poisson

Idea

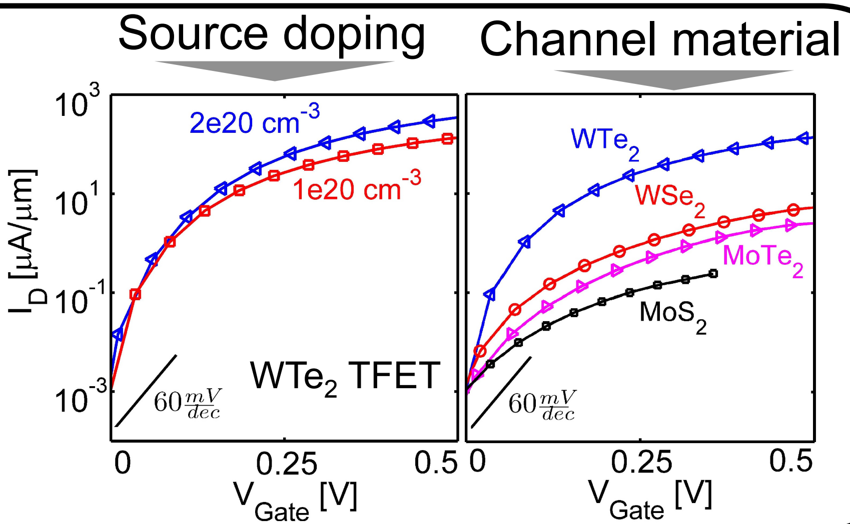


$$t_{ch}\downarrow \Rightarrow \Lambda\downarrow \Rightarrow I_{ON}\uparrow$$

- **Outcome**
  - ➢ Max ON-current: ~350 uA/um
  - ➢ Subthreshold slope: ~15mV/dec
  - ➢ Importance of source doping and low E_g

IEEE JxCDC, vol. 1, pp. 12-18 (2015)

Tunnel Field-Effect Transistors in 2-D Transition Metal Dichalcogenide Materials



TMD Tunnel Field-Effect Transistor

Required high doping levels is experimentally challenging

Max experimental doping level ~ 3e19 cm^{-3}

NANO LETTERS

Letter

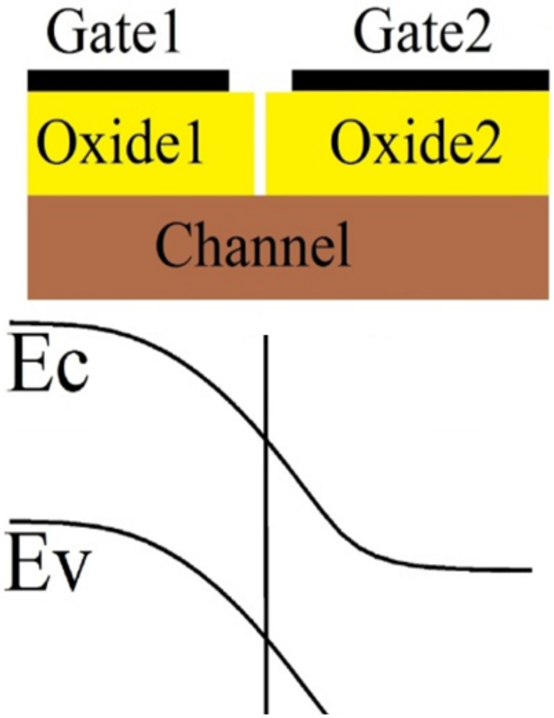
pubs.acs.org/NanoLett

Chloride Molecular Doping Technique on 2D Materials: WS_2 and MoS_2

Lingming Yang,[†] Kausik Majumdar,[‡] Han Liu,[†] Yuchen Du,[†] Heng Wu,[†] Michael Hatzistergos,[§] P. Y. Hung,[‡] Robert Tieckelmann,[‡] Wilman Tsai,[∥] Chris Hobbs,[‡] and Peide D. Ye*[,†]

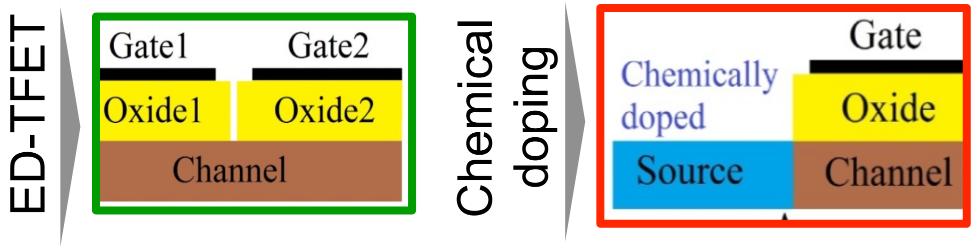
Challenge: N_D=3e19 cm^{-3} → I_{ON} < 0.1 uA/um

Solution: Electrical doping
2 gates to make a PN junction like potential

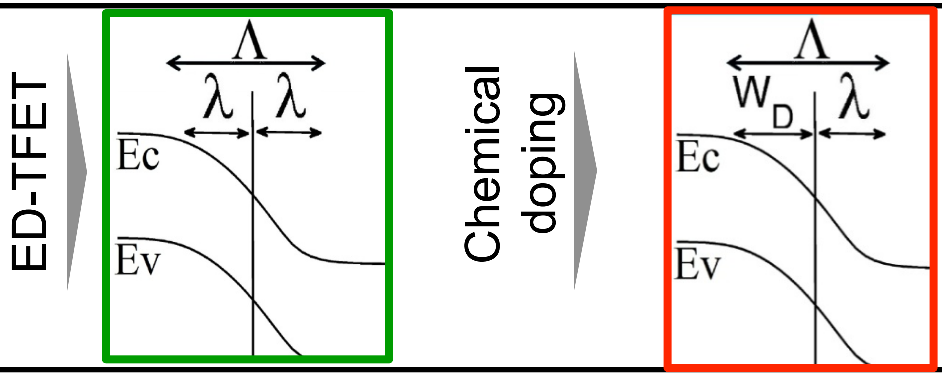


Electrically Doped Tunnel Field-Effect Transistor

- **Device:**
  - Electrically Doped Tunnel FET (ED-TFET)
- **Target:**
  - Avoid high chemical doping at source
  - No dopant fluctuation and gap states



- **Main idea**
  - **$\lambda_{ED\text{-}TFET} = f(t_{ox})$**
  - **$\lambda_{CD\text{-}TFET} = f(EOT)$**
- **Methodology**
  - Analytic verified by full band NEGF + 3D Poisson



- **Outcome**
  - Only t_{ox} matters in 2D ED-TFETs
  - ε_{ox} has no impact due to fringing field

IEEE EDL, vol. 36, n0. 7, pp. 726-729 (2015)

Scaling Theory of Electrically Doped 2D Transistors

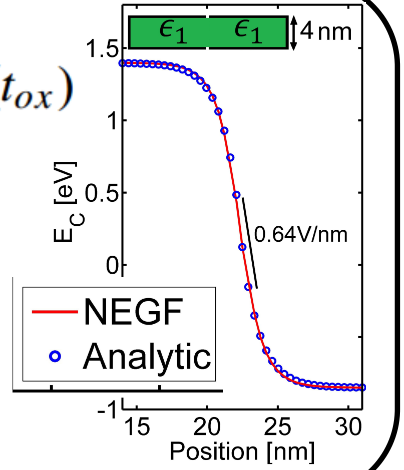
Hesameddin Ilatikhameneh, Gerhard Klimeck, Joerg Appenzeller, and Rajib Rahman

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7111272

$$\lambda_{new} \approx \frac{2t_{ox} + S/4}{\pi} = f(t_{ox})$$

S = spacing btw gates

Analytic: U(x)~exp(-x/λ)



Electrically Doped Tunnel Field-Effect Transistor

ED-TFET require small t_{ox} not high-K→ Gate leakage

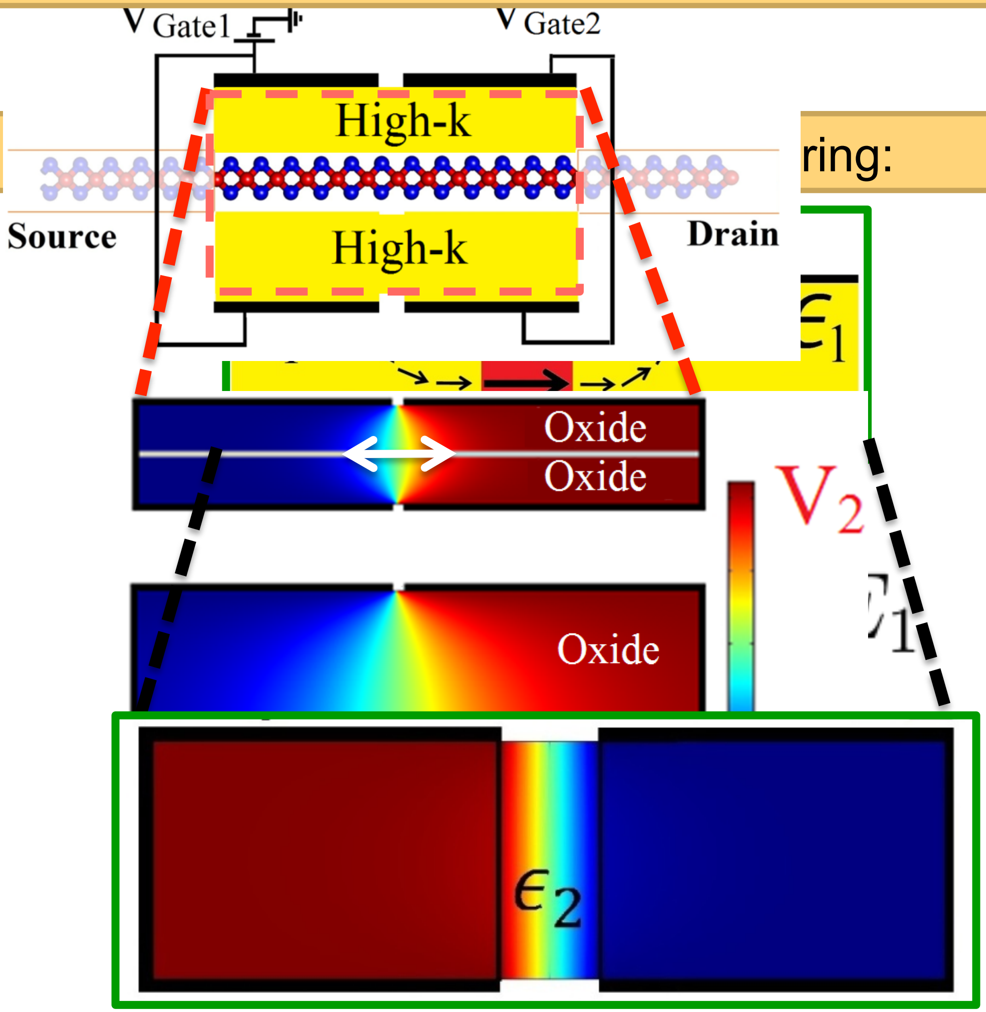
This is due to strong fringing fields between gates.

ring:

Structure

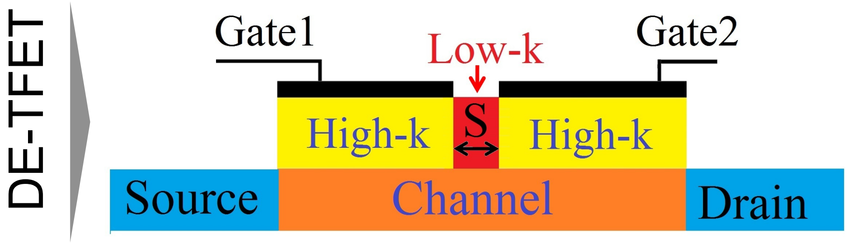
Thin oxide

Thick oxide

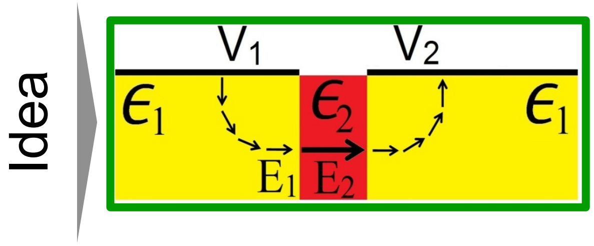


Dielectric Engineered Tunnel Field-Effect Transistor

- **Device:**
  - Dielectric Engineered Tunnel FET (DE-TFET)
- **Target:**
  - High ON-current TFET w/o heterojunction channel.



- **Main idea**
  - Combination of low-k and high-k dielectrics
- **Methodology**
  - Full band NEGF + 3D Poisson



$$\epsilon_1 E_1 = \epsilon_2 E_2$$

$$\epsilon_2 \ll \epsilon_1 \rightarrow E_2 \gg E_1$$

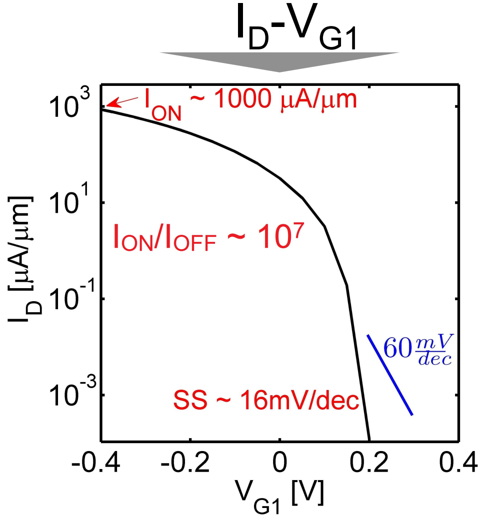
- **Outcome**
  - **High** ON-current: ~1000 uA/um
  - Subthreshold slope: ~15mV/dec
  - Junction electric field: ~1V/nm

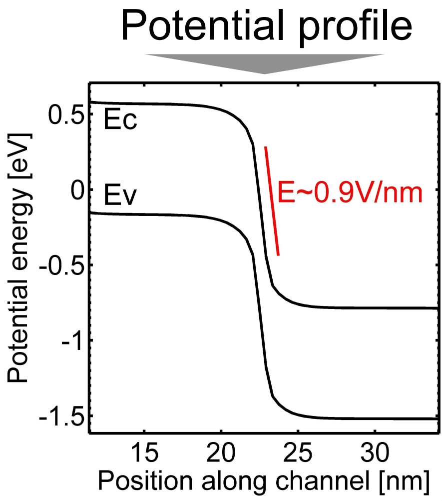
IEEE ELECTRON DEVICE LETTERS, VOL. 36, NO. 10, OCTOBER 2015

Dielectric Engineered Tunnel Field-Effect Transistor

Hesameddin Ilatikhameneh, Tarek A. Ameen, Gerhard Klimeck, Joerg Appenzeller, and Rajib Rahman

http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7229273



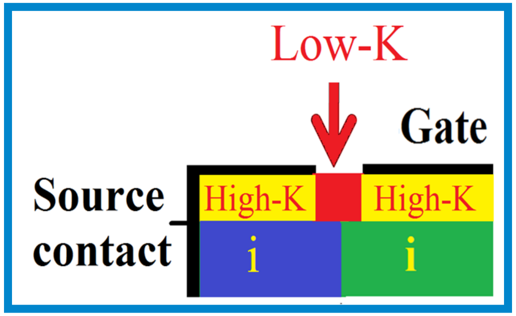


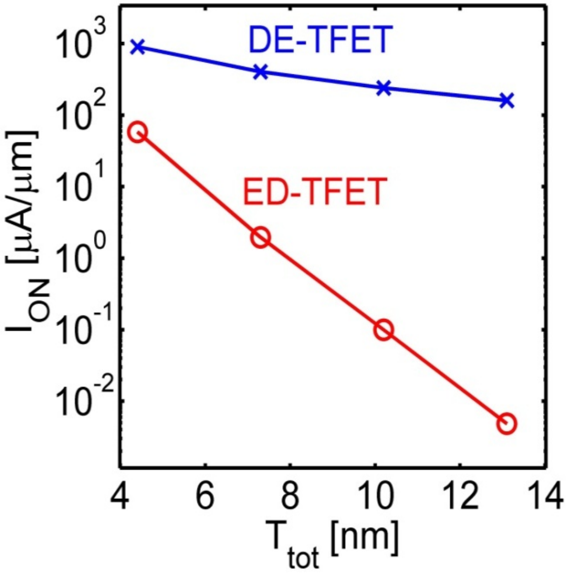
Dielectric Engineered Tunnel Field-Effect Transistor

Advantage of DE-TFET over ED-TFET:

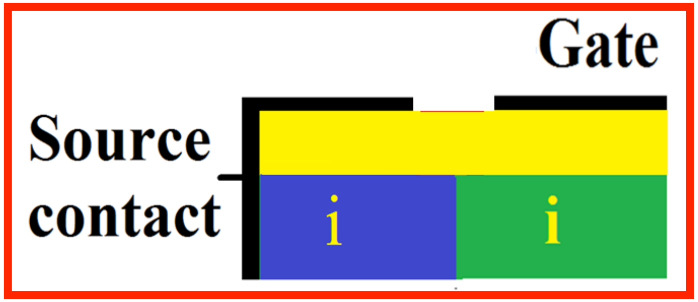
Much less sensitivity on oxide thickness

DE-TFET





ED-TFET

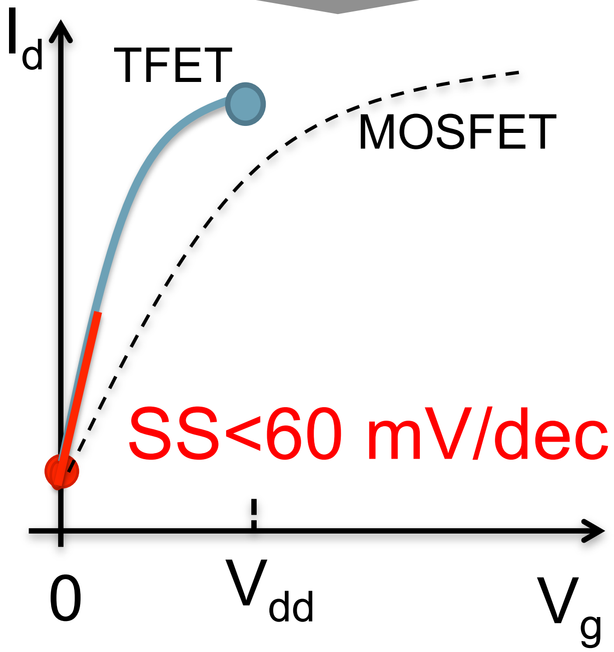


Is it possible to reconfigure btw N-TFET and P-TFET by changing biasing?

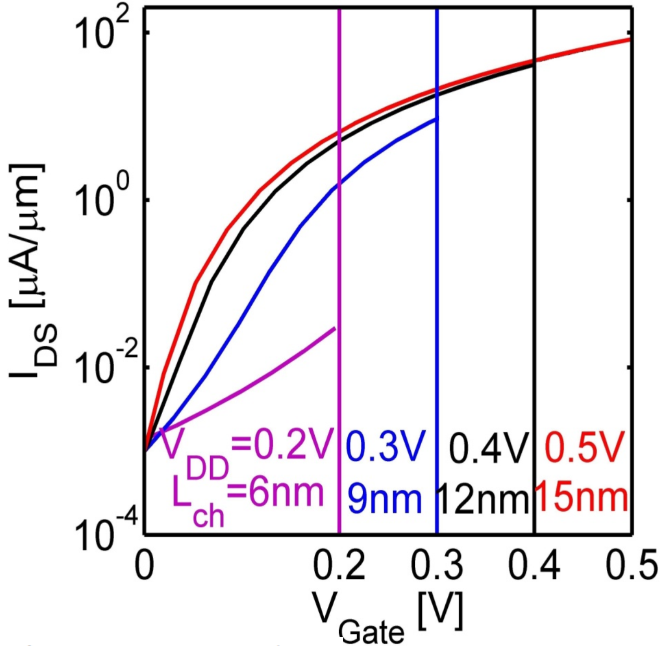
Scaling challenge of TFETs

Goal: Scaling down V_{DD} and L_{ch} simultaneously.

Ideal case



InAs gate-all-around



Can Homojunction Tunnel FETs Scale Below 10 nm?

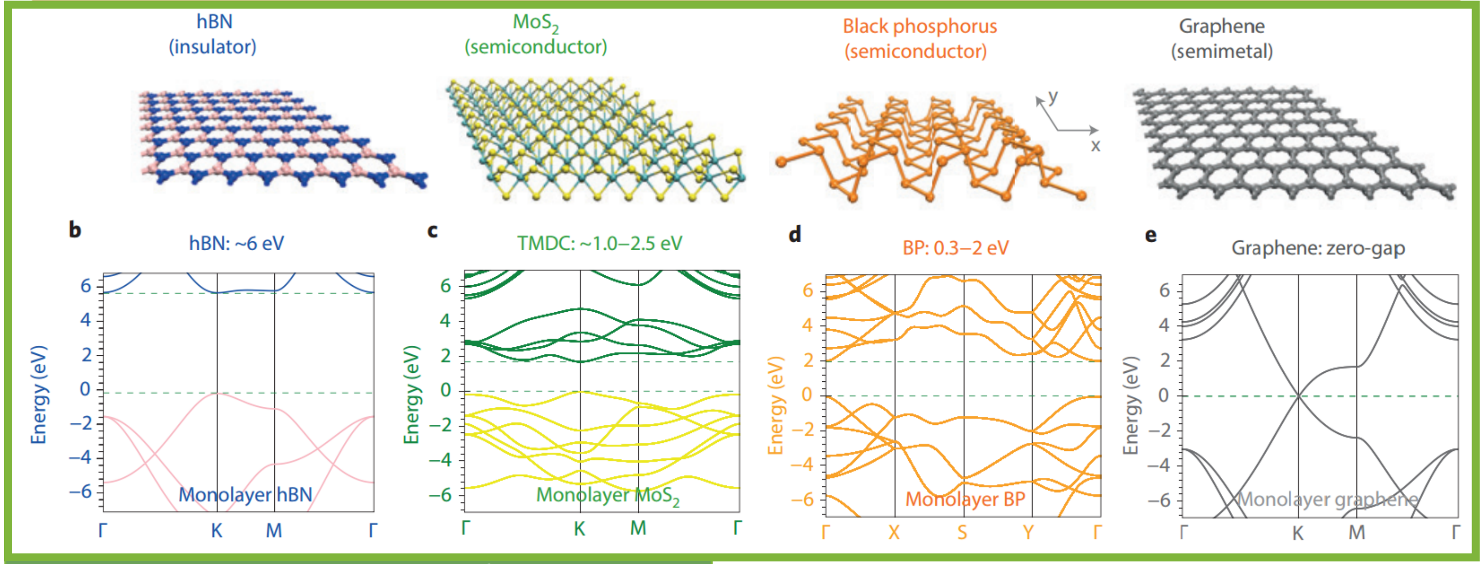
IEEE ELECTRON DEVICE LETTERS, VOL. 37, NO. 1, JANUARY 2016

http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7331599

Scaling down both V_{DD} and L_{ch} deteriorates performance.

Scaling challenge of TFETs

2D material candidates for TFETs with scaled L_{ch} and V_{DD}?




nature photonics

FOCUS | REVIEW ARTICLE

PUBLISHED ONLINE: 27 NOVEMBER 2014 | DOI: 10.1038/NPHOTON.2010.271

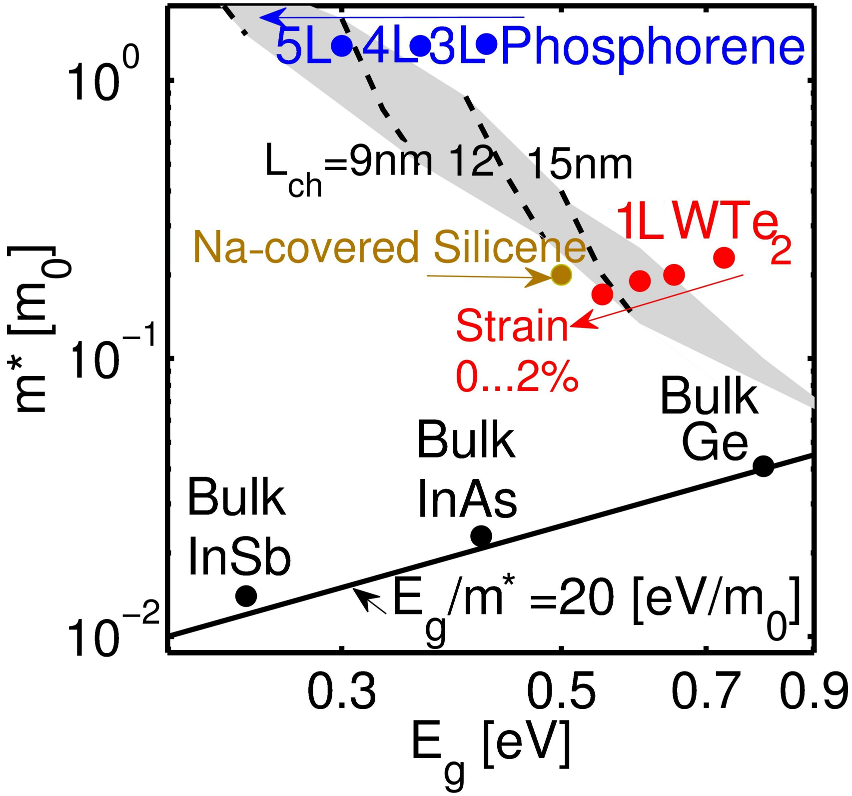
Two-dimensional material nanophotonics

Fengnian Xia[1]*, Han Wang[2], Di Xiao[3], Madan Dubey[4] and Ashwin Ramasubramaniam[5]

Multilayer phosphorene:
- E_g ranges from 1.4eV (1L) to 0.4eV (bulk)
- Smaller E_g and m* compared with TMDs
- Direct bandgap even in multilayer case

Scaling challenge of TFETs

Some materials (gray) can perform with ultra-scaled L_{ch} and V_{DD}



Phosphorene is a good choice.

Can Homojunction Tunnel FETs Scale Below 10 nm?

Hesameddin Ilatikhameneh, Gerhard Klimeck, and Rajib Rahman

IEEE ELECTRON DEVICE LETTERS, VOL. 37, NO. 1, JANUARY 2016

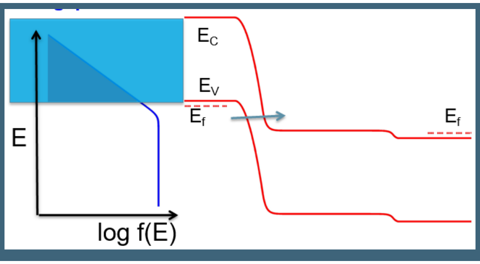
http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7331599

Agenda

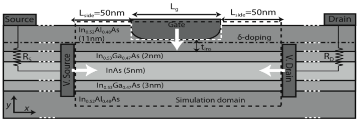
Introduction

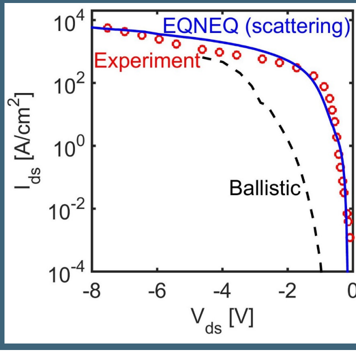
1) Motivation for steep transistors

2) Requirements for steep tunnel transistors



Atomistic quantum transport simulation





1) Device geometry optimization

2) Scattering impact

Homojunction TFET (Small), Heterojunction TFET (Significant)

3) Verify and extend analytic models

a) Fowler-Nordhem, b) WKB

Tunnel transistors

1) III-V materials

2) 2D materials

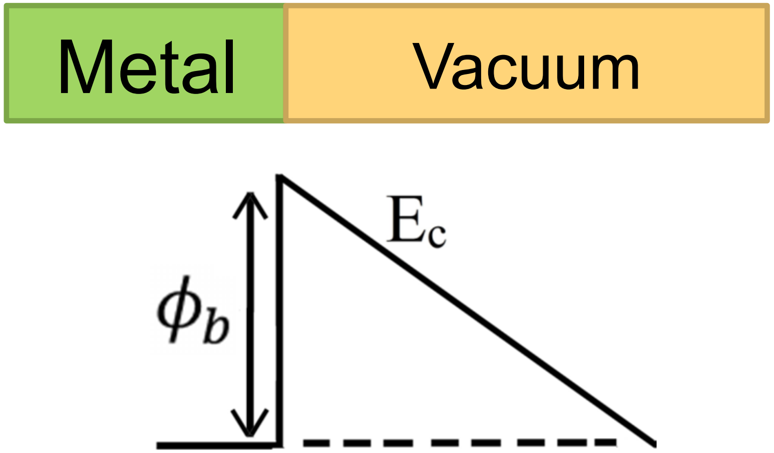
3) Best materials for scaling challenge

Quantum transport: 3) analytic models

1) How good are analytic models?
2) Extending these models for fast & accurate prediction.

A) Fowler-Nordheim

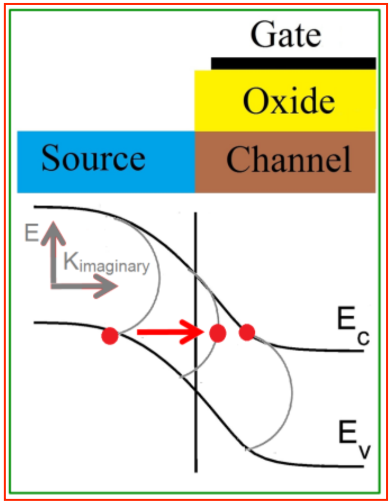
Tunneling from metal due to high electric field



$$T^{FN} = exp\left(-\frac{4}{qF}\frac{\sqrt{2m}\,E_g^{3/2}}{3\hbar}\right)$$

B) WKB

Semiclassical treatment of tunneling



$$T(E) = \exp\left[-2\int dx\,\kappa(x)\right]$$

Quantum transport: 3) analytic models

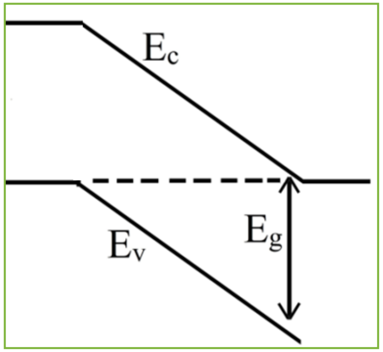
Question: What is the proper definition of tunneling mass m_t ?

Fowler-Nordheim
Tunneling equ.

$$T^{FN} = exp\left(-\frac{4}{qF}\frac{\sqrt{2m}\,E_g^{3/2}}{3\hbar}\right)$$

Tunneling type	**Tunneling mass**

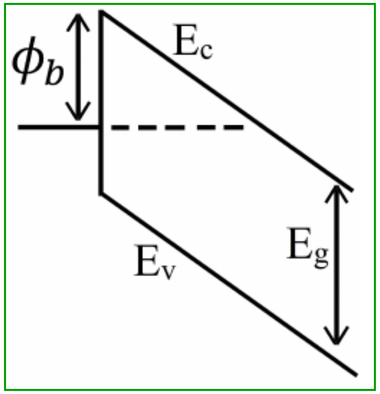
Band to band tunneling



$$m \approx 0.7 m_r^*$$

$$m_r^* = \frac{m_e m_h}{m_e + m_h}$$

Schottky barrier tunneling



$$m_t^* \approx 0.7 m_r^* \left(\frac{\phi_b}{E_g}\right) + m_e^* \left(1 - \frac{\phi_b}{E_g}\right)$$

From Fowler-Nordheim to Non-Equilibrium Green's Function Modeling of Tunneling

Hesameddin Ilatikhemeneh[1*], Ramon B. Salazar[2*], Gerhard Klimeck[1], Rajib Rahman[1], and Joerg Appenzeller[2]

Quantum transport: 3) analytic models

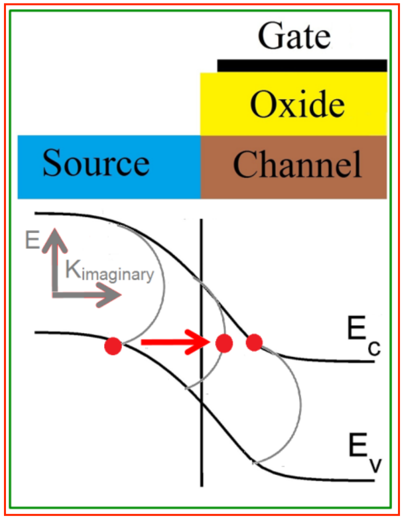
How to make WKB provide results matching atomistic simulations?

WKB

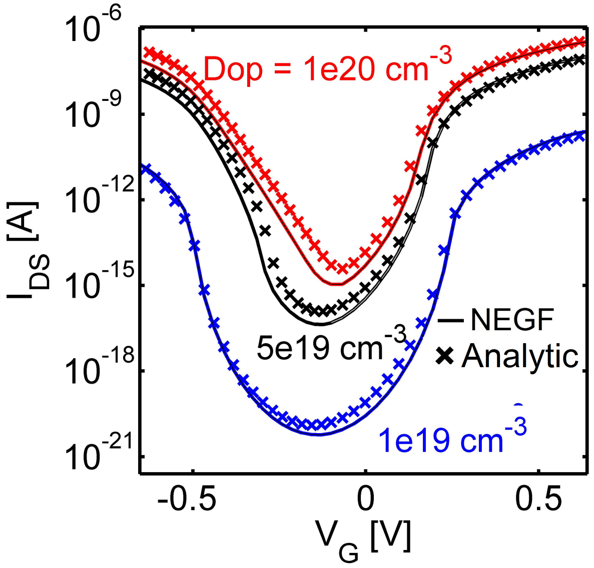
Inputs

1) Complex EK

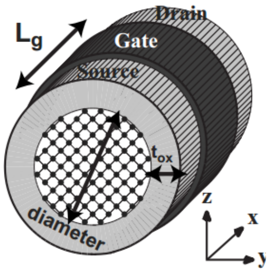
2) Potential Φ(x)



Output



InAs NW



Propose analytic potential → WKB provides close results to NEGF.

JOURNAL OF APPLIED PHYSICS **118**, 164305 (2015)

A predictive analytic model for high-performance tunneling field-effect transistors approaching non-equilibrium Green's function simulations

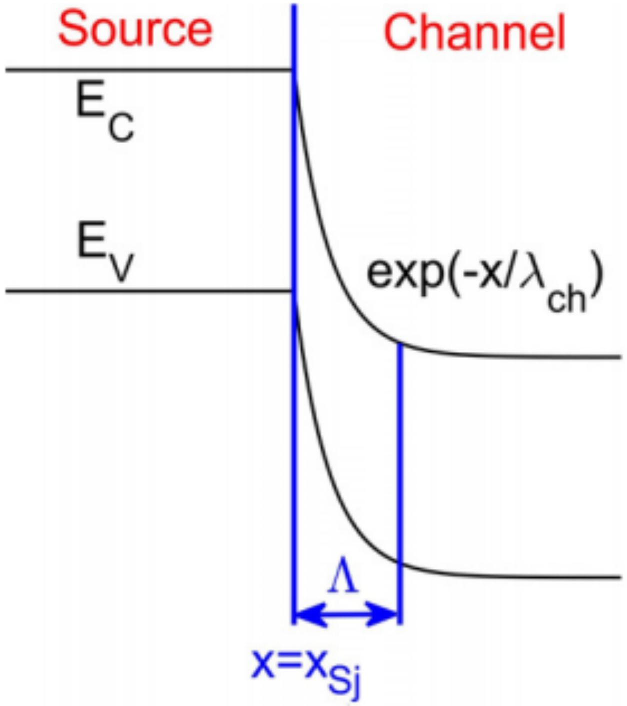
Quantum transport: 3) analytic models

How to make WKB provide results matching atomistic simulations?

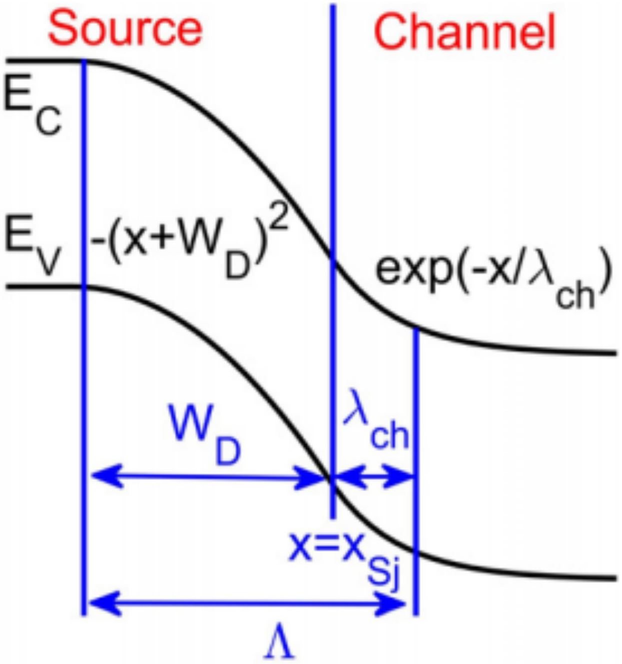
2) Potential $\Phi(x)$

WKB Input: Potential profile

Old potential profile (Wrong)



New potential (Correct)



Depletion width is significant part of tunneling distance

Tunnelfet tool on nanoHUB

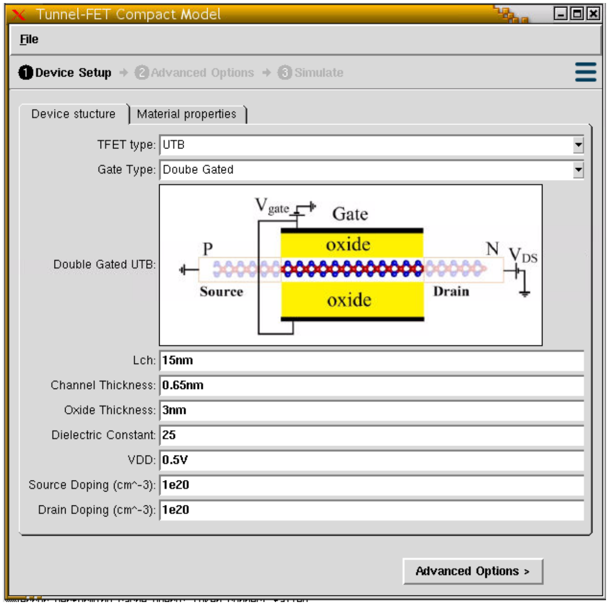
Free online TFET simulation tool

https://nanohub.org/tools/tunnelfet/

Device geometry

Channel material

Outputs



TFET type: UTB

Gate Type: Doube Gated

Double Gated UTB:

Lch: 15nm

Channel Thickness: 0.65nm

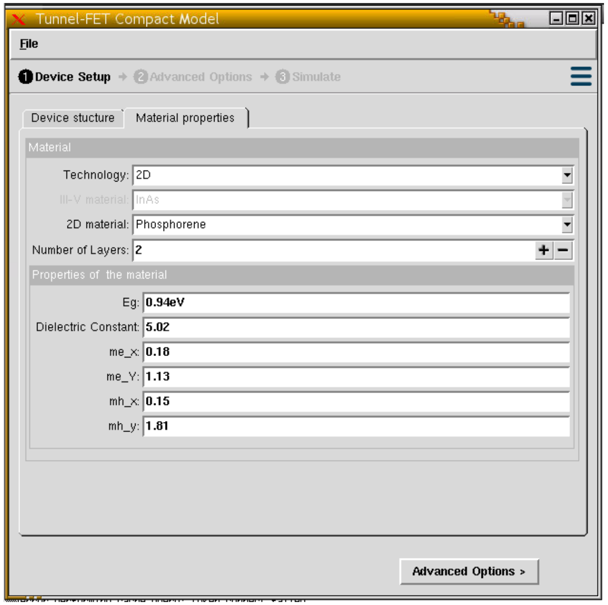
Oxide Thickness: 3nm

Dielectric Constant: 25

VDD: 0.5V

Source Doping (cm^-3): 1e20

Drain Doping (cm^-3): 1e20



Technology: 2D

III-V material: InAs

2D material: Phosphorene

Number of Layers: 2

Eg: 0.94eV

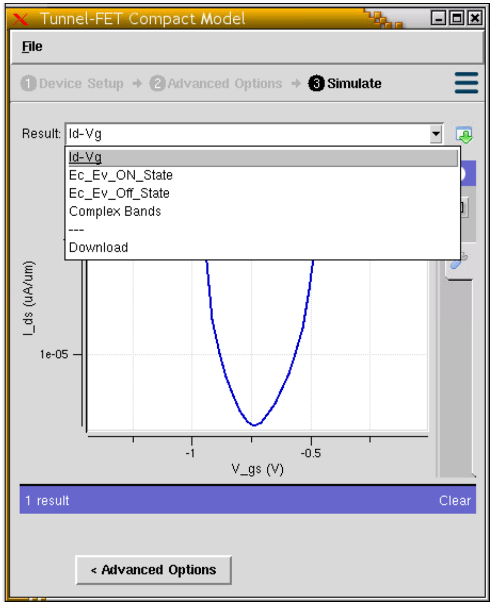
Dielectric Constant: 5.02

me_x: 0.18

me_Y: 1.13

mh_x: 0.15

mh_y: 1.81



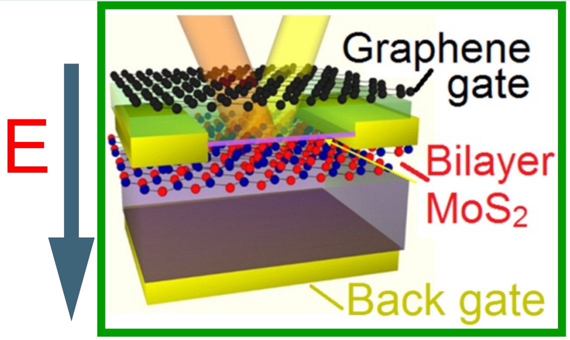
Result: Id-Vg

Steep SS device ideas:
Dynamic bandgap FET

Tao Chu

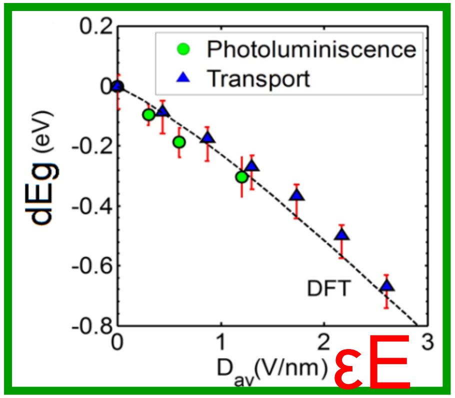
Illustration | **Comments**

Bandgap tuning by E field



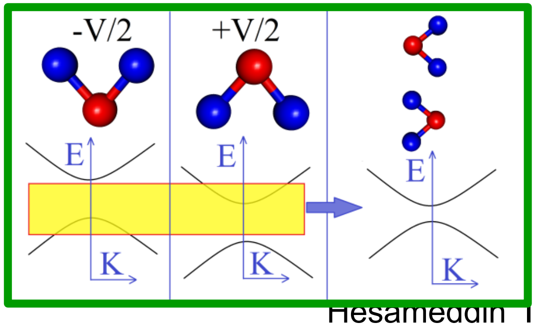
- Top & bottom gates with opposite voltages → E field

Bandgap change



- Increase in electric field → Decrease in Eg

Reason



- Potential difference between 2 layers → band gap change

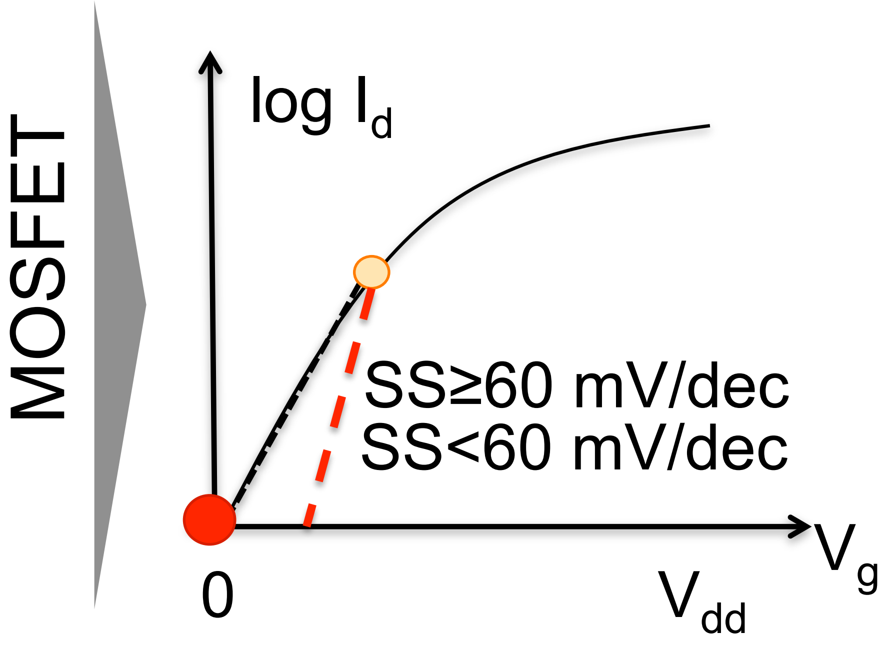
Steep SS device ideas:
Dynamic bandgap FET

Can we use dynamic band gap to make **MOSFETs** steeper?

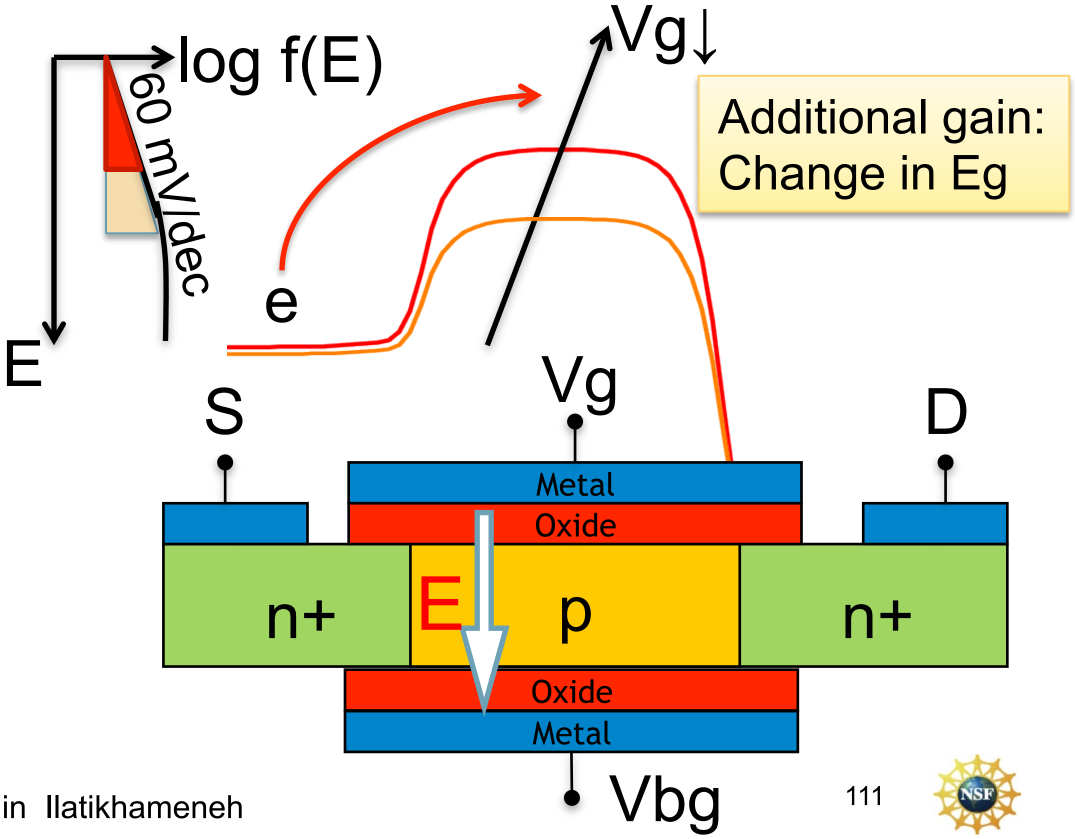
Prof. Chen
Prof. Appenzeller

It seems possible

I_d-V_g



Operation

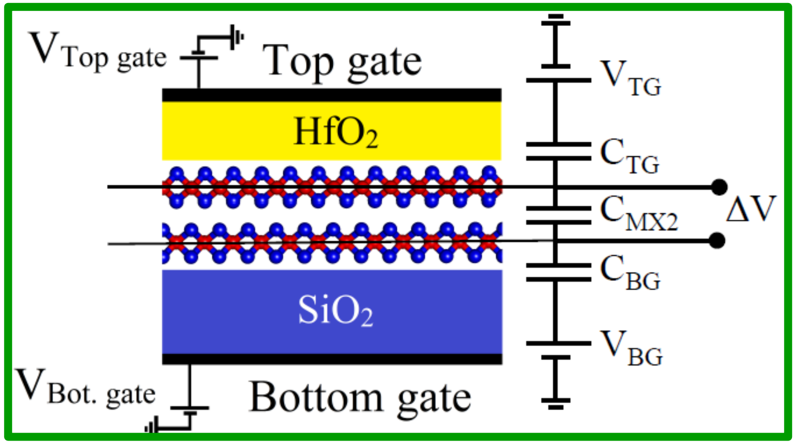


Steep SS device ideas:
Dynamic bandgap FET

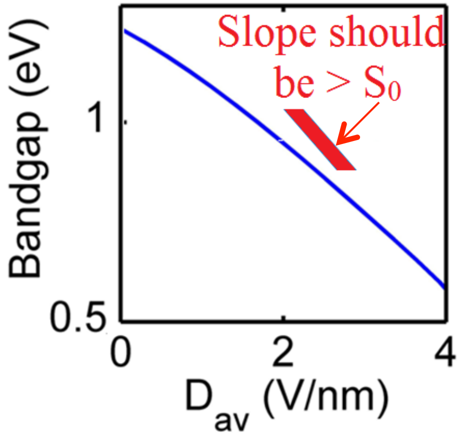
Can we use dynamic band gap to make device steeper?

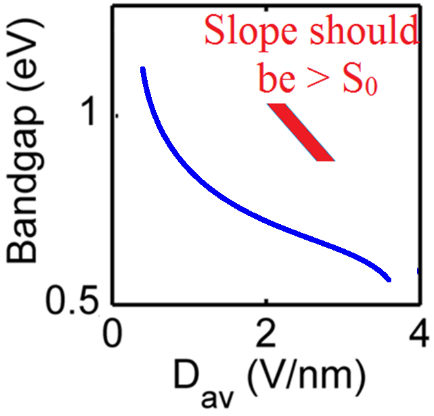
- Only if the rate of change in band gap is high enough.
- This condition is not satisfied in BLG and TMDs

Structure



Bandgap modulation of Bilayer MoS_2

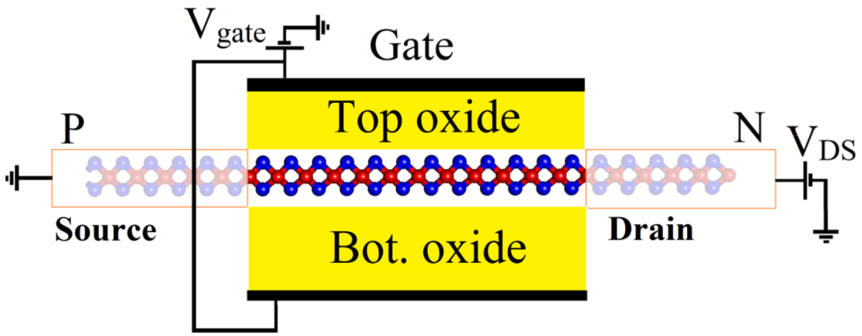




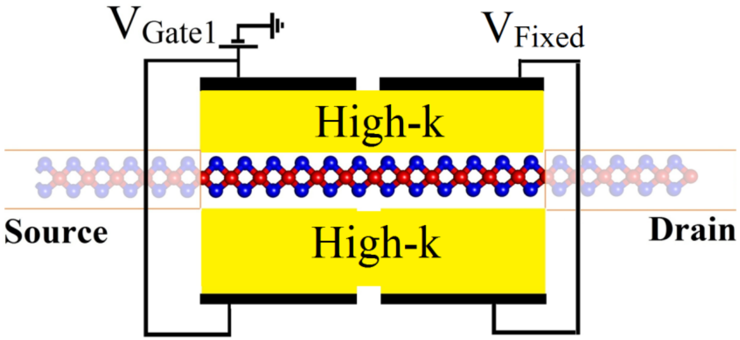
Energy conservation
→ Impossible Slope > S_0

Expectations from electrically doped TFETs

1) Chemically doped



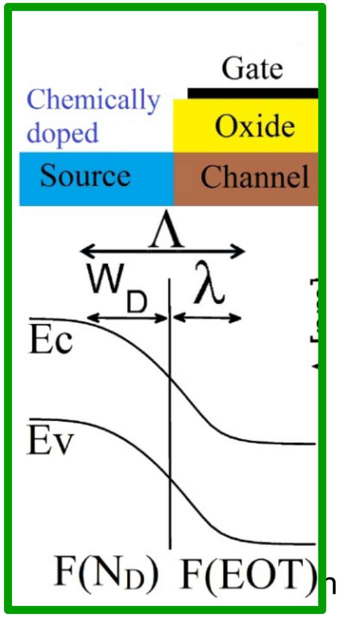
2) Electrically doped



Performance analysis

a) $\lambda = f(\textbf{EOT} \propto t_{ox}/\varepsilon_{ox})$

b) $W_D = f(N_D)$

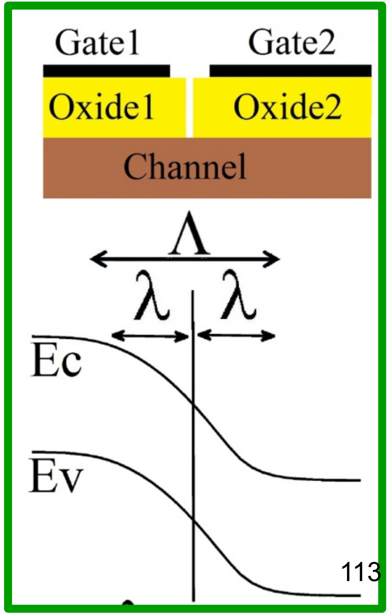


Advantage:
Increase ε_{ox} without reducing t_{ox} → better performance

Prediction:

a) $\lambda = f(\textbf{EOT})$ **?**

✗



Electrically Doped TFET (ED-TFET)

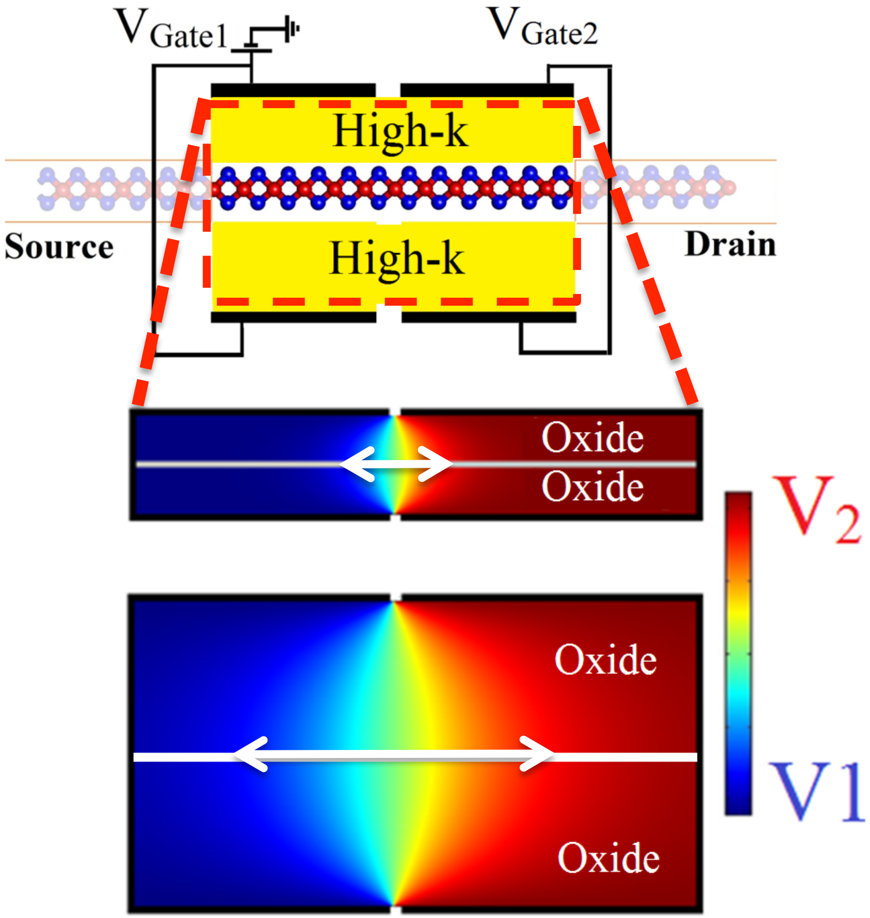
Potential profile

Comment

Structure

Thin oxide

Thick oxide



- **Width of potential spread ~ T_{tot}**

→ Thicker oxides have larger potential spread

Oxide thickness is the major factor

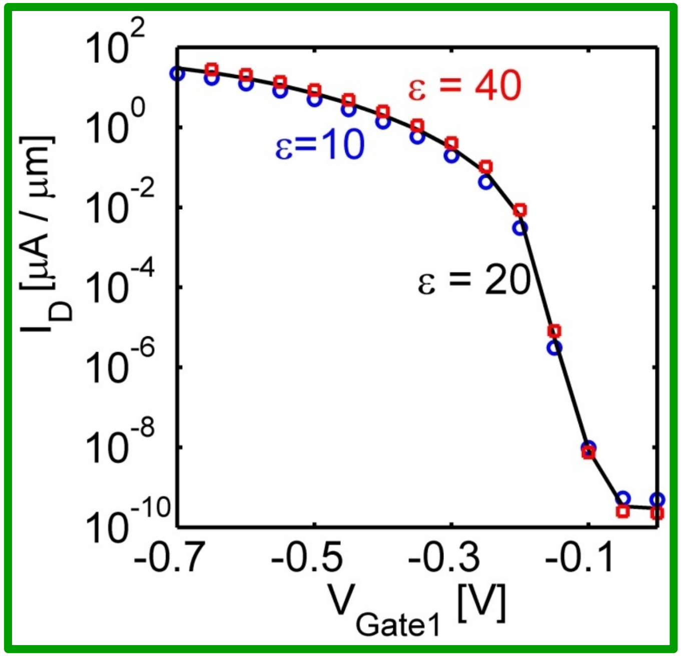
Electrically doped TFETs

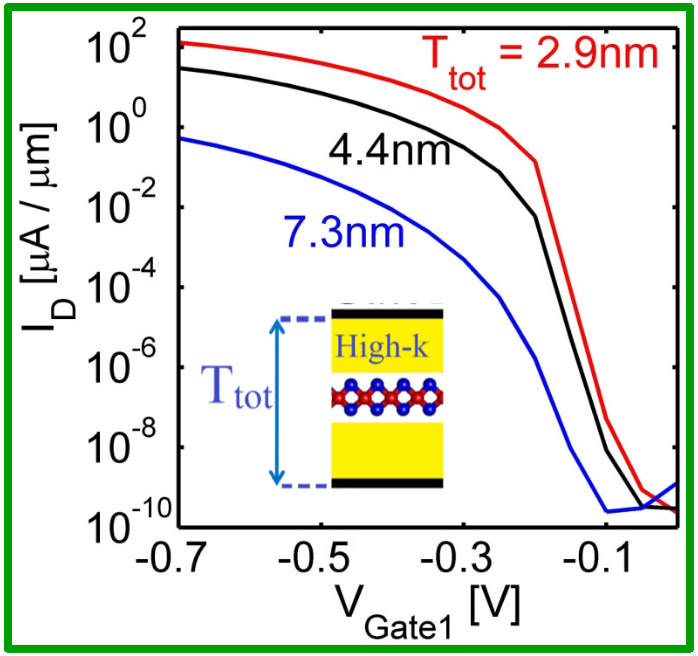
ε_{ox} versus thickness of oxide

Oxide thickness is the major factor

Oxide ε | **Oxide thickness**

Illustration





Comments

- Independence of performance from oxide ε
- Strong dependence of performance on oxide thickness

SISPAD 2015

Electrically Doped WTe_2 Tunnel Transistors

Hesameddin Ilatikhameneh, Rajib Rahman, Joerg Appenzeller, and Gerhard Klimeck

Electrically doped TFETs
Scaling theory

- $\lambda \cancel{=} f(EOT \propto t_{ox}/\varepsilon_{ox})$

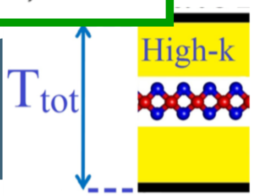
- **Old scaling theory fails**
- **Need a new scaling theory**

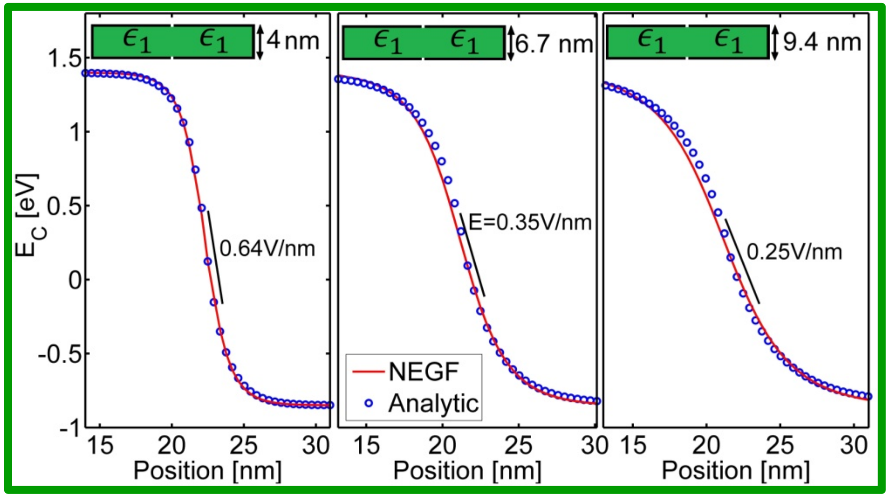
ED-TFET:
Analytic modeling

Potential profile

$$V(x) = \frac{V_1 - V_2}{2} exp\left(-\frac{(x - x_M)}{\lambda_{new}}\right) + V_2$$

Thin oxide…… to thick oxides





Scaling theory

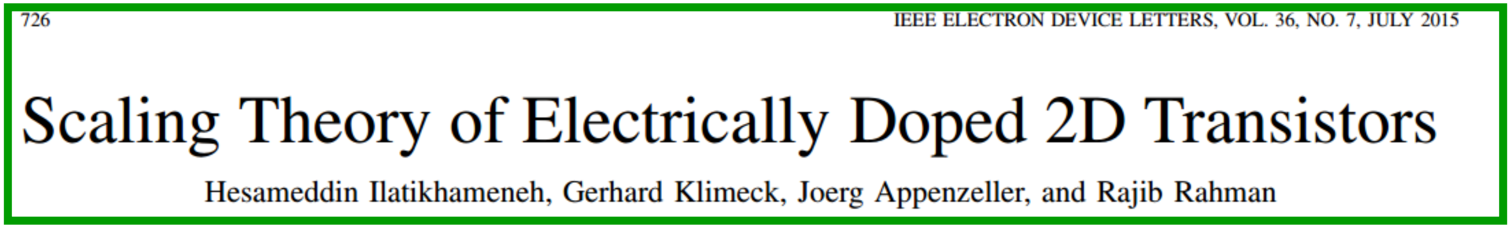
Electrically doped TFETs (New)

$$\lambda_{new} \approx \frac{2t_{ox}}{\pi} = f(t_{ox})$$

Chemically doped TFETs (Old)

$$\lambda_{old} \approx \sqrt{\frac{1}{2}\frac{t_{ox}}{\epsilon_{ox}}\epsilon_{ch}t_{ch}} = f(EOT \propto \frac{t_{ox}}{\epsilon_{ox}})$$

Analytic model confirms: oxide thickness is major factor



726 IEEE ELECTRON DEVICE LETTERS, VOL. 36, NO. 7, JULY 2015

Scaling Theory of Electrically Doped 2D Transistors

Hesameddin Ilatikhameneh, Gerhard Klimeck, Joerg Appenzeller, and Rajib Rahman

Challenges and solutions of steep devices

1) III-V materials

2) 2D materials

Electrically tuned bandgap TFETs

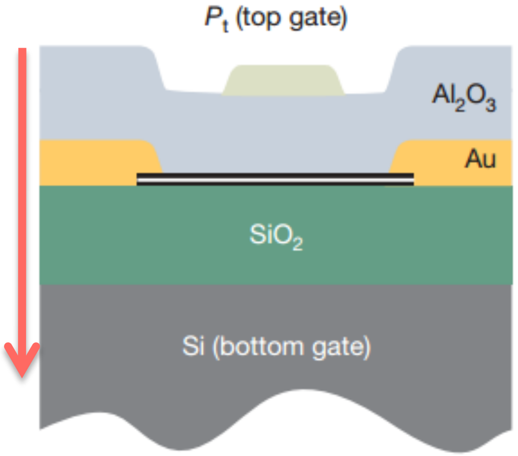
3) Scaling challenge

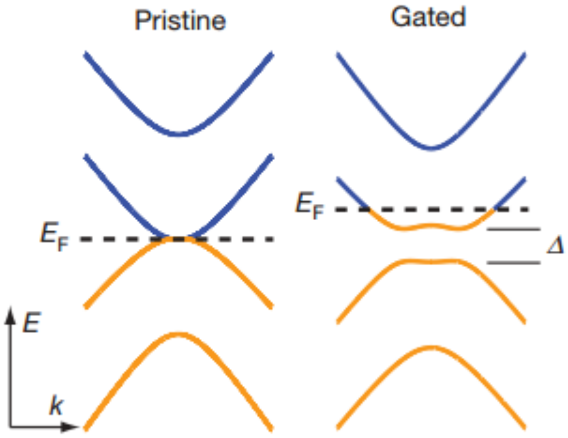
Tunable bandgaps in 2D materials

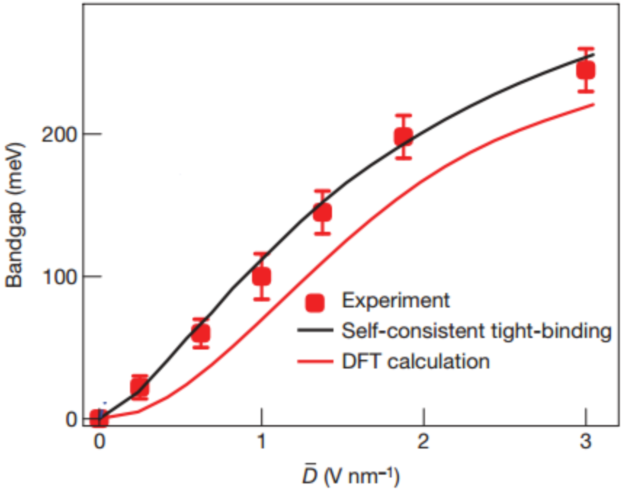
Vertical field changes the bandgap of 2D materials

Direct observation of a widely tunable bandgap in bilayer graphene

Bilayer graphene

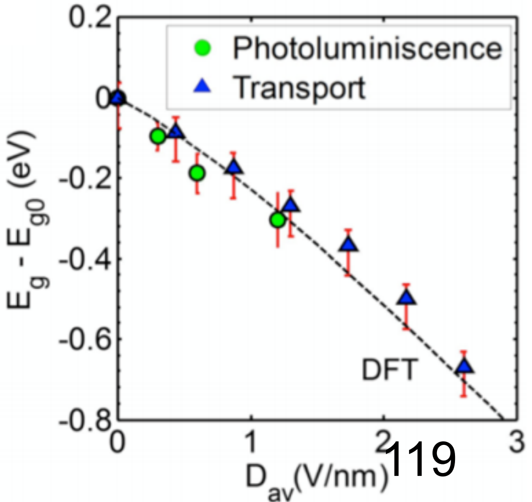






Electrically Tunable Bandgaps in Bilayer MoS_2

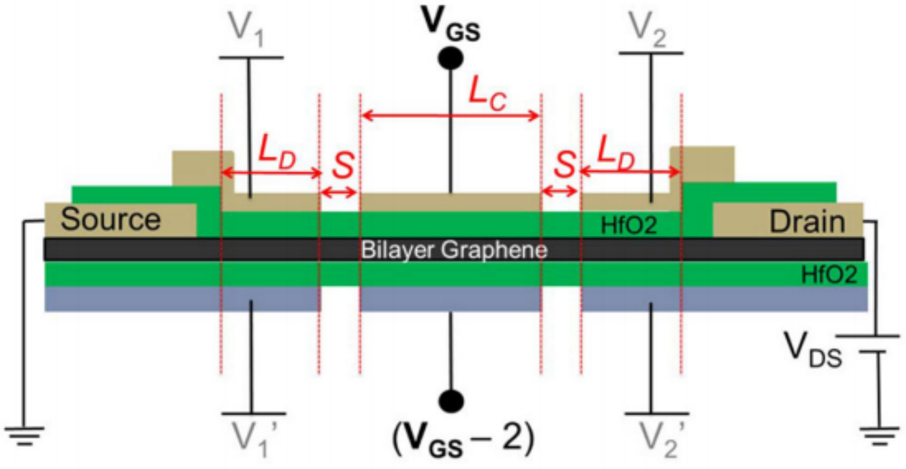
Bilayer TMD

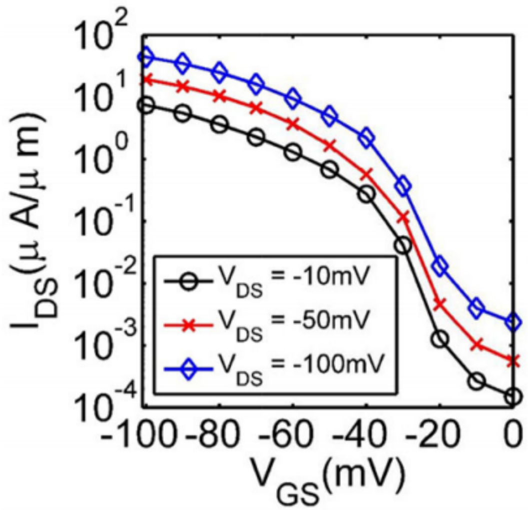


DOI: 10.1021/acs.nanolett.5b03218
Nano Lett. 2015, 15, 8000–8007

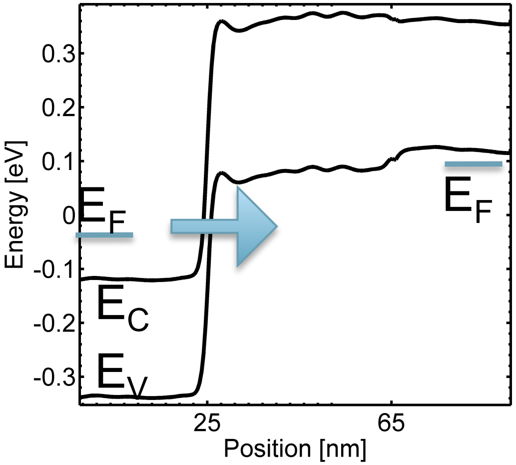
Bilayer Graphene TFET

Vertical field changes the bandgap of 2D materials

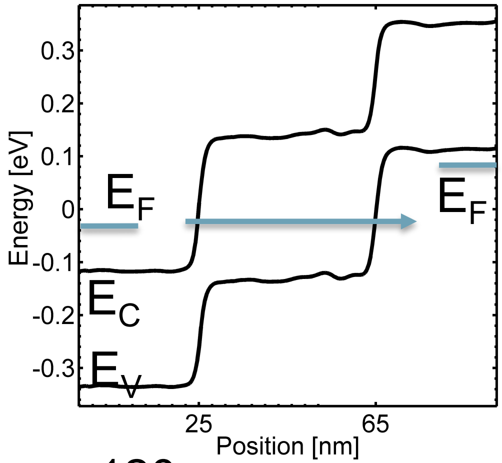


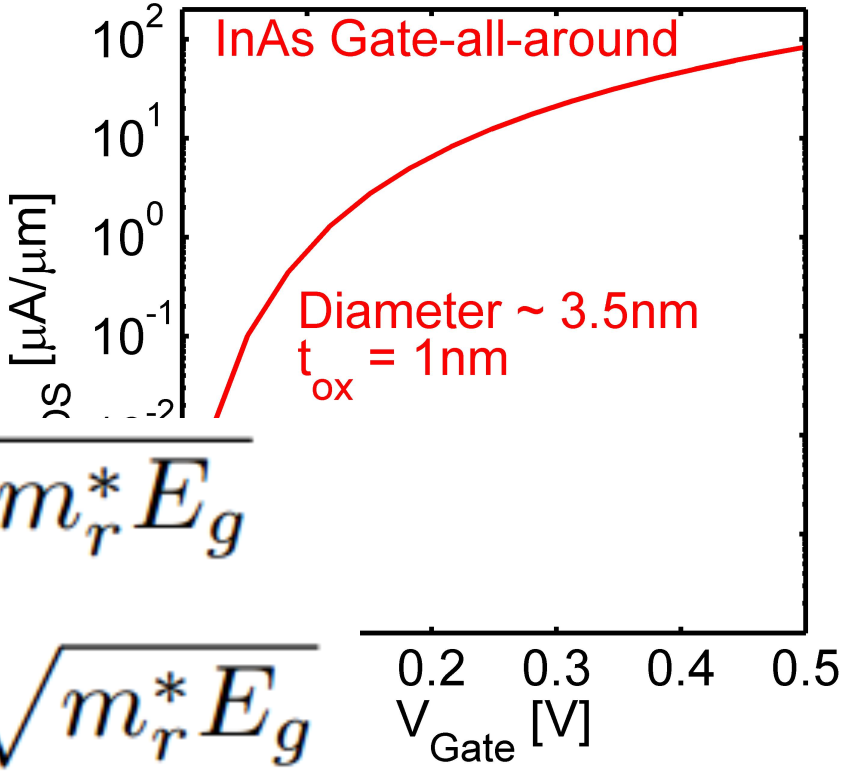


ON-state



OFF-state





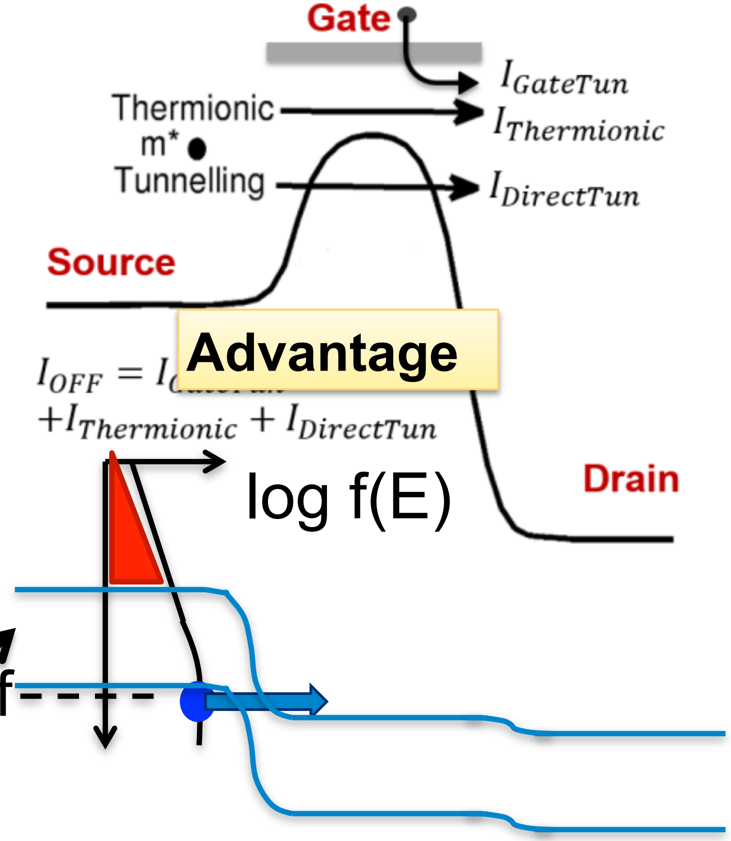
$$log(T_{\mathrm{ON}}) \propto \Lambda\sqrt{m_r^* E_g}$$

$$log(T_{\mathrm{OFF}}) \propto L_{ch}\sqrt{m_r^* E_g}$$

Scaling transistors

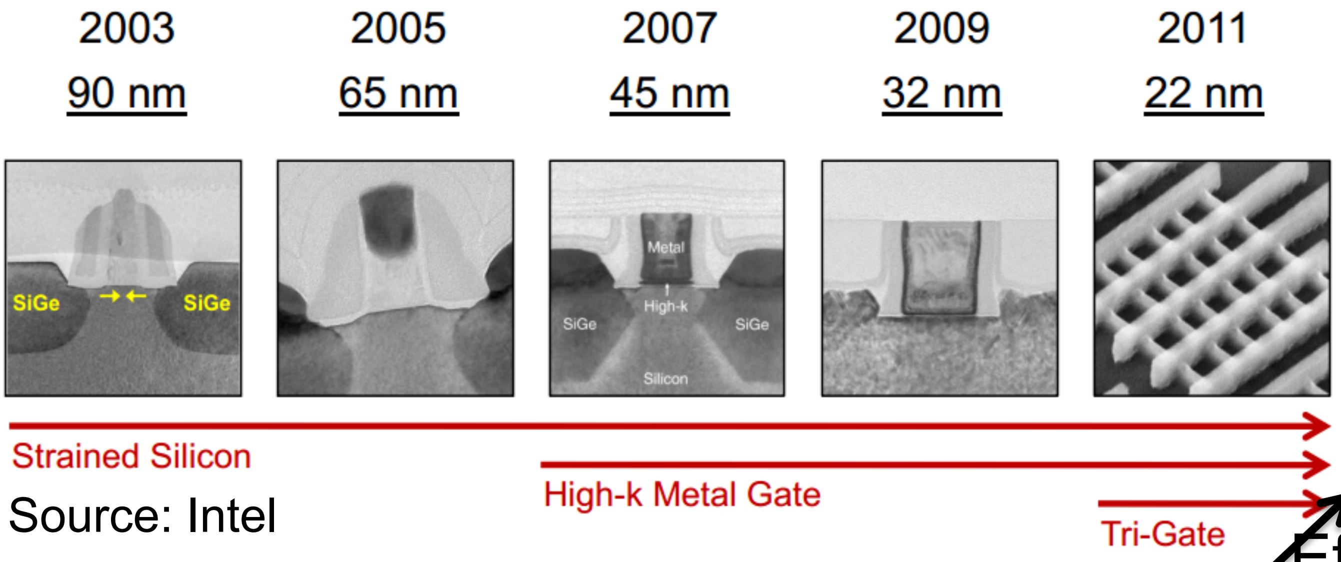
Quantum tunneling era

Drawback



Advantage

$I_{OFF} = I_{GateTun}$
$+I_{Thermionic} + I_{DirectTun}$



Source: Intel

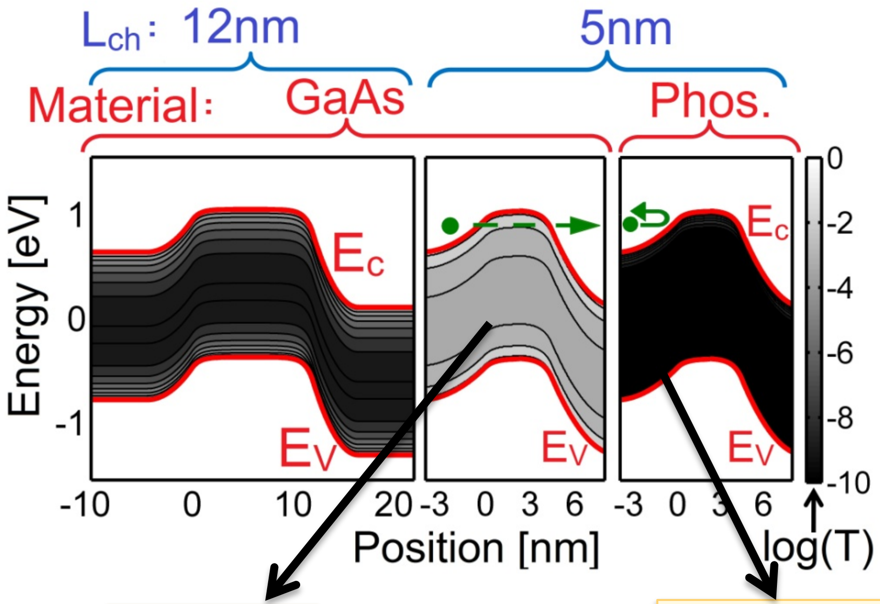
No states available
for hot carriers

ON State: Small
tunneling distance

Sub 10nm MOSFETs

Why did III-V MOSFETs fail?
Low effective mass

Scaling down L_{ch} → Transparent channel barrier

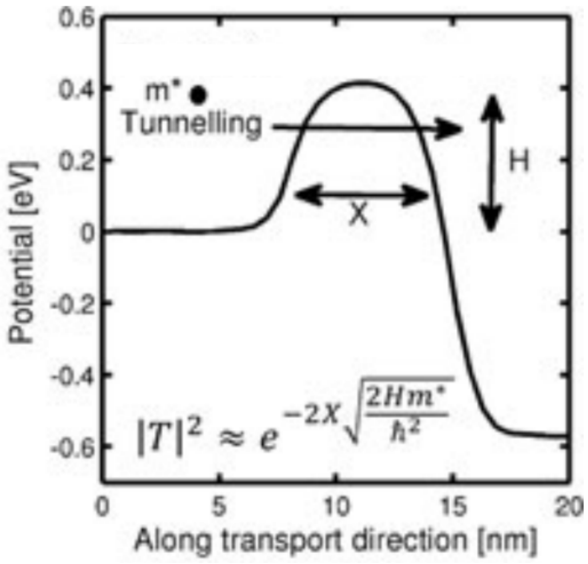


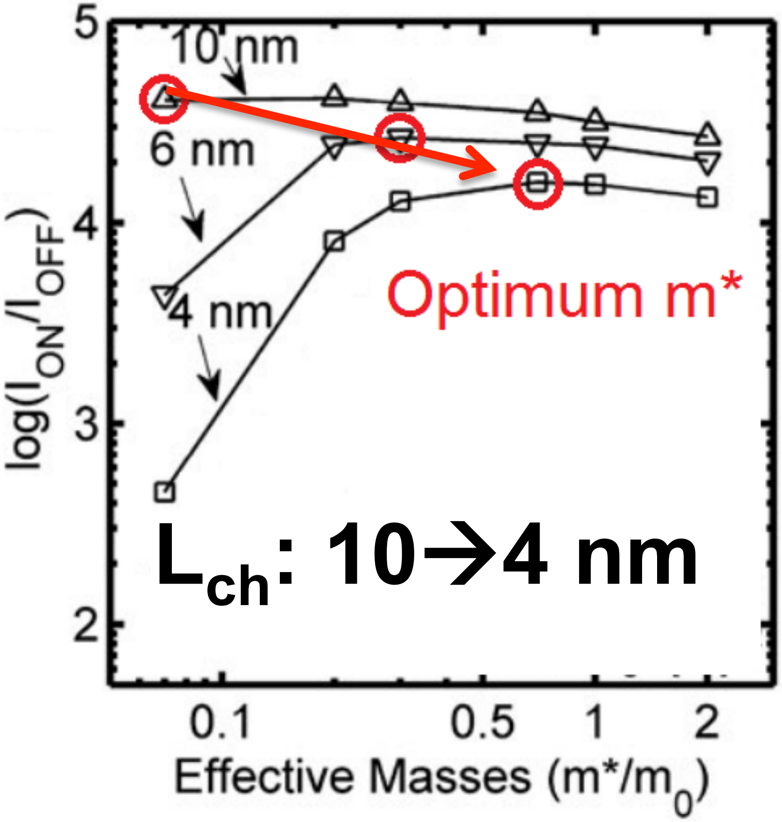
Low m*

High m*

Sub 10nm MOSFETs

We need larger m* in shorter L_{ch}
Due to direct source-to-drain tunneling





What about sub 10nm tunnel FETs?

Introduction:
3) Wentzel–Kramers–Brillouin

Wentzel–Kramers–Brillouin (WKB)

Step description

1 **Φ(x) + Complex EK**
Φ(x): Potential

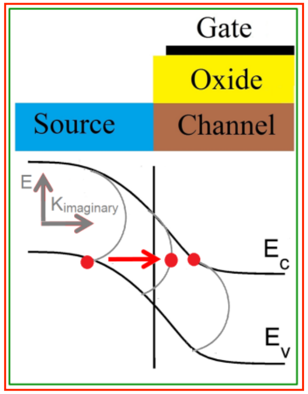
2 → $K_{imaginary}$ (x)

3 Integration $T(E) = \exp\left[-2\int dx\,\kappa(x)\right]$

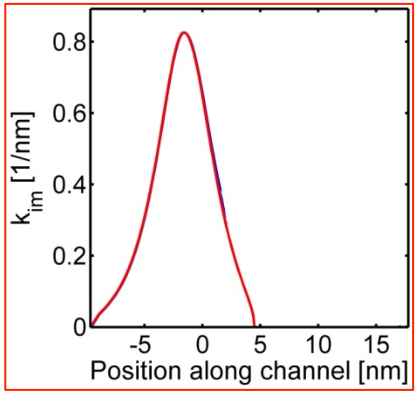
4 → I-V

Step illustration

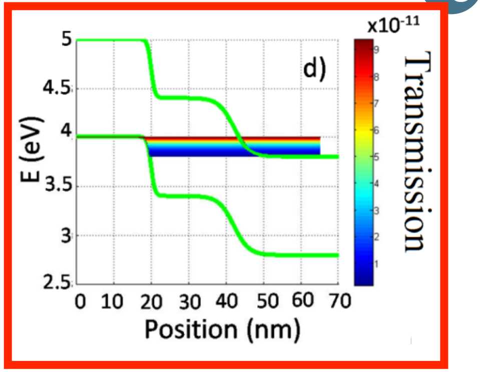
1



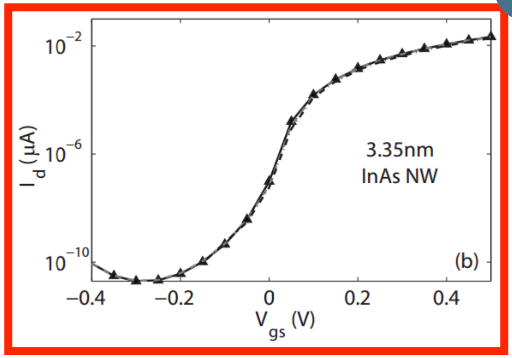
2



3



4



WKB

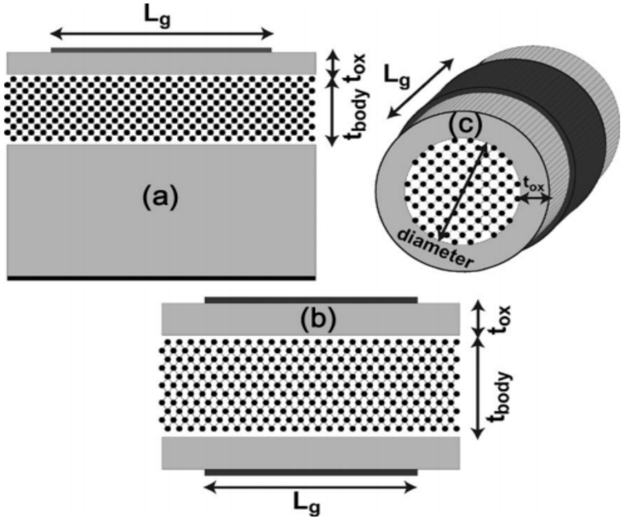
Benchmark our WKB model with NEGF results fom literature

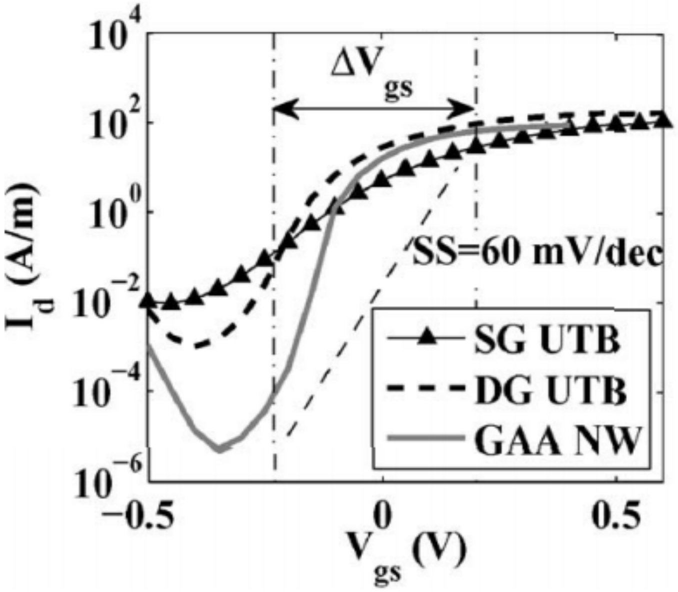
NEGF

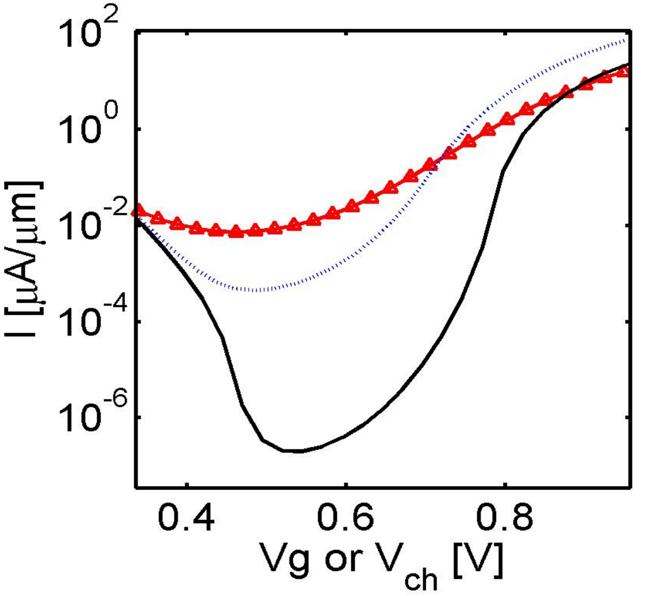
Our WKB

Atomistic Full-Band Design Study of InAs Band-to-Band Tunneling Field-Effect Transistors

Mathieu Luisier and Gerhard Klimeck

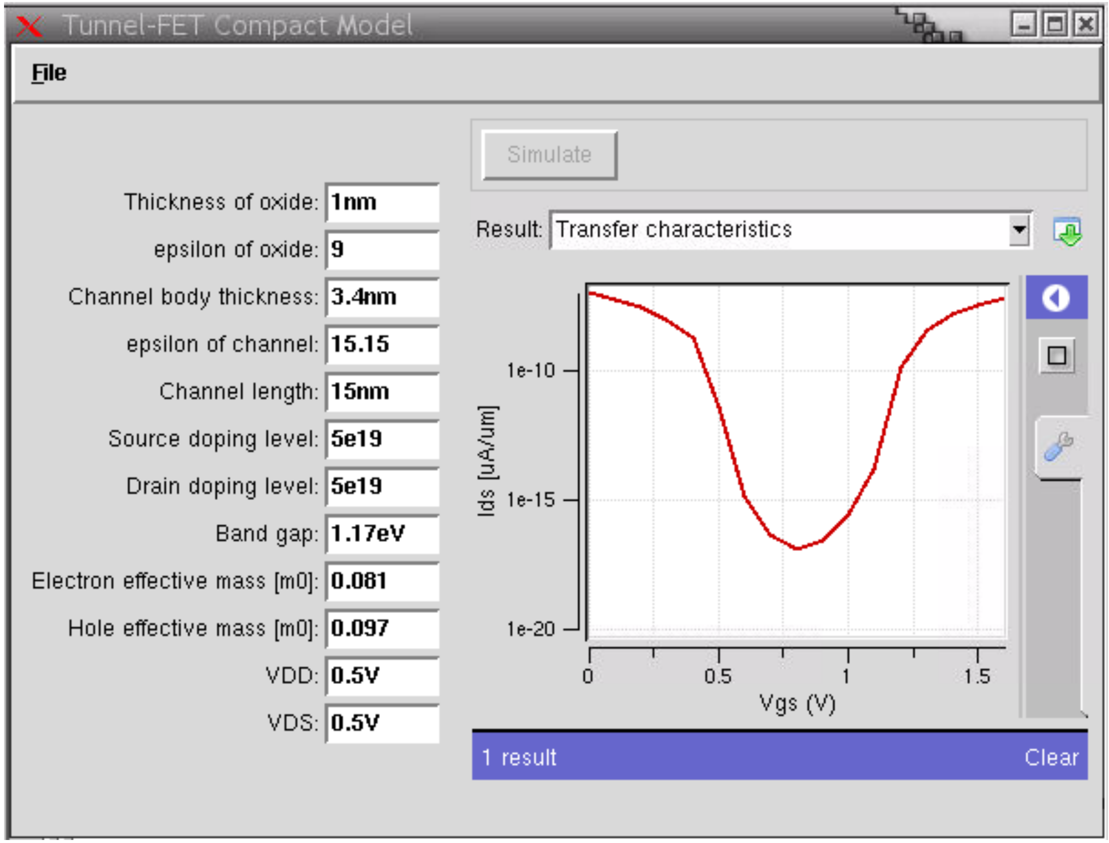






WKB

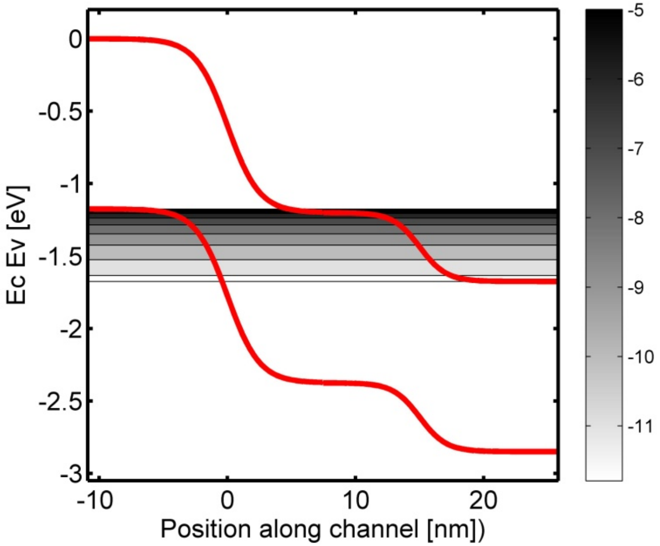
Develop a tool to simulate any **conventional homojunction TFET** in **few minutes**



Thickness of oxide: 1nm
epsilon of oxide: 9
Channel body thickness: 3.4nm
epsilon of channel: 15.15
Channel length: 15nm
Source doping level: 5e19
Drain doping level: 5e19
Band gap: 1.17eV
Electron effective mass [m0]: 0.081
Hole effective mass [m0]: 0.097
VDD: 0.5V
VDS: 0.5V

Result: Transfer characteristics

Other outputs:
Energy resolved current

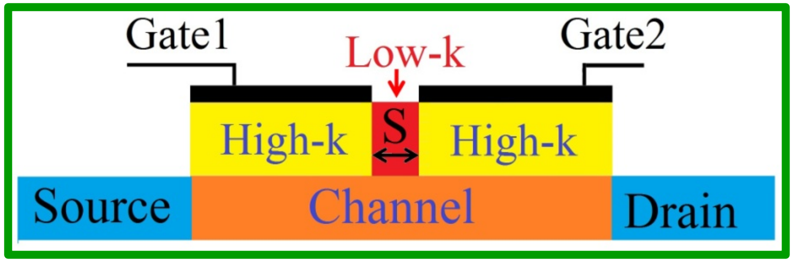


1st Patent: Dielectric Engineered TFET (DE-TFET)

Illustration

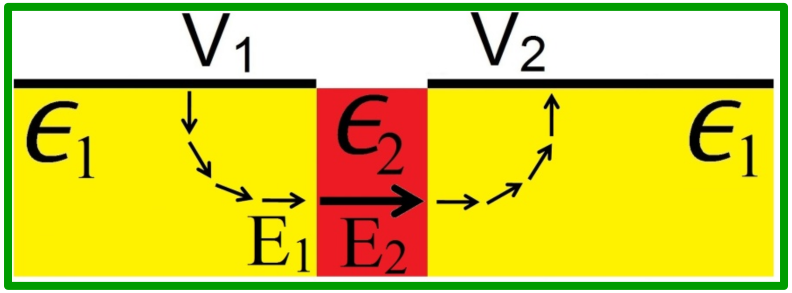
Comments

Structure



- Combination of low-k and high-k dielectrics

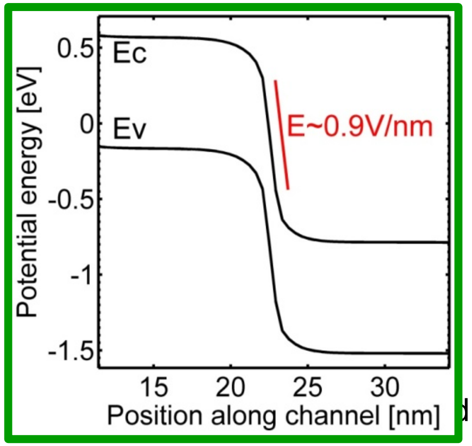
Electric field amplification



$$\epsilon_1 E_1 = \epsilon_2 E_2$$

$$\epsilon_2 \ll \epsilon_1 \rightarrow E_2 \gg E_1$$

Result



- High electric field at the tunnel junction

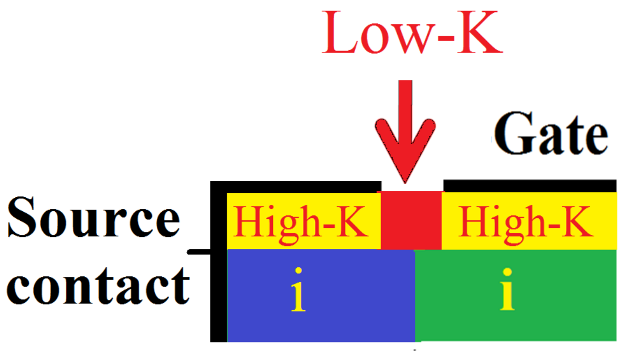
High On-current

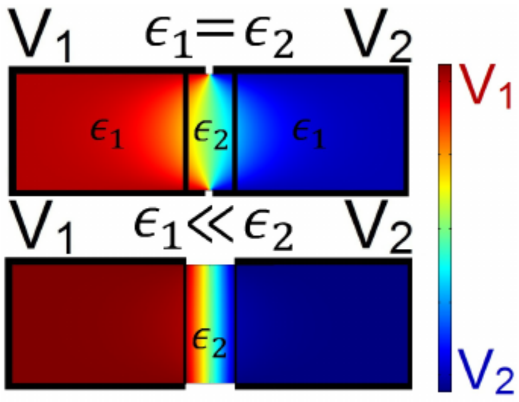
DE-TFET

Illustration

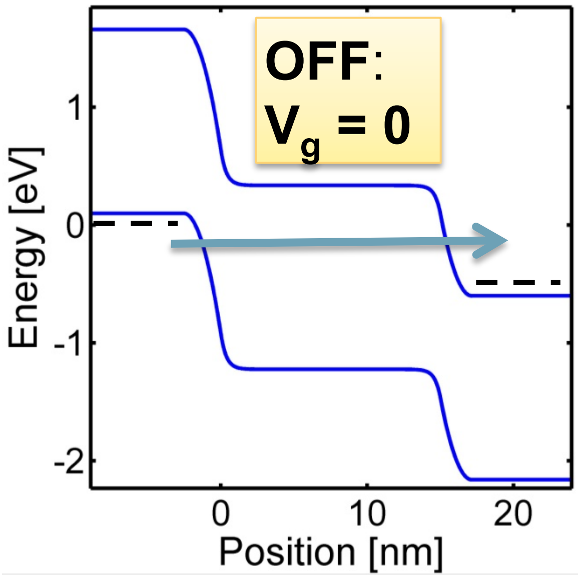
Potential

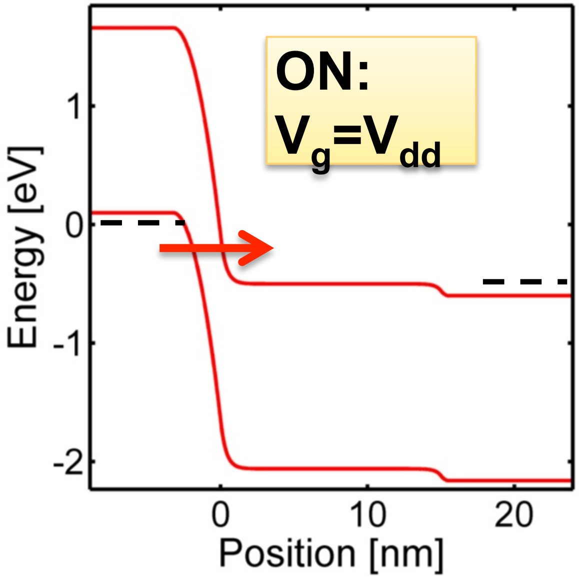
Structure





Band diagram

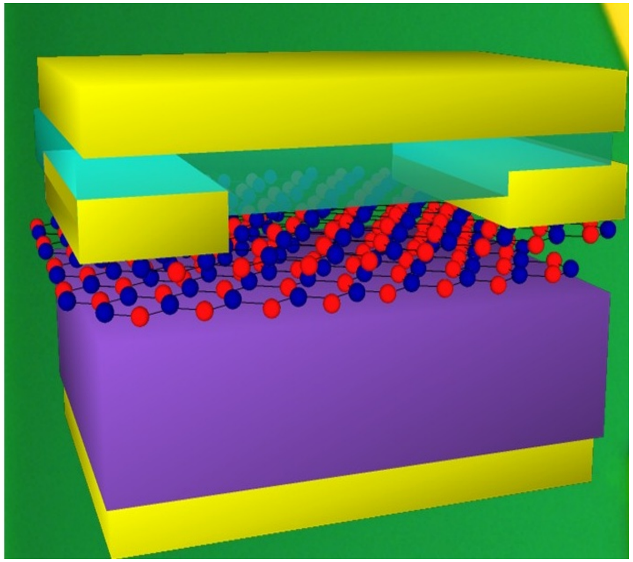


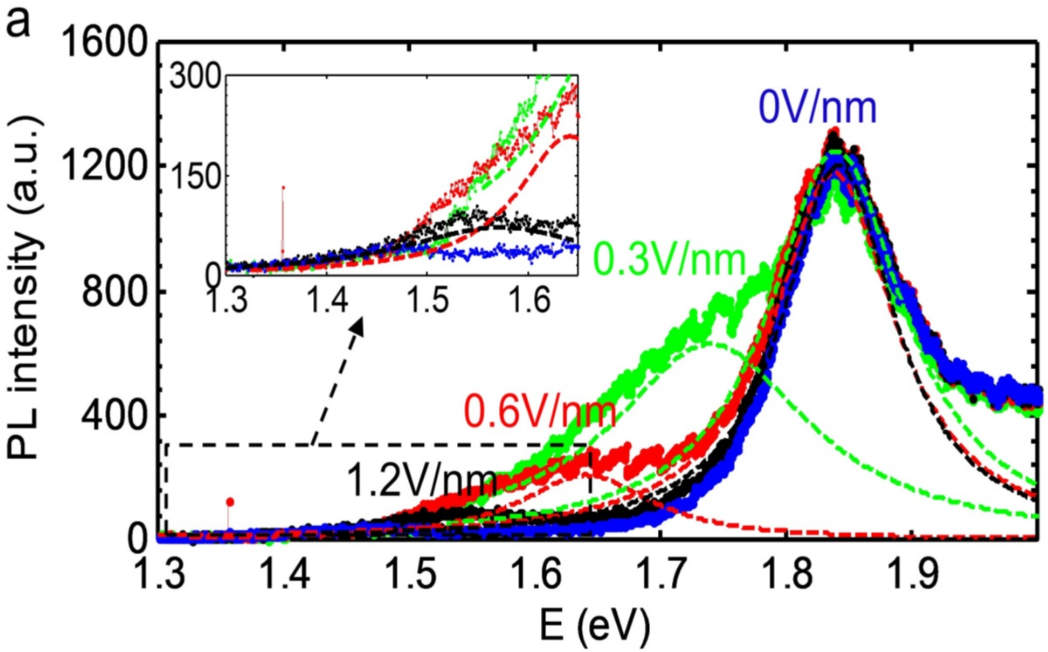


Optics: Quantum dots and quantum wells

Can we electrically tune the optical response of a device?

Bilayer MoS_2 with vertical electric field.

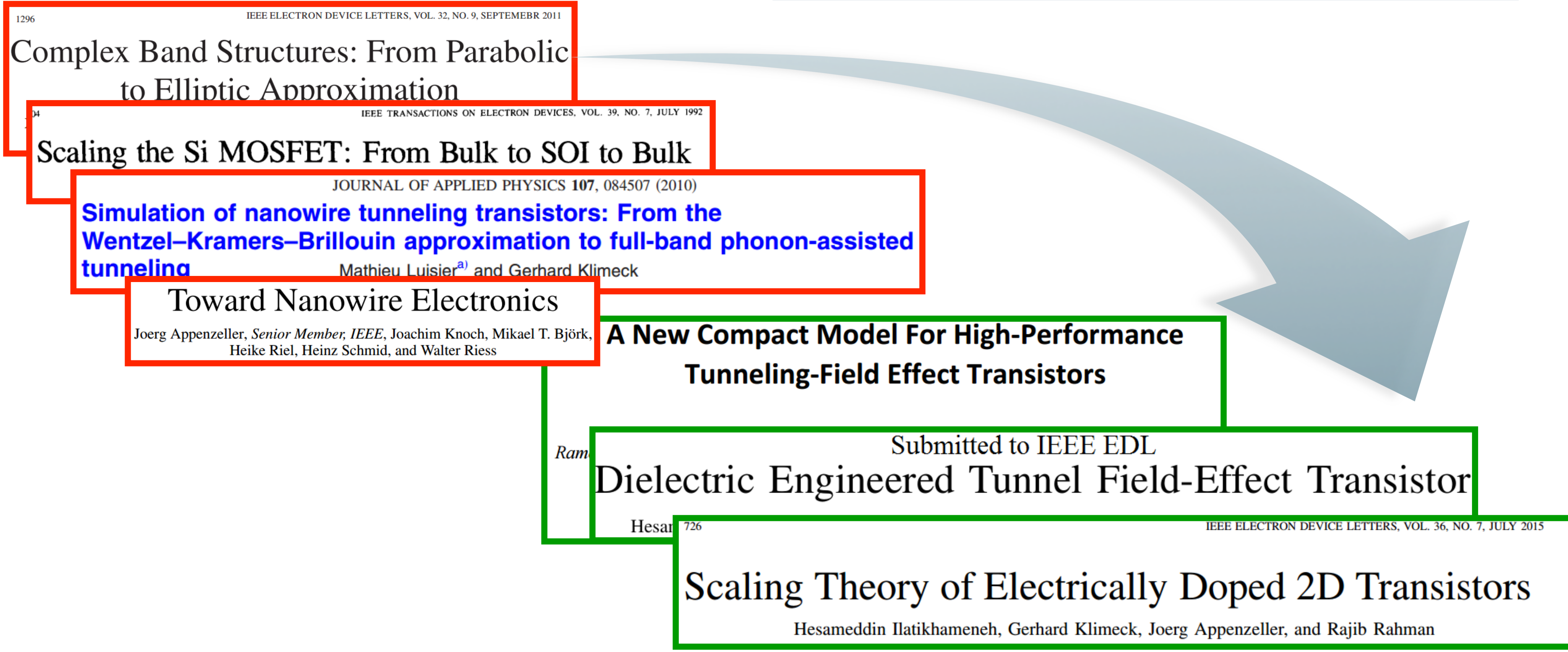




Connection to the previous works

Previous works

Our findings



1296 IEEE ELECTRON DEVICE LETTERS, VOL. 32, NO. 9, SEPTEMEBR 2011

Complex Band Structures: From Parabolic to Elliptic Approximation

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 39, NO. 7, JULY 1992

Scaling the Si MOSFET: From Bulk to SOI to Bulk

JOURNAL OF APPLIED PHYSICS **107**, 084507 (2010)

Simulation of nanowire tunneling transistors: From the Wentzel–Kramers–Brillouin approximation to full-band phonon-assisted tunneling

Mathieu Luisier[a] and Gerhard Klimeck

Toward Nanowire Electronics

Joerg Appenzeller, *Senior Member, IEEE*, Joachim Knoch, Mikael T. Björk, Heike Riel, Heinz Schmid, and Walter Riess

A New Compact Model For High-Performance Tunneling-Field Effect Transistors

Ram

Submitted to IEEE EDL

Dielectric Engineered Tunnel Field-Effect Transistor

Hesar

726 IEEE ELECTRON DEVICE LETTERS, VOL. 36, NO. 7, JULY 2015

Scaling Theory of Electrically Doped 2D Transistors

Hesameddin Ilatikhameneh, Gerhard Klimeck, Joerg Appenzeller, and Rajib Rahman

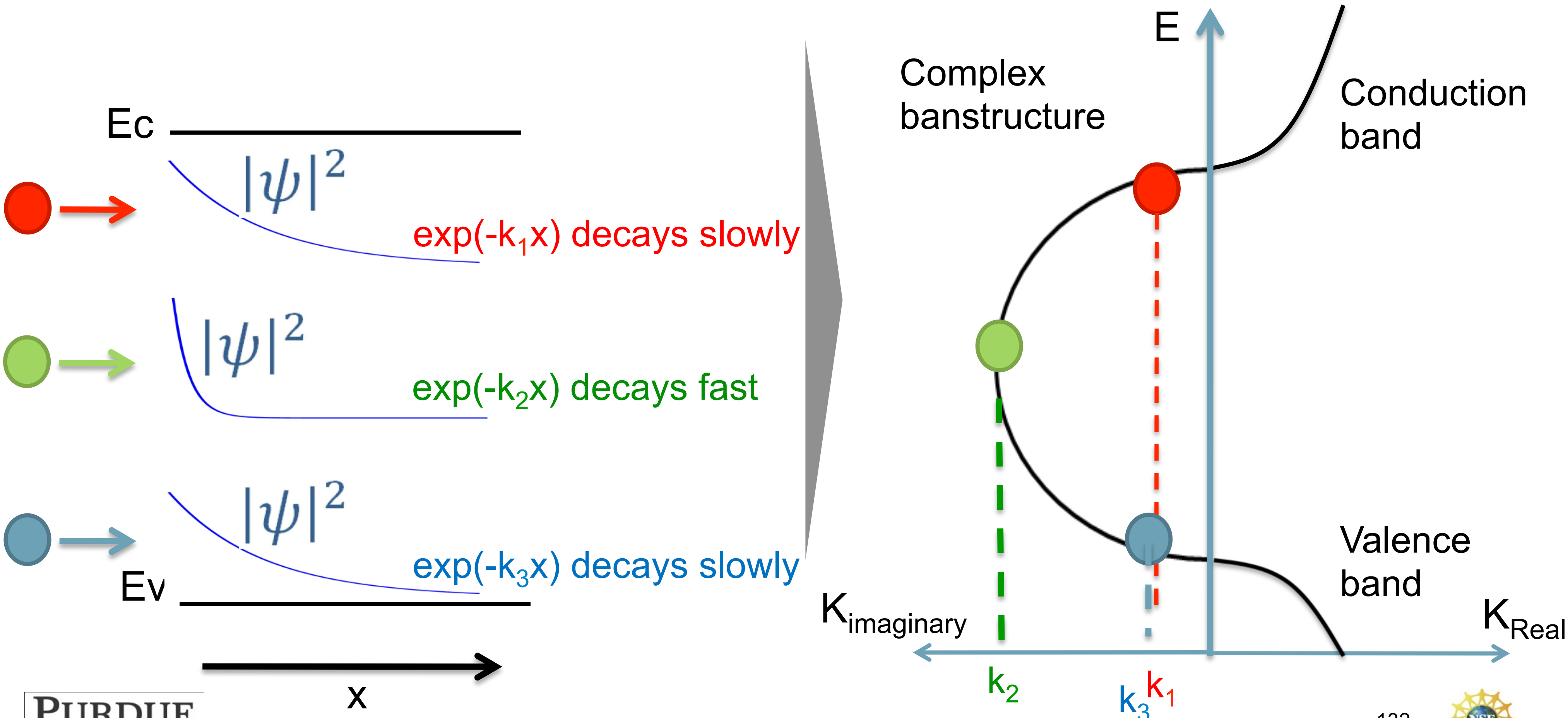
1) Complex EK

2) Scaling theory

3) WKB

Introduction:
1) Complex bandstructure

Band diagram | **Bandstructure**



Ec

$|\psi|^2$

exp($-k_1x$) decays slowly

$|\psi|^2$

exp($-k_2x$) decays fast

$|\psi|^2$

exp($-k_3x$) decays slowly

Ev

x

E

Complex banstructure

Conduction band

Valence band

$K_{imaginary}$

K_{Real}

k_2

k_3 k_1

Introduction:
1) Complex bandstructure

Previous work

Appropriate methods for complex EK

- Full band methods → accurate complex EK
- Captures ellipticity
- Numerical calculation burden

Analytic equation for complex EK

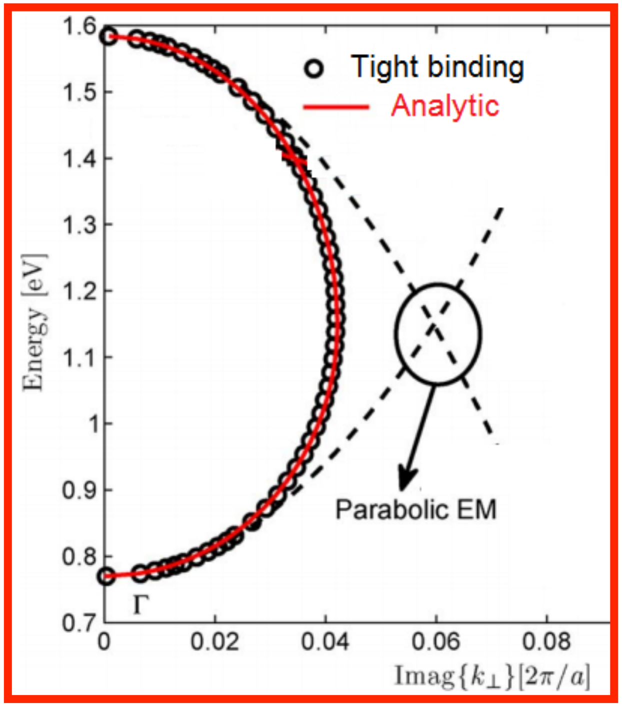
- Recently Guan et al. provide an analytic equation
- Error less than 1.4% compared to TB

1296 IEEE ELECTRON DEVICE LETTERS, VOL. 32, NO. 9, SEPTEMEBR 2011

Complex Band Structures: From Parabolic to Elliptic Approximation

Ximeng Guan, *Member, IEEE*, Donghyun Kim, Krishna C. Saraswat, *Fellow, IEEE*, and H.-S. Philip Wong, *Fellow, IEEE*

Analytic vs numerical complex EK



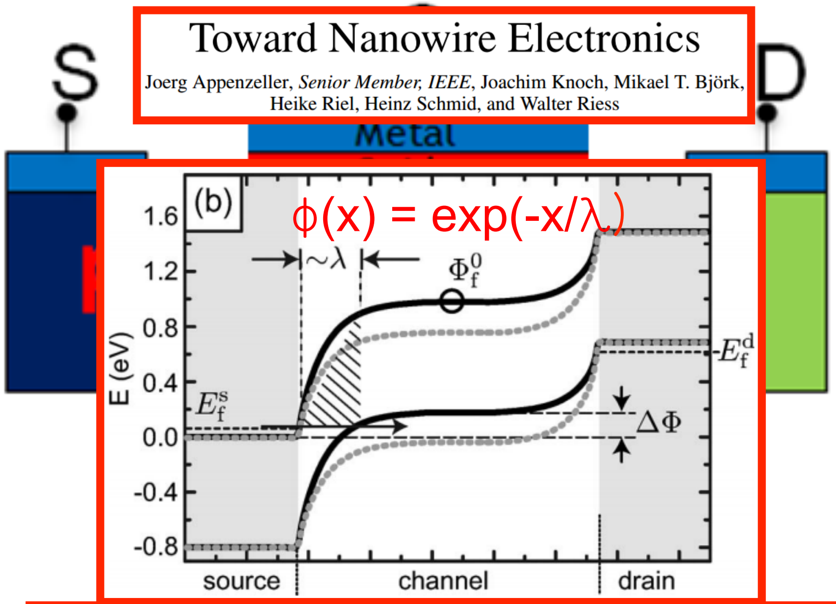
Analytic equation for complex bandstructure

Introduction:
2) Scaling length

Hard to solve 3D Poisson equation analytically → Is there a way to approximate?

Modeling domain | **Poisson equation**

3D



Toward Nanowire Electronics

Joerg Appenzeller, *Senior Member, IEEE*, Joachim Knoch, Mikael T. Björk, Heike Riel, Heinz Schmid, and Walter Riess

$\phi(x) = \exp(-x/\lambda)$

Scaling theory:

$$\frac{d^2\phi}{dx^2} + \frac{d^2\phi}{dy^2} + \frac{d^2\phi}{dz^2} = -\frac{\rho}{\epsilon}$$

$$\lambda = \sqrt{\frac{\epsilon_{si}}{2\epsilon_{ox}} t_{si} t_{ox}}$$

04 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 39, NO. 7, JULY 1992

Scaling the Si MOSFET: From Bulk to SOI to Bulk

Ran-Hong Yan, *Member, IEEE*, Abbas Ourmazd, and Kwing F. Lee, *Member, IEEE*

Introduction:
3) Wentzel–Kramers–Brillouin

Wentzel–Kramers–Brillouin (WKB)

Step description

1 **$\Phi(x)$ + Complex EK**

$\Phi(x)$: Potential

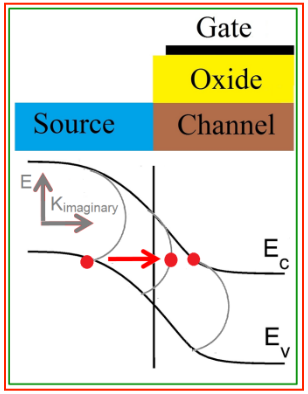
2 **→ $K_{imaginary}(x)$**

3 Integration $T(E) = \exp\left[-2\int dx\,\kappa(x)\right]$

4 **→ I-V**

Step illustration

①



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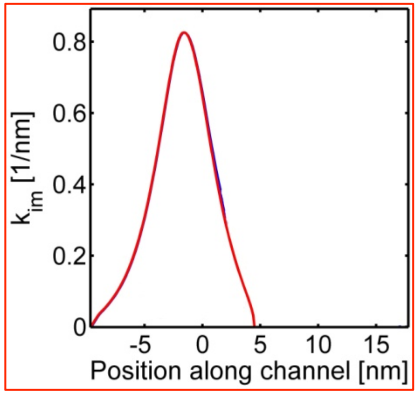

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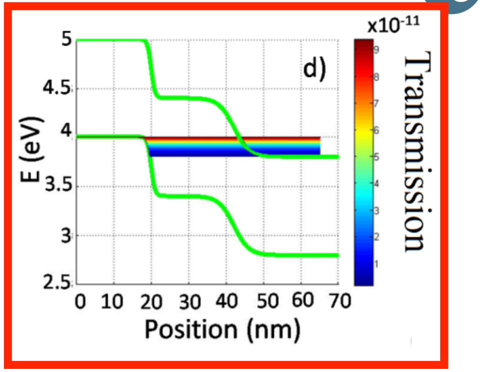

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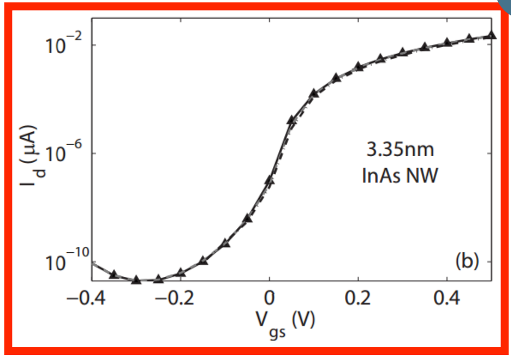
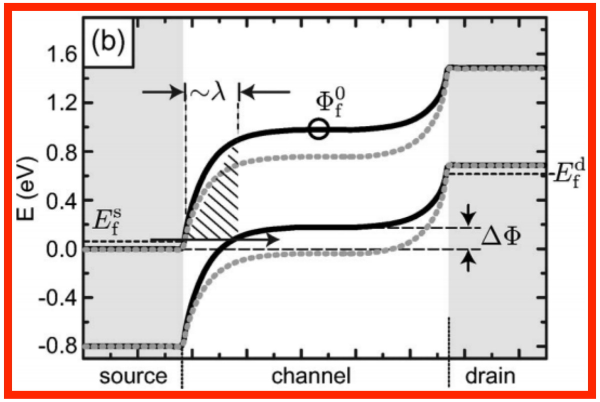
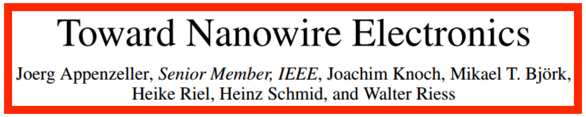


Steep SS device ideas
2D TFETs

Thinner the channel → shorter the tunneling distance



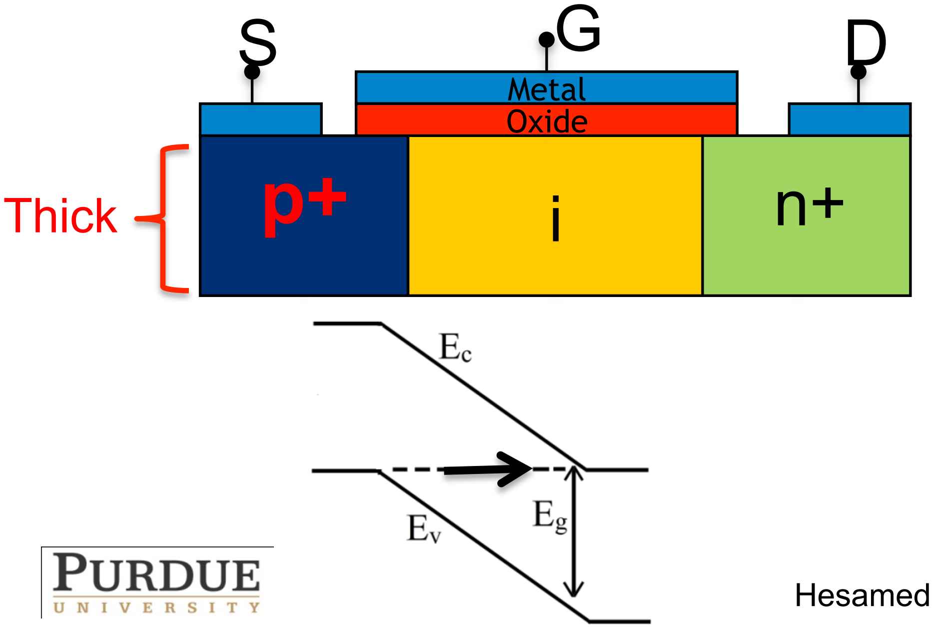

Toward Nanowire Electronics

Joerg Appenzeller, *Senior Member, IEEE*, Joachim Knoch, Mikael T. Björk, Heike Riel, Heinz Schmid, and Walter Riess

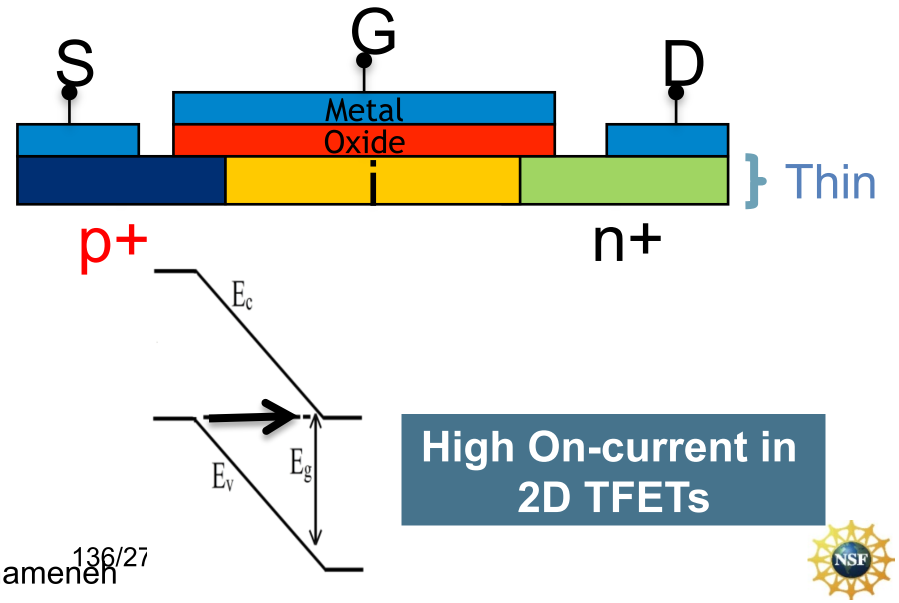
$$\lambda = \sqrt{\frac{\epsilon_{si}}{2\epsilon_{ox}} t_{si} t_{ox}}$$

$t_{si}\downarrow \rightarrow \lambda \downarrow$

Thick channel



Thin channel

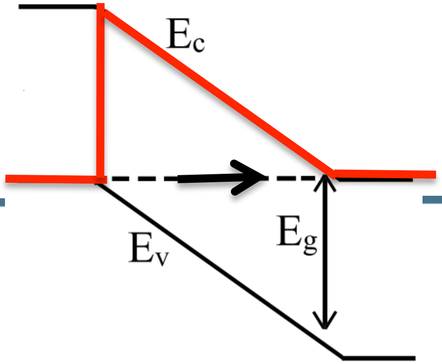


High On-current in 2D TFETs

Analytic modeling:
Modified Fowler-Nordheim

R. Salazar

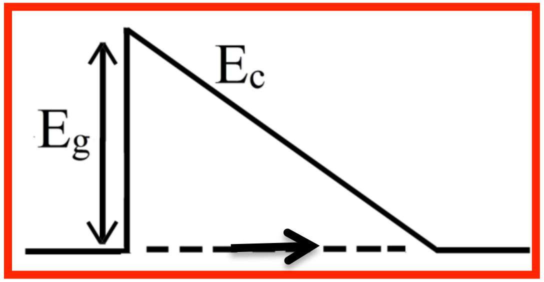
Goal: analytic equation for BTBT transmission



Fowler-Nordheim

Approach:

- Triangular barrier + effective mass



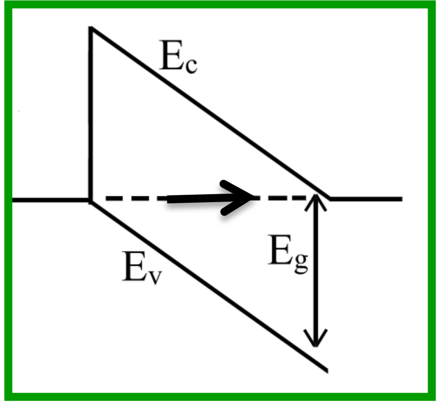
Result:

$$T^{FN} = exp\left(-\frac{4}{qF}\frac{\sqrt{2m}\,E_g^{3/2}}{3\hbar}\right)$$

Modified Fowler-Nordheim

Approach:

- Triangular barrier + elliptic complex EK



Result:

$$T^{Elliptic} = exp\left(-\frac{\pi}{qF}\frac{\sqrt{m_r^*}\,E_g^{3/2}}{2\hbar}\right)$$

$$m_r^* = \frac{m_e m_h}{m_e + m_h}$$

Analytic modeling:
Modified Fowler-Nordheim

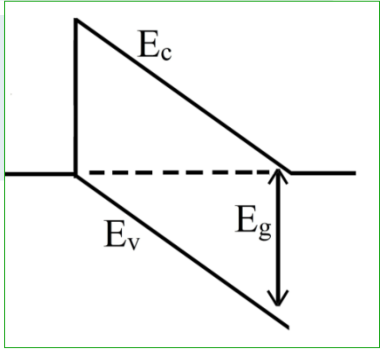
R. Salazar

Achievement: a modified FN equation which considers both conduction and valence bands

Tunneling type	Modified Fowler-Nordheim

BTBT: use old FN but

- Replace m with 0.7m$_r$



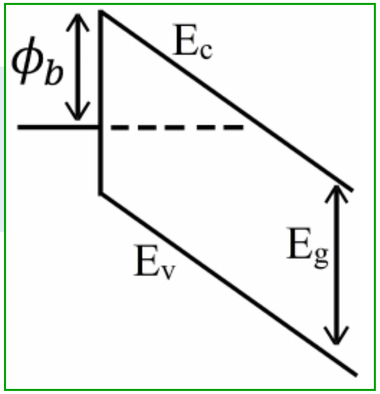
$$\boxed{m \approx 0.7 m_r^*}$$

$$\boxed{T^{FN} = exp\left(-\frac{4}{qF}\frac{\sqrt{2m}\,E_g^{3/2}}{3\hbar}\right)}$$

$$\boxed{m \approx 0.7 m_r^* \left(\frac{\phi_b}{E_g}\right)^2}$$

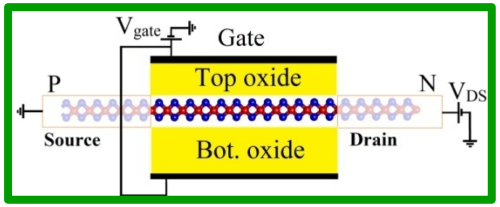
Schottky barrier tunneling:

- Replace m with 0.7m$_r$ $(\phi_b/E_g)^2$

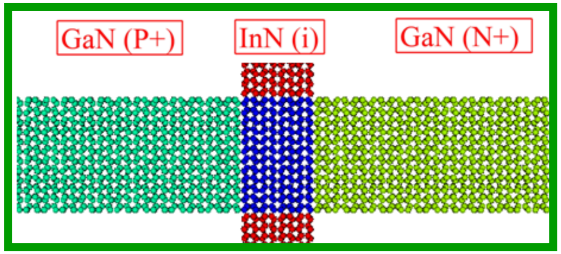


Steep SS device ideas

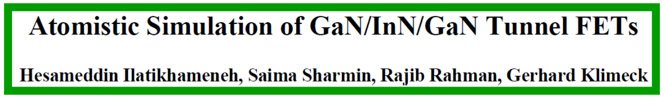
1 2D TFETs



2 Nitride TFETs



Publications



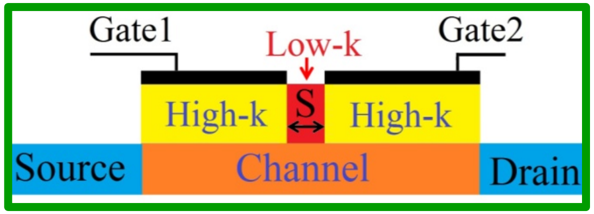
Atomistic Simulation of GaN/InN/GaN Tunnel FETs

Hesameddin Ilatikhameneh, Saima Sharmin, Rajib Rahman, Gerhard Klimeck

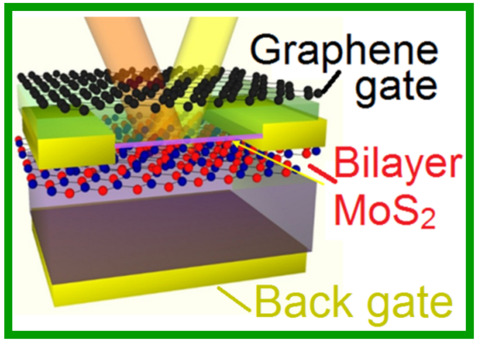
Polarization-Engineered III-Nitride Heterojunction Tunnel Field-Effect Transistors

WENJUN LI[1], SAIMA SHARMIN[2], HESAMEDDIN ILATIKHAMENEH[2], RAJIB RAHMAN[2], YEQING LU[3], JINGSHAN WANG[1], XIAODONG YAN[1], ALAN SEABAUGH[1] (Fellow, IEEE), GERHARD KLIMECK[2] (Fellow, IEEE), DEBDEEP JENA[1] (Senior Member, IEEE), AND PATRICK FAY[1] (Senior Member, IEEE)

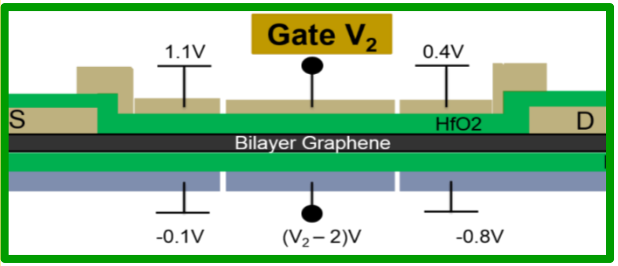
3 Dielectric engineered TFET



4 Dynamic band gap FET



5 Electrically doped BLG TFET

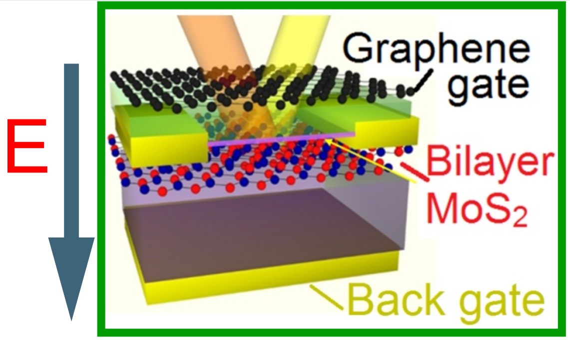


Steep SS device ideas:
Dynamic bandgap FET

Tao Chu

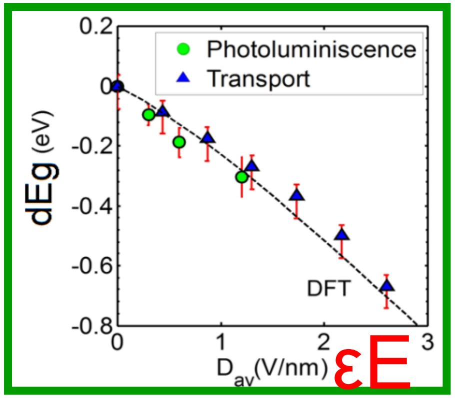
Illustration | **Comments**

Bandgap tuning by E field



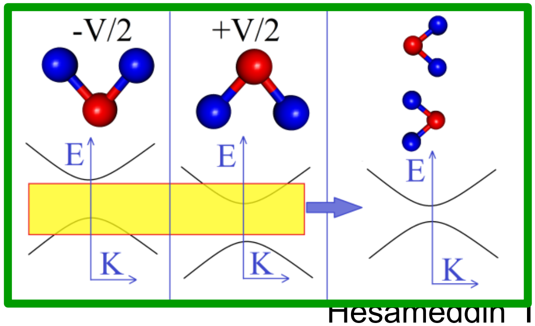
- Top & bottom gates with opposite voltages
  → E field

Bandgap change



- Increase in electric field
  → Decrease in Eg

Reason



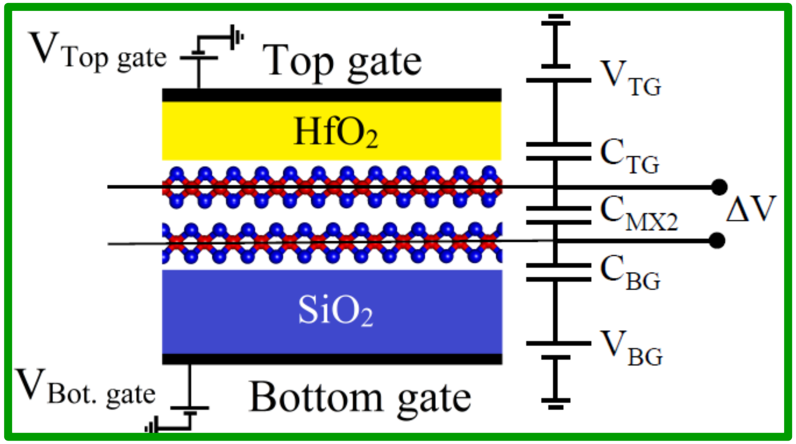
- Potential difference between 2 layers
  → band gap change

Steep SS device ideas:
Dynamic bandgap FET

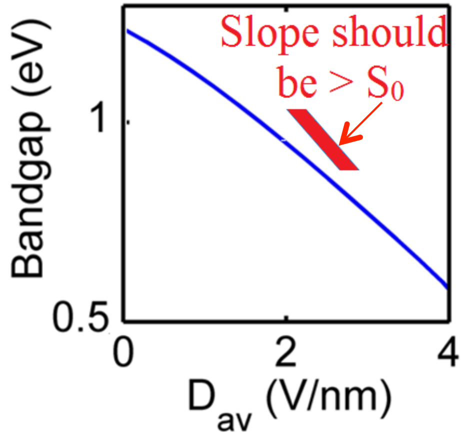
Can we use dynamic band gap to make device steeper?

- Only if the rate of change in band gap is high enough.
- This condition is not satisfied in BLG and TMDs

Structure

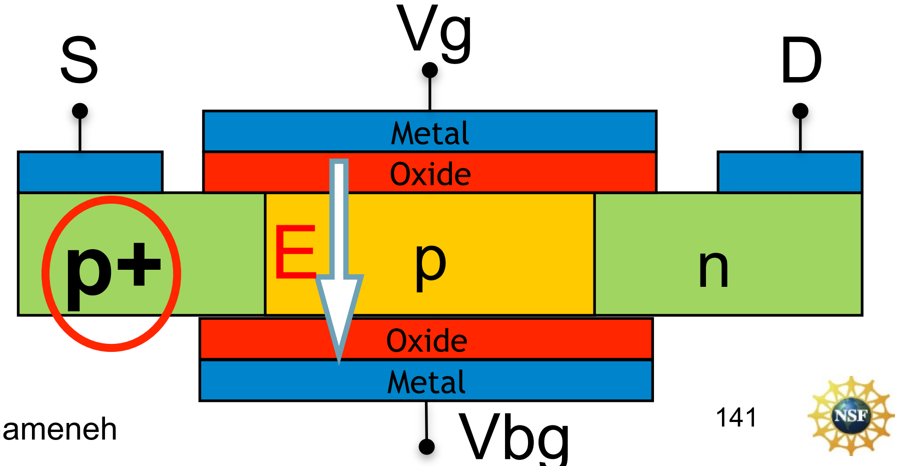


Bandgap modulation of Bilayer MoS_2



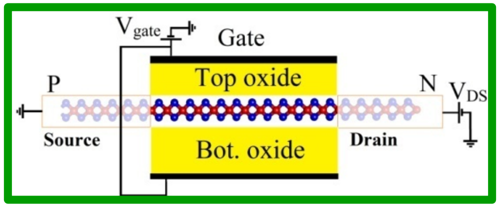
Future work proposal:

Use dynamic band gap in **Tunnel FET** to obtain higher ON-current

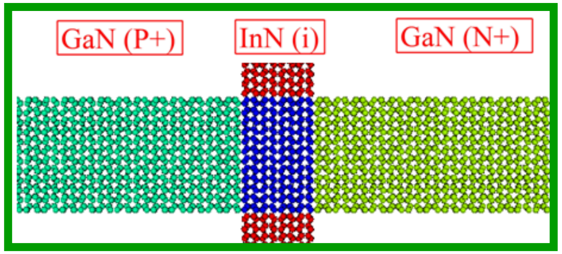


Steep SS device ideas

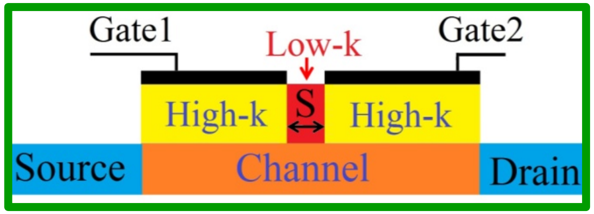
1 2D TFETs



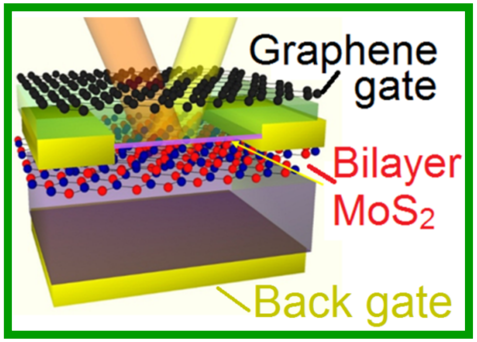
2 Nitride TFETs



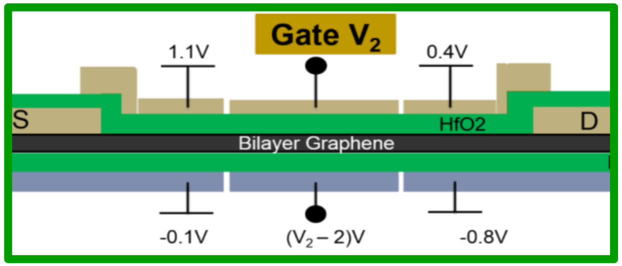
3 Dielectric engineered TFET



4 Dynamic band gap FET



5 **Electrically doped BLG TFET**



Steep SS device ideas:
Prior art: BLG FET

Structure

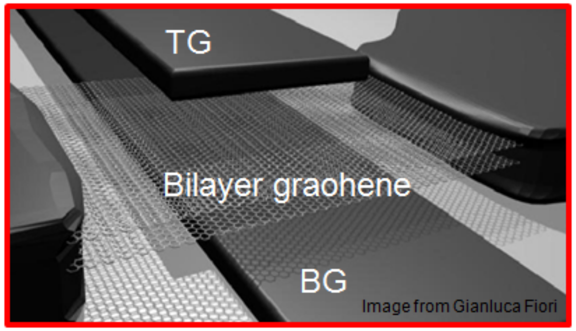
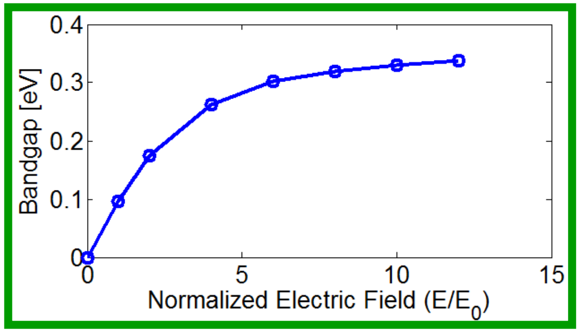
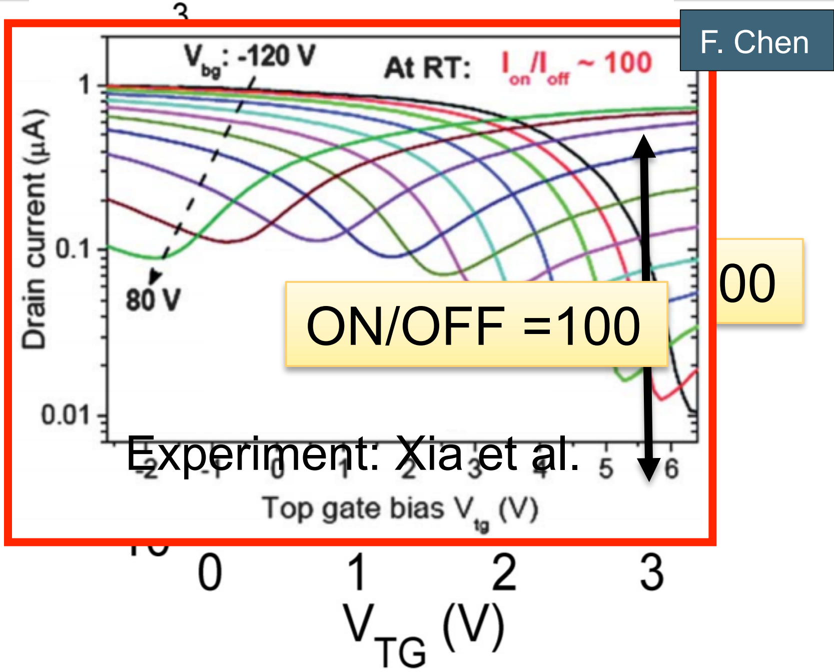


Image from Gianluca Fiori

Band gap opening



I-V

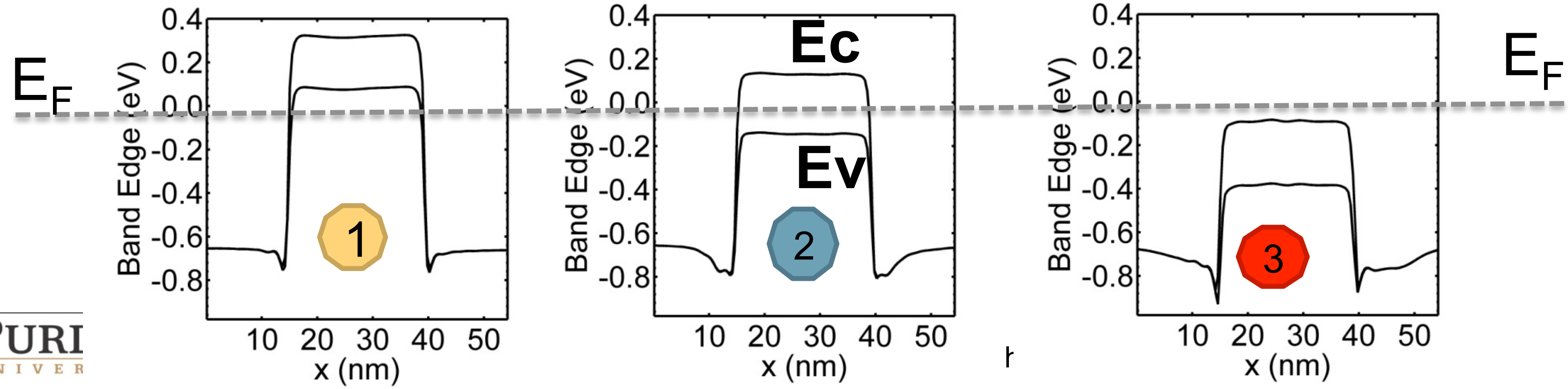


F. Chen

ON/OFF =100

Experiment: Xia et al.

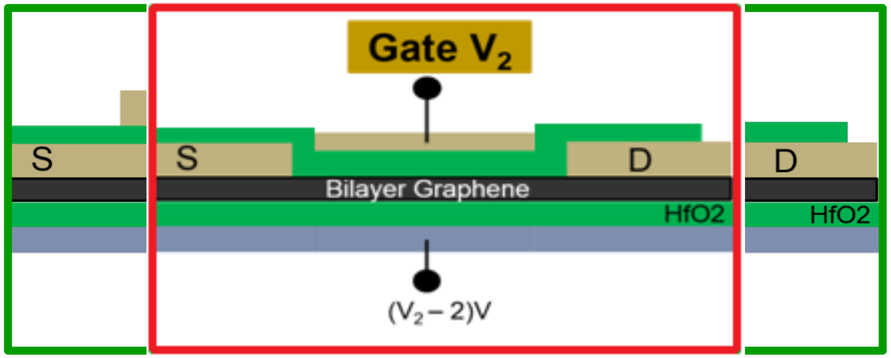
Band diagrams



Working Principle

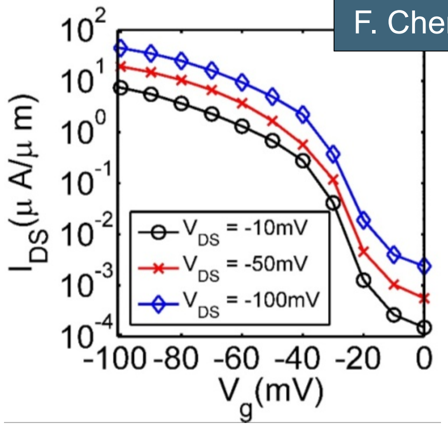
Old Structure

New Structure

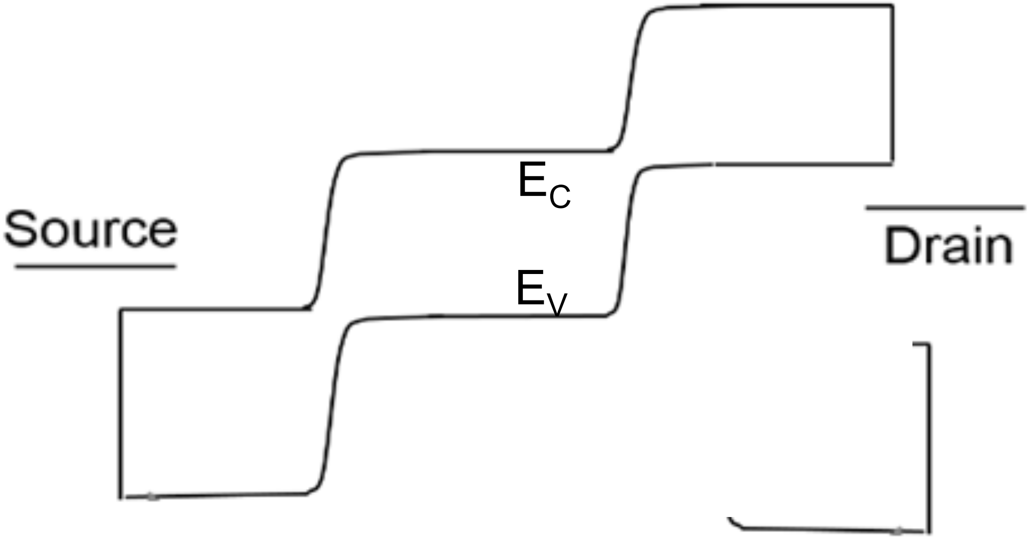


IV

F. Chen



Electrically reconfigurable to N-TFET (p-i-n) and P-TFET (n-i-p)



Review

Ideas:

1) How to increase ON-current of TFETs?

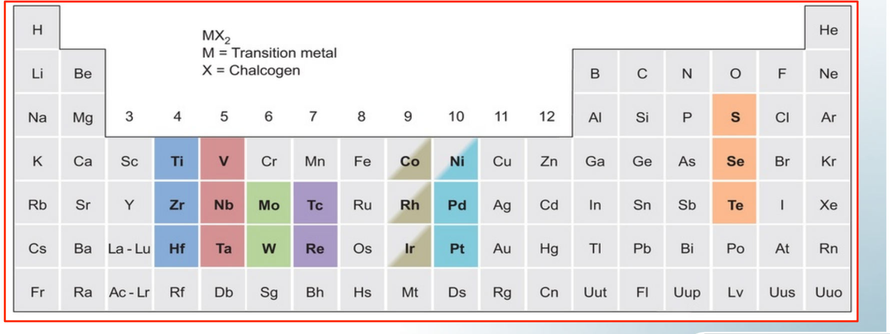
Increase electric field by

- a) Internal polarization
- b) 2D channel material
- c) dielectric engineering

Or use dynamic band gap

Channel material:
Transition metal dichalcogenide

Chemical formula: MX_2
MoS_2, WSe_2

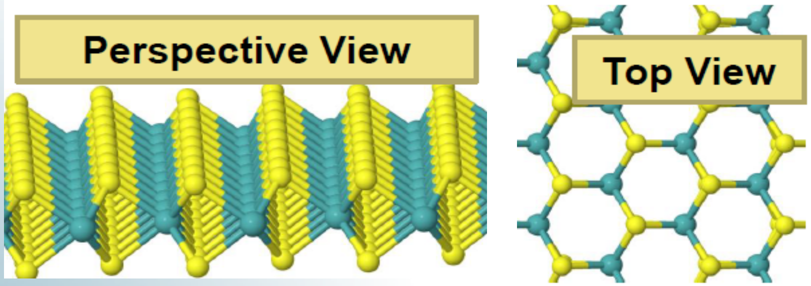


H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg	3	4	5	6	7	8	9	10	11	12	Al	Si	P	**S**	Cl	Ar
K	Ca	Sc	**Ti**	**V**	Cr	Mn	Fe	**Co**	**Ni**	Cu	Zn	Ga	Ge	As	**Se**	Br	Kr
Rb	Sr	Y	**Zr**	**Nb**	**Mo**	**Tc**	Ru	**Rh**	**Pd**	Ag	Cd	In	Sn	Sb	**Te**	I	Xe
Cs	Ba	La - Lu	**Hf**	**Ta**	**W**	**Re**	Os	**Ir**	**Pt**	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ac - Lr	Rf	Db	Sg	Bh	Hs	Mt	Ds	Rg	Cn	Uut	Fl	Uup	Lv	Uus	Uuo

MX_2
M = Transition metal
X = Chalcogen

Nature Chemistry 5, 263–275 (2013)

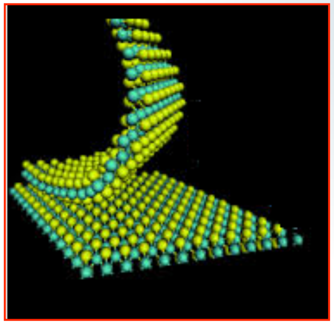
Crystal structure: Hexagonal



Transition Metal Dichalcogenides (TMD)

Fabrication technique

- Exfoliation (scotch tape)



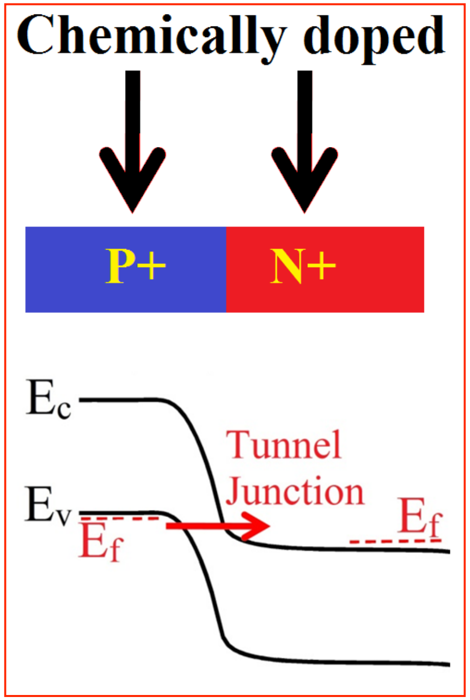
Promises

- Good gate control
- Low interface traps, roughness, dangling bonds.

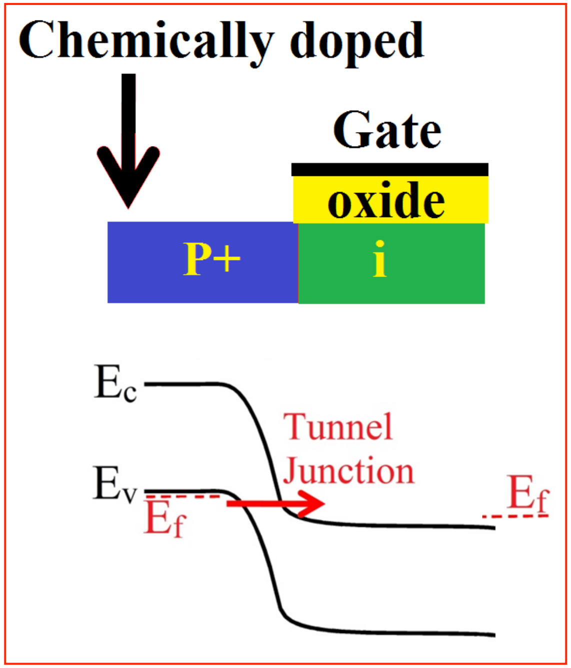
Performance of TMD TFETs

Methods to create tunnel junction

1) PN junction

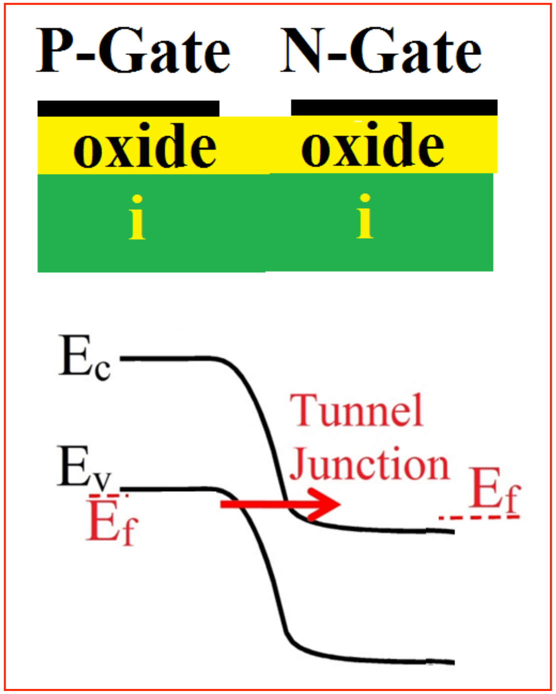


2) Conventional Tunnel transistor



Gate induced N-doped region

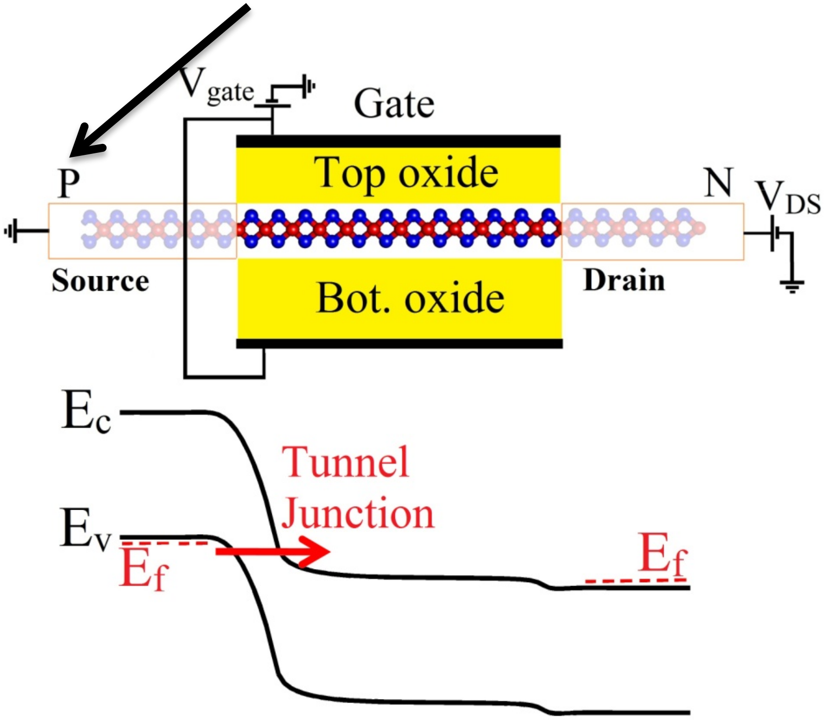
3) Electrically doped tunnel FET



Gate induced P-doped & N-doped regions

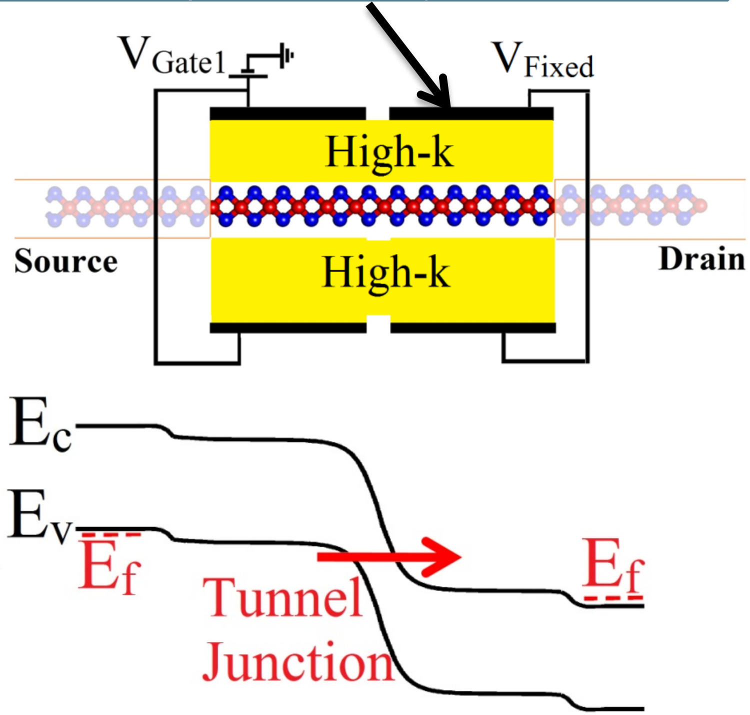
Methods to create tunnel junction

1) Chemically doped



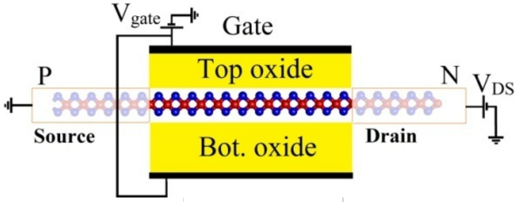
Tunnel junction is between
- a) **Highly doped source**
- b) **Channel**

2) Electrically doped



Tunnel junction is between
- a) **Gate1**
- b) **Gate2 (fixed potential)**

Previous works on TMD TFETs



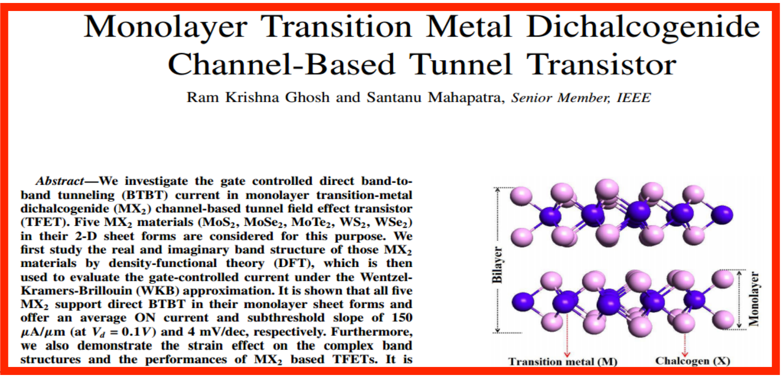
Previous works

Key messages

- Thin channel is enough for high performance.
- Channel material is NOT an important factor.
- I_{ON} > 150 uA/um for almost all TMDs.

Method

- Non-self-consistent WKB simulation
- Source junction is neglected in the modeling.



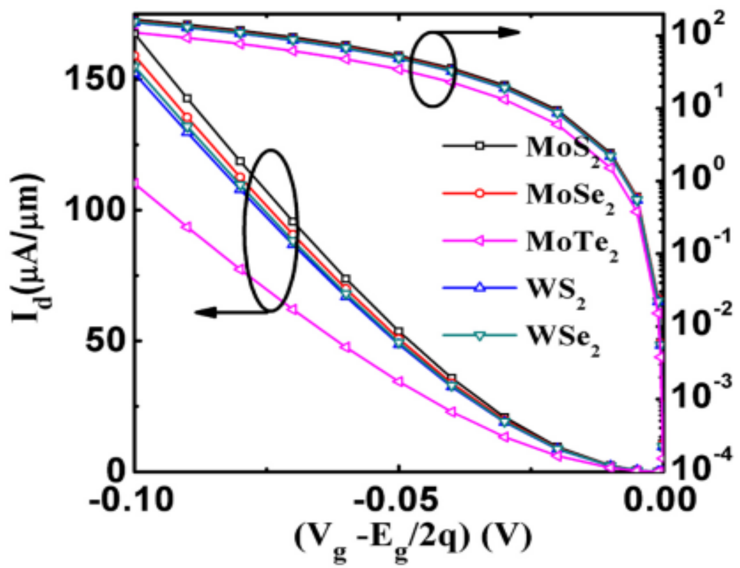
Monolayer Transition Metal Dichalcogenide Channel-Based Tunnel Transistor

Ram Krishna Ghosh and Santanu Mahapatra, *Senior Member, IEEE*

Abstract—We investigate the gate controlled direct band-to-band tunneling (BTBT) current in monolayer transition-metal dichalcogenide (MX_2) channel-based tunnel field effect transistor (TFET). Five MX_2 materials (MoS_2, $MoSe_2$, $MoTe_2$, WS_2, WSe_2) in their 2-D sheet forms are considered for this purpose. We first study the real and imaginary band structure of those MX_2 materials by density-functional theory (DFT), which is then used to evaluate the gate-controlled current under the Wentzel-Kramers-Brillouin (WKB) approximation. It is shown that all five MX_2 support direct BTBT in their monolayer sheet forms and offer an average ON current and subthreshold slope of 150 $\mu A/\mu m$ (at $V_d = 0.1V$) and 4 mV/dec, respectively. Furthermore, we also demonstrate the strain effect on the complex band structures and the performances of MX_2 based TFETs. It is

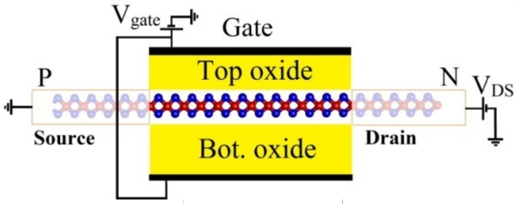
Results

I_d-V_g of different TMDs



V_{dd} = 0.1V

Atomistic simulation of chemically doped TMD TFETs



Atomistic simulation

Key messages

- Thin channel is **NOT** enough for high performance.
- Channel material **is** an important factor.
- I_{ON} < 150 uA/um for almost all TMDs.

Simulation method

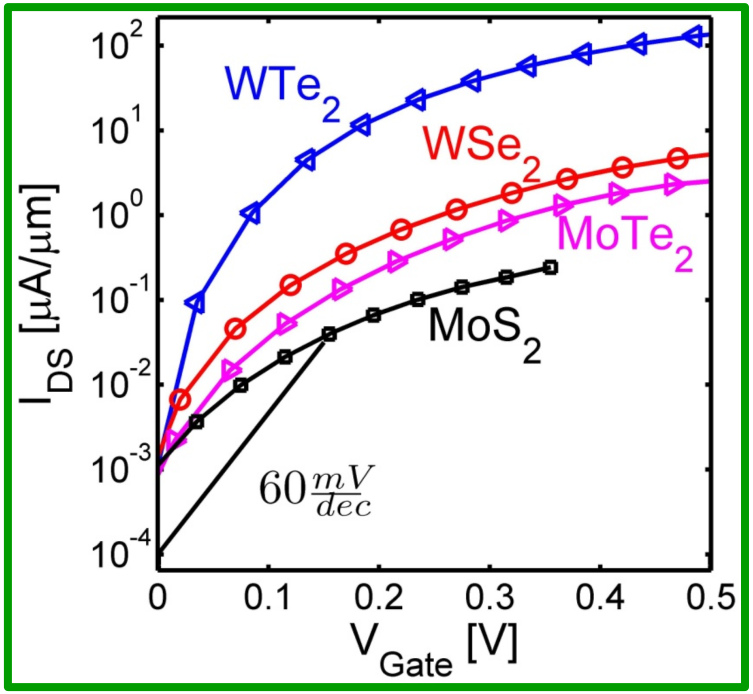
- Self-consistent Poisson-NEGF simulation
- Full band sp^3d^5 2^{nd} nearest neighbor tight binding

Tunnel Field-Effect Transistors in 2-D Transition Metal Dichalcogenide Materials

HESAMEDDIN ILATIKHAMENEH[1], YAOHUA TAN[1], BOZIDAR NOVAKOVIC[1], GERHARD KLIMECK[1], RAJIB RAHMAN[1], AND JOERG APPENZELLER[2]

Results

I_d-V_g of different TMDs



V_{dd} = 0.5V

Old vs. new analytic potentials

R. Salazar

What was wrong in the previous analytic WKB models?

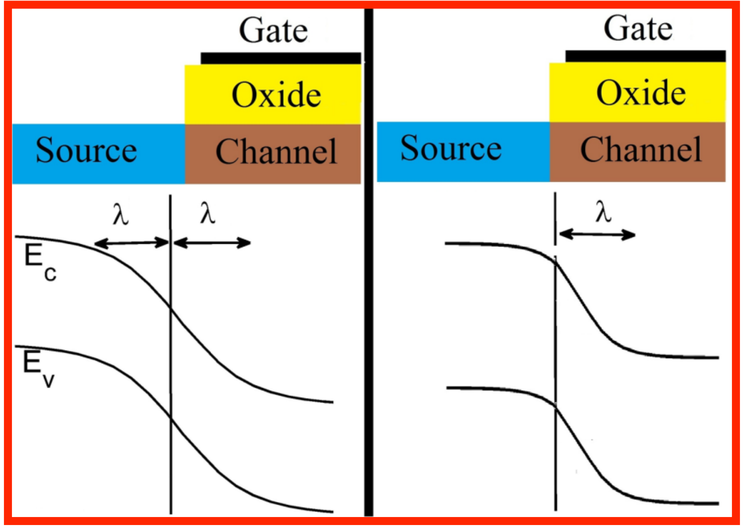
Correct potential + WKB → NEGF results

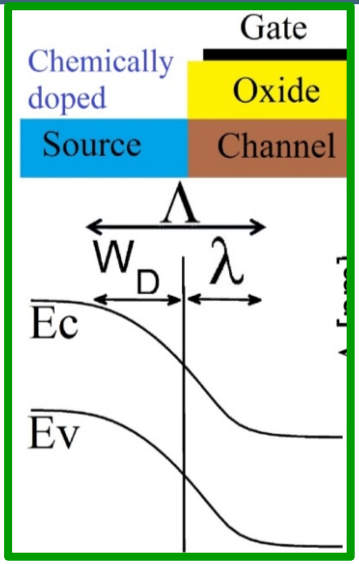
Old analytic profile

New analytic profile

Illustration

Band diagrams





Comments

- Bending distance in tunnel junction is due to λ

Underestimation of tunneling distance Λ

- Both depletion width of source (W_D) and λ are important.

Old vs. new analytic potentials

Comparison with NEGF + 3D Poisson

WKB + old potential vs. SCF NEGF

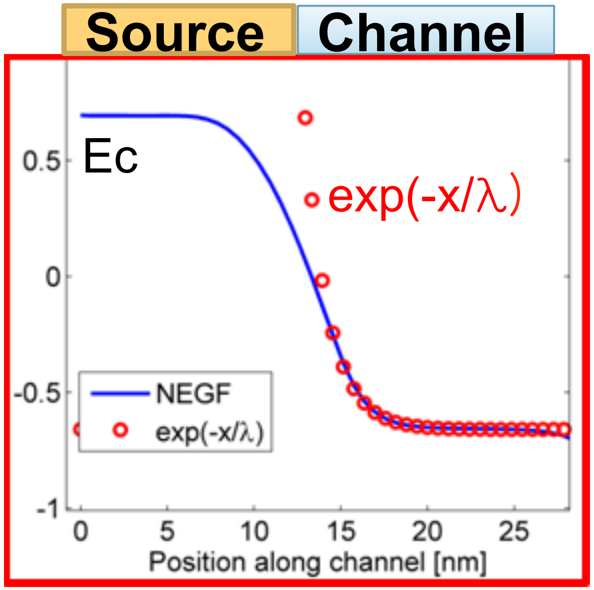
WKB + new potential vs. SCF NEGF

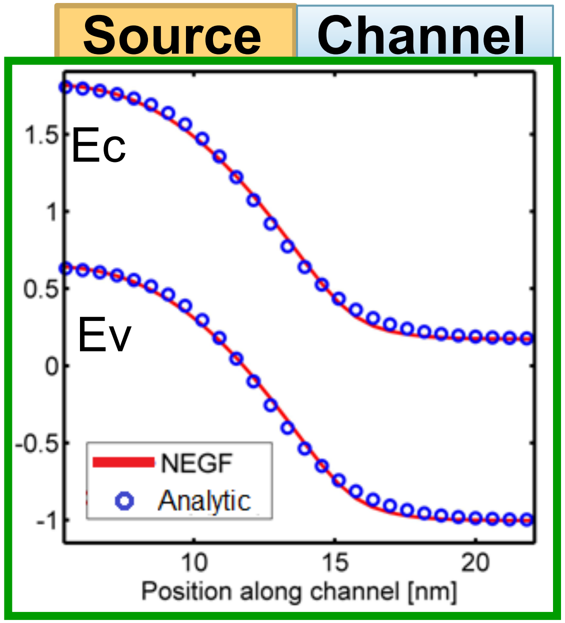
Old analytic profile

New analytic profile

Illustration

Band diagrams





Comments

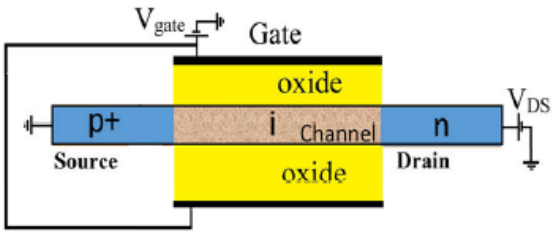
- Bending distance in tunnel junction is due to λ

- Good match all over the device.

New analytic model
Comparison with NEGF + 3D Poisson

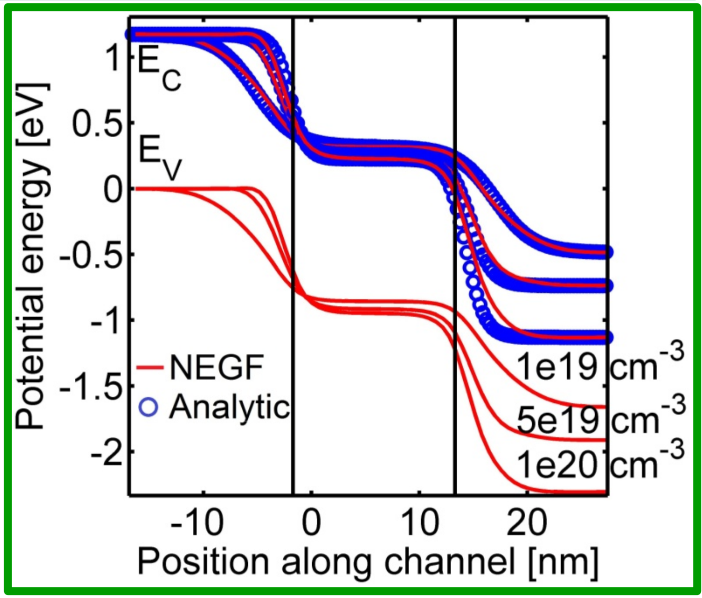
WKB + new potential vs. SCF NEGF

Modeling domain

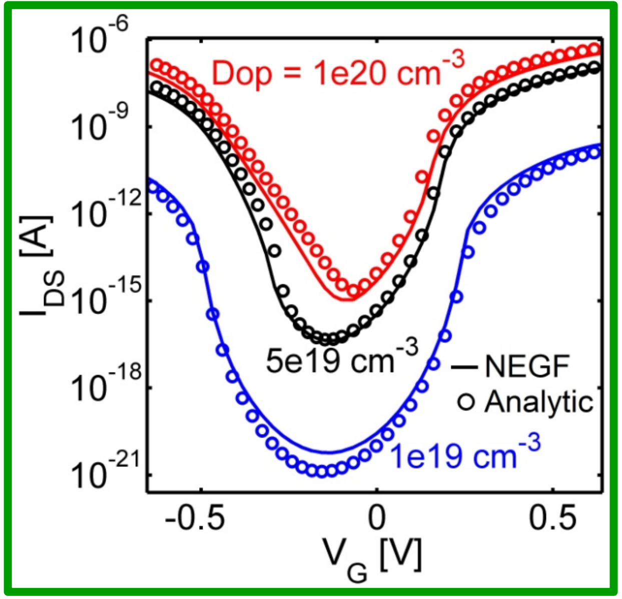


- InAs nanowire
- Lch = 15 nm
- Diameter ~ 4nm

Impact of doping on potential



Impact of doping on I-V



WKB + new analytic potential

- matches the NEGF results well
- captures the effect of doping accurately

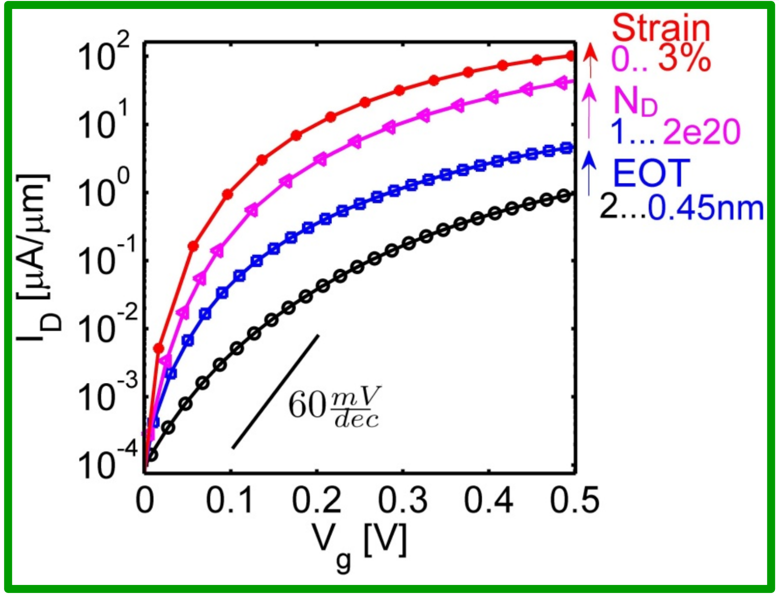
A New Compact Model For High-Performance Tunneling-Field Effect Transistors

Ramon B. Salazar, Hesameddin Ilatikhameneh*, Rajib Rahman†, Gerhard Klimeck†, and Joerg Appenzeller§*

* These two authors contributed equally to this work.

Performance boosters for TMD TFETs

Analysis of performance boosters



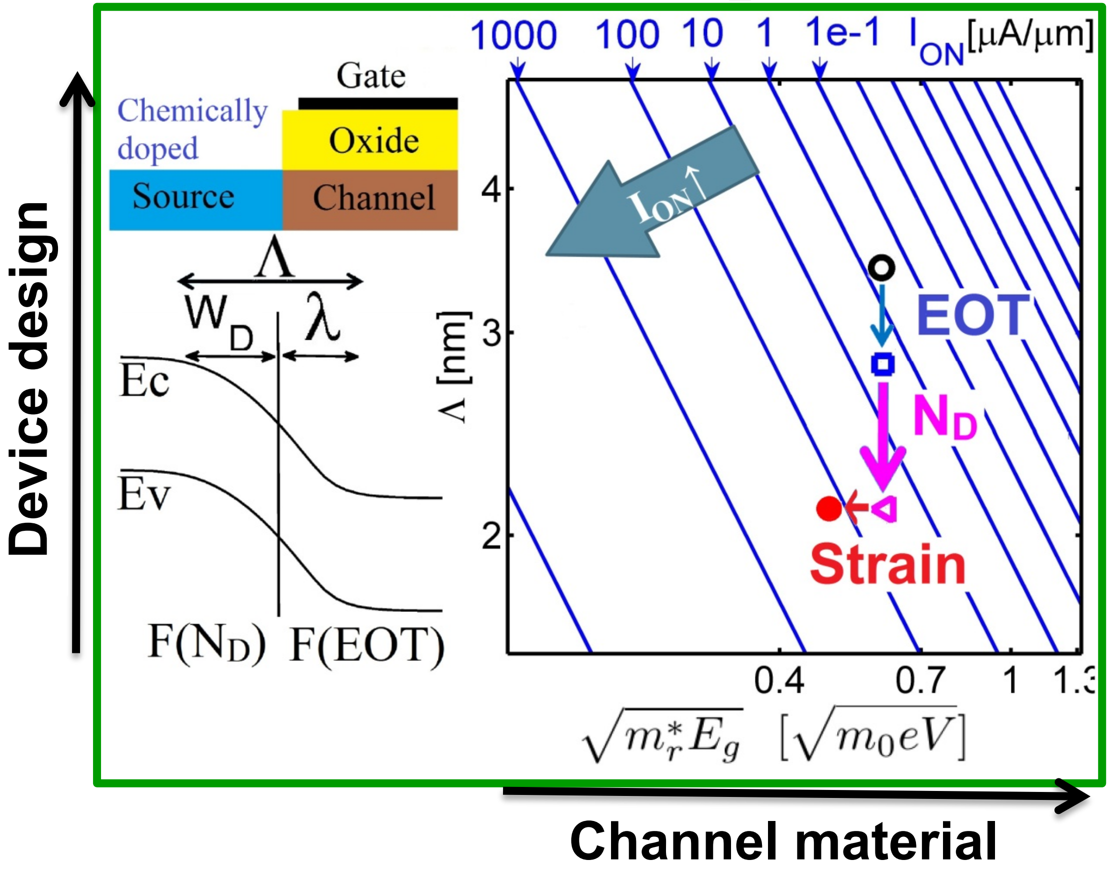
W_D

- W_D = function(N_D)

λ

- λ = function(EOT)

EOT↓ + Doping↑ + Strain↑



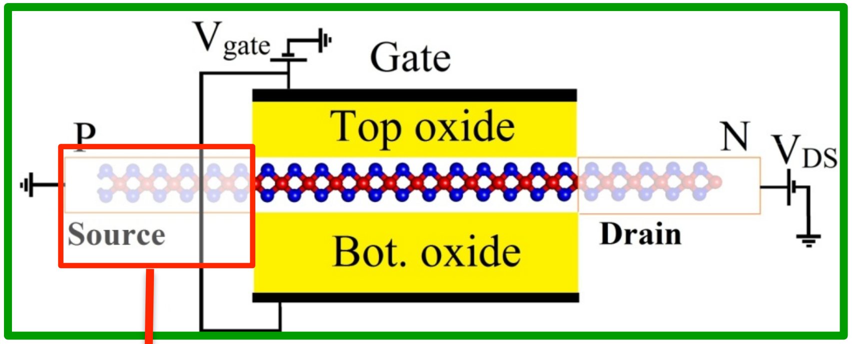
Design Rules for High Performance Tunnel Transistors from 2D Materials

Chemically doped TFETs
Non-idealities

Future work proposal:

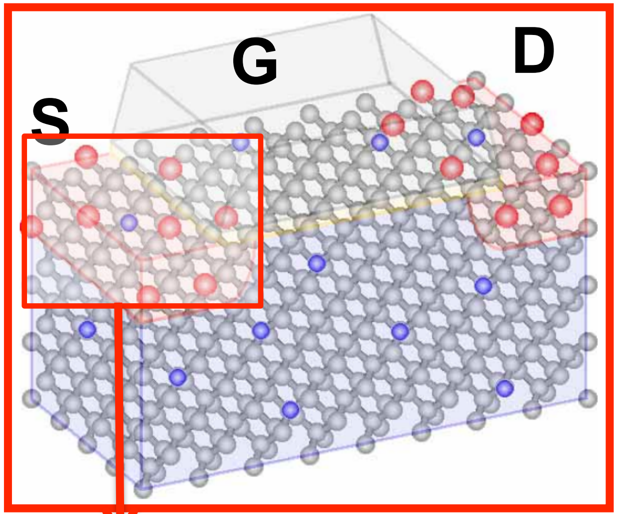
Systematic study of non-idealities such as atomistic dopants:

Uniform doping



All source atoms have same doping charge

Atomistic doping



Random dopants

Previously, effect of edge roughness on performance is studied.

SISPAD 2002. pp. 87-90. IEEE, 2002.

Chemically doped TFETs

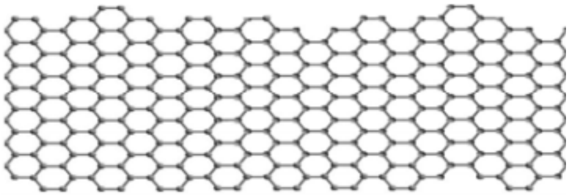
Non-idealities

Future work proposal

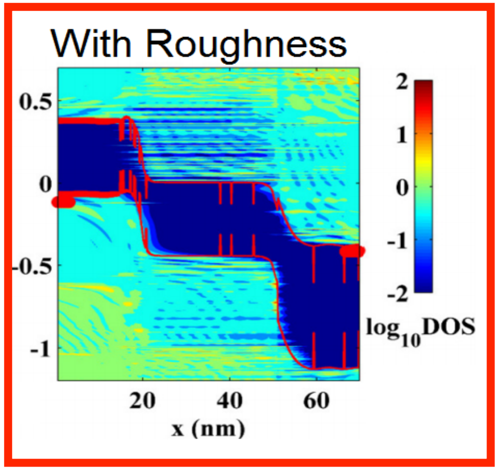
Previous works: roughness in graphene nano-ribbons

Edge roughness creates local states inside the band gap

Structure

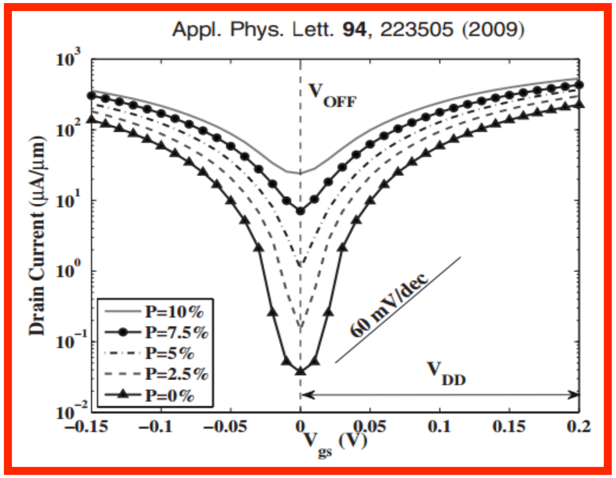


LDOS



Impact on IV

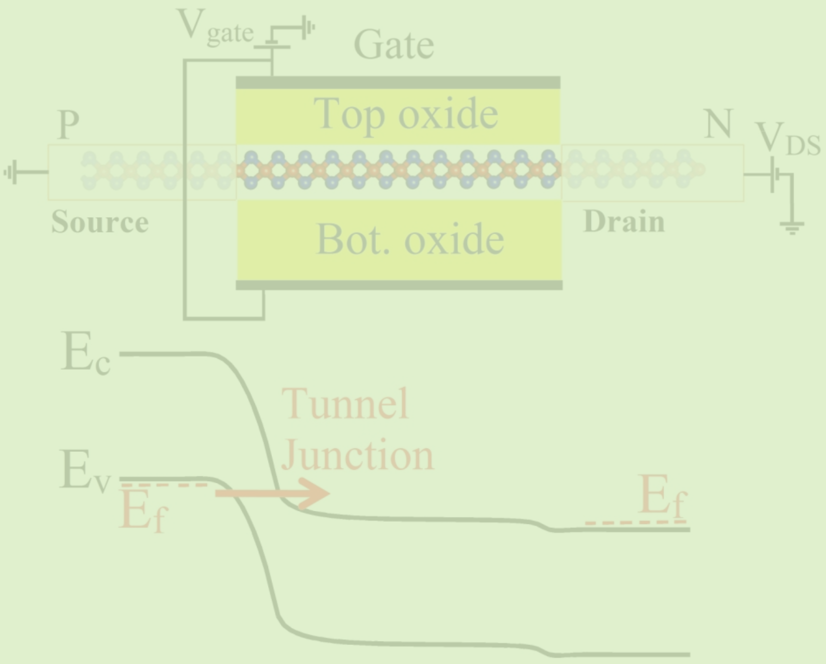
Appl. Phys. Lett. **94**, 223505 (2009)



Appl. Phys. Lett. **104**, 243113 (2014)

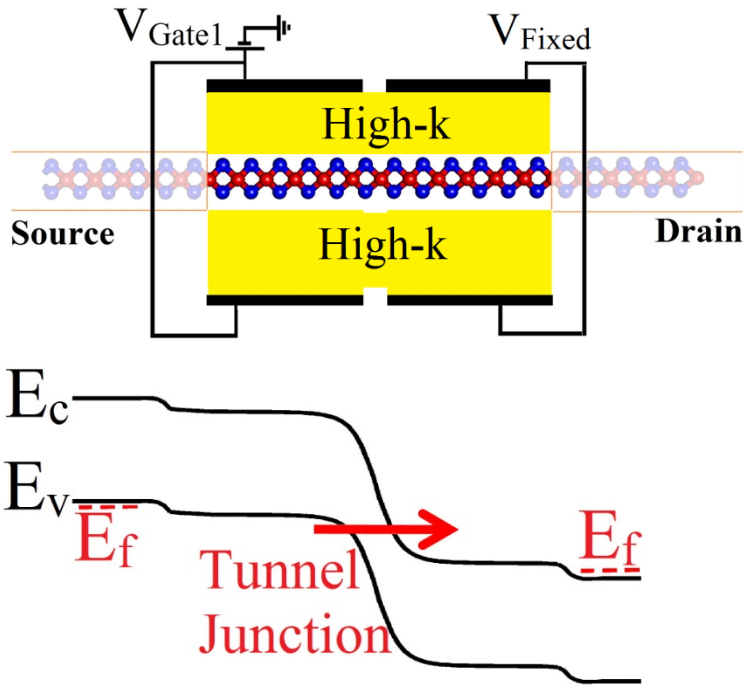
Methods to create tunnel junction

1) Chemically doped



Tunnel junction is between
a) Highly doped source
b) Channel

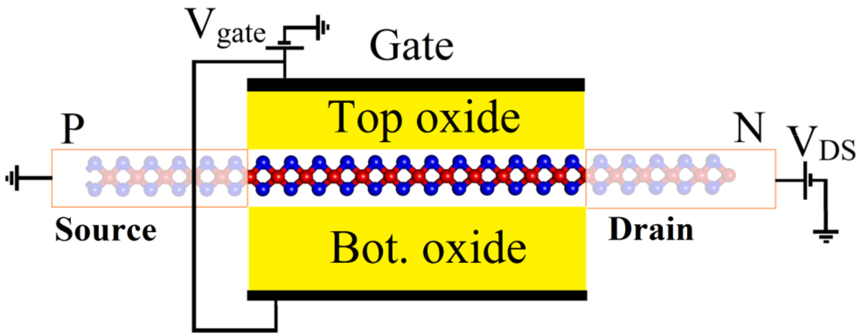
2) Electrically doped



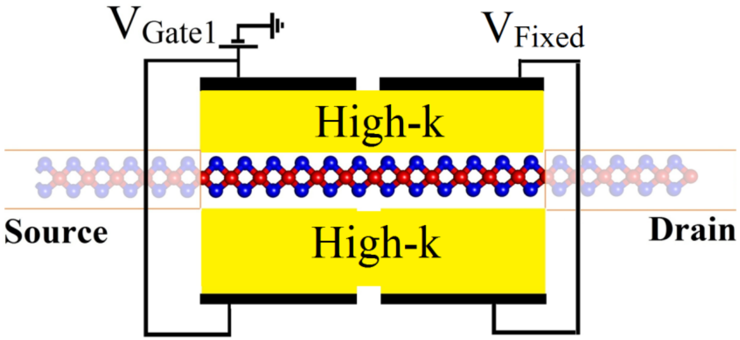
Advantage:
No dopant states within the bandgap
→ Good OFF-state performance

Expectations from electrically doped TFETs

1) Chemically doped



2) Electrically doped

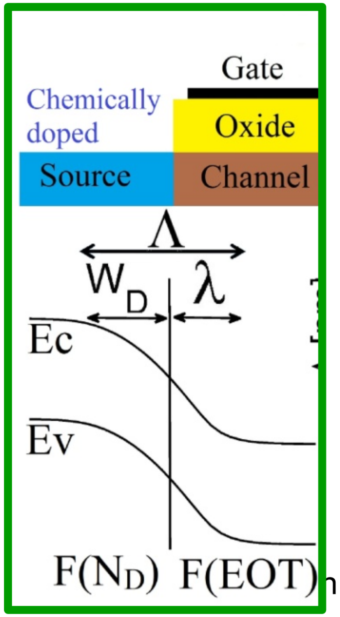


Performance analysis

a) $\lambda = f(\mathbf{EOT} \propto t_{ox}/\varepsilon_{ox})$

b) $W_D = f(N_D)$

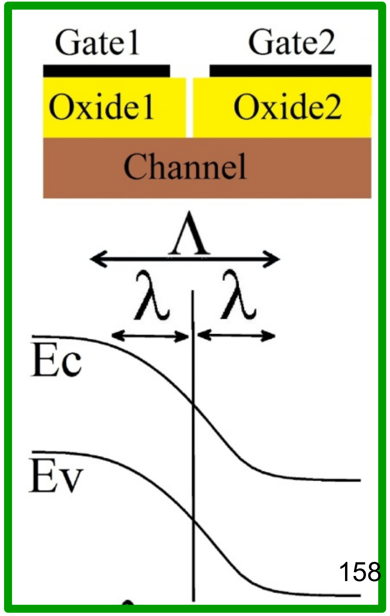
Advantage:
Increase ε_{ox} without reducing t_{ox} → better performance



Prediction:

a) $\lambda = f(\mathbf{EOT})$ **?**

✗



Electrically Doped TFET (ED-TFET)

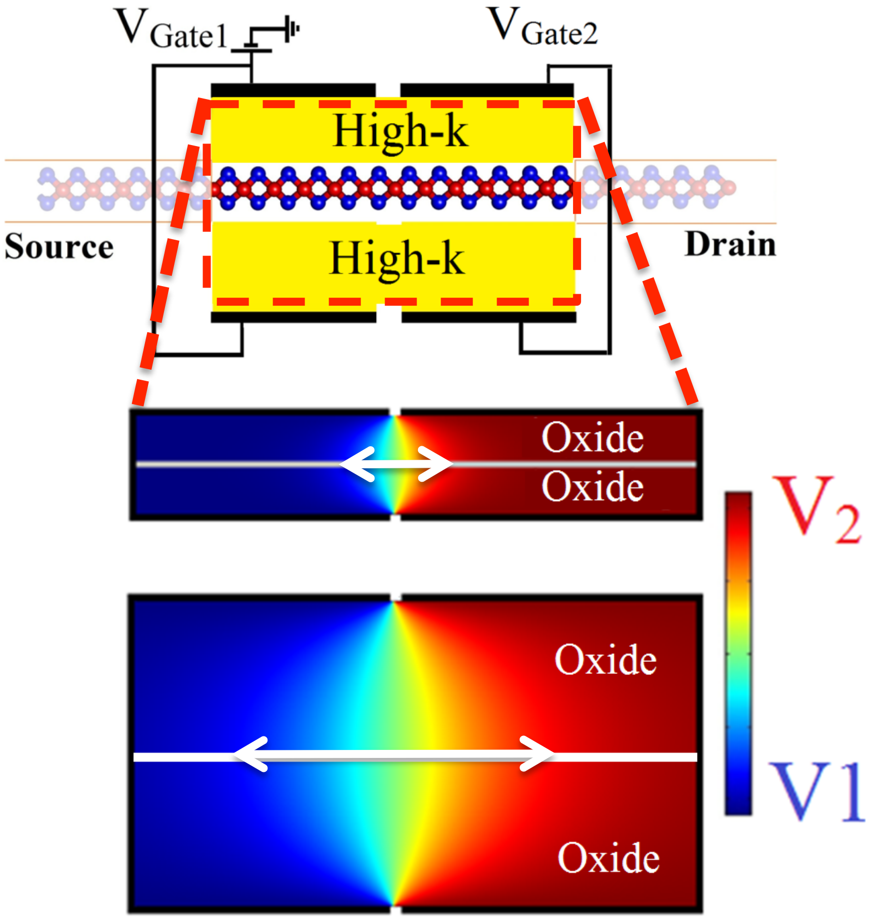
Potential profile

Comment

Structure

Thin oxide

Thick oxide



- **Width of potential spread ~ T_{tot}**

→ Thicker oxides have larger potential spread

Oxide thickness is the major factor

Hesameddin Ilatikhameneh

Electrically doped TFETs

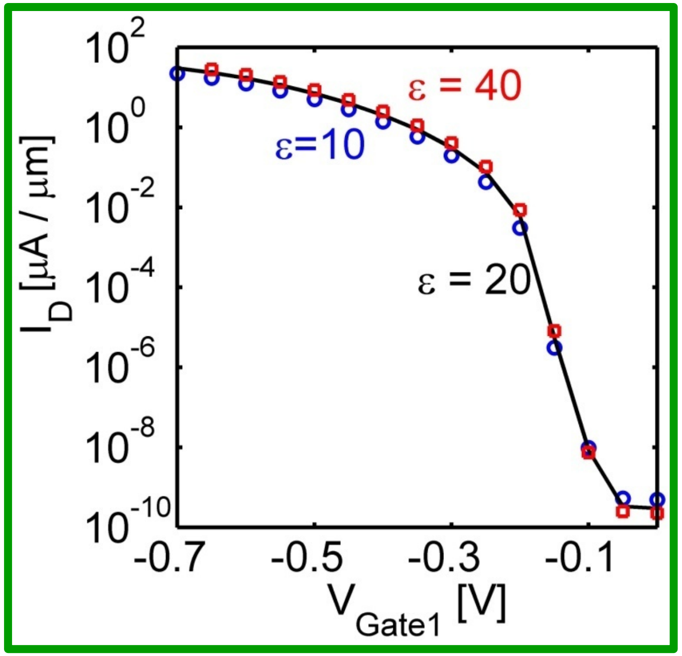
ε_{ox} versus thickness of oxide

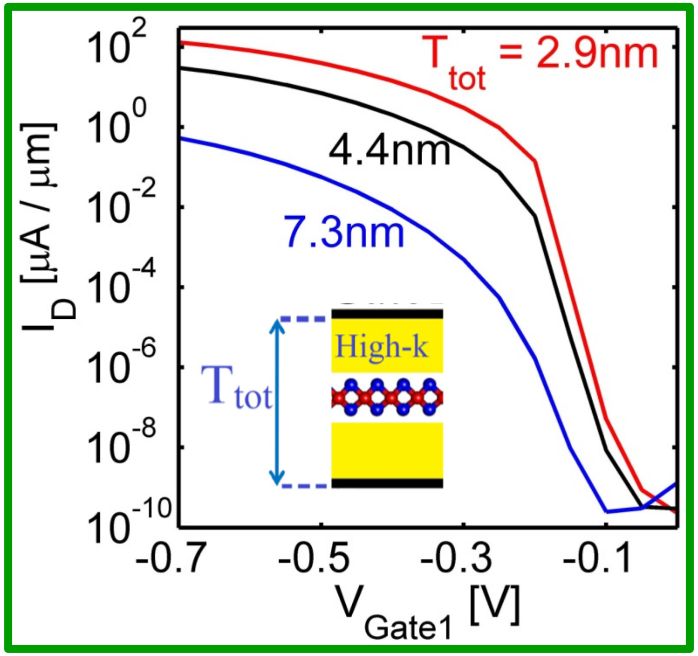
Oxide thickness is the major factor

Oxide ε

Oxide thickness

Illustration





Comments

- Independence of performance from oxide ε

- Strong dependence of performance on oxide thickness

SISPAD 2015

Electrically Doped WTe_2 Tunnel Transistors

Hesameddin Ilatikhameneh, Rajib Rahman, Joerg Appenzeller, and Gerhard Klimeck

Electrically doped TFETs

Scaling theory

- $\lambda \cancel{=} f(EOT \propto t_{ox}/\varepsilon_{ox})$

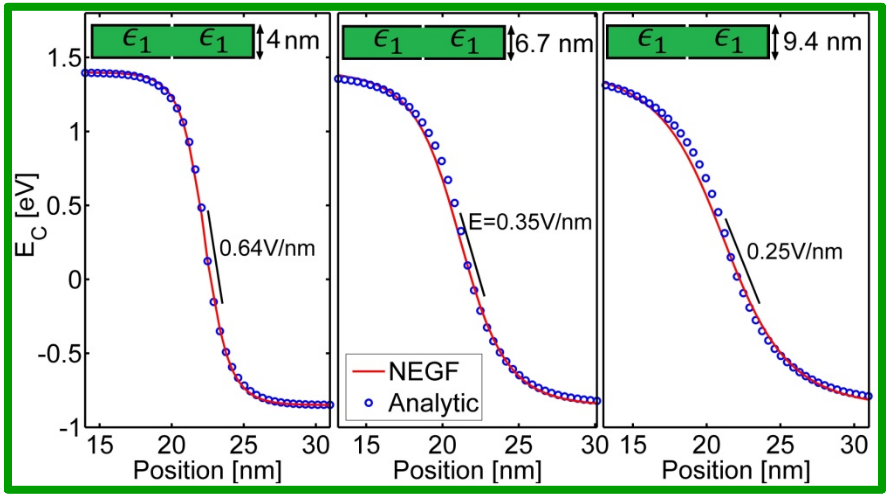
- Old scaling theory fails
- Need a new scaling theory

ED-TFET:
Analytic modeling

Potential profile

$$V(x) = \frac{V_1 - V_2}{2} exp\left(-\frac{(x - x_M)}{\lambda_{new}}\right) + V_2$$

Thin oxide…… to thick oxides



Scaling theory

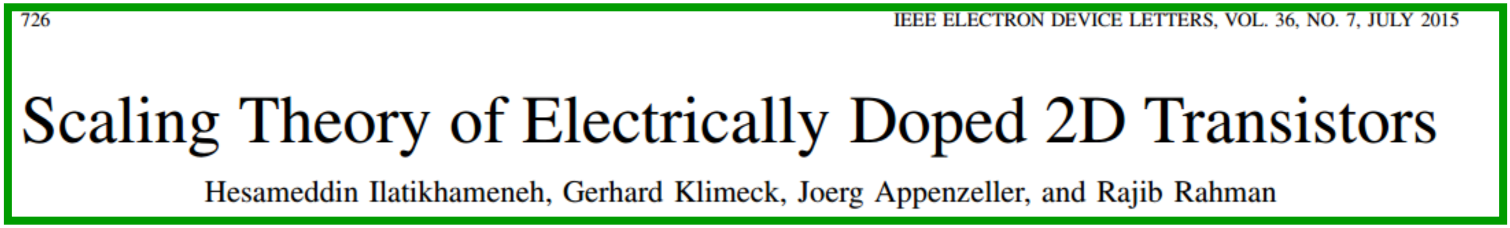
Electrically doped TFETs (New)

$$\lambda_{new} \approx \frac{2t_{ox}}{\pi} = f(t_{ox})$$

Chemically doped TFETs (Old)

$$\lambda_{old} \approx \sqrt{\frac{1}{2}\frac{t_{ox}}{\epsilon_{ox}}\epsilon_{ch}t_{ch}} = f(EOT \propto \frac{t_{ox}}{\epsilon_{ox}})$$

Analytic model confirms: oxide thickness is major factor



726 IEEE ELECTRON DEVICE LETTERS, VOL. 36, NO. 7, JULY 2015

Scaling Theory of Electrically Doped 2D Transistors

Hesameddin Ilatikhameneh, Gerhard Klimeck, Joerg Appenzeller, and Rajib Rahman

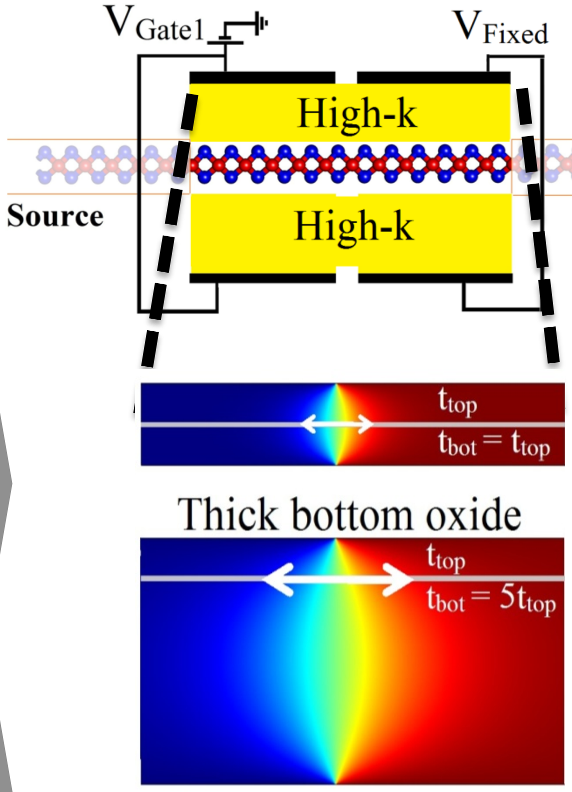
Electrically Doped TFETs

Structure

Thin oxide

Thick oxide

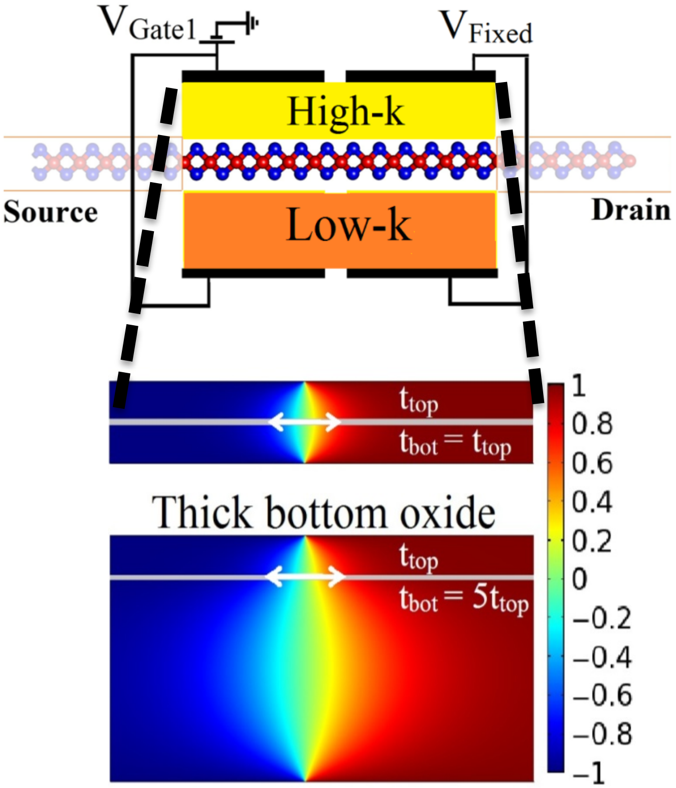
Problem



(b) $\epsilon_{top} = \epsilon_{bot}$

- Width of potential spread ~ T_{tot}

Solution



(c) $\epsilon_{top} = 10\ \epsilon_{bot}$

- Width of potential spread ~ t_{top}

A low-k dielectric should be used for thick back oxides

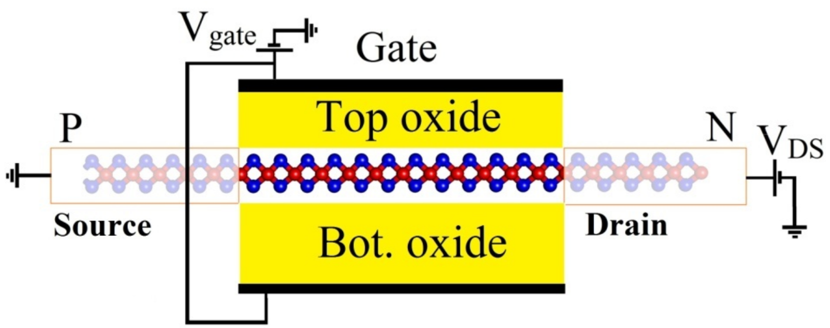
Future work

Future work proposal:

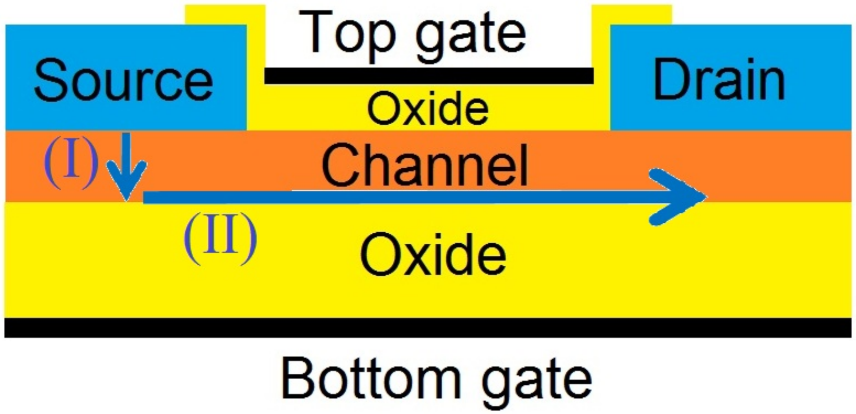
Simulation and analysis of device structures closer to the experimental setups (experiments by A. Prakash and T. Shen)

1) Contacts on top (not side) of 2D material
2) Strained channels

Simulation: side contacts



Experiment: contacts on top of channel



Review

Electrically Doped TFETs:

- Advantages:

  No chemical doping → Less dopant states
- Main challenge:

  $\lambda = f(t_{ox})$ → Higher ε_{OX} doesn't help.
- Solution:

  DE-TFET

Agenda

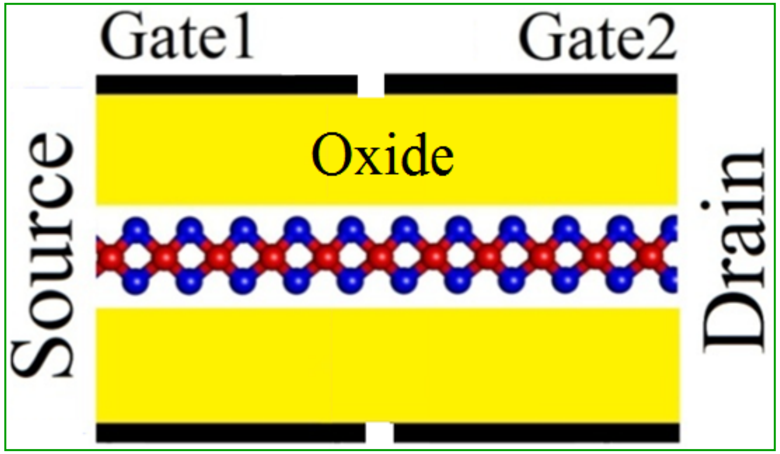
Dielectric Engineered TFET (DE-TFET)

DE-TFET vs ED-TFET

Structure

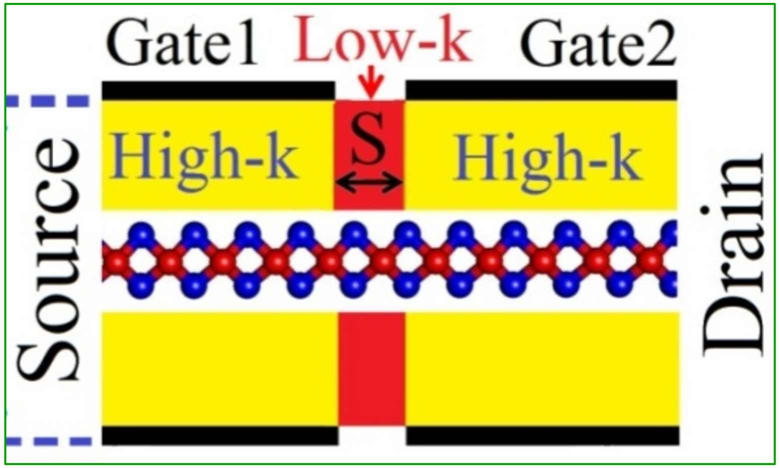
Conventional Electrically doped

(ED-TFET)



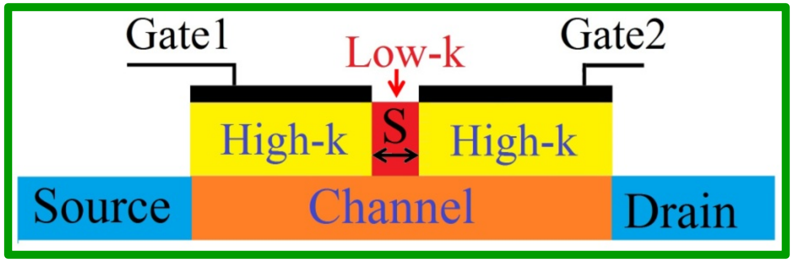
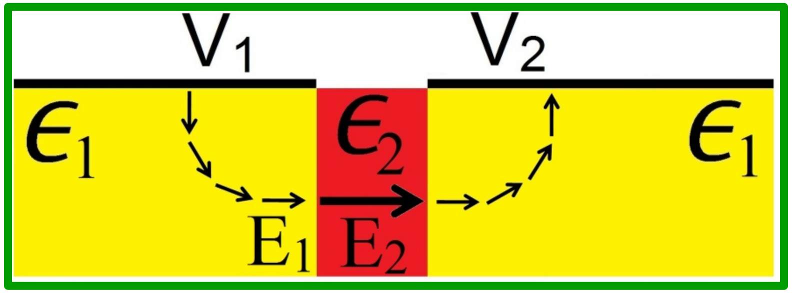
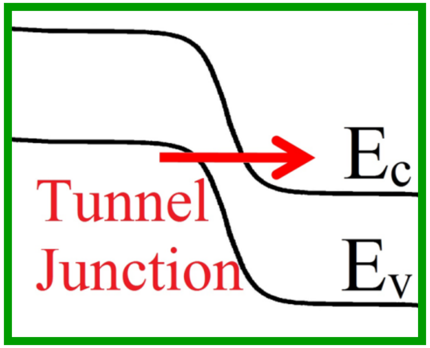
Dielectric engineered

(DE-TFET)



Dielectric Engineered TFET (DE-TFET)

Idea

	Illustration	Comments
Structure		- Combination of low-k and high-k dielectrics
Electric field amplification		$\epsilon_1 E_1 = \epsilon_2 E_2$ $\epsilon_2 \ll \epsilon_1 \rightarrow E_2 \gg E_1$
Result		- High electric field at the tunnel junction

Hesameddin Ilatikhameneh

Dielectric Engineered TFET (DE-TFET)
Idea

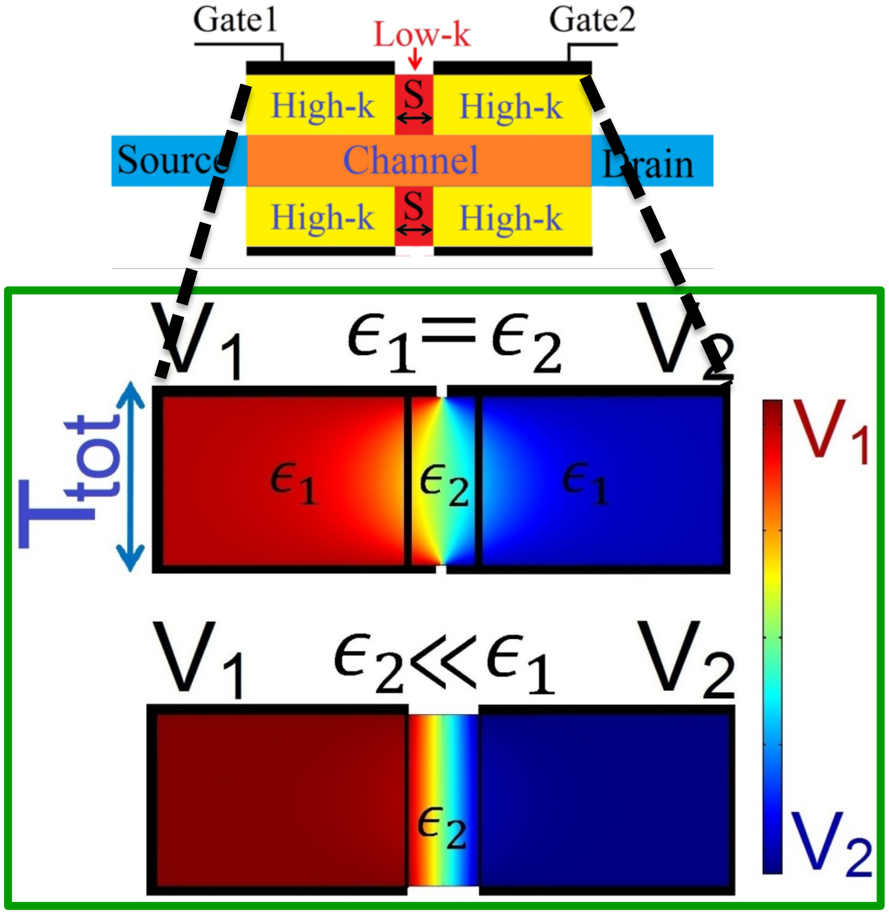
Potential profile

Electric field

Structure

Conventional ED-TFET

DE-TFET



- **Width of potential spread ~ T_{tot}**

$$\langle E_{ED-TFET} \rangle \approx \frac{\pi}{4} \frac{V_1 - V_2}{T_{tot}}$$

- **Potential drops over low-k**

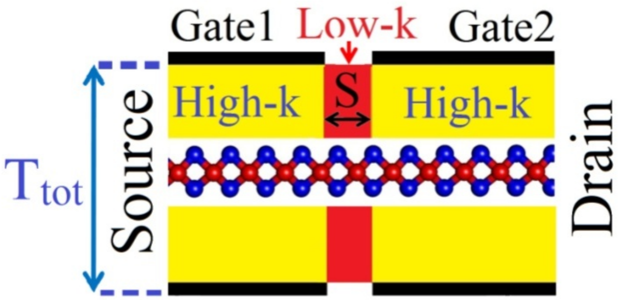
$$\langle E_{DE-TFET} \rangle \approx \frac{V_1 - V_2}{S}$$

Possible gain in electric field in DE-TFETs

Dielectric Engineered TFET (DE-TFET)
Performance

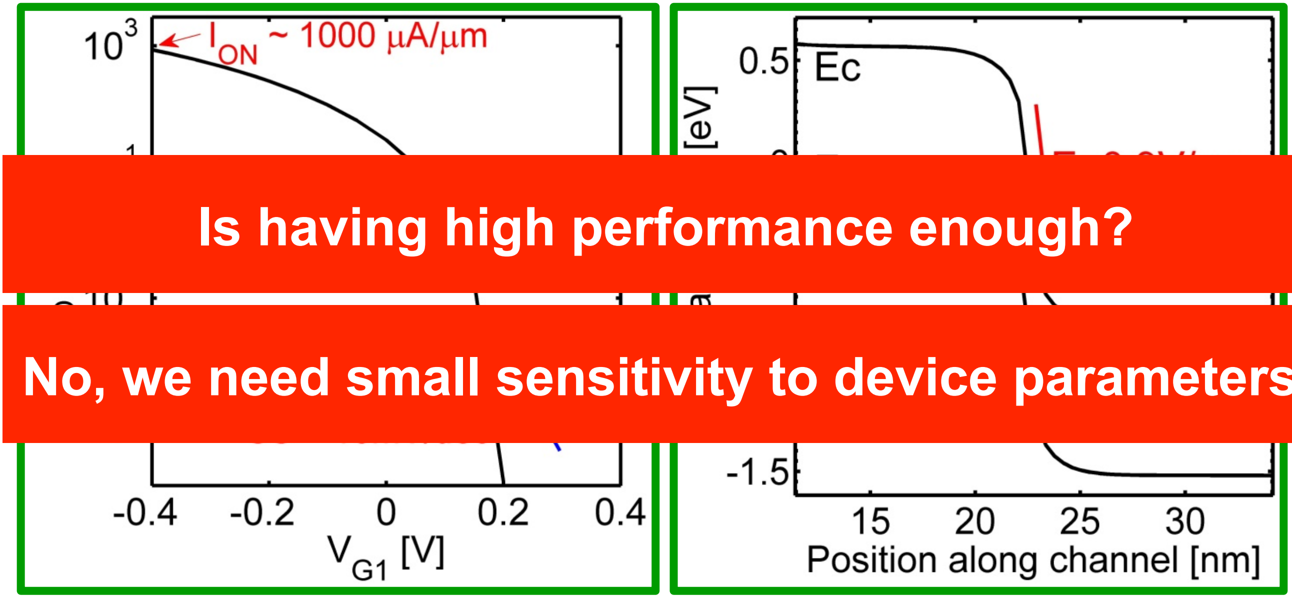
DE-TFET: High performance steep transistor

Structure



- Monolayer WTe_2 channel
- Gate2 = 1V (fixed)
- Low-k = air gap
- High-k = HfO_2

Atomistic simulation results



Is having high performance enough?

No, we need small sensitivity to device parameters

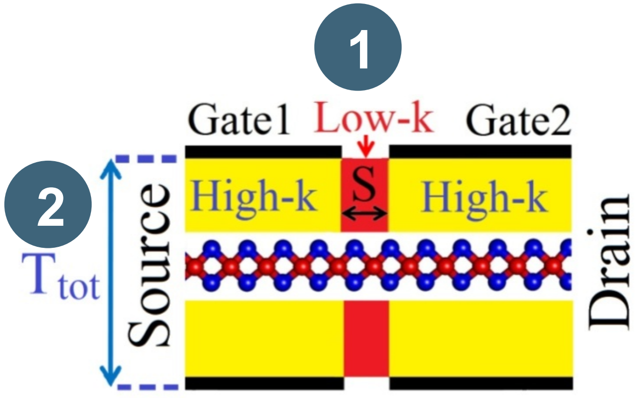
- I_{ON} is in the same level as ultra-scaled MOSFETs.
- SS = 16 mV/dec
- No chemical doping or heterostructure → No dopant or interface state

Dielectric Engineered TFET (DE-TFET)

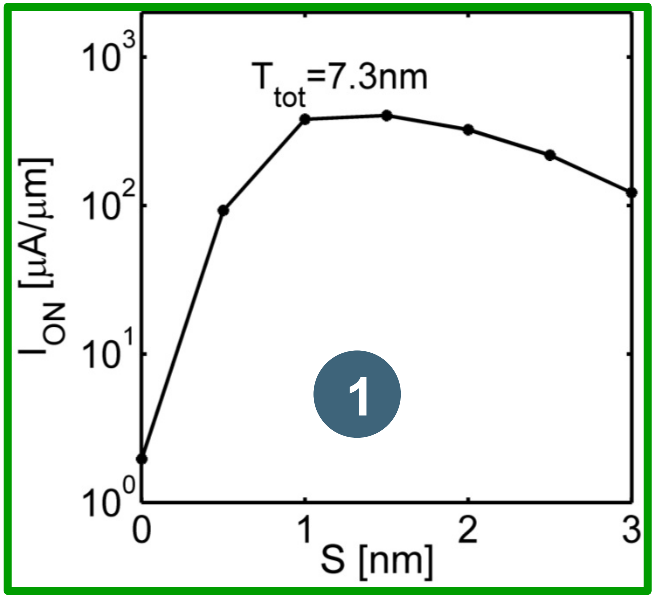
Sensitivity

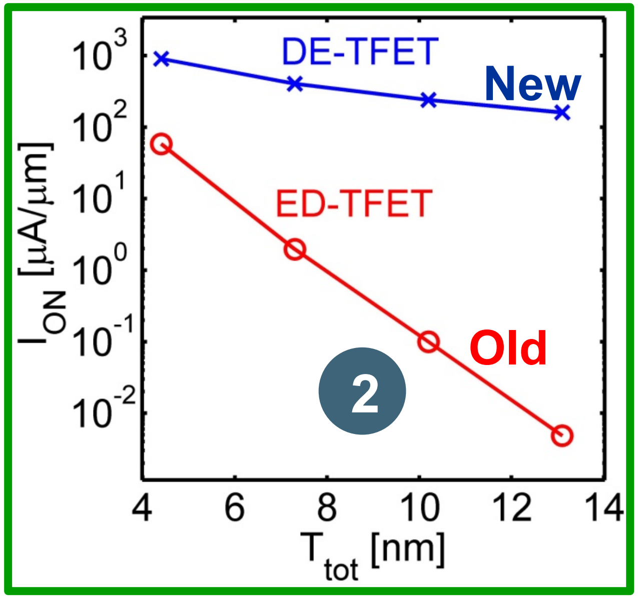
DE-TFET: Less sensitivity to the device dimensions

Structure



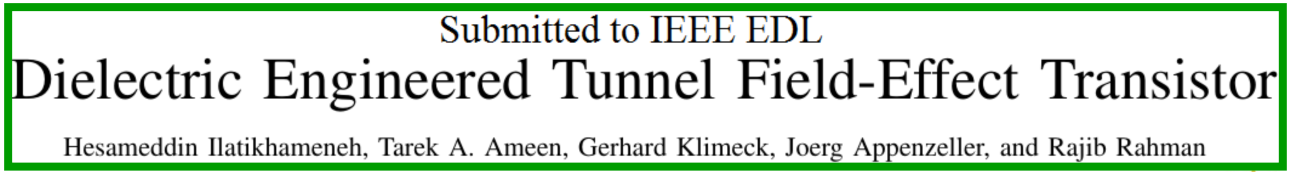
Atomistic simulation: sensitivity





- Monolayer WTe_2 channel
- Gate2 = 1V (fixed)
- Low-k = air gap
- High-k = HfO_2

- Less sensitivity to spacing and thickness of oxide compared to ED-TFETs



Submitted to IEEE EDL

Dielectric Engineered Tunnel Field-Effect Transistor

Hesameddin Ilatikhameneh, Tarek A. Ameen, Gerhard Klimeck, Joerg Appenzeller, and Rajib Rahman

DE-TFET
Analytical model

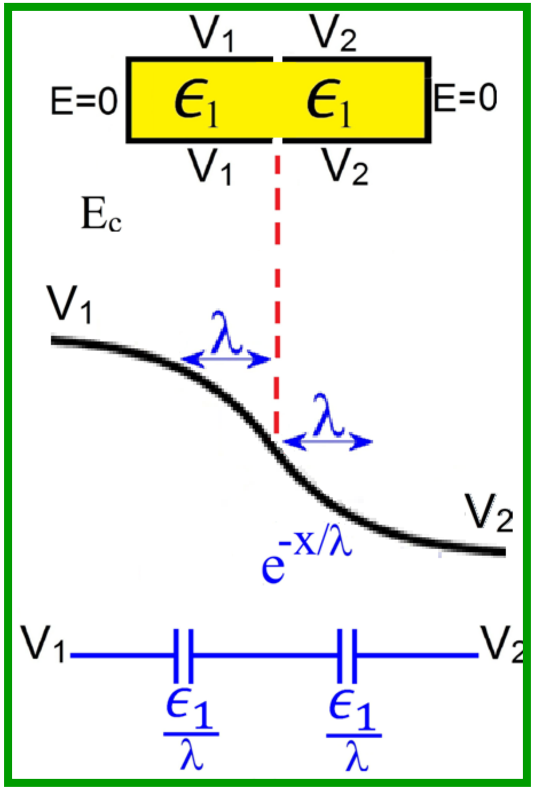
Analytical model

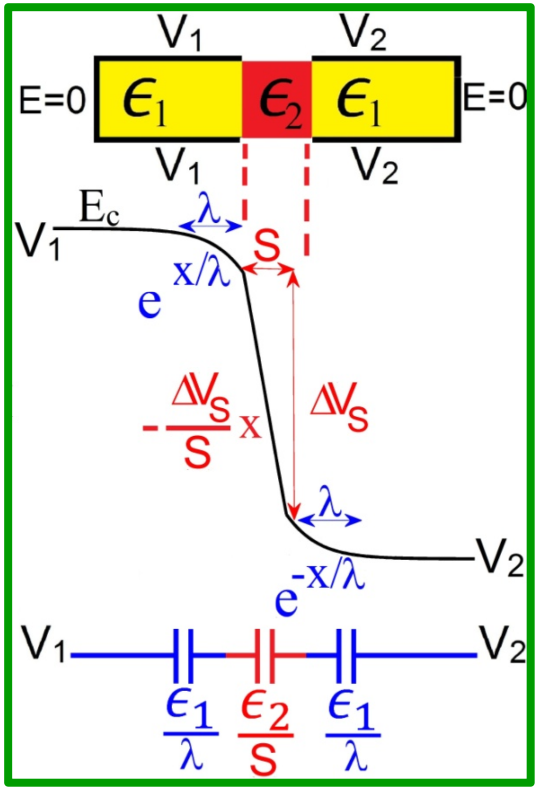
Electrically Doped TFET | **DE-TFET**

Simplified Structure

E_C

Equivalent circuit





Hesameddin Ilatikhameneh

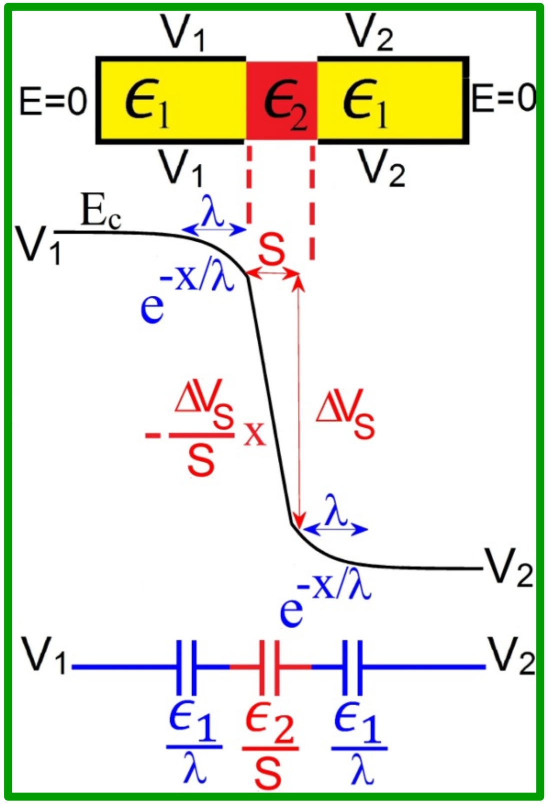
DE-TFET
Analytic modeling

Potential profile

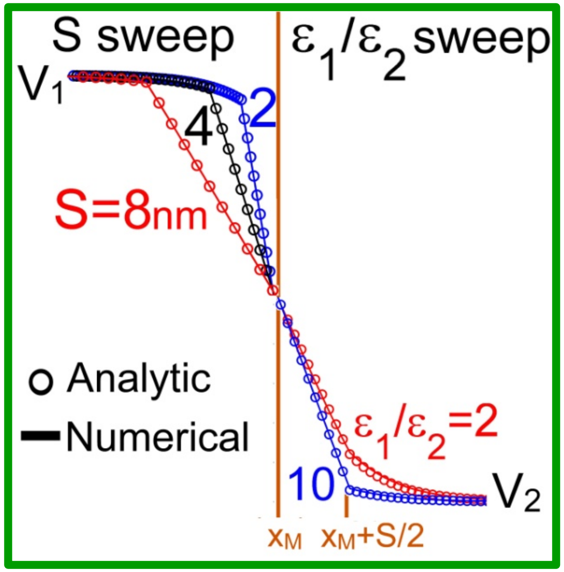
Simplified Structure

E_C

Equivalent circuit



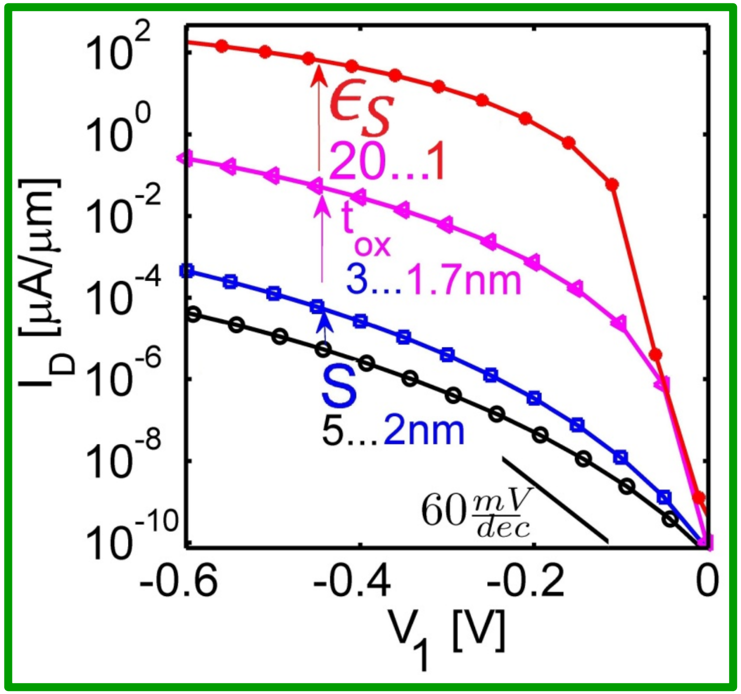
Numerical vs Analytic potential

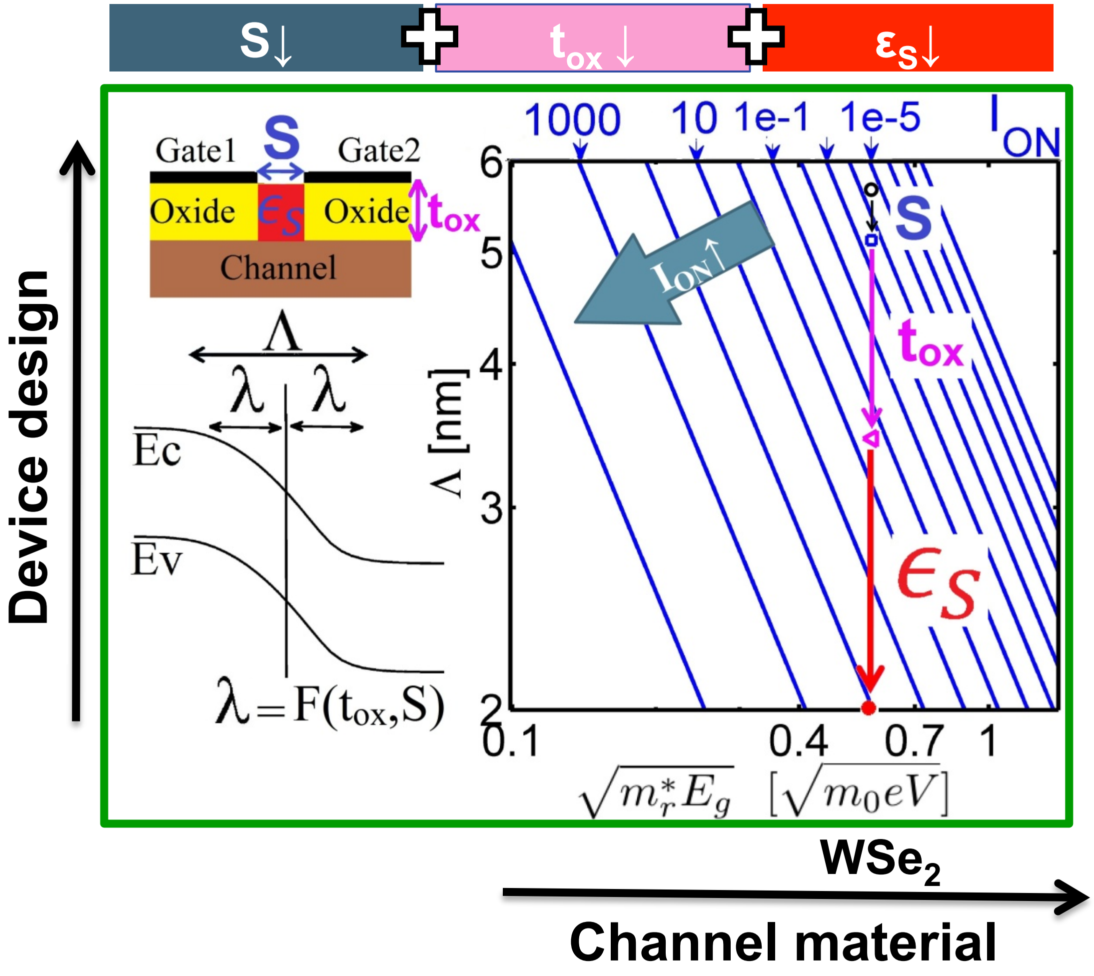


Good match

Electrically doped TFETs
Performance boosters

Analysis of performance boosters





λ

- λ = function(t_{ox}, S, ε_S)

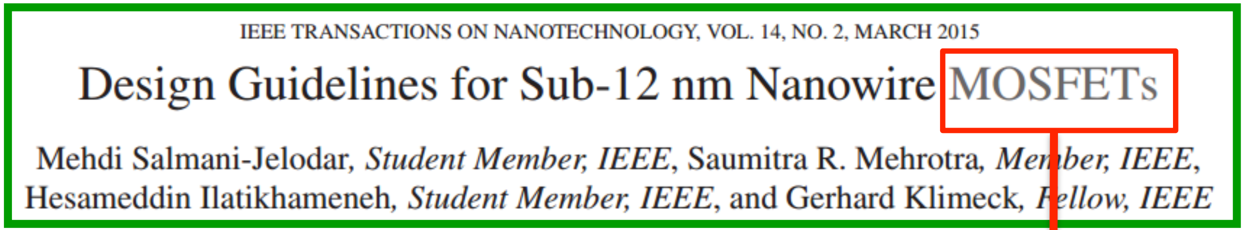
Design Rules for High Performance Tunnel Transistors from 2D Materials

DE-TFETs
Future work

Future work proposal for DE-TFET:

1) **Optimize the device:**
- For low V_{dd} applications
- Find the best channel material and geometry (e.g. nanowires)

2) **Provide a road-map:**
- Make a generation of optimized DE-TFETs (L_{ch} = 15nm to L_{ch} = 5nm)

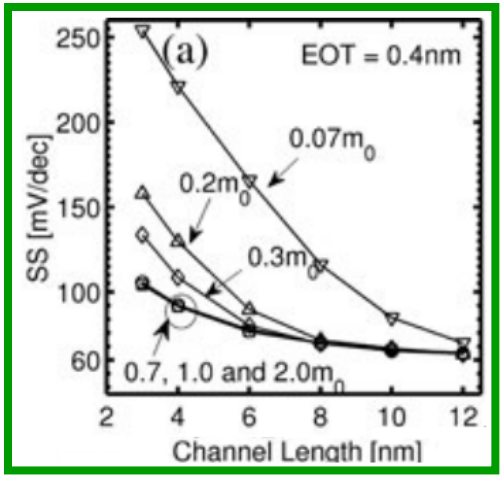


IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 14, NO. 2, MARCH 2015

Design Guidelines for Sub-12 nm Nanowire MOSFETs

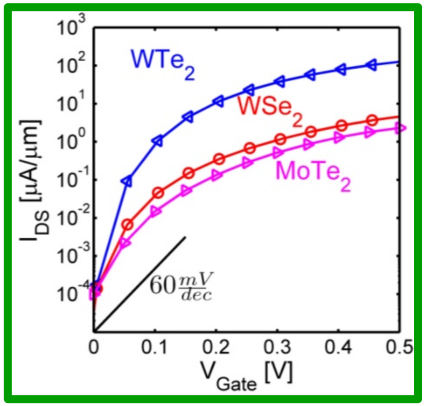
Mehdi Salmani-Jelodar, *Student Member, IEEE*, Saumitra R. Mehrotra, *Member, IEEE*, Hesameddin Ilatikhameneh, *Student Member, IEEE*, and Gerhard Klimeck, *Fellow, IEEE*

DE-TFETs

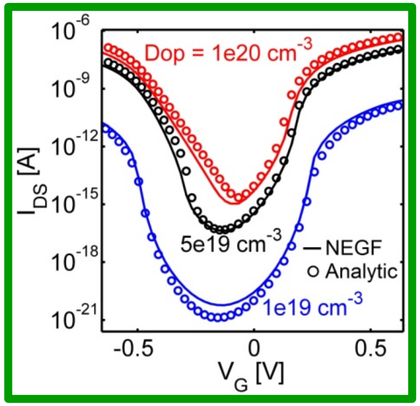


Summary

Atomistic modeling



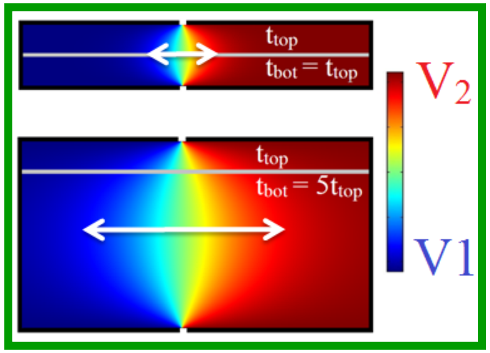
Corrected U(x) + WKB



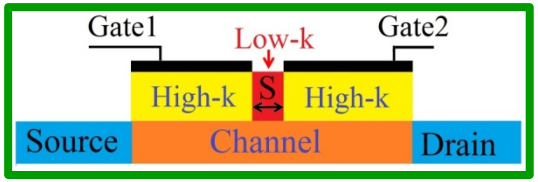
$$T^{Elliptic} = exp\left(-\frac{\pi}{qF}\frac{\sqrt{m_r^* E_g^{3/2}}}{2\hbar}\right)$$

Develop Scaling theory

$$\lambda_{new} \approx \frac{2t_{ox}}{\pi} = f(t_{ox})$$



Propose New devices



Other works:

Strain + Phonons

T. Ameen
K. Miao

Quantum transport + tunneling

B. Novakovich
A. Ajoy
NEMO5 team

Generic Mode-space

J. Huang

Backup slides

Backup Slides

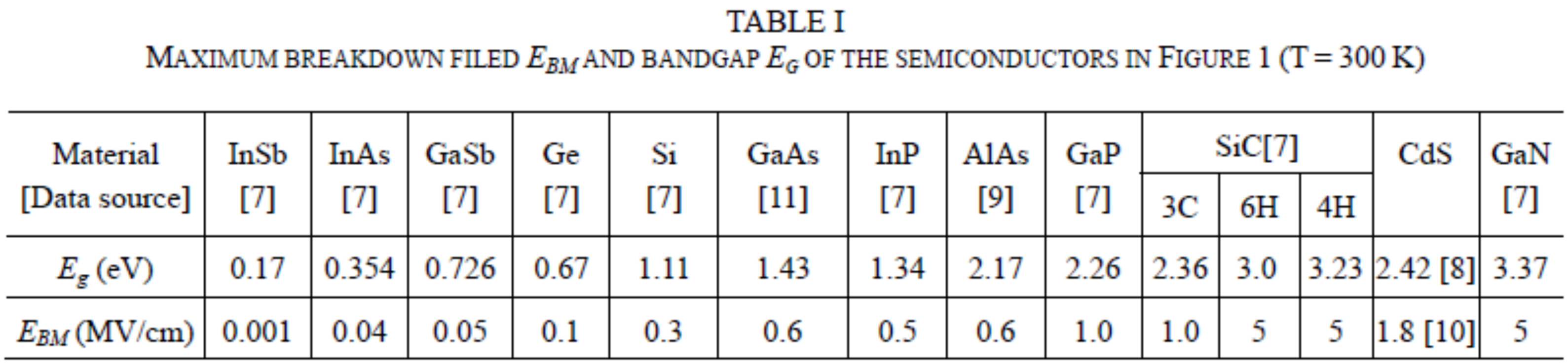
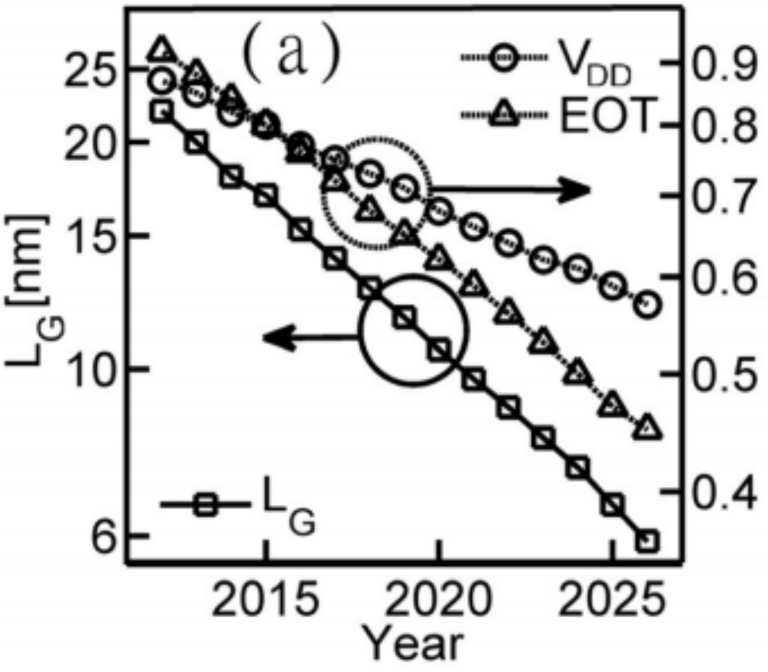
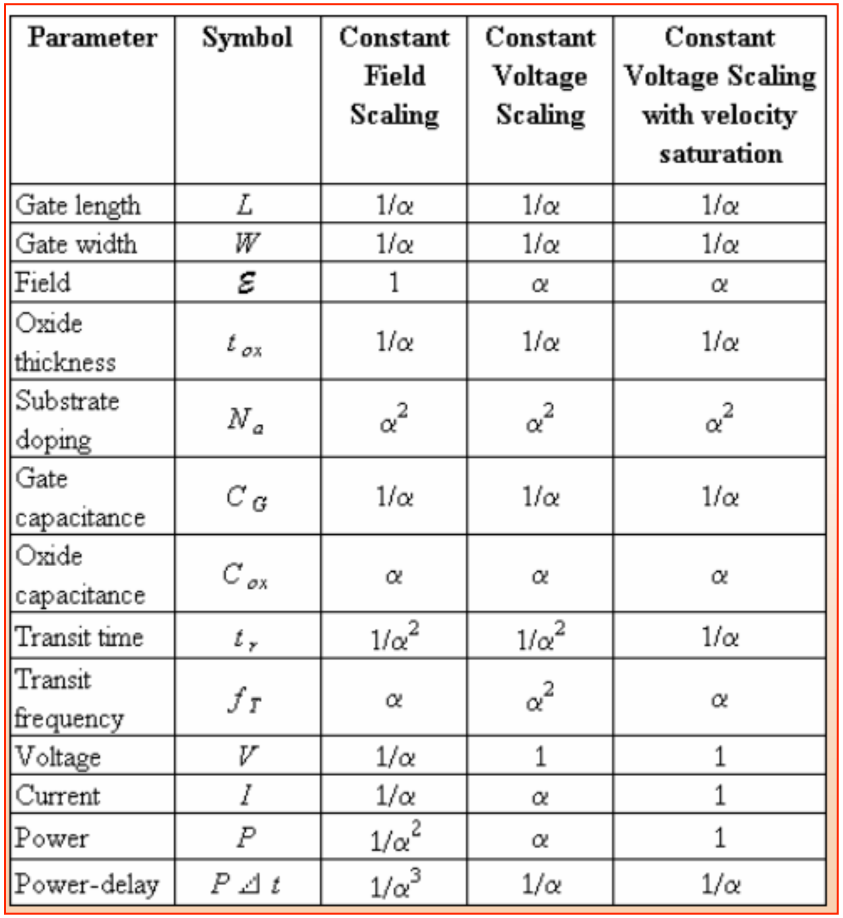


TABLE I
MAXIMUM BREAKDOWN FILED E_{BM} AND BANDGAP E_G OF THE SEMICONDUCTORS IN FIGURE 1 (T = 300 K)

Material [Data source]	InSb [7]	InAs [7]	GaSb [7]	Ge [7]	Si [7]	GaAs [11]	InP [7]	AlAs [9]	GaP [7]	SiC[7]			CdS	GaN [7]
										3C	6H	4H		
E_g (eV)	0.17	0.354	0.726	0.67	1.11	1.43	1.34	2.17	2.26	2.36	3.0	3.23	2.42 [8]	3.37
E_{BM} (MV/cm)	0.001	0.04	0.05	0.1	0.3	0.6	0.5	0.6	1.0	1.0	5	5	1.8 [10]	5

Appl. Phys. Lett. **105**, 083508 (2014)

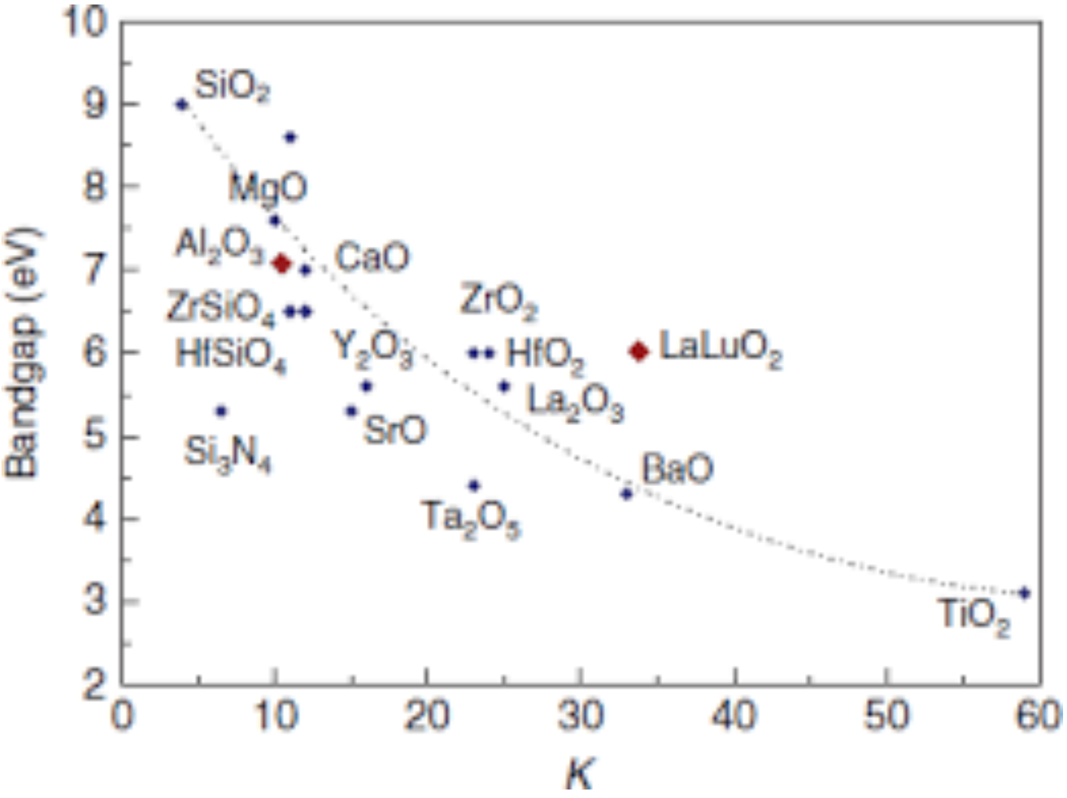


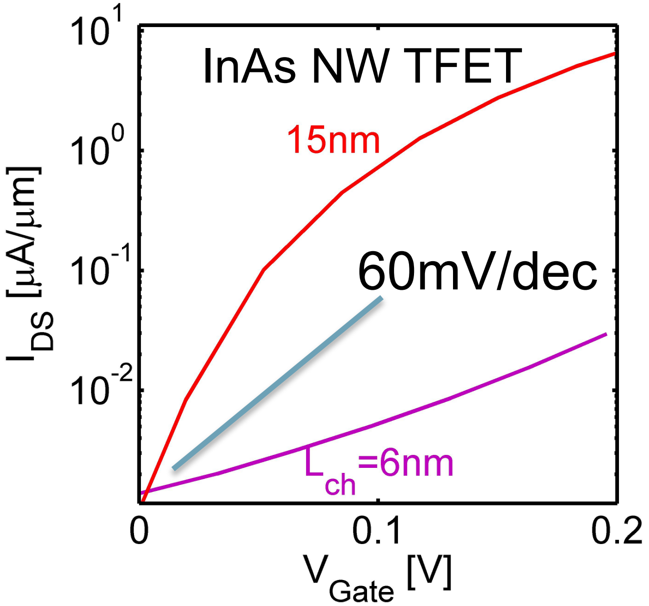


Parameter	Symbol	Constant Field Scaling	Constant Voltage Scaling	Constant Voltage Scaling with velocity saturation
Gate length	L	$1/\alpha$	$1/\alpha$	$1/\alpha$
Gate width	W	$1/\alpha$	$1/\alpha$	$1/\alpha$
Field	$\mathcal{E}$	1	α	α
Oxide thickness	t_{ox}	$1/\alpha$	$1/\alpha$	$1/\alpha$
Substrate doping	N_a	α^2	α^2	α^2
Gate capacitance	C_G	$1/\alpha$	$1/\alpha$	$1/\alpha$
Oxide capacitance	C_{ox}	α	α	α
Transit time	t_r	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha$
Transit frequency	f_T	α	α^2	α
Voltage	V	$1/\alpha$	1	1
Current	I	$1/\alpha$	α	1
Power	P	$1/\alpha^2$	α	1
Power-delay	$P \Delta t$	$1/\alpha^3$	$1/\alpha$	$1/\alpha$

http://www.leb.eei.uni-erlangen.de/winterakademie/2006/result/content/course03/pdf/0306.pdf

Materials **2014**, *7*(4), 2913-2944; doi:10.3390/ma7042913 *Review*
Emerging Applications for High K Materials in VLSI Technology Robert D. Clark
TEL Technology Center, America, LLC, NanoFab South 3

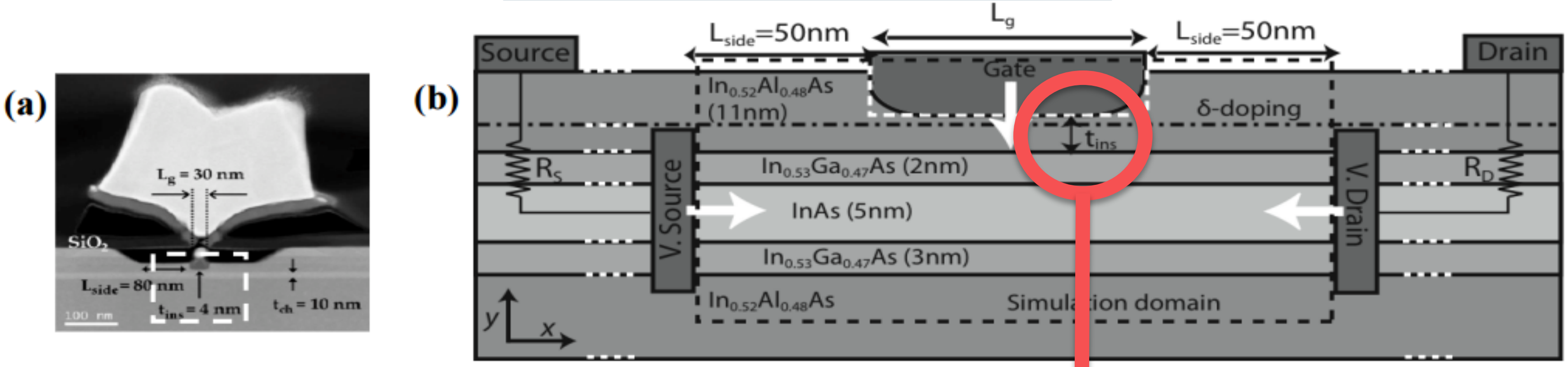



InAs NW TFET
15nm
60mV/dec
L_{ch}=6nm
I_{DS} [μA/μm]
10^{1}
10^{0}
10^{-1}
10^{-2}
0
0.1
0.2
V_{Gate} [V]

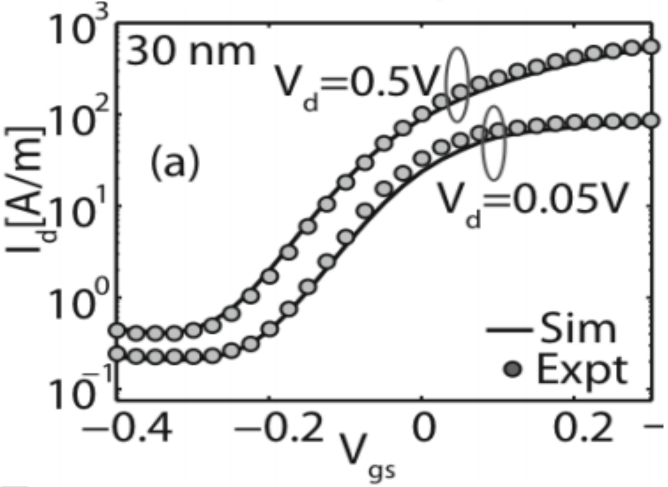
Quantum transport: 1) device optimization

Simulation of III-V HEMTs → Match with experiment
→ Fast optimization

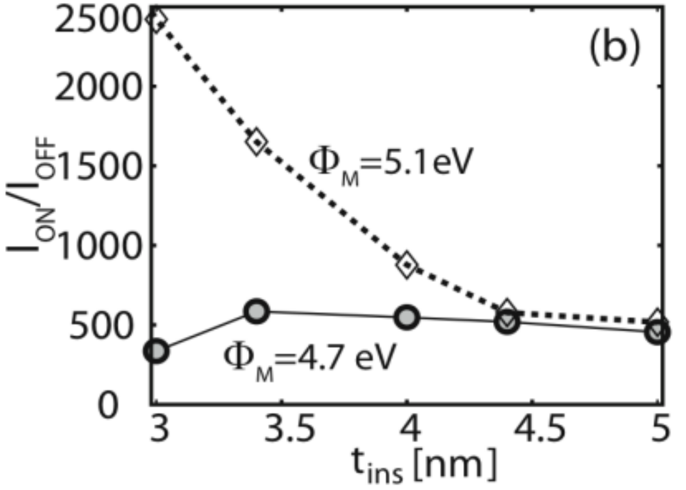
Device structure



Match w/ experiment



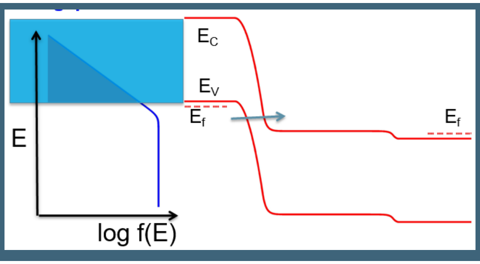
Optimization



Agenda

Introduction

1) Motivation for steep transistors
2) Requirements for steep tunnel transistors



Atomistic quantum transport simulation

1) Device geometry optimization
2) Scattering impact
3) Verify and extend analytic models

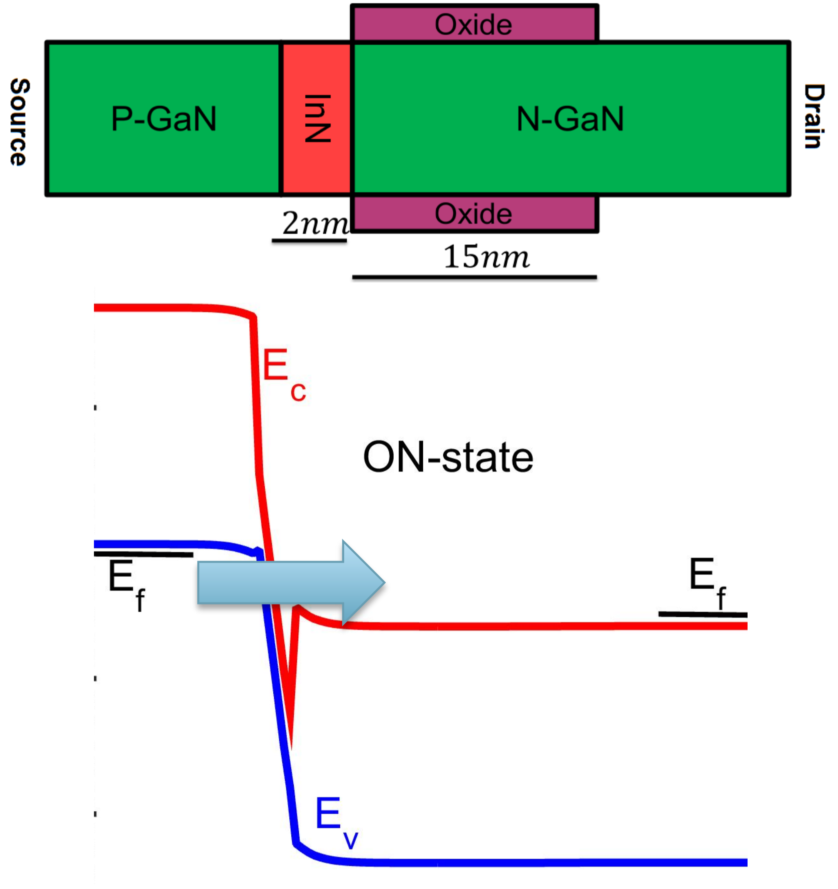
Tunnel transistors

1) III-V materials
2) 2D materials
3) Best materials for scaling challenge

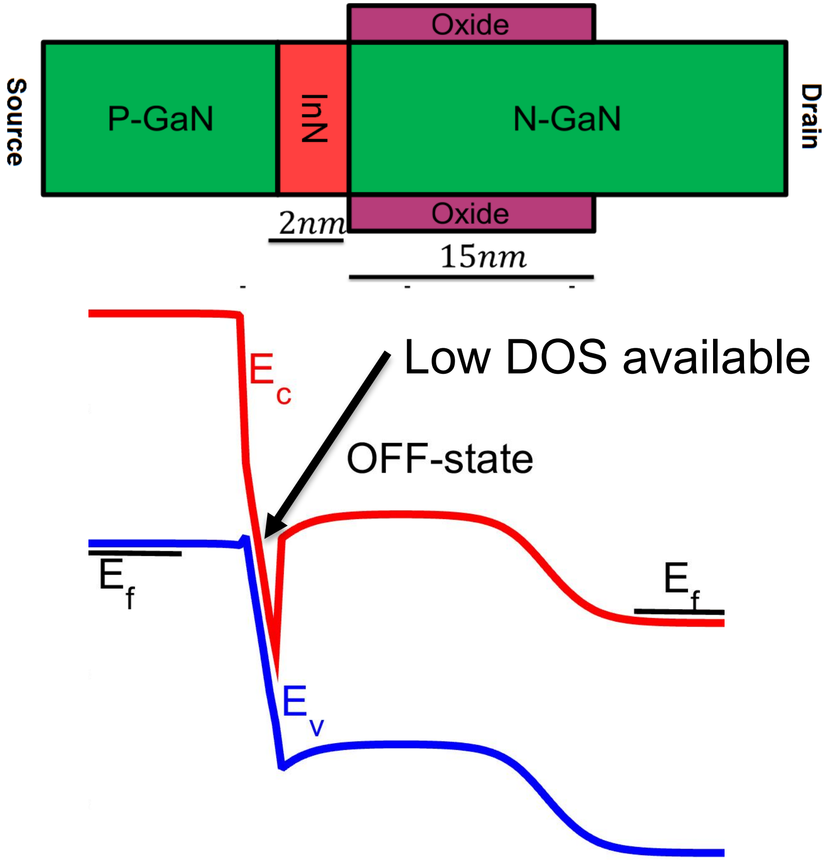
Challenge of broken gap III-V TFETs

Solution: Nitride Hetero-structure

ON: Tunneling through small gap InN



OFF: Tunneling through large gap GaN



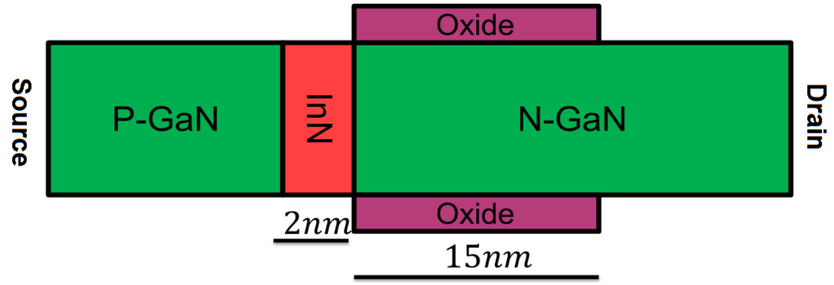
Polarization-Engineered III-Nitride Heterojunction Tunnel Field-Effect Transistors

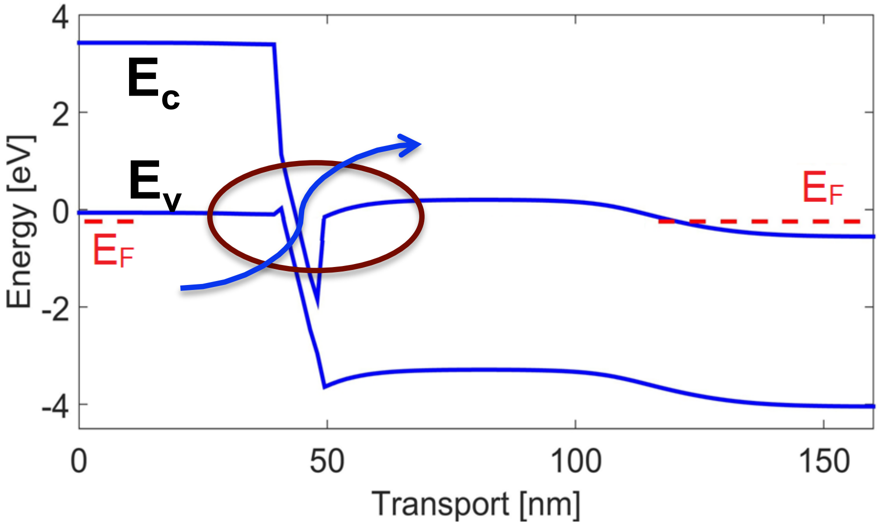
WENJUN LI[1], SAIMA SHARMIN[2], HESAMEDDIN ILATIKHAMENEH[2], RAJIB RAHMAN[2],
YEQING LU[3], JINGSHAN WANG[1], XIAODONG YAN[1], ALAN SEABAUGH[1] (Fellow, IEEE),
GERHARD KLIMECK[2] (Fellow, IEEE), DEBDEEP JENA[1] (Senior Member, IEEE),
AND PATRICK FAY[1] (Senior Member, IEEE)

Solution: Nitride Heterostructure TFETs

Why SS < 60 mV/dec can be achieved in Nitride TFETs?

Device structure

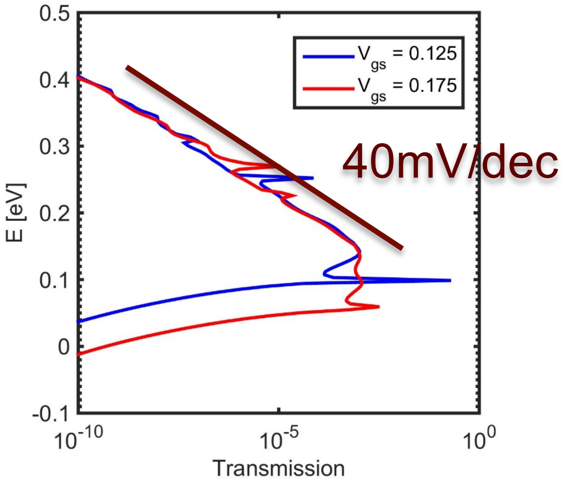




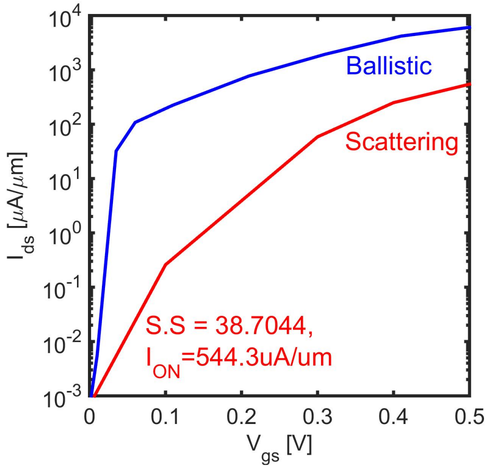
Reduced thermionic injection

Atomistic simulation results

Transmission



I-V



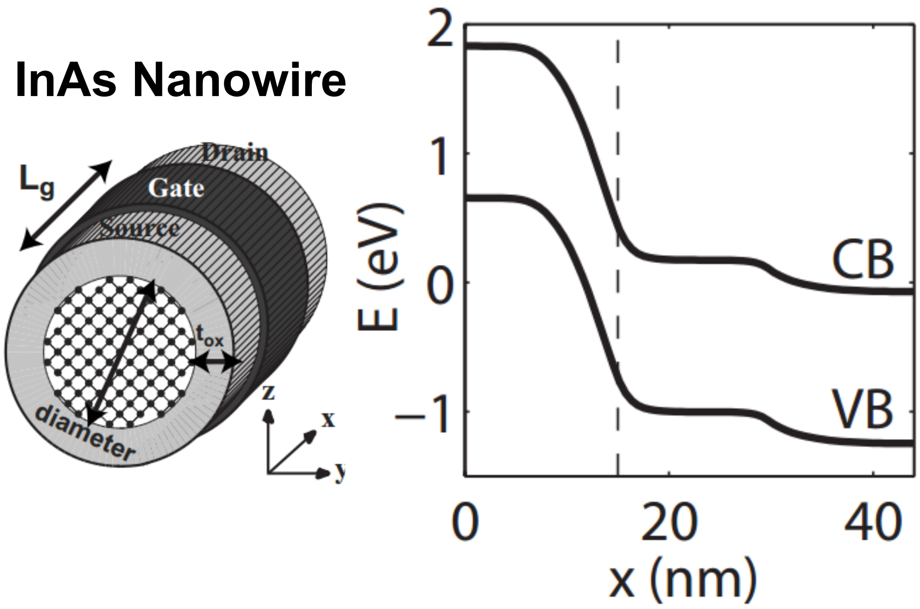
Quantum transport: 2) Important physics

Question: Does scattering affect the performance of TFET?

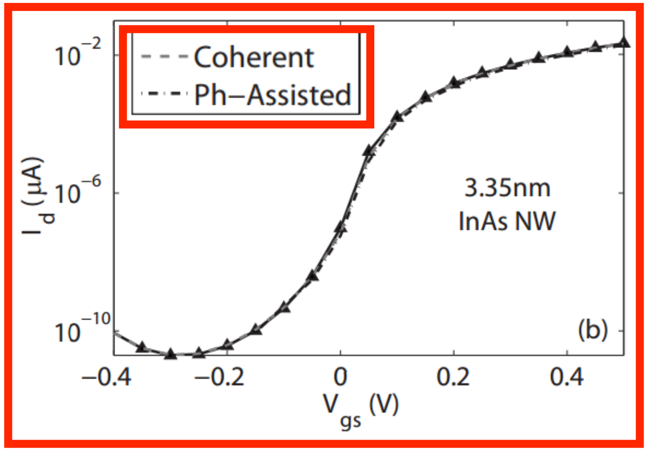
Homojunction TFET

Device structure – band diagram

InAs Nanowire



Output



Scattering has NO impact on homojunction TFETs w/ direct gap materials.

JOURNAL OF APPLIED PHYSICS **107**, 084507 (2010)

Simulation of nanowire tunneling transistors: From the Wentzel–Kramers–Brillouin approximation to full-band phonon-assisted tunneling

Mathieu Luisier[a] and Gerhard Klimeck