# Multi-scale simulations for high performance low power nanoelectronic devices

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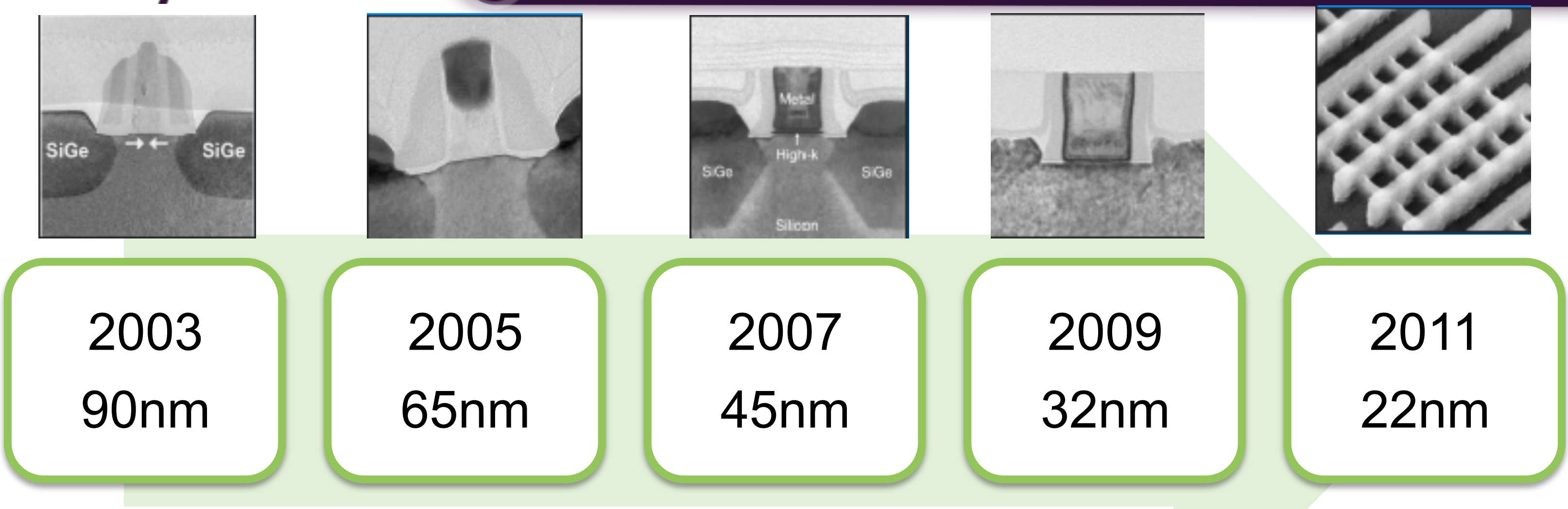
# Outline

- Scaling of MOSFET
  - » Impact
  - » Improve electrostatics, increase mobility, reduce leakage
- Device design beyond MOSFET
  - » Motivations
  - » Challenges
- Multi-scale simulations
  - » TFET
  - » Piezoelectronic Transistor
  - » CBRAM
  - » Cu grain boundary
- Summary

# Then and Now

http://www.nydailynews.com/news/world/check-contrasting-pics-st-peter-square-article-1.1288700
http://abc7ny.com/entertainment/marty-mcfly-and-doc-brown-time-travel-to-jimmy-kimmel-live/1045057/

# Success of Moore's Law



2003
90nm

2005
65nm

2007
45nm

2009
32nm

2011
22nm

Personal Electronics

Google data center (http://www.google.com/about/datacenters/gallery/#/all/20)

data center HPC

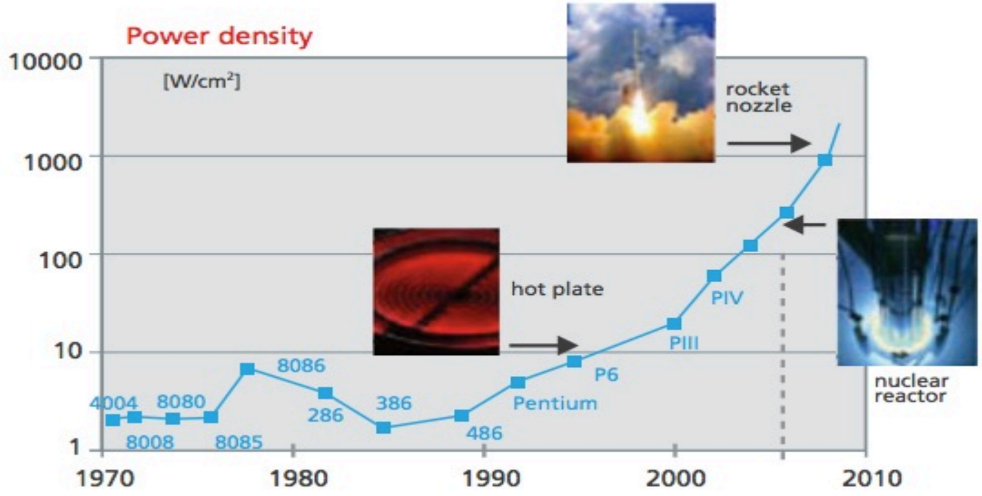
HPC Tianhe-2
http://bit.ly/11fwqLq

Scaling of transistor has changed our life style!

# Behind Moore's Law: Challenge - Reduce power dissipation

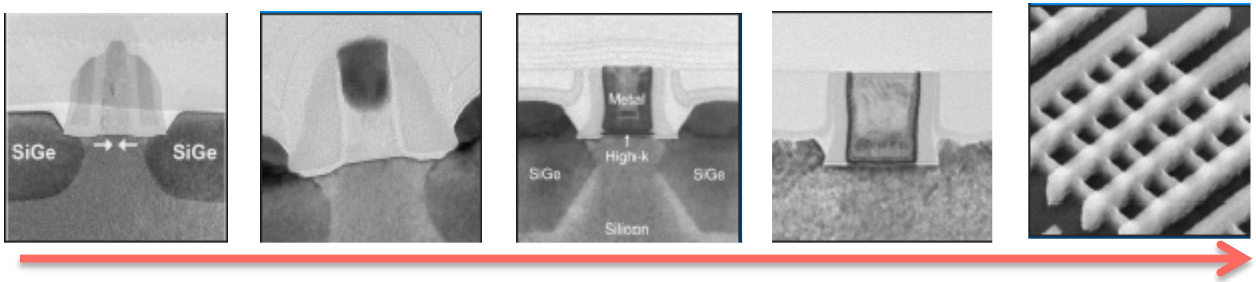
- Short channel effects
- Tunneling
- Mobility degradation
- …

- Increase sub-threshold slope
- On-current reduction
- …



http://www.semiwiki.com/forum/content/attachments/6084d1359678676-intel-processor-power.jpg,

*Figure 2: The growing power density (measured in W/cm2) of Intel's microchip processor families. (Source: Intel)*



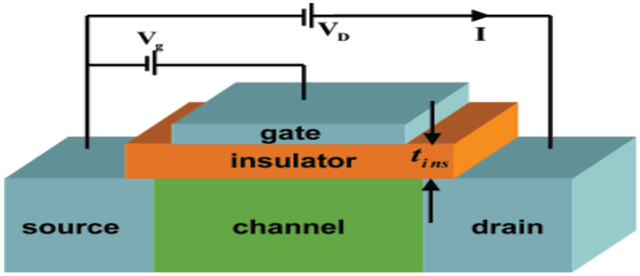
Strained Si

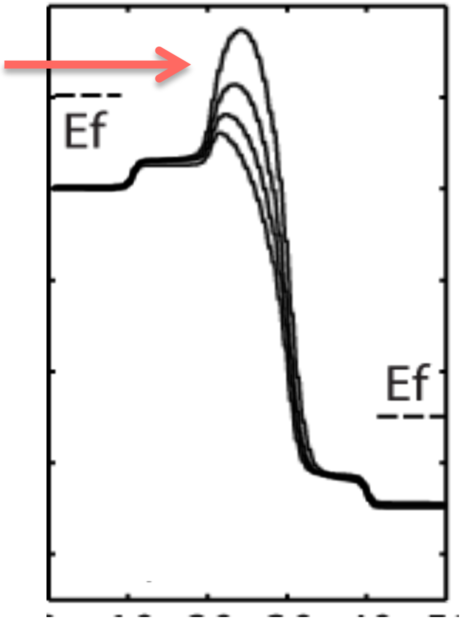
Metal Gate
High κ

FinFET

MOSFET: improve electrostatics, increase mobility, reduce leakage → continue Moore's Law

# Fundamental limitation of MOSFET

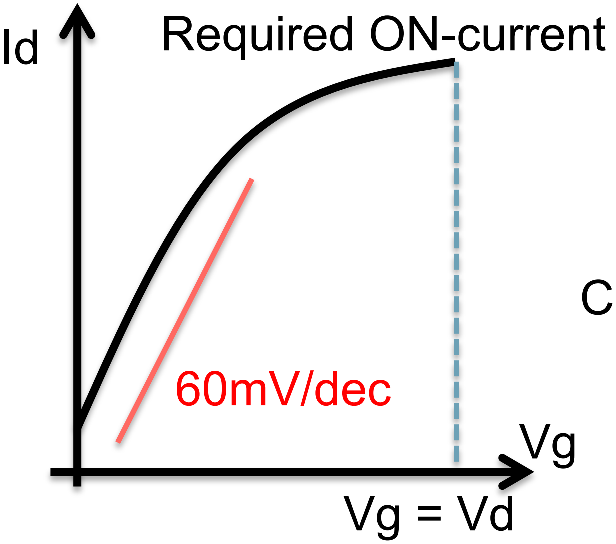




**MOSFET: voltage controls channel resistance**

Gate Voltage → Surface Potential → Conductance

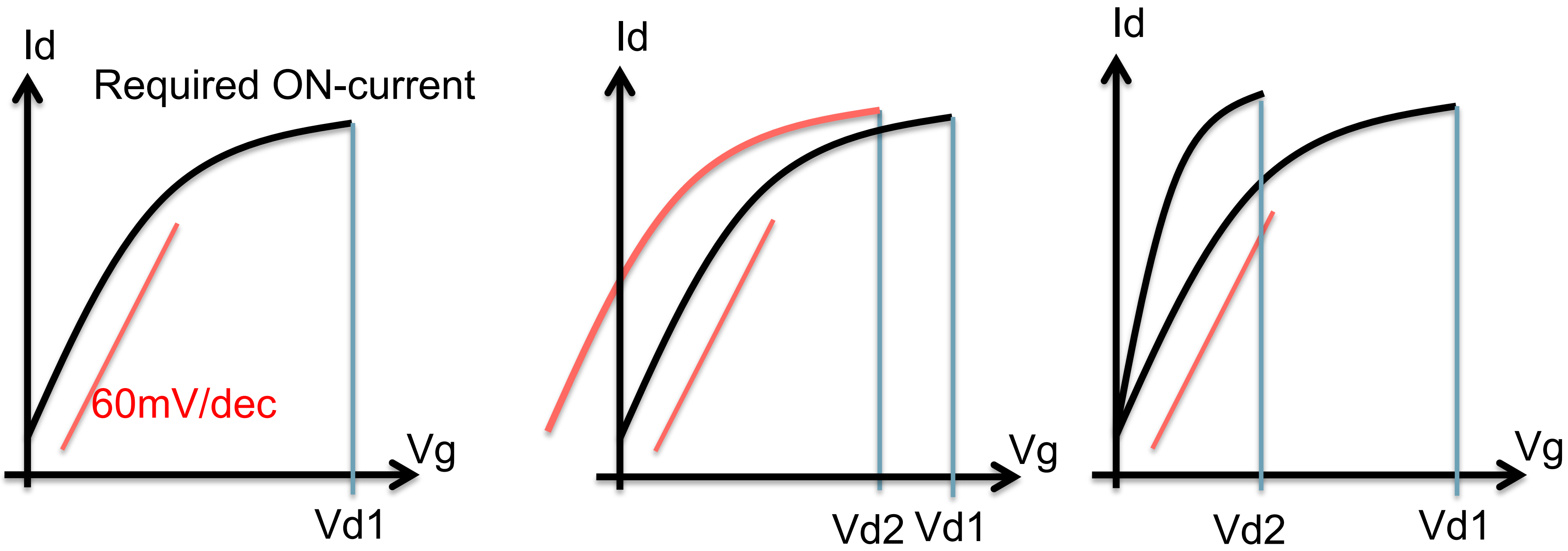
Thermionic emission



Vg: 60mV
Conductance: 10X

60mV/dec SS is the fundamental limitation of MOSFET

# Motivations: Reduce supply voltage (Vd)



60mV/dec SS is the fundamental limitation of MOSFET

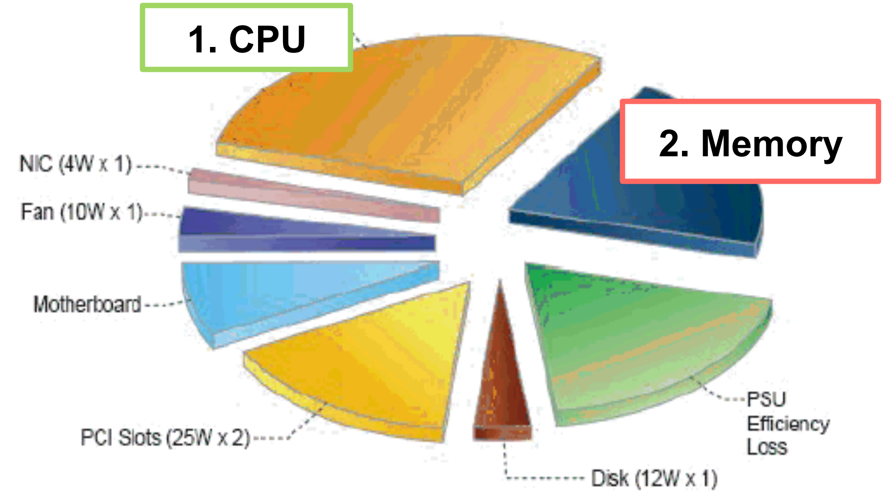
Reduce Vd → higher leakage current

Low SS → low supply voltage

Beyond MOSFET (1): How to design transistors with **SS < 60mV/dec**.

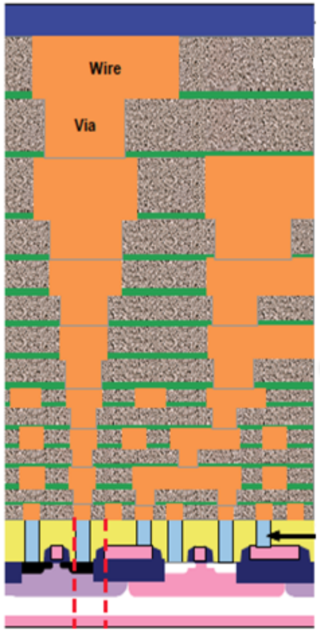
# Motivations: Reduce power beyond MOSFET

Power breakdown in a server



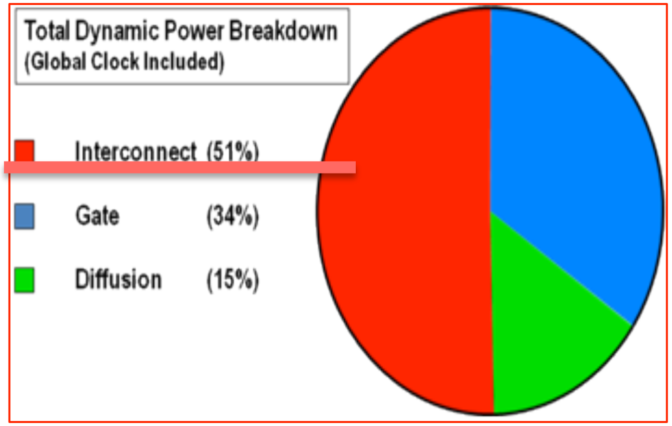
Source: Intel Labs, 2008

**Memory** consumes large portion of power.



ITRS – 2011 edition

**Interconnect** resistance increases at smaller linewidth.



***2004, Nir Magen, Intel***

http://lp-hp.com/pangrle/files/2011/09/barry1.png

Beyond MOSFET (2): Design **new memory cell** and reduce **interconnect** resistance.

# Challenges: Design new device

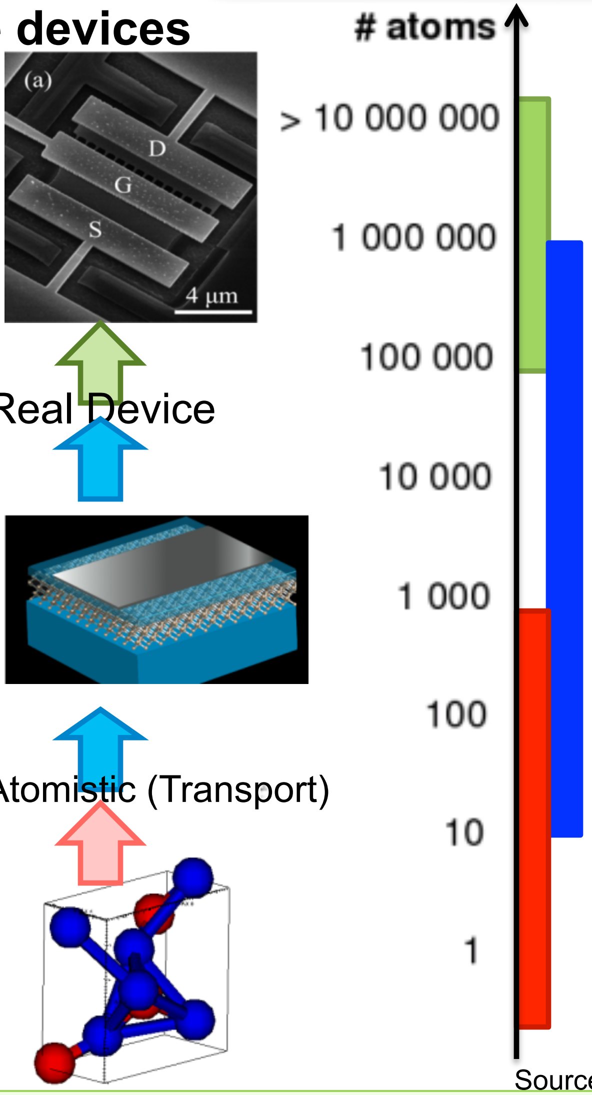
## Multi-scale devices

Match experiments
Predict
performance

Optimization
Scaling trend

Device prototype
Model validation

New material
Basic physics



## Multi-scale modeling

**Continuous medium approximations**

Examples: Classical elasticity, effective mass

**Atomistic "semi-empirical" methods**

Parameterized Hamiltonians

Example: Inter-atomic potentials, empirical tight-binding

**"*Ab initio*" methods**

A few adjustable parameters

Example: Density Functional Theory (DFT)

Source: http://inac.cea.fr/sp2m/L_Sim/TB_Sim/index.html

Choose **right** model for predictive simulation.

# Challenges: Accuracy and efficiency

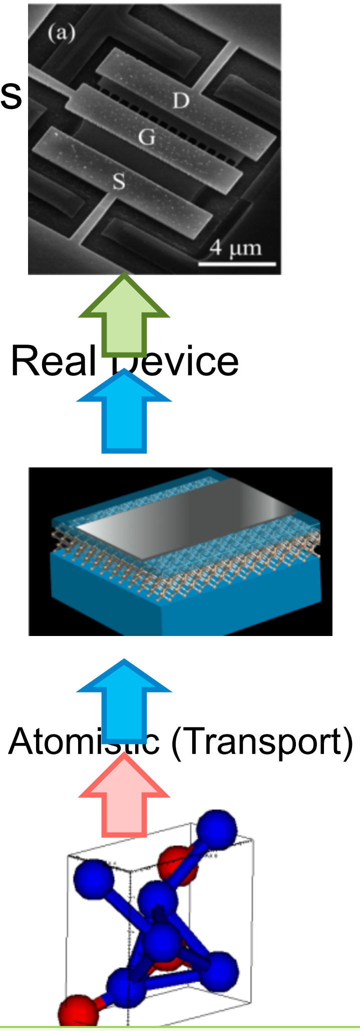
## Multi-scale devices

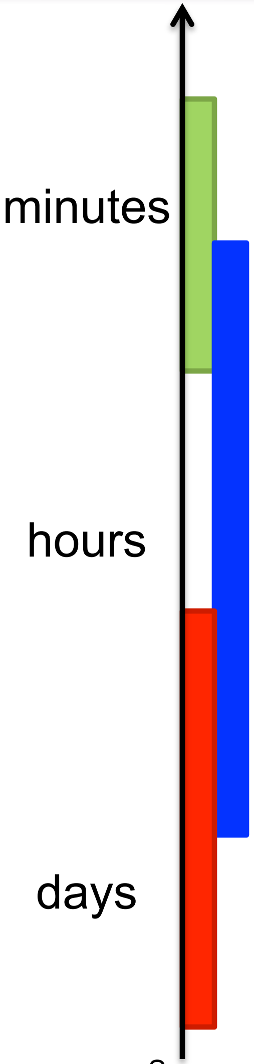
Match experiments
Predict
performance

Optimization
Scaling trend

Device prototype
Model validation

New material
Basic physics





## Multi-scale modeling

**Continuous medium approximations**

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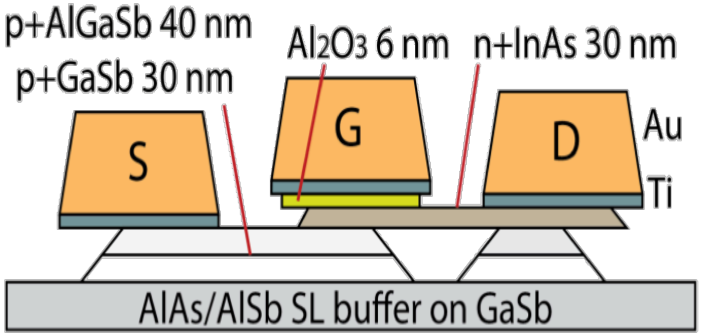
Example: Density Functional Theory (DFT)

Source: http://inac.cea.fr/sp2m/L_Sim/TB_Sim/index.html

Simulation is limited by computational resources.
Think of **accuracy** / **efficiency** trade-off.

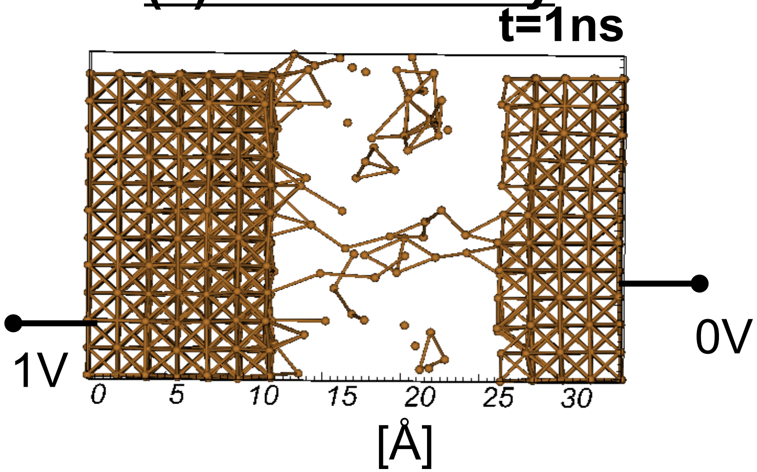
# Applications: multi-scale modeling

## (1) Low SS transistors I

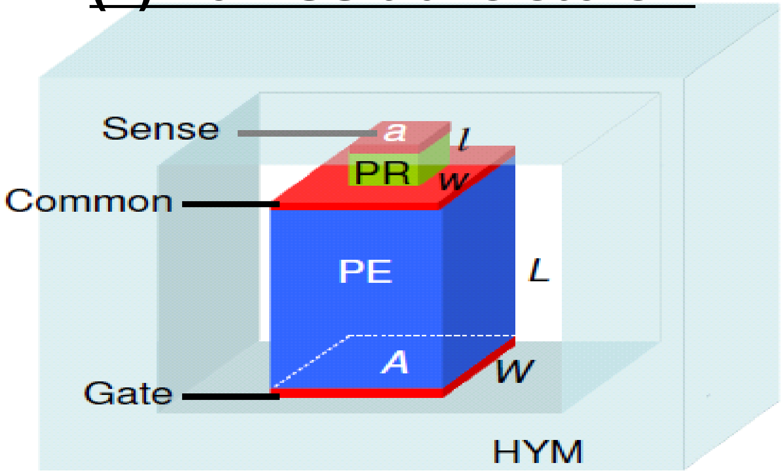


*p-n* vertical TFET - top gated

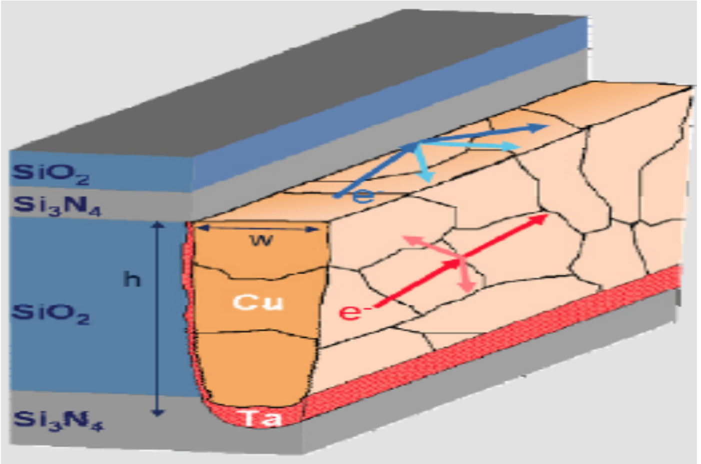
## (3) New Memory



## (2) Low SS transistors II

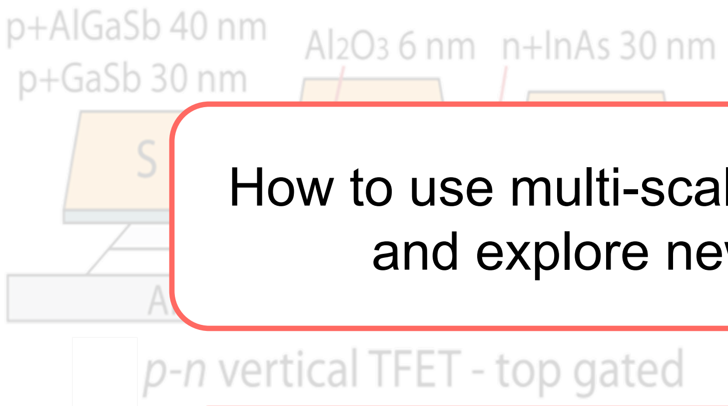


## (4) Interconnect



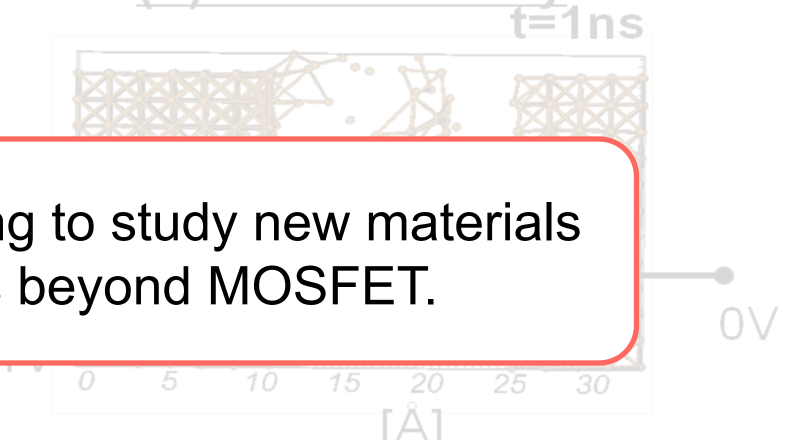
# Applications: multi-scale modeling

(1) Low SS transistors I

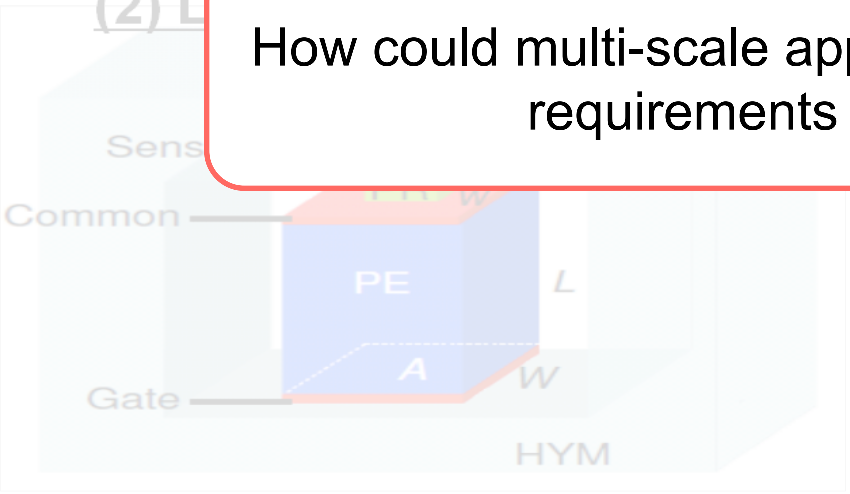


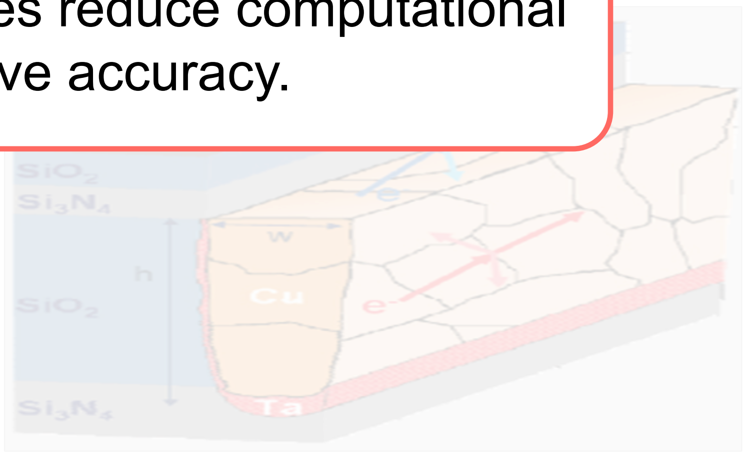
p-n vertical TFET - top gated

(3) New Memory



(2) L



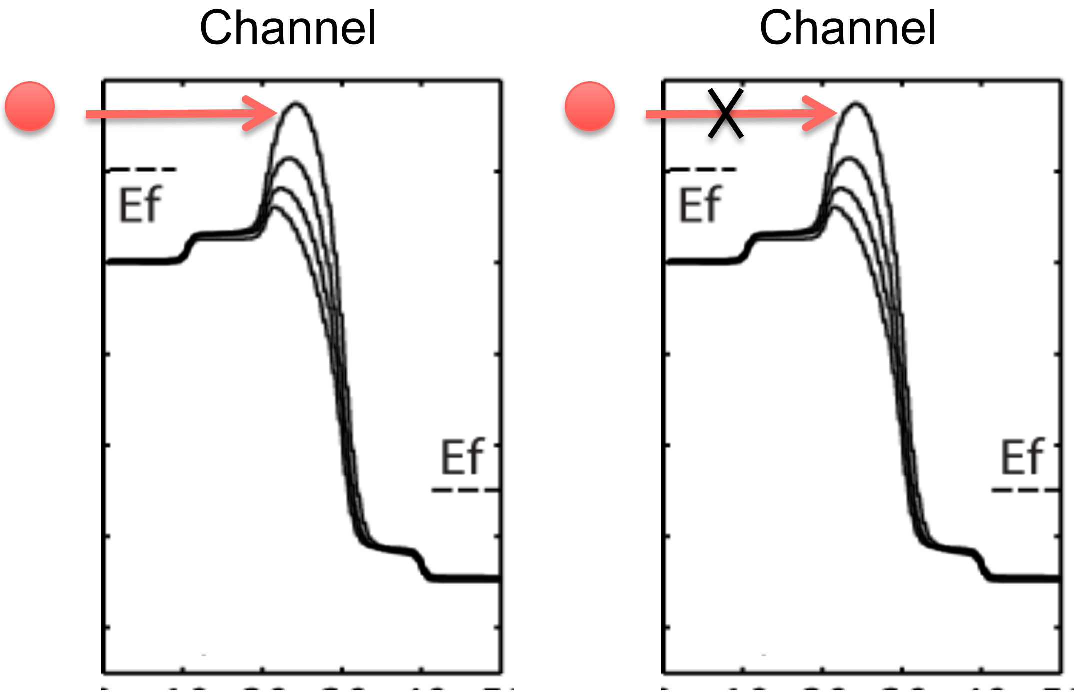


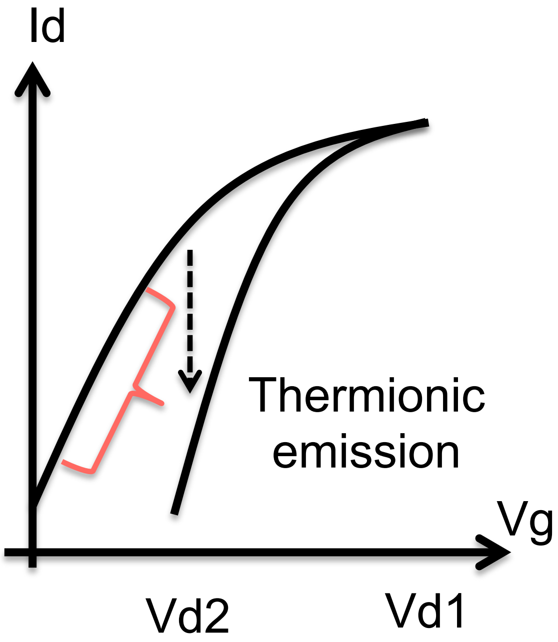
How to use multi-scale modeling to study new materials and explore new designs beyond MOSFET.

How could multi-scale approaches reduce computational requirements / improve accuracy.

# (1) Low SS transistors

**MOSFET: voltage controls channel resistance**





Motivation: control the energy of current-carrying carriers.

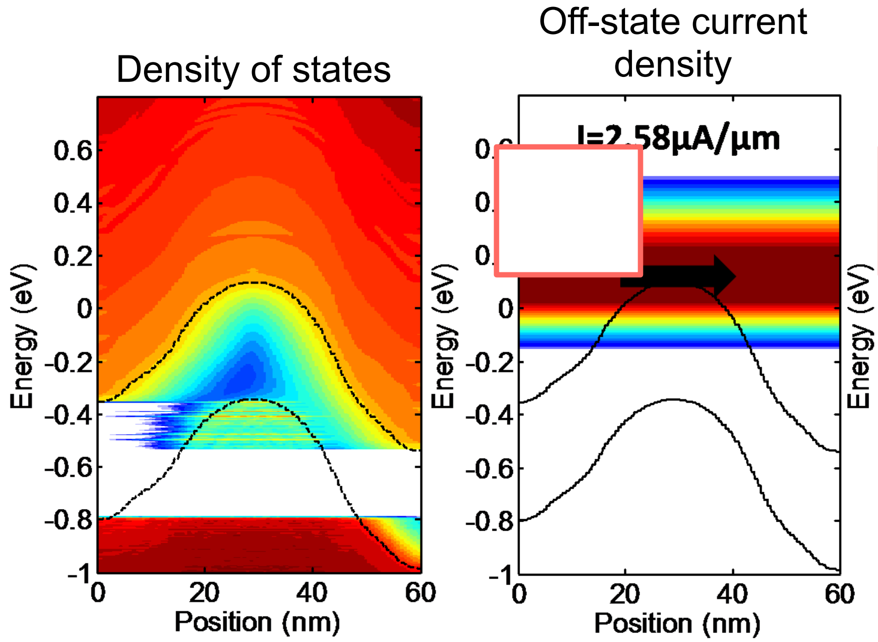
# TFET: Energy filtering

## InAs MOSFET

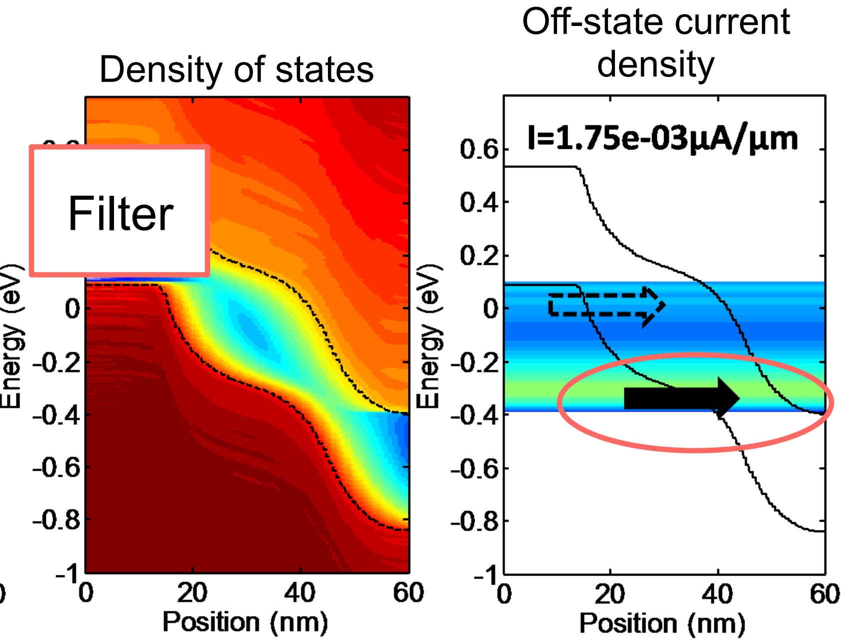
$N^{++}$ | N | $N^{++}$

## InAs TFET

$P^{++}$ | N | $N^{++}$


Density of states

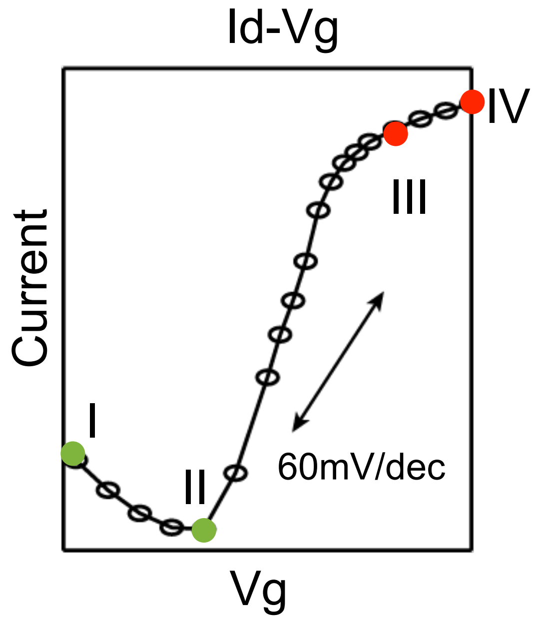
Off-state current density

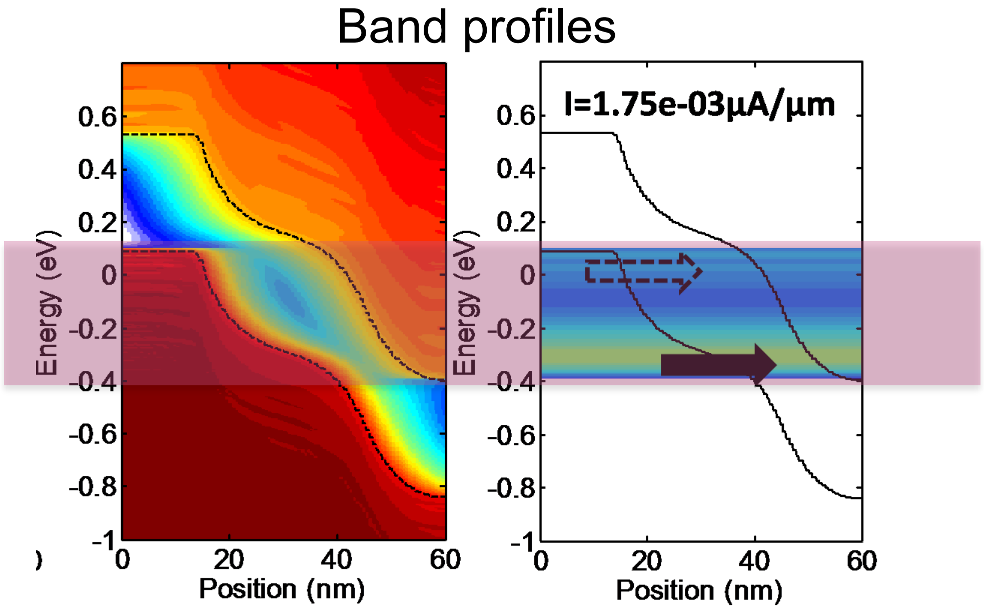

Density of states

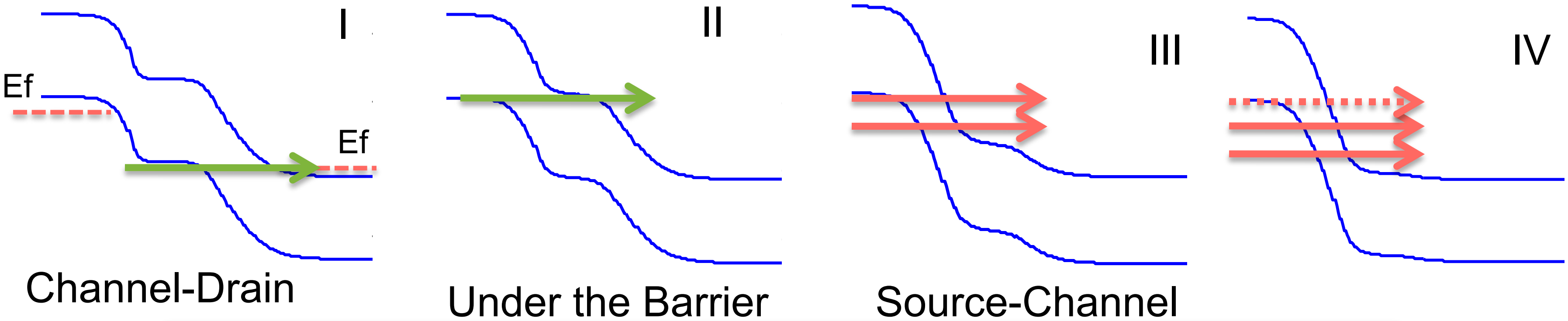
Off-state current density

Off current of TFET is not limited by thermionic emission.
SS of TFET could be smaller than 60mV/dec.

# Working Principle





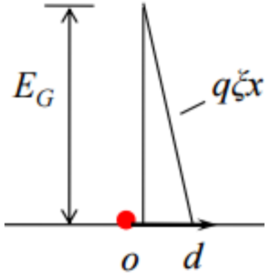


Design nTFET to maximize current from source-channel junction.

# Maximize tunneling current

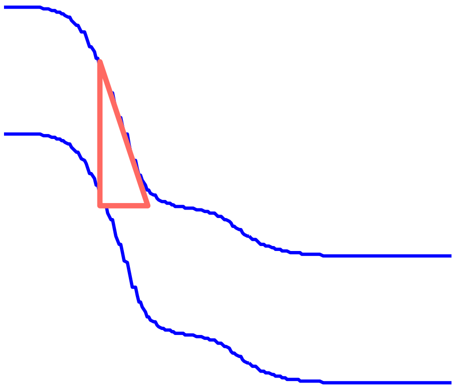
WKB approximation:

$$T^{1D}_{WKB} = \exp\left(-\frac{4\sqrt{2m_r^*}\,E_G^{3/2}}{3q\hbar\xi}\right)$$

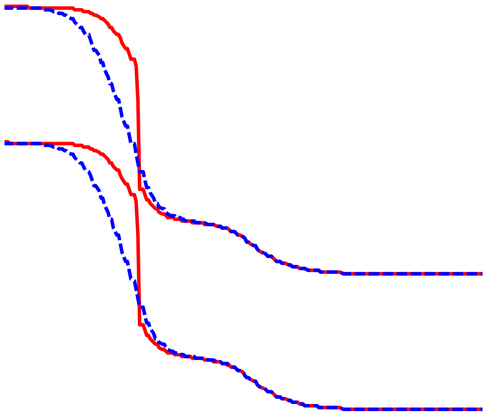


**Small bandgap ($E_G$)**
Small effective mass ($m^*_r$)
Steep doping profile ($\xi$)

Homo-junction

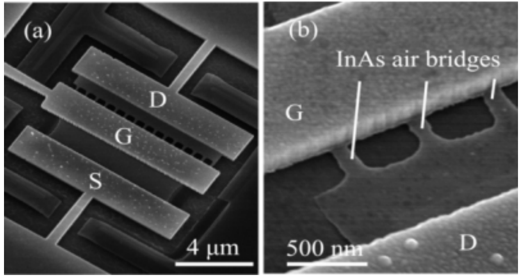


Hetero-junction

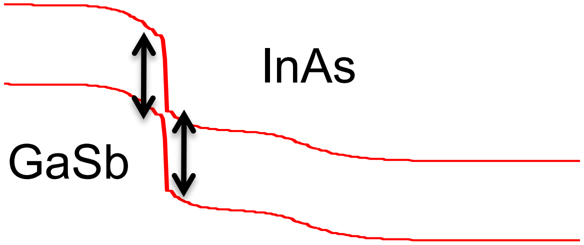


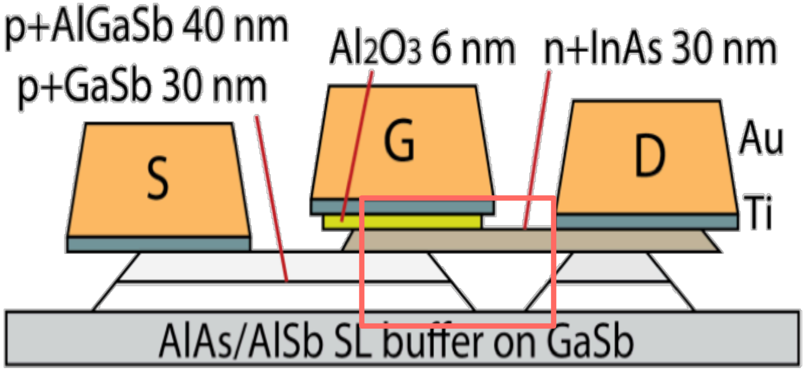
Small band overlap or even zero overlap could be achieved in hetero-junction.

# Prototype of the top gated TFET

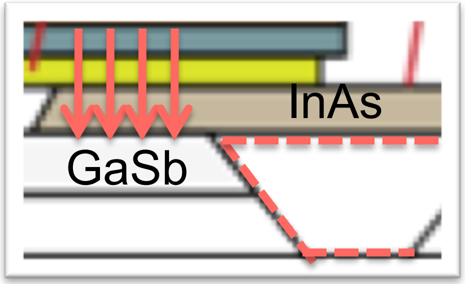


Top-gated TFET could provide record high on-current [1,2].





*p-n* vertical TFET - top gated



Air bridge: terminate leakage current

1. Heterogeneous: Source/channel made from GaSb/InAs ($E_G$)
2. Vertical gate: increase tunneling area and electric field (ξ)
3. Include air bridge at drain contact: reduce leakage

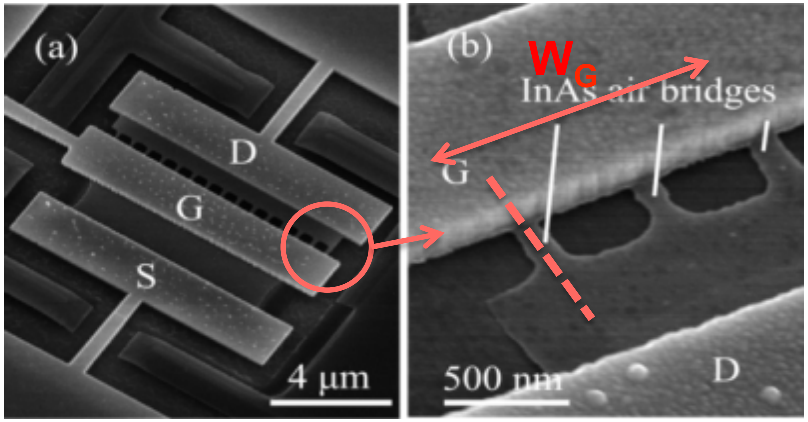
**Objective**: Explore the scaling limit of top-gated TFET with quantum transport simulations.

*[1]R. Li, Y*

*[2]Li, R., L*

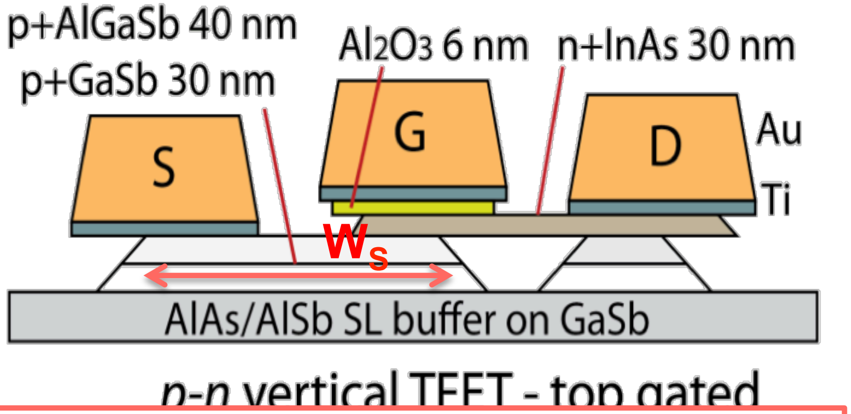
# Challenges: Geometry

Real device is too big for quantum transport simulations!

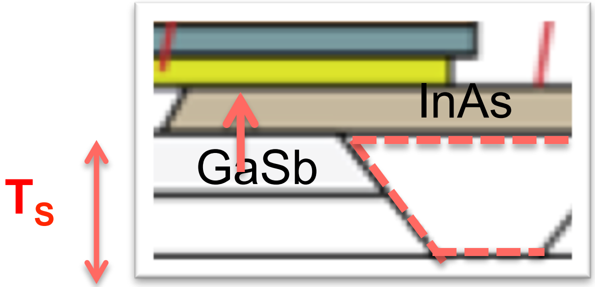


(1) $W_G$ is huge (3D) → Periodic (2D).

**2D**

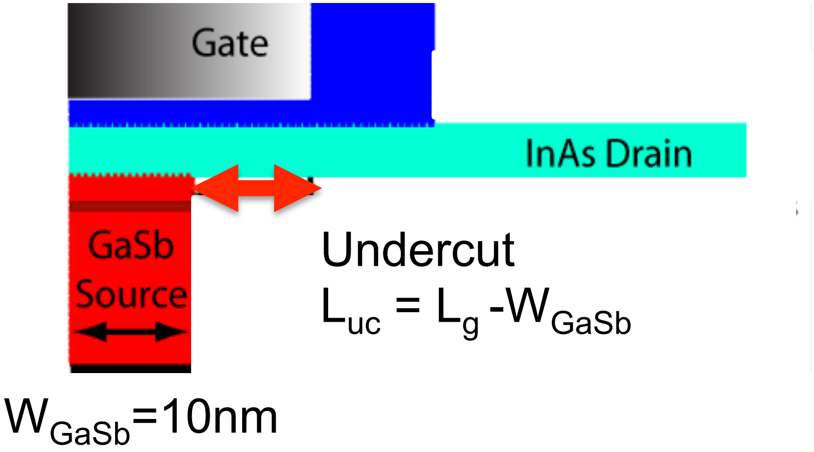


(2) $W_S$ is long → no lateral confinement
Reduce length of $W_S$.



(3) $T_S$ is large → equilibrium reservoir.
Carrier injection vertical to gate.
Large $W_S$ → Reduce confinement.

**final**



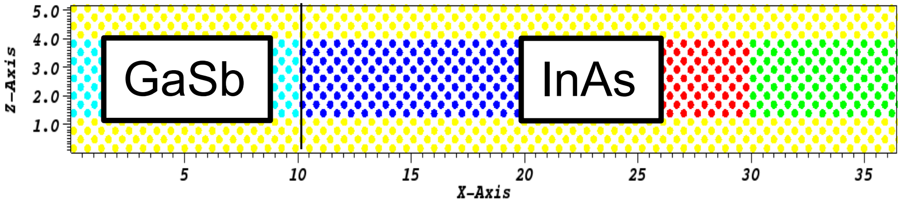
Undercut
$L_{uc} = L_g - W_{GaSb}$

$W_{GaSb}$=10nm

# Challenges: Geometry

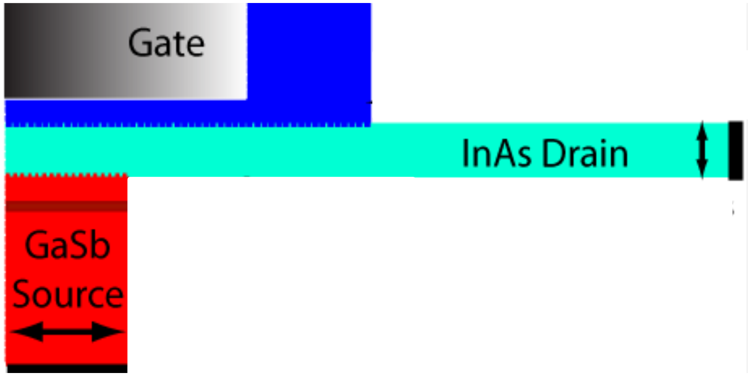
**Normal NW-TFET simulation**

GaSb-InAs nanowire TFET



- Homogeneous structure → Same matrix size for all slabs.
- Similar properties for all slabs.
- Source and drain in the same direction → Easy RGF implementation.

**L-shape TFET simulation**

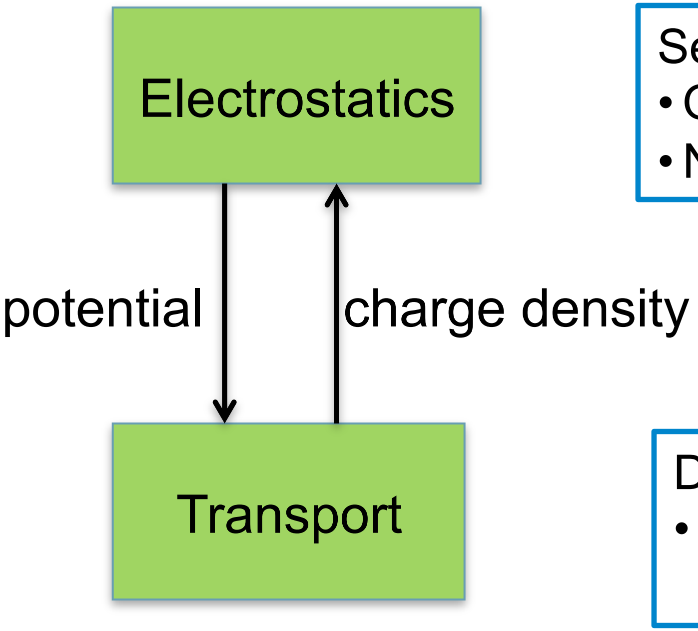


- Inhomogeneous structure → Different matrix sizes require **general** RGF.
- Variation of local band profile → Bad **convergence** for ballistic simulations.
- Source and drain in different directions → Complicated slab **connectivity** requires smart **repartition** solver.

Non-trivial task to simulate L-shaped geometry!
Generalized geometry construction and NEGF solver required.

# Challenges: Modeling efficiency and accuracy

**Two common methods for electronic device simulation:**



Semiclassical density:
- Quasi-equilibrium
- No spatial correlation

Drift-Diffusion+WKB:
- Tunneling: Fitting parameters

Quantum density:
- Atomistic
- Spatial correlated

NEGF:
- Bandstructure effects
- Quantum tunneling

**Fast** | **Accuracy**

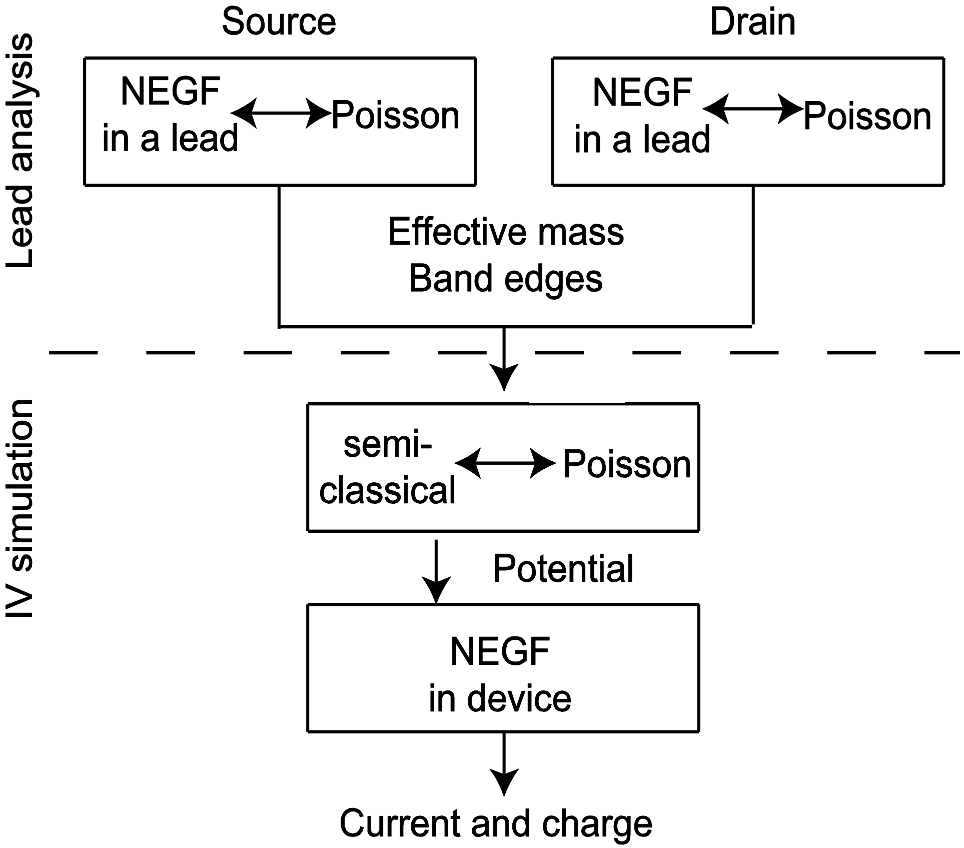
Propose a method to combine two approaches.

# Methods

**Method:**

- Drift Diffusion density for electrostatic potential (similar to TCAD)
  - ➢ Extracting band edges & DOS mass from full band calculation
- NEGF transport on top of Semiclassical potential

- Semiclassical density with corrected parameters well describes electrostatics.
- Tunneling captured by NEGF
- Low numerical load, very fast

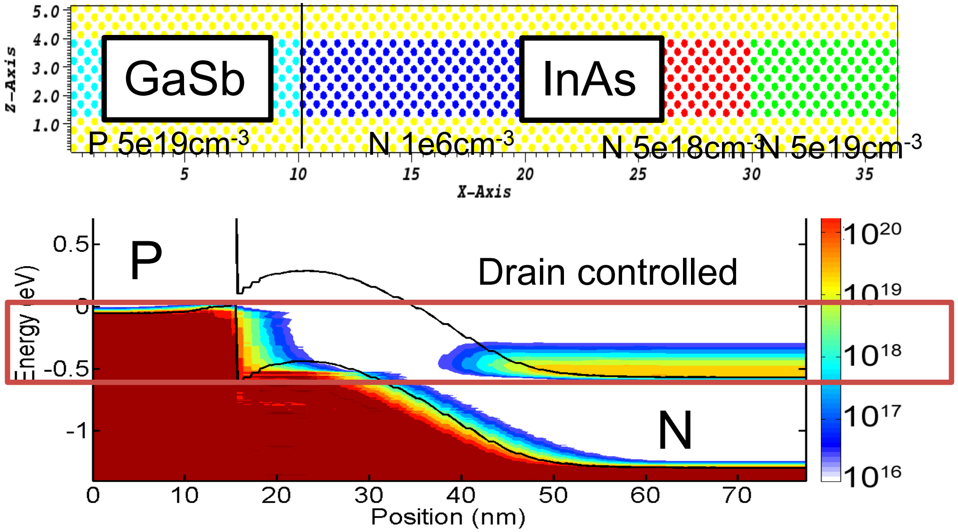


# Methods

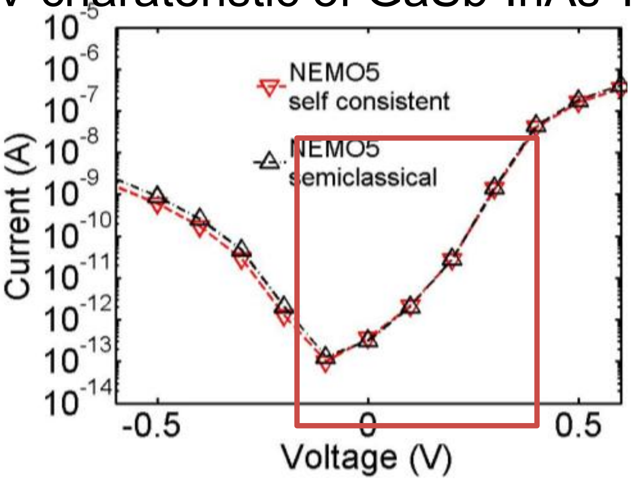
**Method:**

- Drift Diffusion density for electrostatic potential (similar to TCAD)
  - ➢ Extracting band edges & DOS mass from full band calculation
- NEGF transport on top of Semiclassical potential

Example: GaSb-InAs nanowire TFET



I-V charateristic of GaSb-InAs TFET



Our methods are proved to be fast and with high accuracy for TFET simulations.

# Comparison of NEGF with TCAD model

**Objectives:**

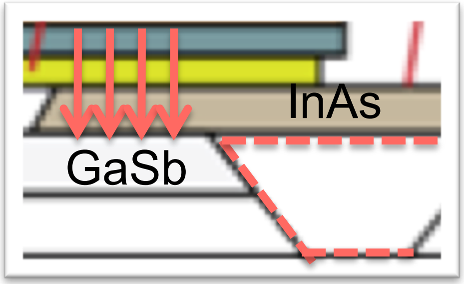
- Optimize design of top gated TFETs for low SS.
- Explore scaling limits of top gated TFETs.
- Evaluation the accuracy of transport models.

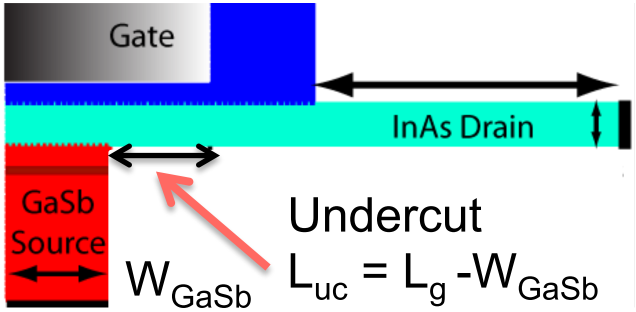
**Methods:**

- Drift-Diffusion potential + NEGF.
- Drift-Diffusion + dynamic non-local band to band tunneling model (Synopsys TCAD).

**Results:**

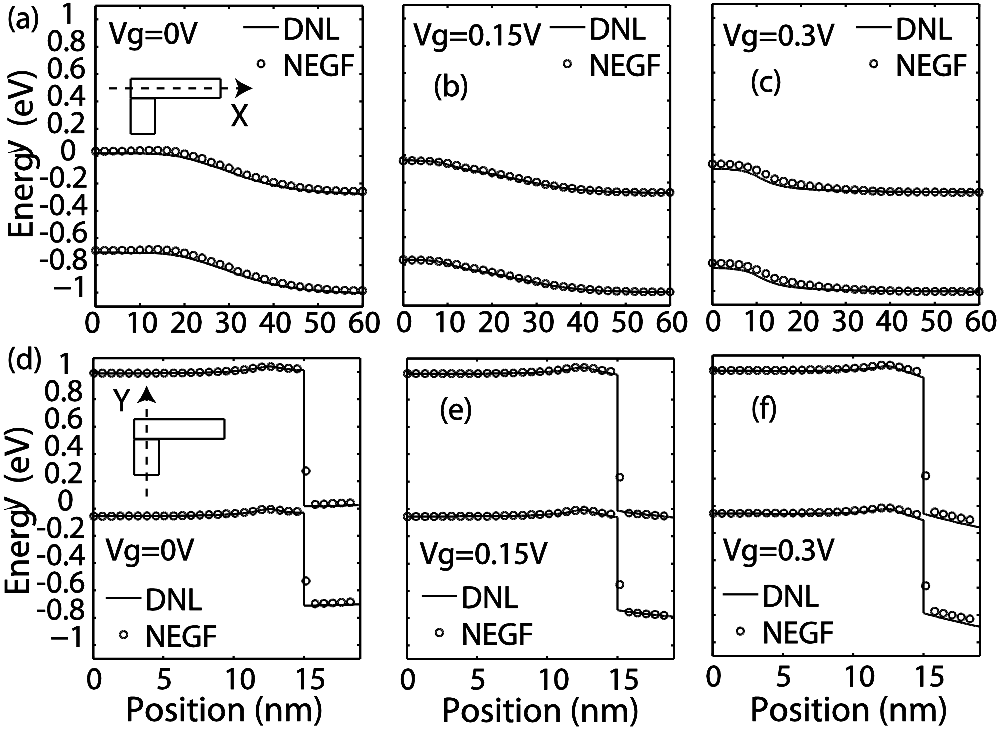
- Extract confined bandgap and density of states effective mass.
- Similar electrostatic potential from different models.



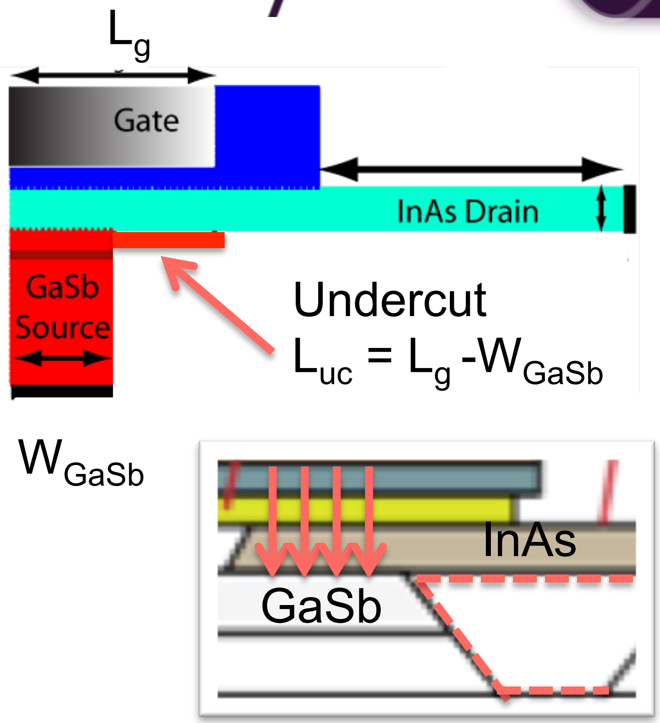


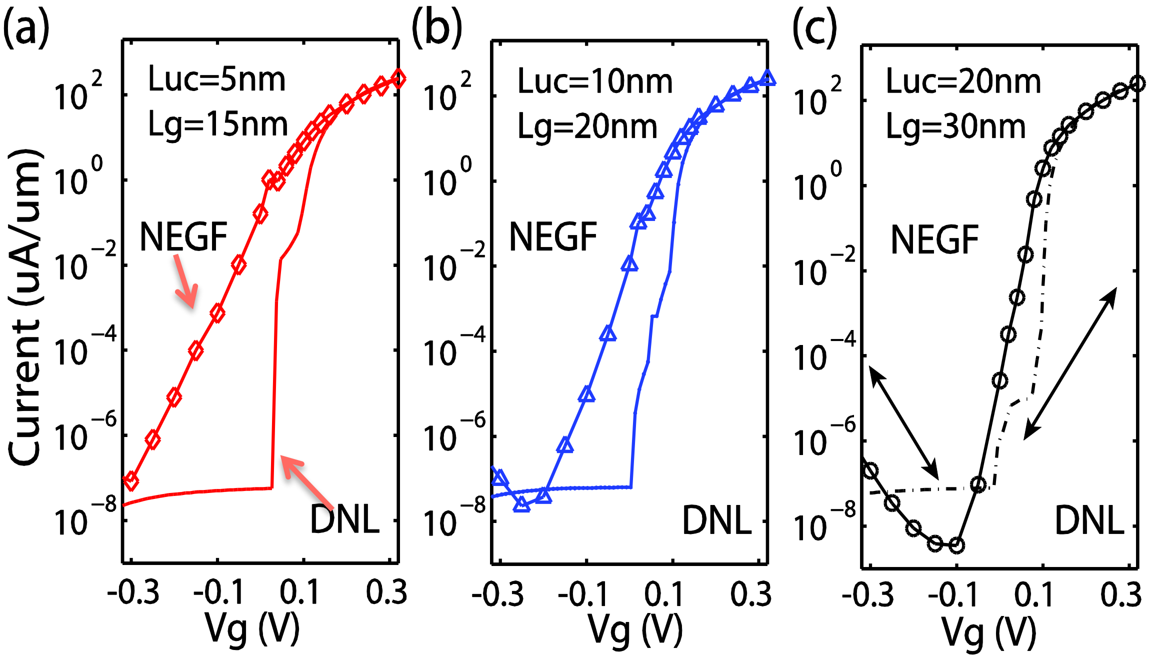
Undercut $L_{uc} = L_g - W_{GaSb}$

## Band profile at different bias conditions



# Comparison of NEGF with TCAD model





**Results:**

- Undercut length is important to reduce leakage.
- TCAD underestimate leakage current. TCAD does not include all tunneling paths due to the complexity of geometry.
- NEGF predicts more accurate scaling limit for top-gated TFET.
- Reduce simulation time compared with full self-consistent simulations.

# TFET Summary & contributions

- Top-gated TFETs improve TFET performance
  - Heterojunction: InAs/GaSb
  - Enhanced gate control: top-gate TFET

- Scaling of top-gated TFET is ultimately limited by undercut length.

- Drift-Diffusion potential + NEGF gives efficient and accurate evaluation of TFET performance.

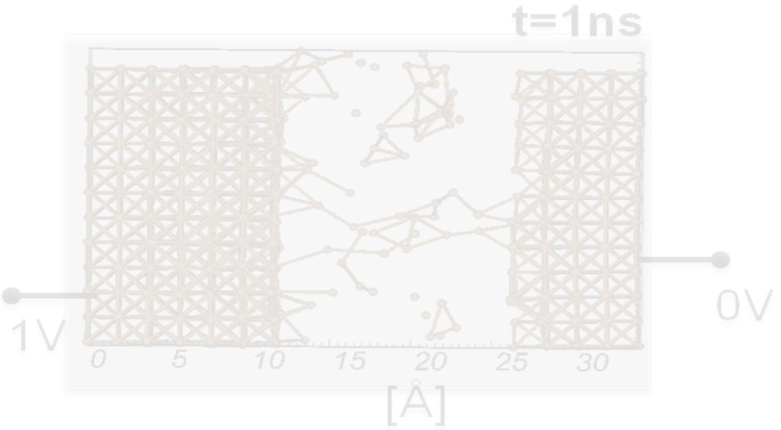
# Outline

## (1) Low SS transistors I

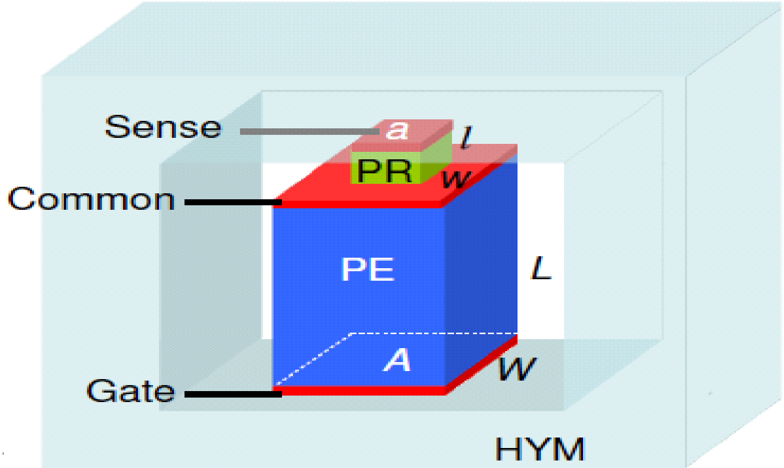
- **Energy filtering**
- **Full band bandstructure → effective mass, Eg**
- **Drift – Diffusion + NEGF**
- **Improve efficiency**

*p-n* vertical TFET - top gated

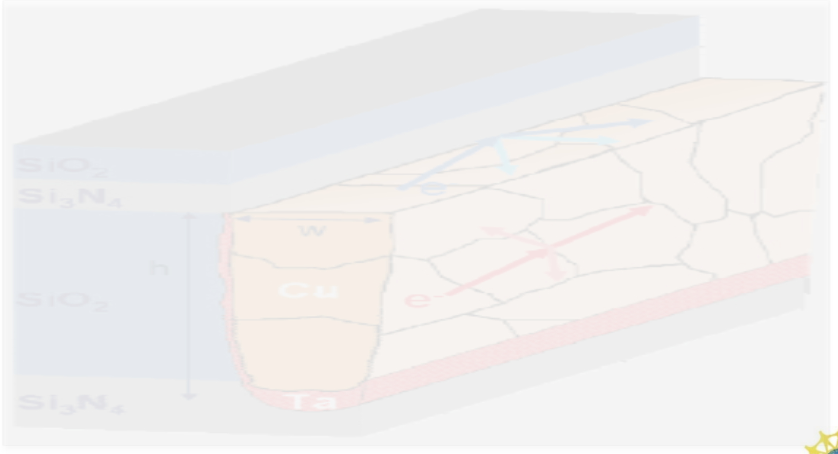
## (3) New Memory



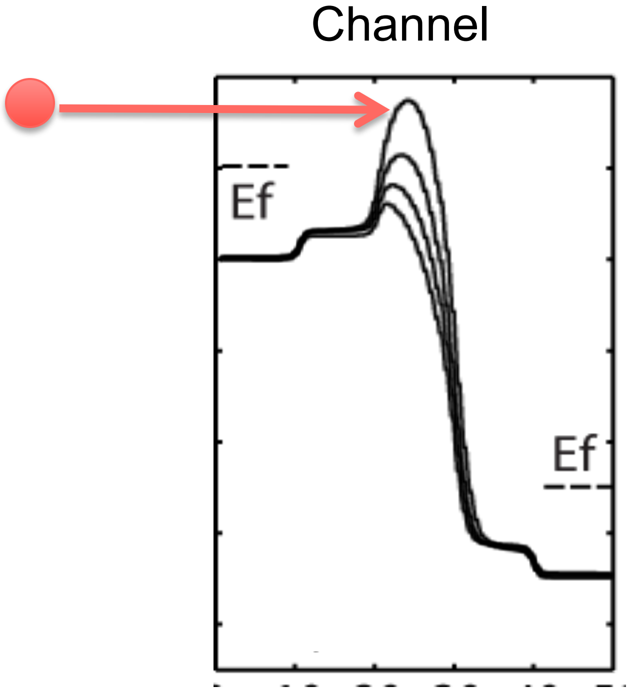
## (2) Low SS transistors II



## (4) Interconnect



# (2) Low SS transistors: transduction



**MOSFET barrier controls channel resistance:**

60mV Gate Voltage → 60mV Surface Potential → 10× Conductance

Electric Signal Electric Signal

60mV Gate Voltage → ? → >10× Conductance

Transduction
From electric to other energy forms

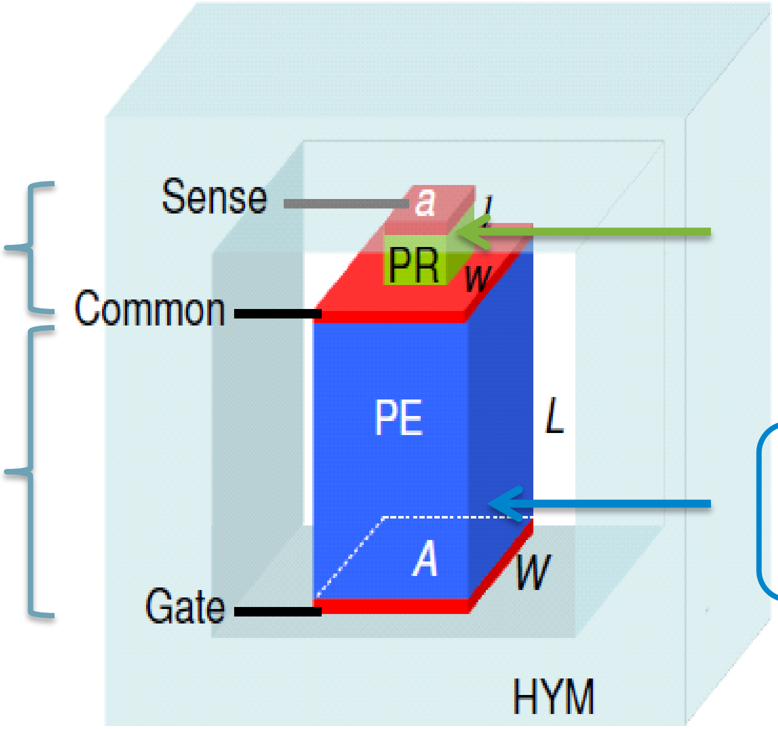
Motivation: energy transduction.

# Piezoelectronic Transistor (PET)

Contacts

Current
OUTPUT

Voltage
INPUT



Channels

**P**iezo**R**esistive Material
(e.g. SmSe)

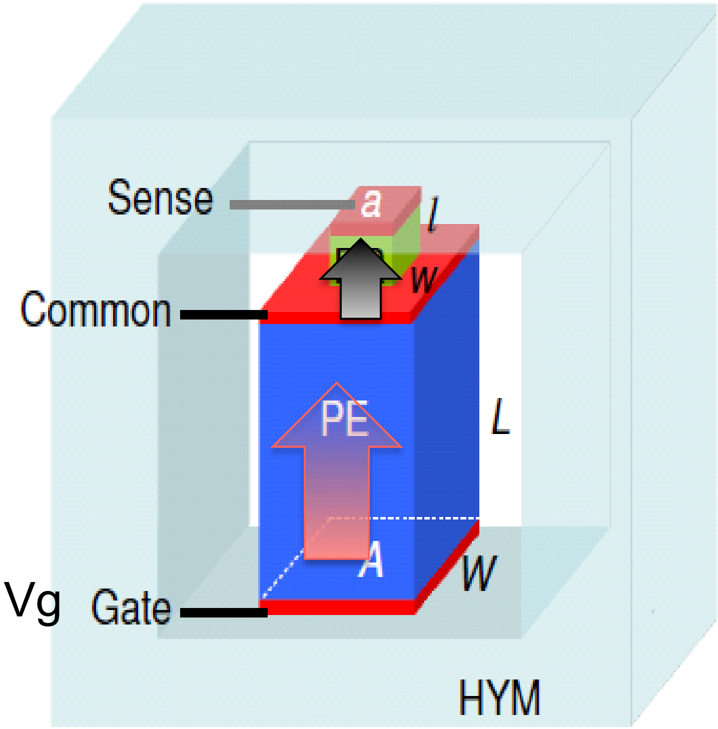
Pressure → Conductance change

Relaxor **P**iezo**E**lectric Material
(e.g. PMN-PT)

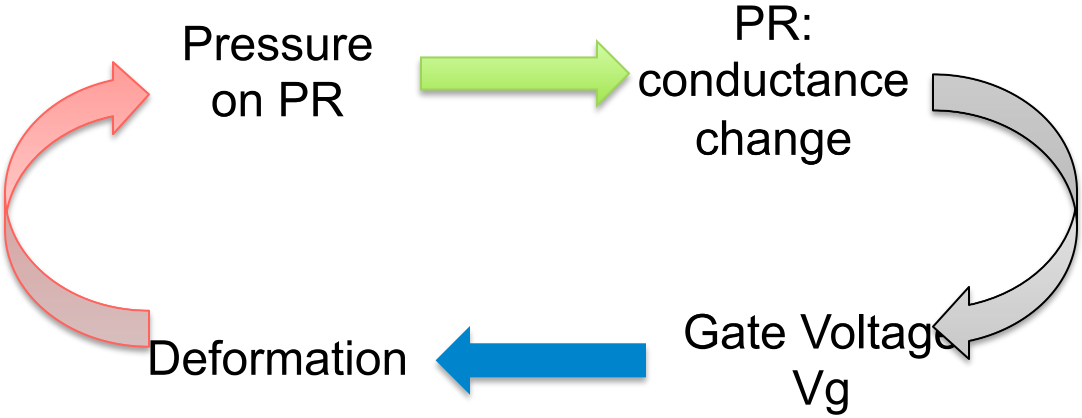
Gate voltage → Volume change

Properties of PE and PR enable **internal transduction** of acoustic and electrical signals.

# Working principle



Voltage applied on Gate – Common terminals:
Deformation inside PE channel
**Electrical → Acoustic**



Pressure on PR

PR: conductance change

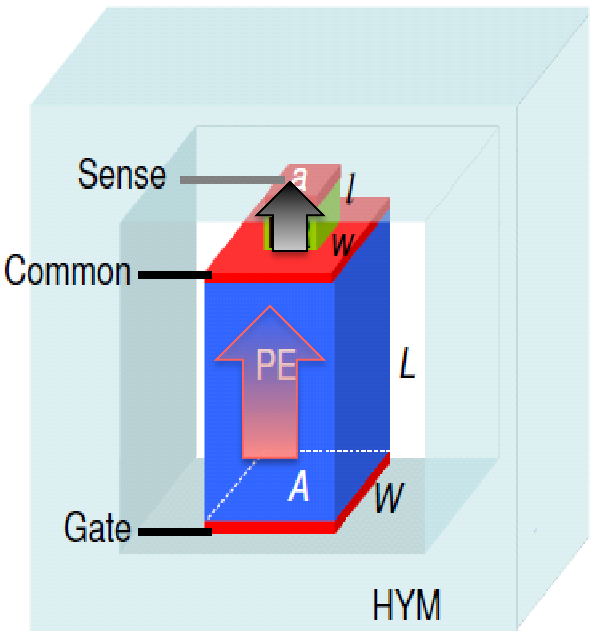
Gate Voltage Vg

Deformation

Current in PE channel
**Acoustic → Electrical**

How does acoustic signal improve conductance?

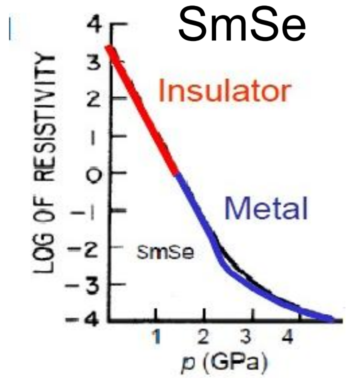
# Mechanical and Electrical Features



60mV Gate Voltage → Acoustic → >10× Conductance

Transduction
From electric to other energy forms

Small Volume Change → Big Resistivity Change in PR (**>10× per 60mV** gate voltage) - Metal-Insulator Transition

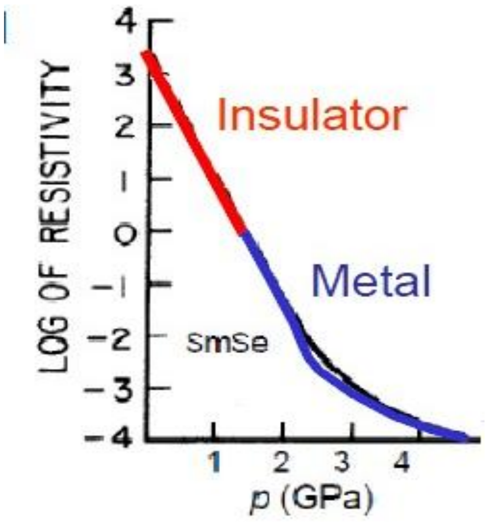


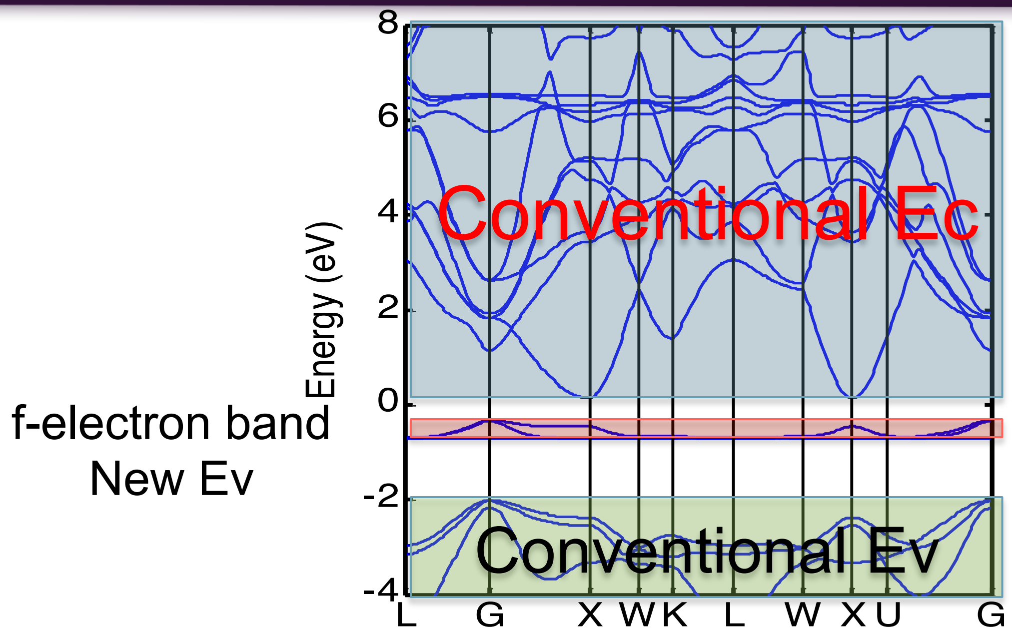
Phys. Rev. Lett. 25, 1430 (1970)

Need to understand the conductance change inside **SmX** (X=Se, Te).

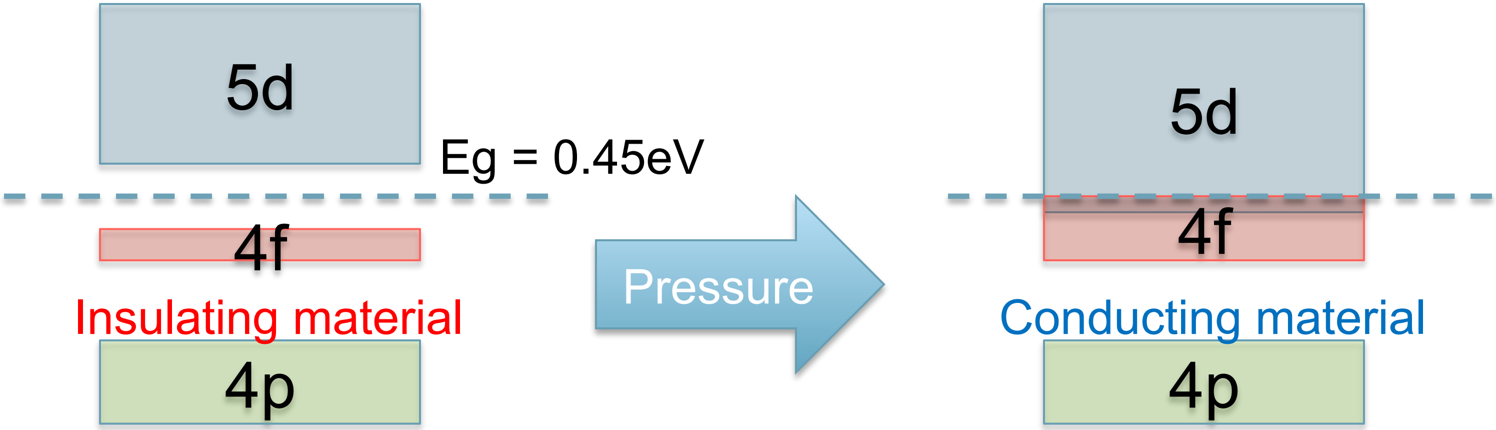
D. M. Newns, B. G. Elmegreen, X. H. Liu and G. J. Martyna, Advanced Materials (2012).

# SmSe: Metal-Insulator Transition (DFT+U)





f-electron band
New Ev



Insulating material

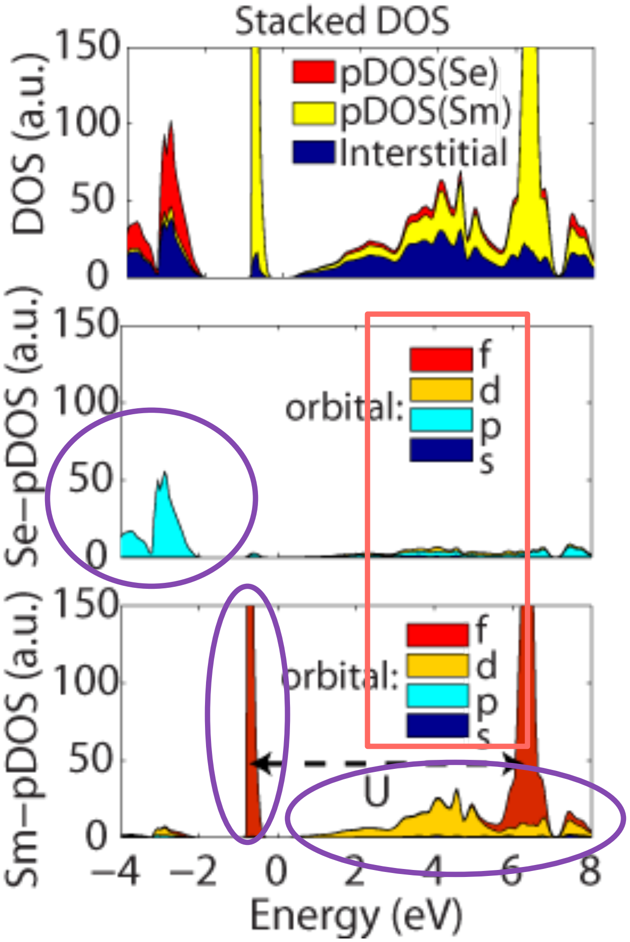
Conducting material

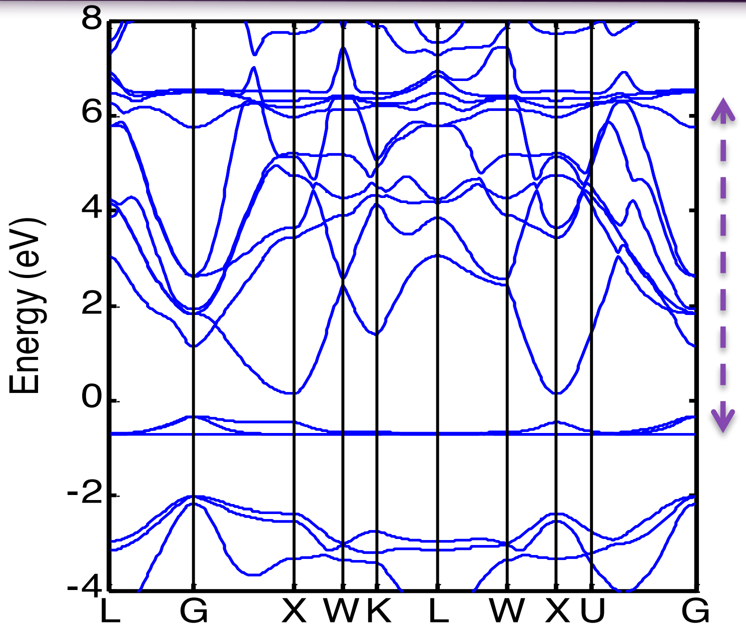
DFT+U with f-band is too expensive for transport study.
Need to parameterize MIT in tight-binding.

# Methods: Determine tight binding model

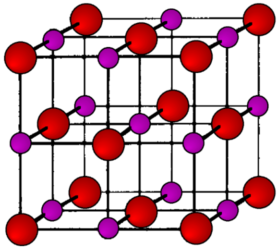
Calculation with GGA+U

DFT density of states:





f-electron splitting due to strong correlation



SmSe: DFT bandstructure

DFT decomposition: DOS into angular momentum

- Se p-orbital: lower valence band
- Sm d-orbital: conduction band
- Sm f-orbital: top valence band
- Splitting of f-orbital: covered through SO coupling
- Pure orbital bands: 2nd nearest neighbor interaction

Require 2NN TB model: $sp^3d^5f^7s^*$ + SO

# Methods

| Challenges | Divide and conquer! |
|---|---|

Include f-orbitals →

1. Matrix size increase by 7
2. More parameters:
   - 16 onsite + SO
   - 39 1NN two center integral
   - 50 2NN two center integral
   - 82 strain parameters

Difficulty for fitting →

1. Increase computational burden, time for fitness function evaluation.
2. Too much degrees of freedom

Get **initial value** from direct mapping of DFT Hamiltonian to TB Hamiltonian

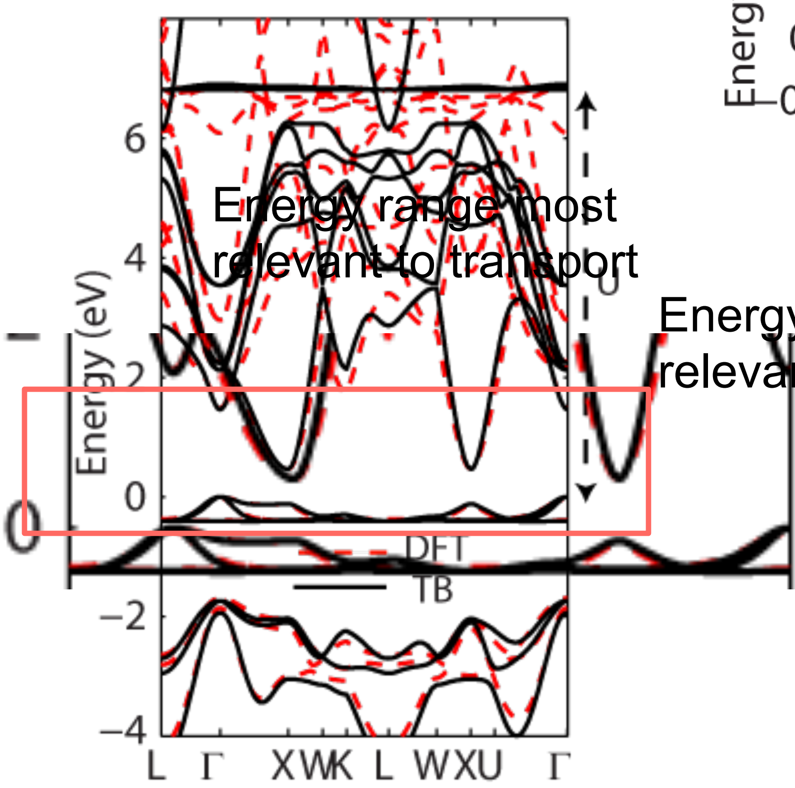
Optimize sub-groups of parameters with fitting targets on certain bands. e.g. Se-p/Se-p related parameters for lower valence bands

Adjust fitting targets according to wavefunction angular momentum decomposition, crystal field theory, crystal symmetry, etc.

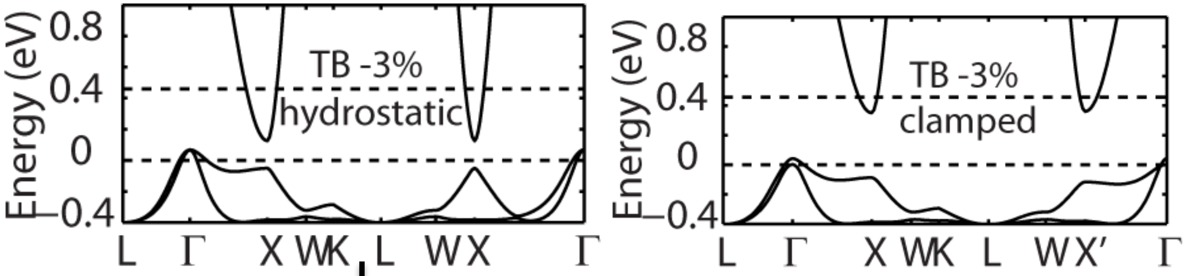
**Physical insights** from DFT and basic crystal field theory required for TB parameterization.

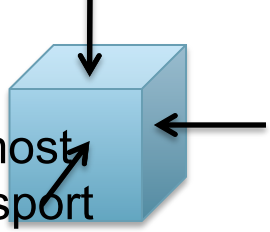
# Strain effects on bandstructure of SmSe

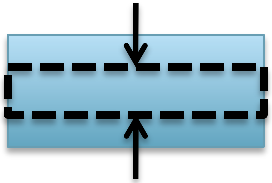
Bandstructure without strain



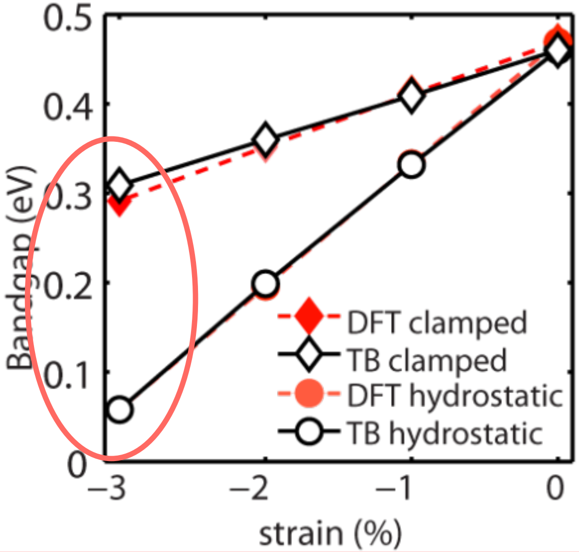
Energy range most relevant to transport







Energy range most relevant to transport



Parameter fitted to band structure of hydrostatic strain and applied to clamped (uniaxial) strain with no modification.

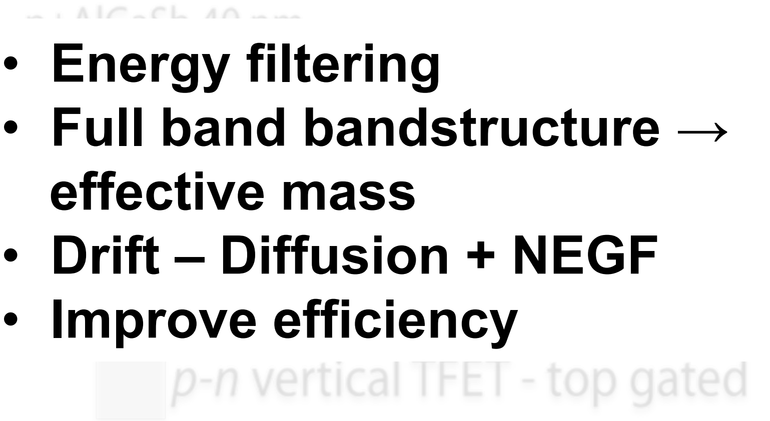
Bandgap is closing with strain in linear trend
TB matches DFT trend!

# PET Summary

- DFT+U used for bandstructure
  - » strong electron-electron interaction of f-electrons.
- Splitting of f-bands → spin-orbit splitting in tight-binding
- Metal-insulator transition in SmSe is due to band shifting in conduction band.
- Quantum transport simulation
  - » Scaling of PET will be limited by tunneling current in PR

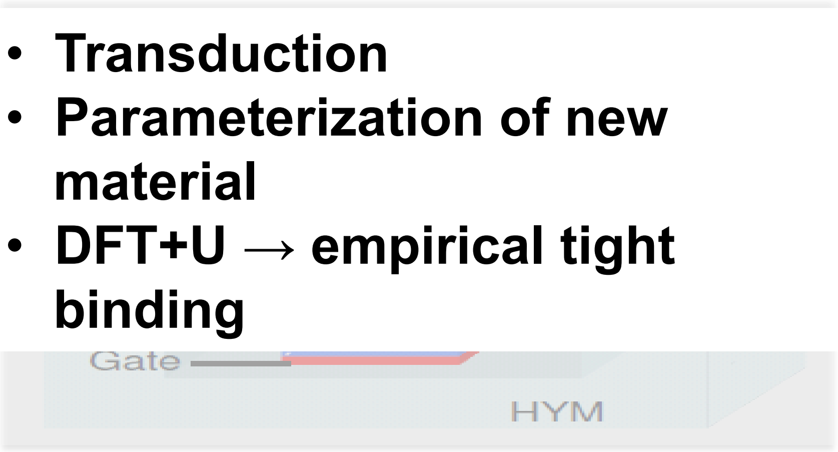
# Outline

## (1) Low SS transistors I



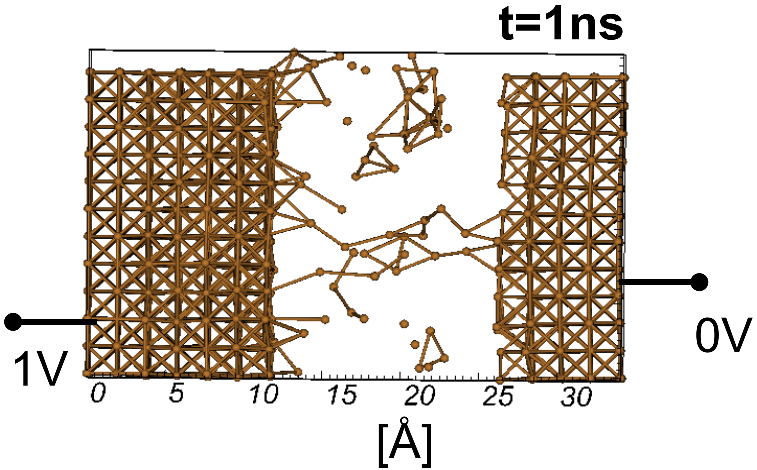
- Energy filtering
- Full band bandstructure → effective mass
- Drift – Diffusion + NEGF
- Improve efficiency

## (2) Low SS transistors II

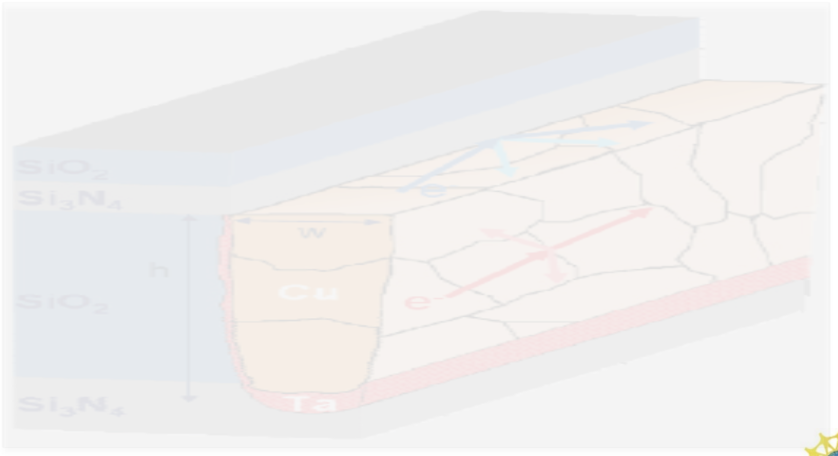


- Transduction
- Parameterization of new material
- DFT+U → empirical tight binding

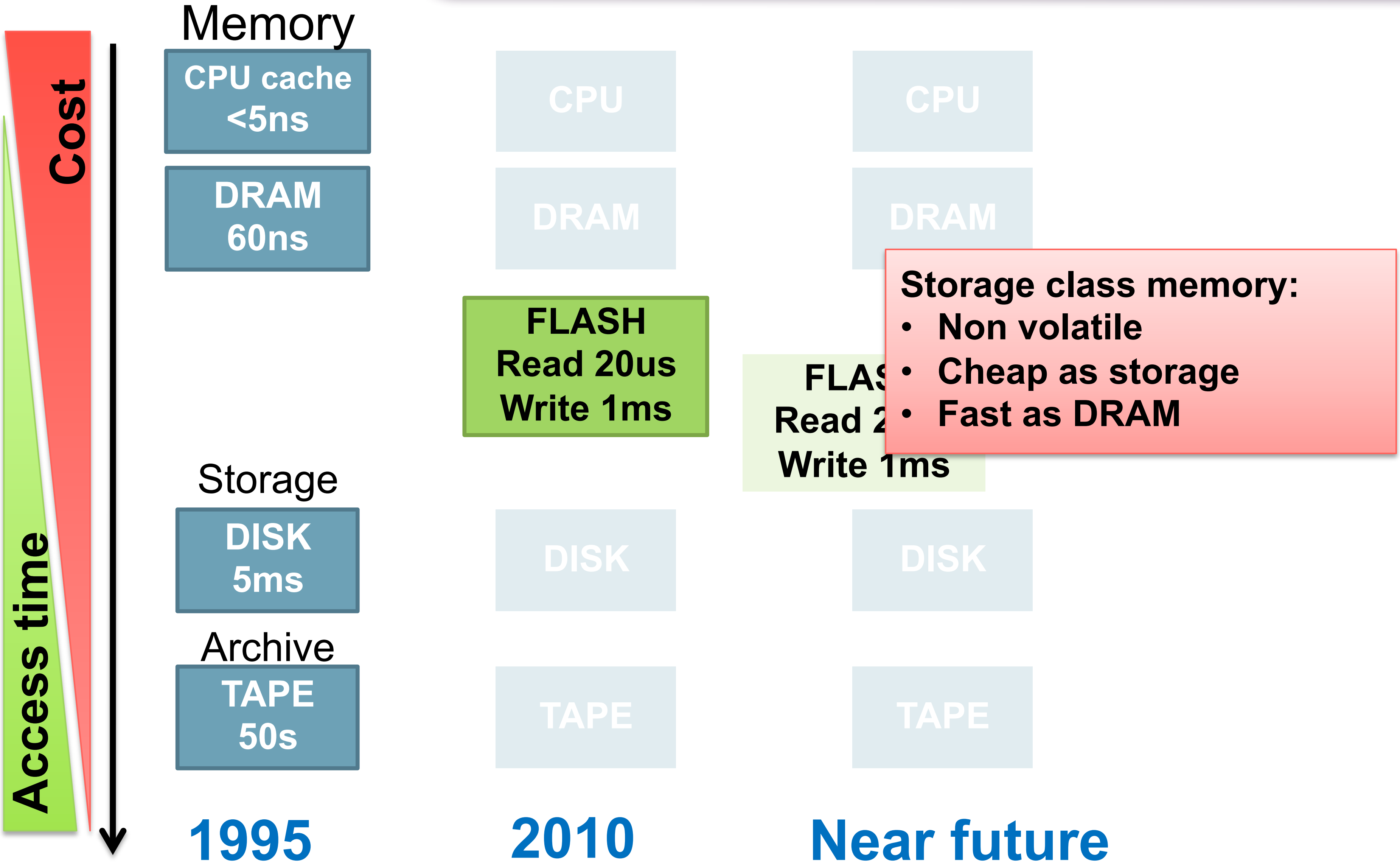
## (3) New Memory



## (4) Interconnect



# Performance gap in memory hierarchy: storage class memory



Cost

Access time

Memory

**CPU cache**
**<5ns**

**DRAM**
**60ns**

Storage

**DISK**
**5ms**

Archive

**TAPE**
**50s**

**1995**

CPU

DRAM

**FLASH**
**Read 20us**
**Write 1ms**

DISK

TAPE

**2010**

CPU

DRAM

**FLAS**
**Read 2**
**Write 1ms**

DISK

TAPE

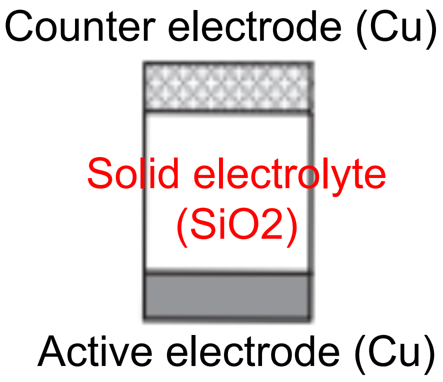
**Near future**

**Storage class memory:**
- **Non volatile**
- **Cheap as storage**
- **Fast as DRAM**

http://researcher.watson.ibm.com/researcher/files/us-gwburr/Almaden_SCM_overview_Jan2013.pdf

# Proposed storage class memory: Conductive-Bridging RAM (CBRAM)

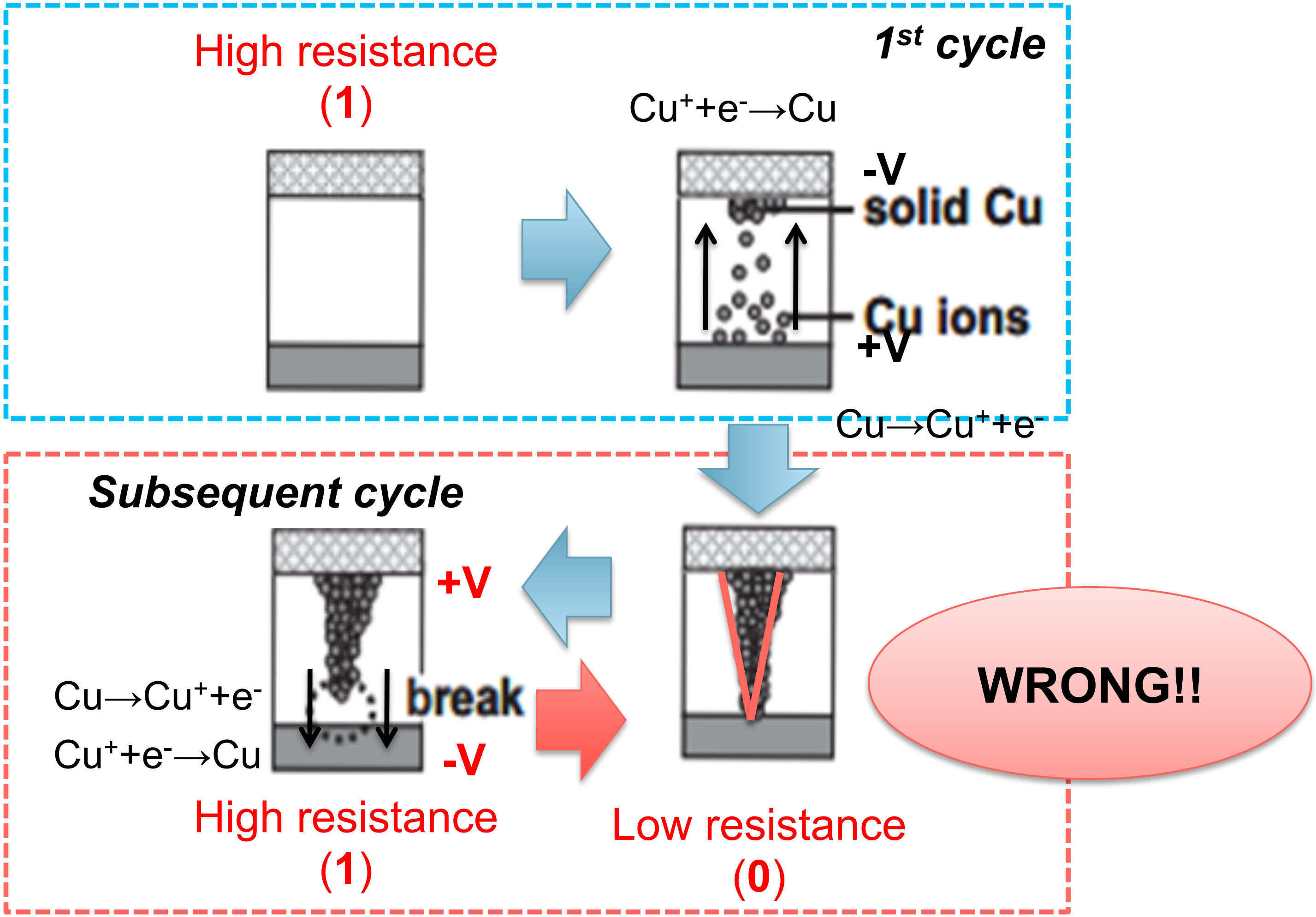
- Highly scalable:
  - » Simple geometry
  - » 20 nm – 30 nm in diameter demonstrated
- Low operation voltage:
  - » CBRAM 1~2V
  - e.g. Flash memory: programming voltage more than 10V, read voltage ~2V
- High speed:
  - » Program/erase speed depends on SET voltage (ns)
  - e.g. Flash memory 1us to 1ms
  - » Read speed: 1~10 ns
  - e.g. comparable to DRAM/SRAM



CBRAM meets the requirements for high speed and high scalability.

Ilia Valov *et al. Nanotechnology* 22 (2011)

# Working principles: “0” and “1”



1st cycle

High resistance
(1)

$Cu^+ + e^- \rightarrow Cu$

-V
solid Cu
Cu ions
+V

$Cu \rightarrow Cu^+ + e^-$

Subsequent cycle

+V

$Cu \rightarrow Cu^+ + e^-$

$Cu^+ + e^- \rightarrow Cu$

break

-V

High resistance
(1)

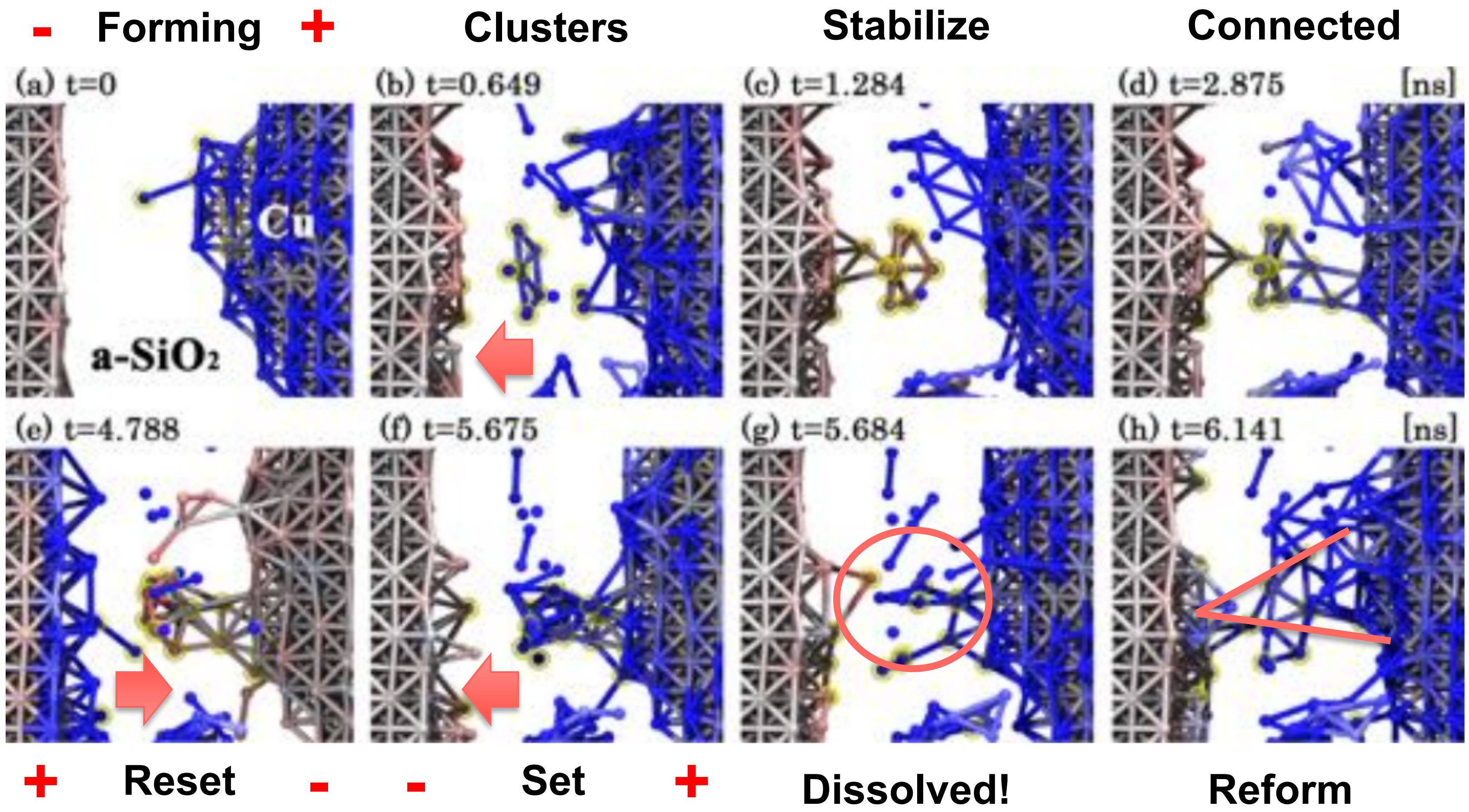
Low resistance
(0)

**WRONG!!**

CBRAM has simple geometry, but complicated reduction and oxidation reactions in electrode.

Y. Bernard,

# CBRAM at nanoscale

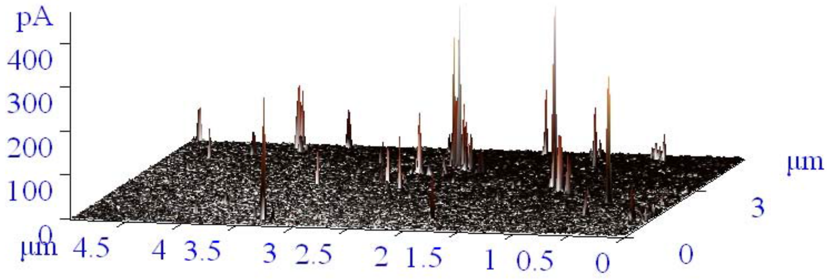


After set stage, a conical shape filament is formed and it is thicker at the active electrode, consistent with microscopy observations in larger cells.

Nicolas Onofrio, David Guzman & Alejandro Strachan. Nature Materials 14, 440–446 (2015) doi:10.1038/nmat4221
Yuchao Yang, Peng Gao, Siddharth Gaba, Ting Chang, Xiaoqing Pan, and Wei Lu. Nature communication, 3, Mar 2012.

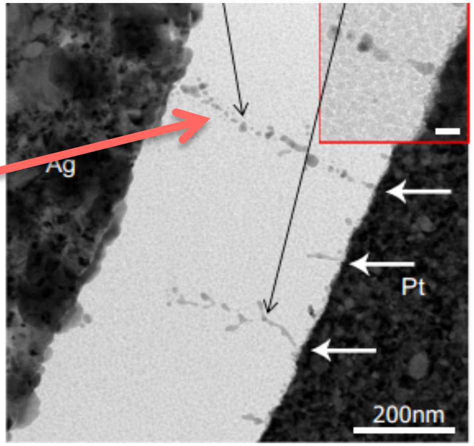
# Simulation Challenges

Experimental evidences show current is carried by nanoscale metal filaments in CBRAM



*D. Lee et al. IEDM* 2006

Observed filaments **in thin films.**
Lu et al. Nature Comm. 3, 732 (2012)



No direct observation in a **nanowire** cell:

- minimal cell size?
- parasitic tunneling current?

Simulation challenges:

- Modeling of electrochemical process
- Quantum transport in a disordered system
- Many atoms – heavy computations

Multi-physics atomistic simulations

# Methods: multi-scale simulation

- DFT: **Parameterization for Tight Binding method**
  - » Properties of certain materials
  - » System with small number of atoms

- Molecular Dynamics: **Atom position and Mulliken charge**
  - » ReaxFF –force field for chemical reaction

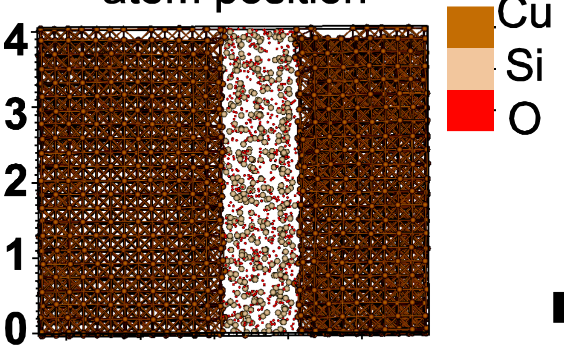
- Environment-dependent Semi-Empirical Tight Binding*: **Electric current**
  - » Parameters depend on distances between neighbors

*G. Hegde, et al. J. Appl. Phys. 115, 123704 (2014)

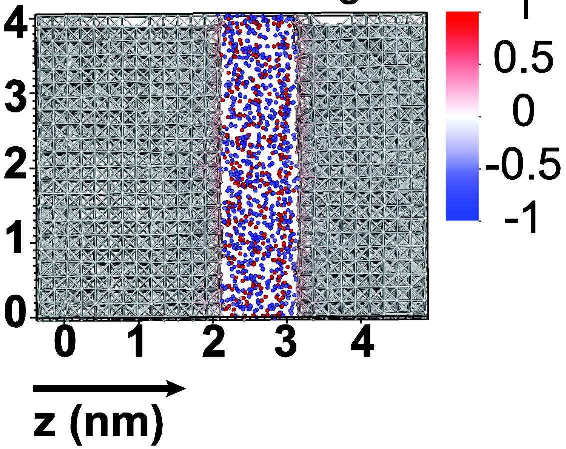
# Multi-scale simulation flow

**Molecular dynamics**

atom position

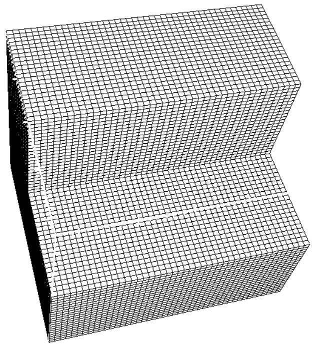


Mulliken charge

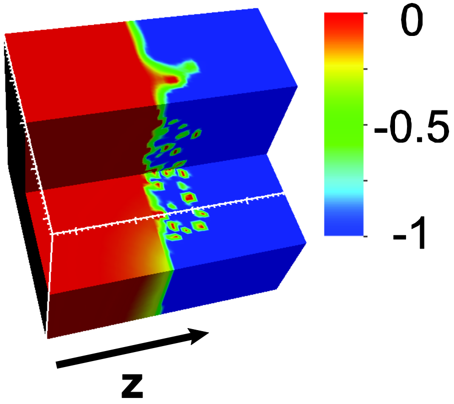


**The Poisson equation**

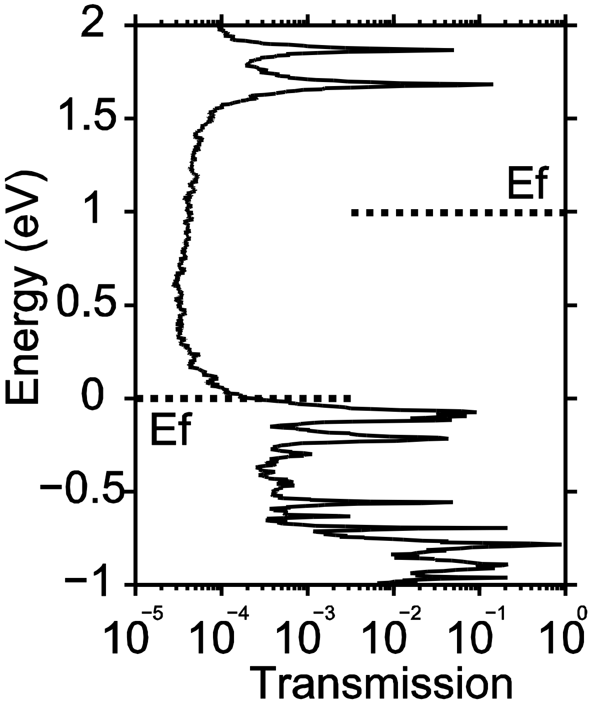
fem mesh 45x45x45



electrostatic potential



**Quantum transport**

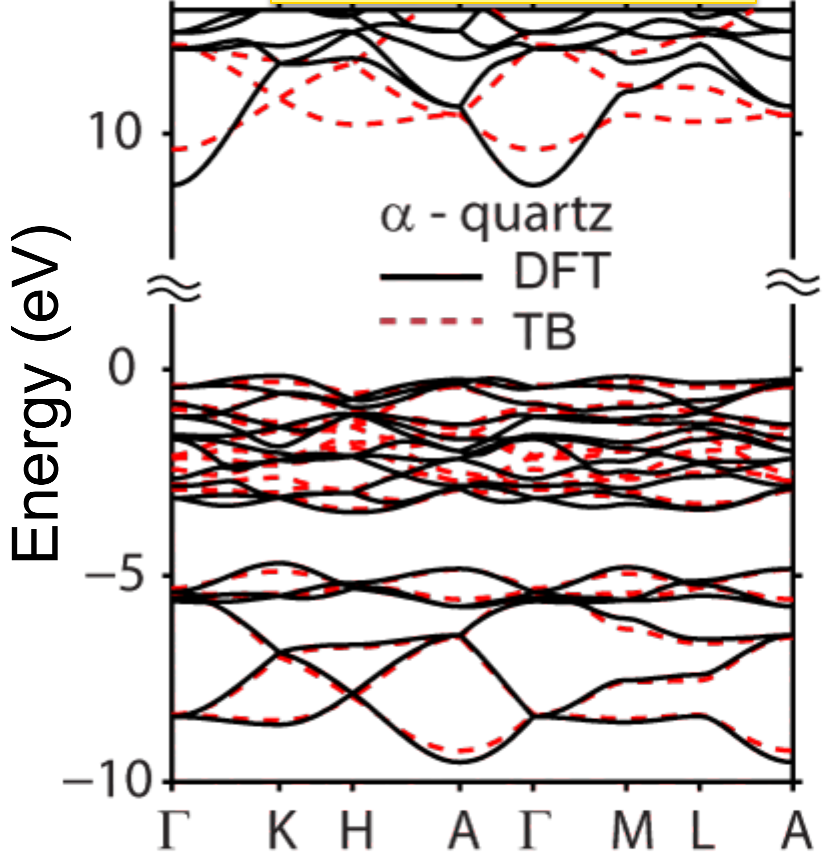


LAMMPS

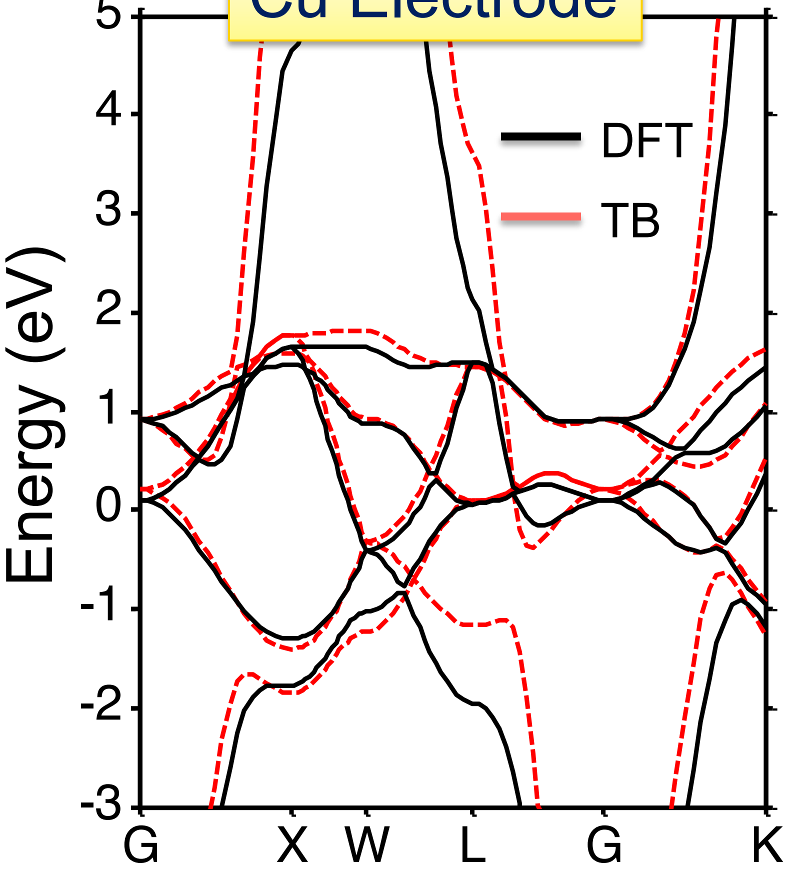
NEMO5

# Results: Tight Binding parameterization of materials

## $SiO_2$ Electrolyte



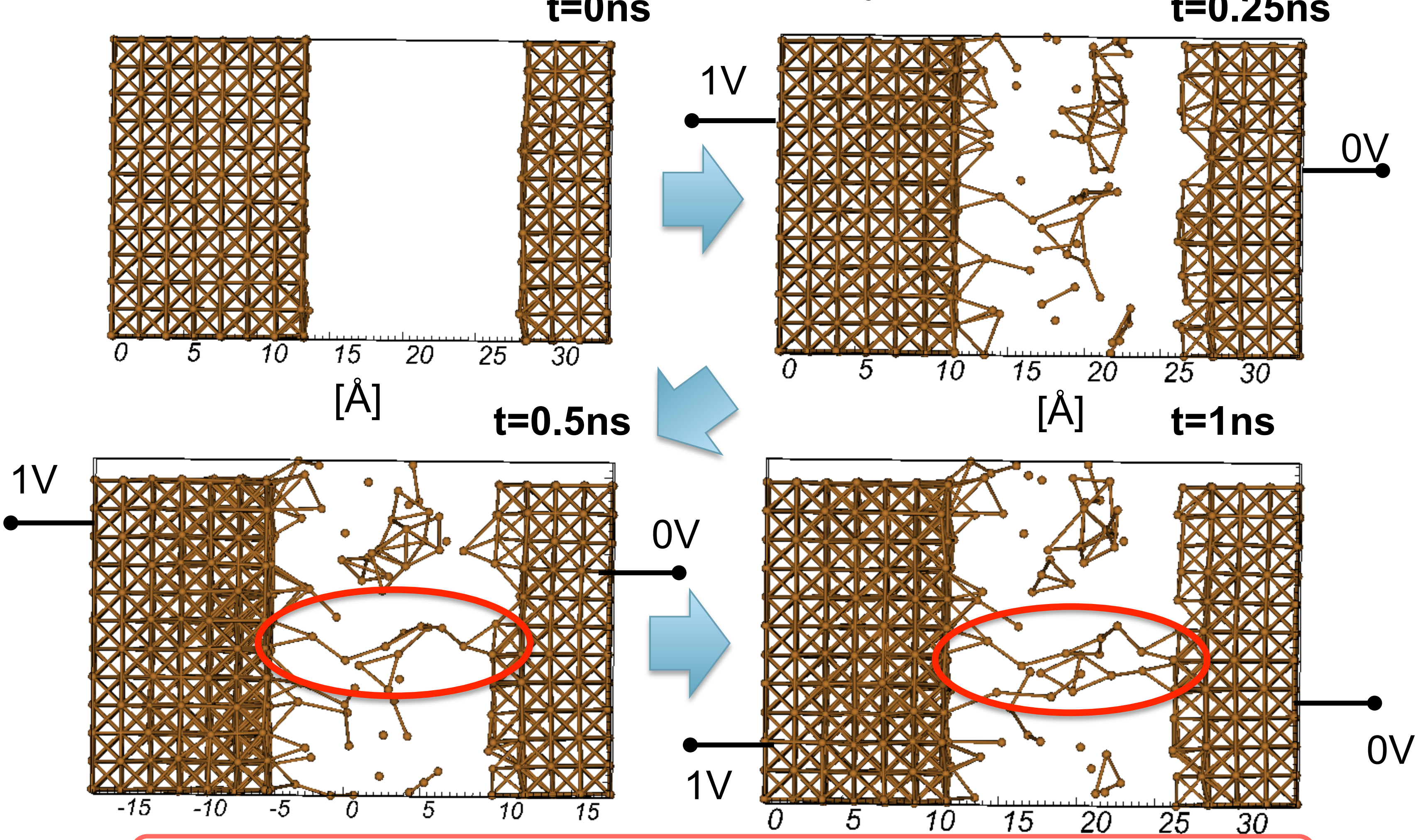
## Cu Electrode



Band structures for $SiO_2$ and Cu can be reproduced by the empirical tight binding (TB) method with *s*, *p* an *d* orbitals.

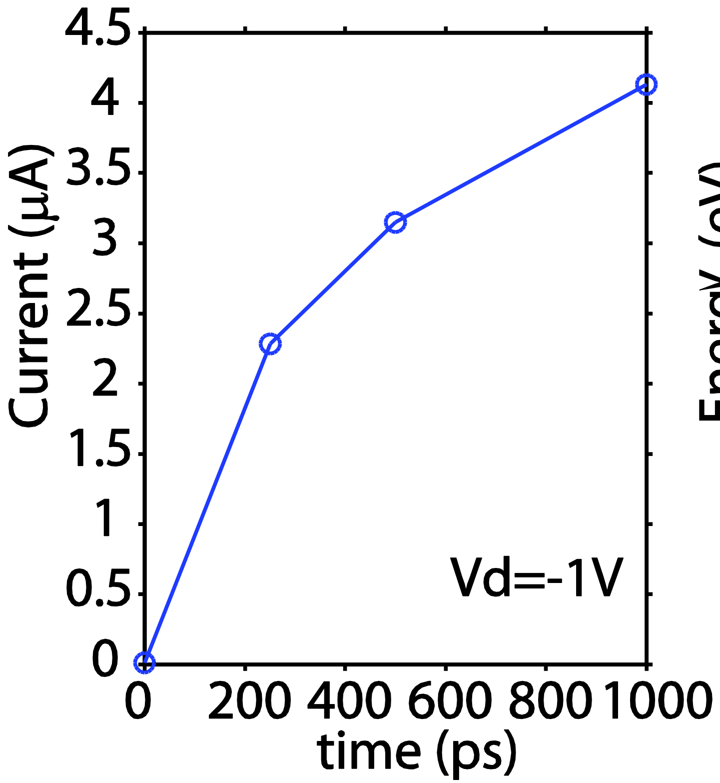
# Results: Molecular Dynamics of the filament formation

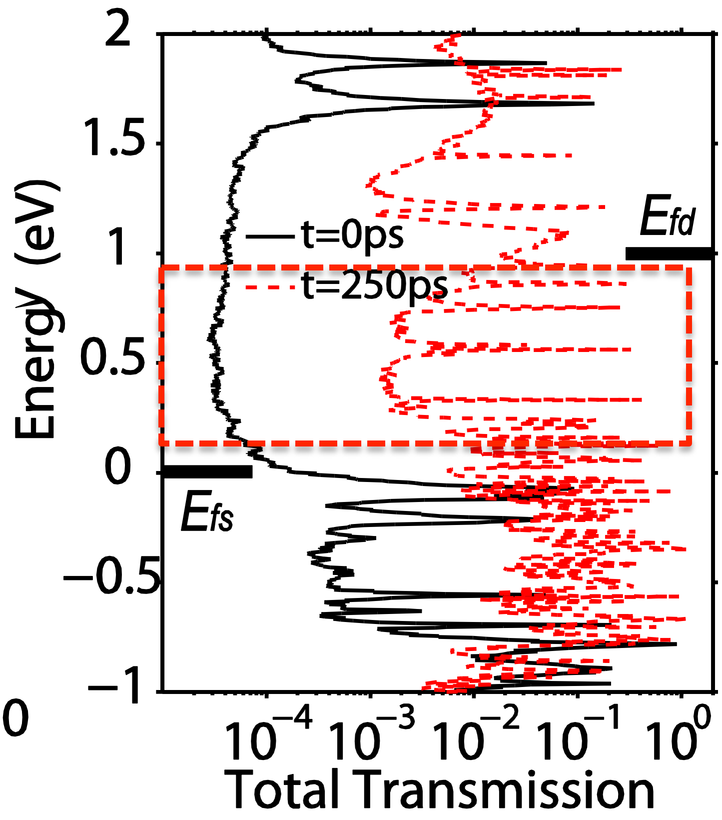
- Formation of Cu filament is simulated by MD with ReaxFF potential



Conducting bridge with a few atoms are formed at ~ 1ns.

# Results: Ballistic quantum conductance. Recursive Green's function method





Transmission at this energy range contributes to final current.

Current ON/OFF ratio of I($t_0$=0ps)/I($t_1$=250ps) = 195 is predicted.
Represents stable "0" and "1" states.

# CBRAM Summary

- CBRAM is a potentially promising storage class memory

- Simulation of CBRAM requires different models
  - » Electrochemical process
  - » Quantum transport

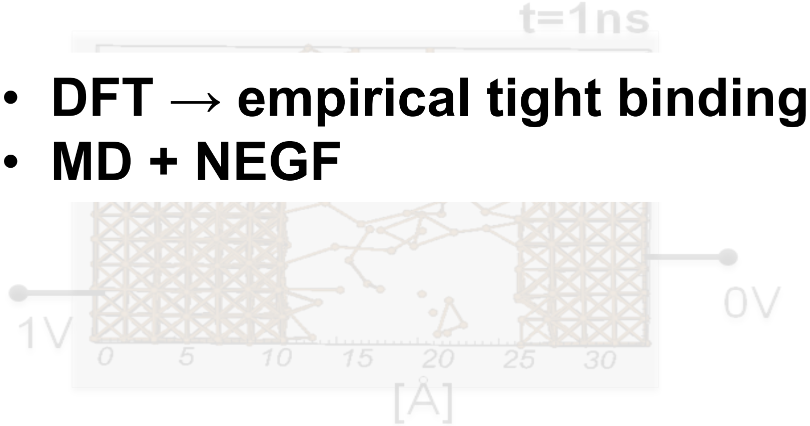
- Solution:
  - » Multi-scale simulation (Density Functional theory, Molecular Dynamics, Tight Binding)

# Outline

## (1) Low SS transistors I

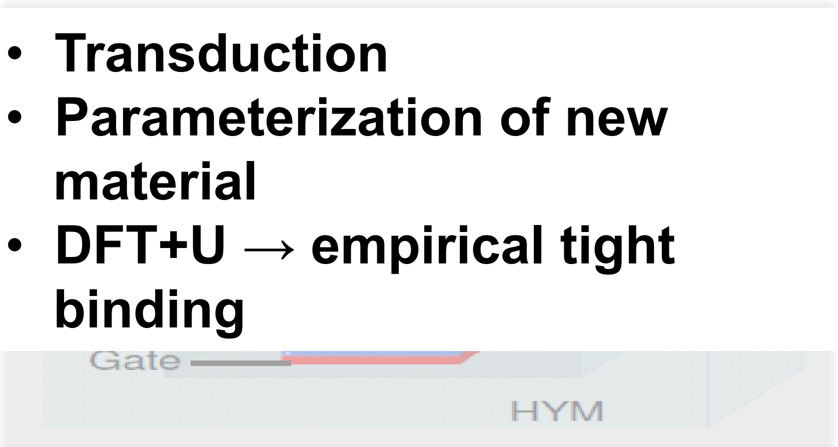
- Energy filtering
- Full band bandstructure → effective mass
- Drift – Diffusion + NEGF
- Improve efficiency

## (3) New Memory



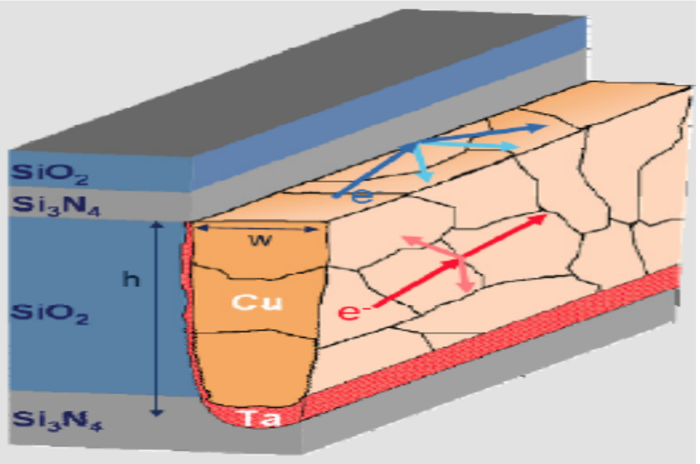
- DFT → empirical tight binding
- MD + NEGF

## (2) Low SS transistors II

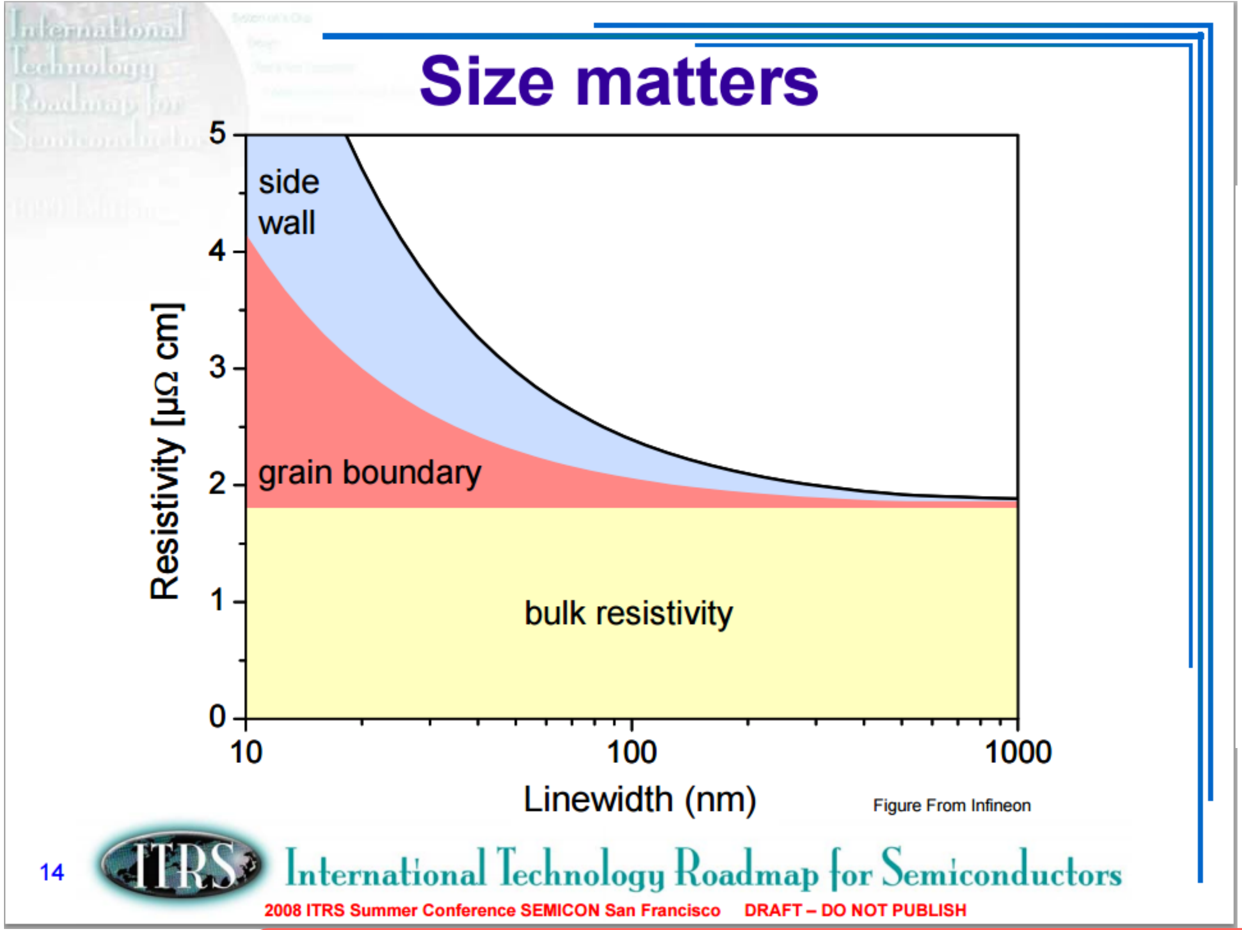


- Transduction
- Parameterization of new material
- DFT+U → empirical tight binding

## (4) Interconnect



# Motivation

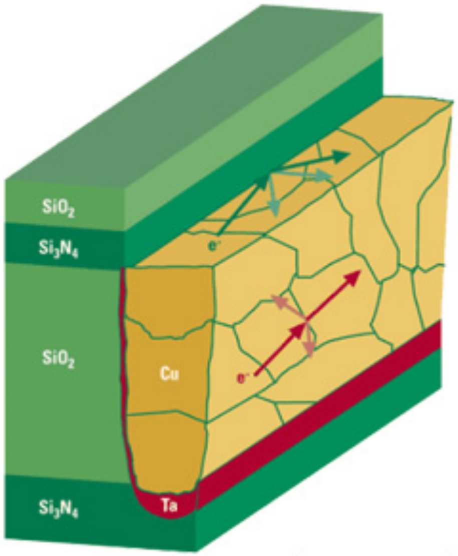


## Size matters

Figure From Infineon

14 International Technology Roadmap for Semiconductors

2008 ITRS Summer Conference SEMICON San Francisco DRAFT – DO NOT PUBLISH

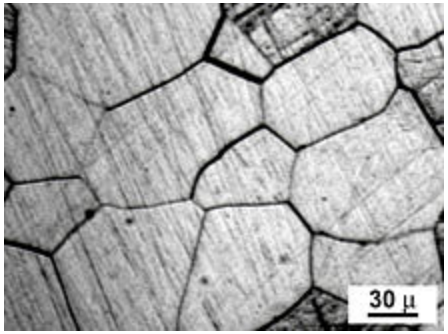


Surface and grain boundary (GB) scatterings are important!

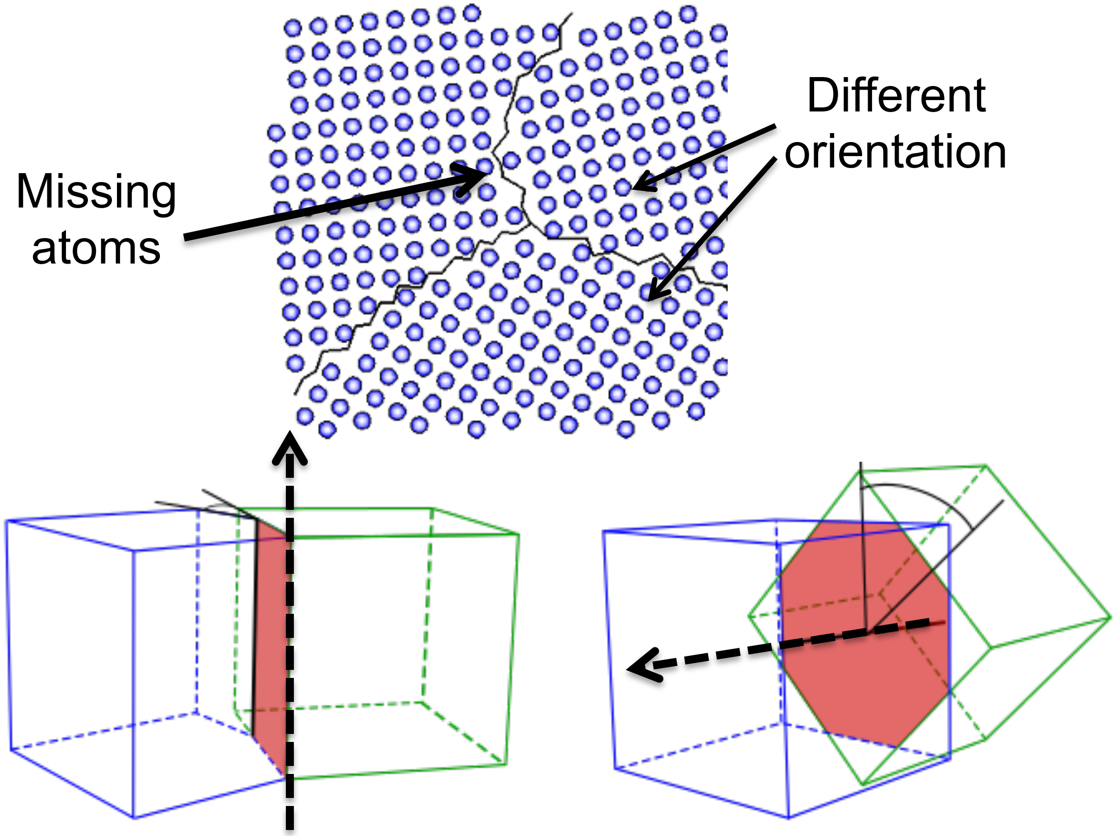
http://cseweb.ucsd.edu/

# Grains in materials

Micrograph of Real Grains



Computer Generated Grains


Missing atoms

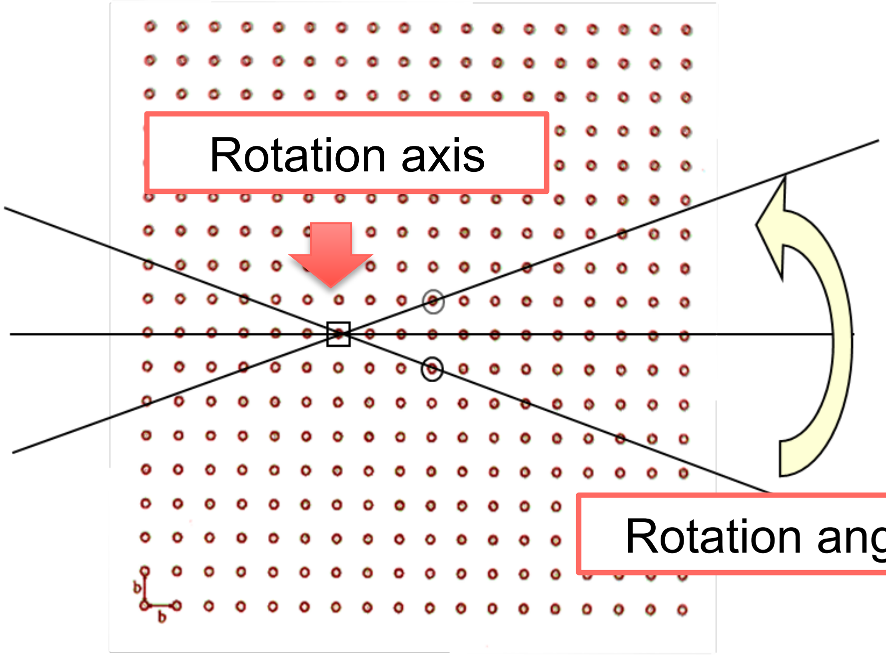
Different orientation

GB could be characterized by relative rotation of neighboring grains:
→ **Rotation axis and angle.**

Grain boundary is a type of defects in crystals.

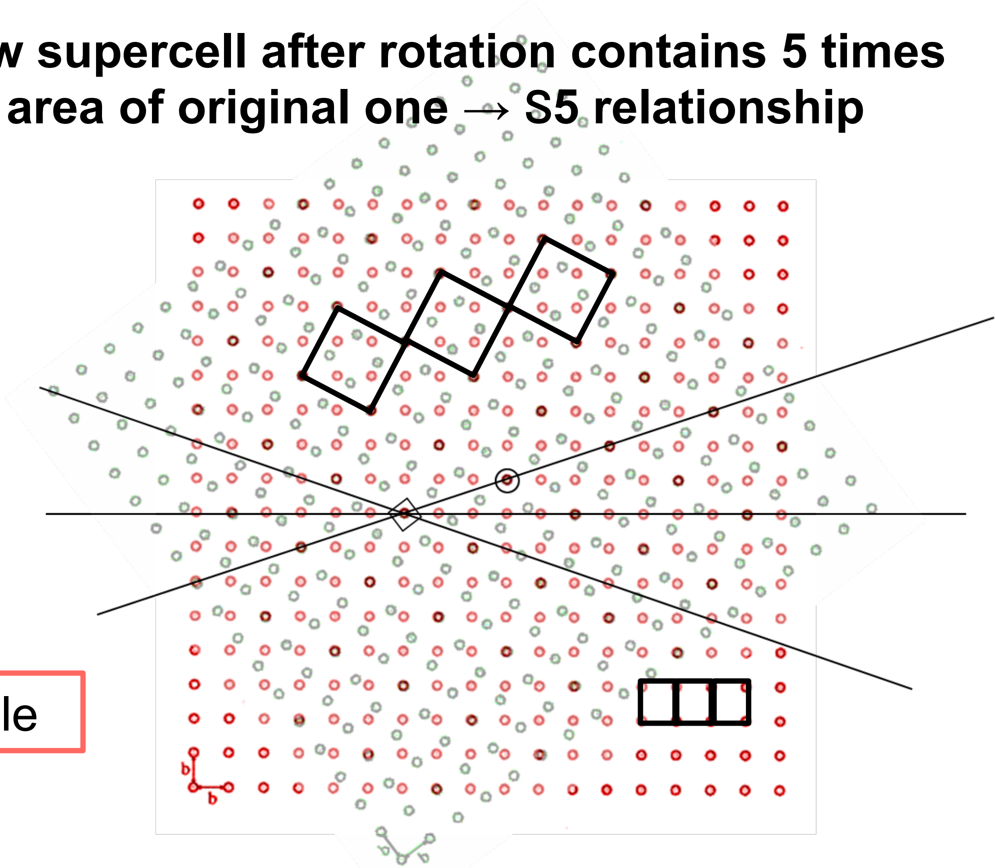
# Example: Coincident Site Lattice

**New supercell after rotation contains 5 times area of original one → S5 relationship**



Rotation axis

Rotation angle



Red and Green lattices coincide after rotation of *36.9°*

Coincident site lattices have lower energy.
Lower energy → preferable in real materials.

# Simulation steps

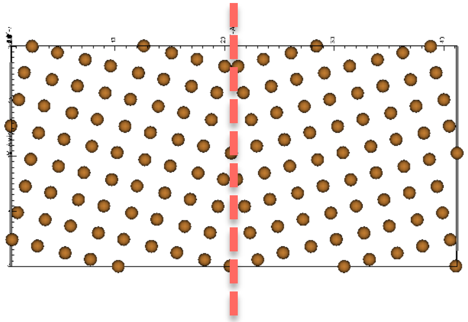
I. Resistivity of **coincident site lattice** grain boundaries
  - Geometry: single coherent grain boundary
  - Benchmark with DFT, Extended Hückel and experimental resistivity
  - Validation of tight binding parameterization

II. Simple grain boundary
  - Geometry: **2D** and **3D** double grain boundaries
  - Study effects of rotation angle

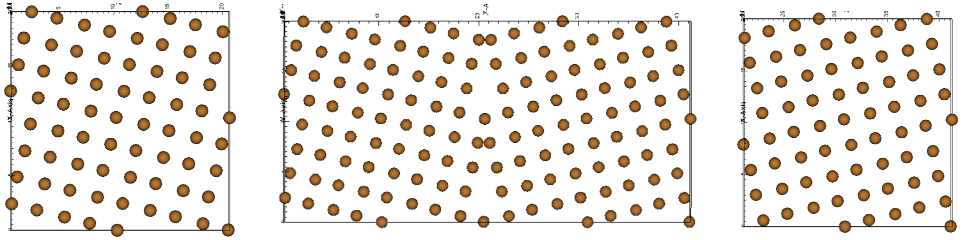
III. General grain boundaries
  - Geometry: Copper **nanowire**
  - Realistic grain geometries
  - Random rotation angle

# I. Method: Extract single GB resistivity

Σ17a single grain boundary

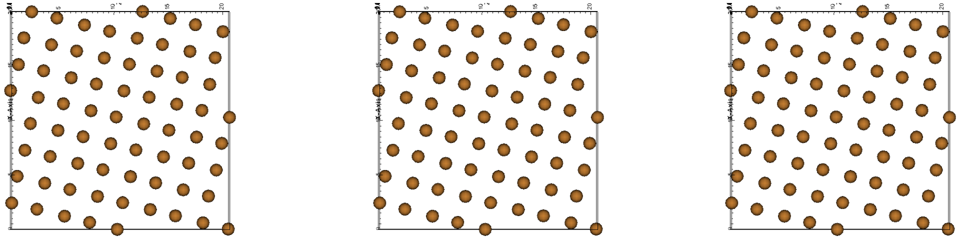


Single GB
$R_s$



**lead** **device** **lead**

Bulk Cu
R



GB resistivity: $R_{GB}=R_s-R$

**Single GB** is used to characterize GB resistivity.

# I. Results: Relaxation & resistivity

**Objectives:**

- Test accuracy of empirical tight binding (ETB) model for grain boundary resistivity.
- Test geometry relaxation of copper grain boundary with EAM potential.

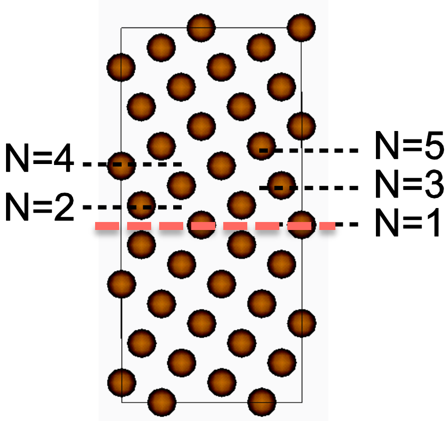
**Methods:**

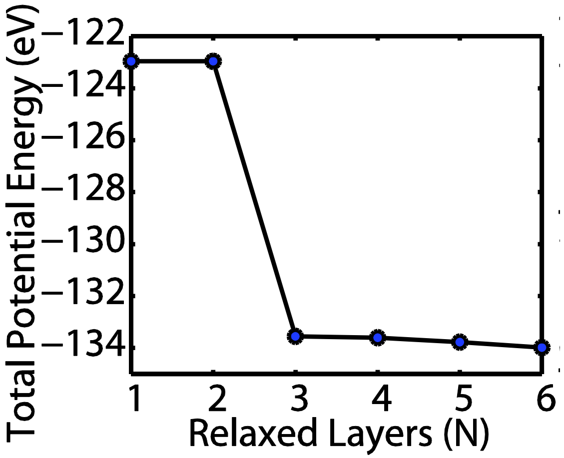
- Energy minimization with EAM potential
- Empirical tight binding parameterization
- NEGF

**Results:**

- ETB gives good matching with DFT, EHT for single grain boundary resistivity.
- Speed-up.
- Possibility to model realistic geometry with ETB.

**Relaxation by energy minimization with EAM**





| | Resistivity ($10^{-12}$ Ω-cm$^2$) | | |
|---|---|---|---|
| | DFT(exp.)* | ETB 2NN | EHT 3NN |
| Σ3 | 0.158 / 0.148 / 0.155 / 0.202 (0.17) | 0.116 | 0.248 |
| Σ5 | 1.49 / 1.885 | 1.28 | 0.997 |
| Σ9 | 1.75 | 1.49 | 1.008 |
| Σ11 | 0.75 | 0.715 | 0.574 |
| Σ13a | 2.41 | 2.272 | 1.368 |
| Σ17a | 2.01 | 1.916 | 1.15 |

*M. César, *et al.*, *Physical Review Applied*, vol. 2, p. 044007, 2014.

# II. “tilt” and “twist” GBs

**Objectives:**

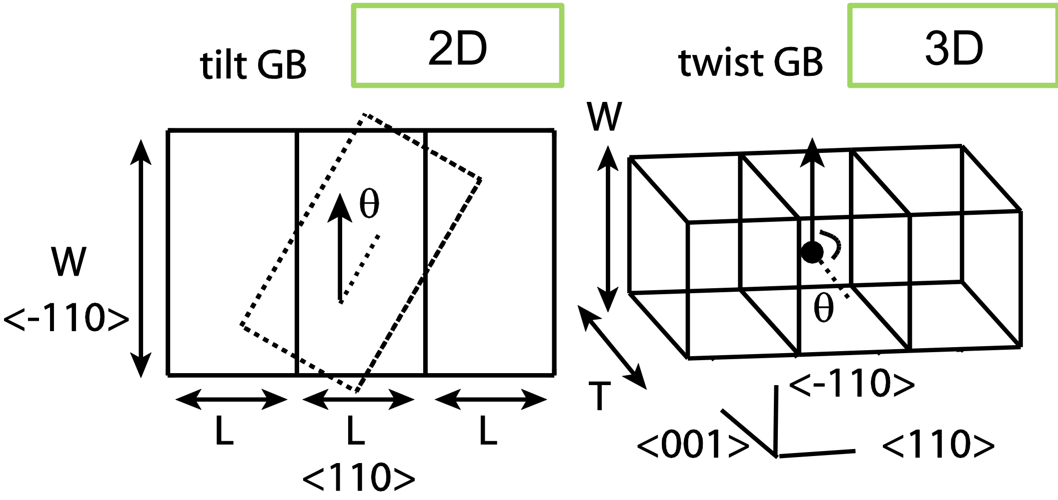
- Study effects of misorientation angle on grain boundary resistance

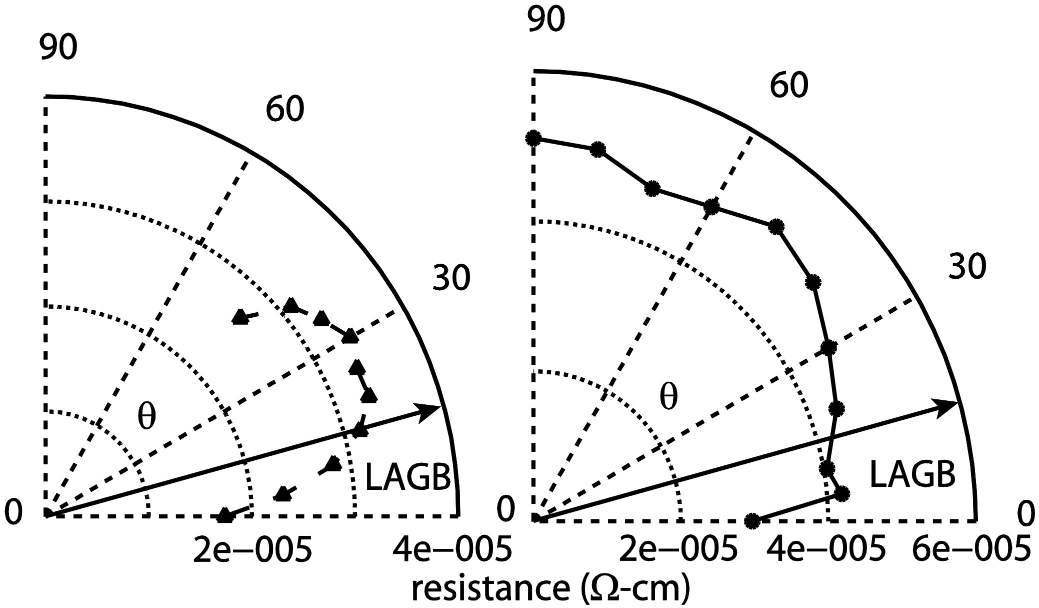
**Methods:**

- Energy minimization with EAM potential
- Empirical tight binding parameterization
- NEGF
- Construct 2D grains with tilt grain boundary along <110> Cu wire.
- Construct 3D grains with twist grain boundary along <110> Cu wire.

**Results:**

- Low angle grain boundaries (θ<15 degrees) has lower resistance than high angle grain boundaries.
- Calculated trend matches with expectation.





# III. Multi-grain boundary

**Objectives:**

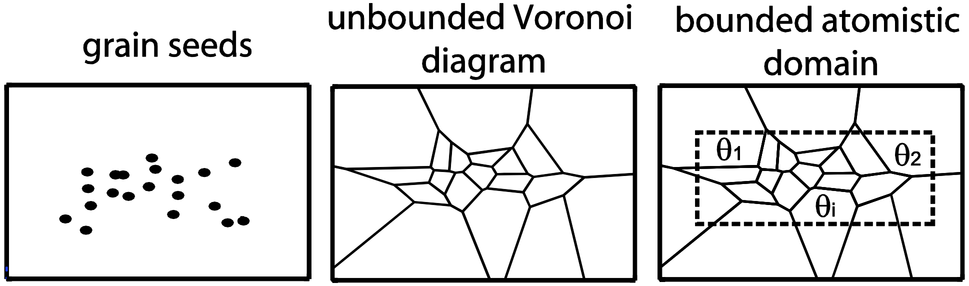
- Study impacts of general grain boundaries on interconnects resistance.
- Study effects of grain shapes on interconnects resistance.

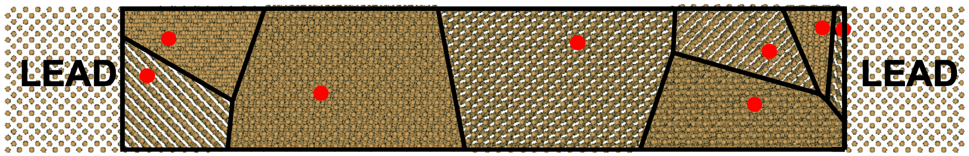
**Methods:**

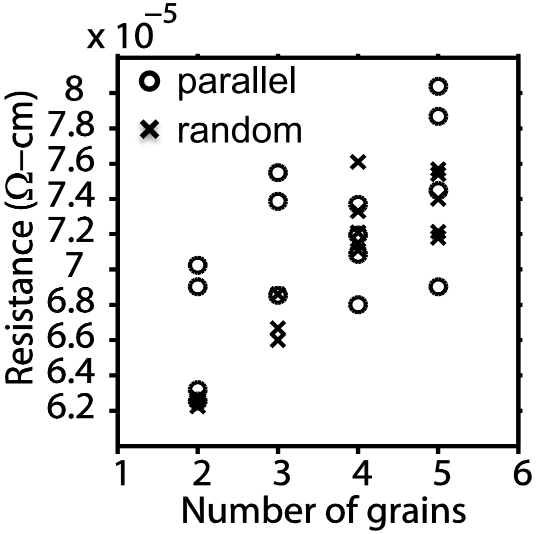
- Empirical tight binding parameterization
- Random grain generation: Voronoi diagram
- Energy minimization with EAM potential
- NEGF
- General misorientation = tilt + twist

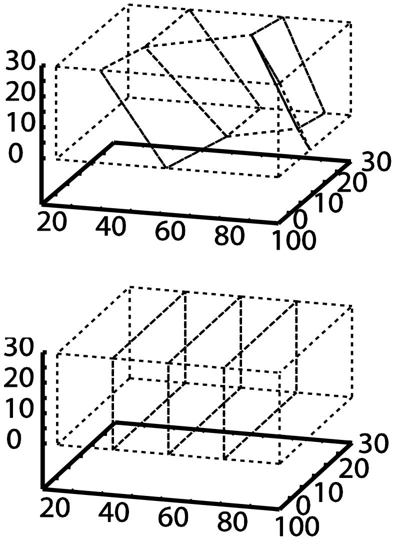
**Results:**

- Resistance of interconnect is dominated by misorientation of grains.
- Resistance is proportional to number of grain boundaries.









# Grain Boundary Summary

- Properties of GBs
  - » Coherent grain boundary gives small GB resistivity.
  - » Low angle grain boundary gives small GB resistivity.

- Energy minimization with EAM potential + ETB-NEGF gives similar accuracy in single grain boundary calculations as DFT-NEGF

- With ETB, it is possible to simulate more realistic interconnect structures with multiple grain boundaries.

# Outline

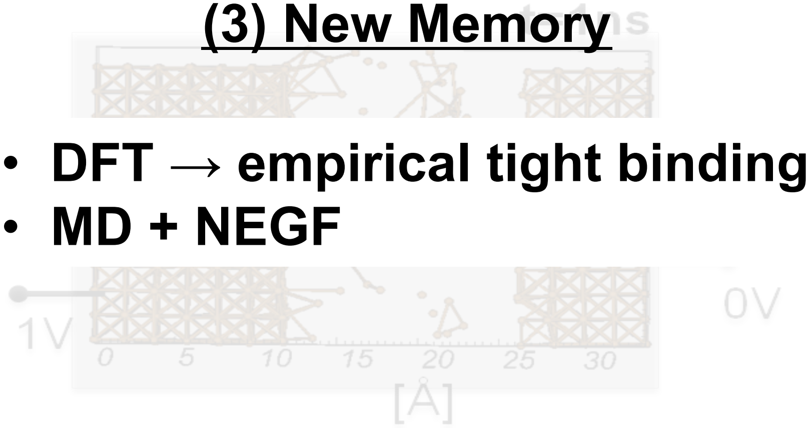
## (1) Low SS transistors I

- Energy filtering
- Full band bandstructure → effective mass
- Drift – Diffusion + NEGF
- Improve efficiency

## (2) Low SS transistors II

- Transduction
- Parameterization of new material
- DFT+U → empirical tight binding

## (3) New Memory



- DFT → empirical tight binding
- MD + NEGF

## (4) Interconnect

- Relaxation by EAM compared with DFT
- TB-NEGF compared with DFT and EHT
- Large scale simulation

# Summary

- Tight-binding is powerful model to bridge “continuous” and “*ab-initio”* world
  - » Accuracy
  - » Flexibility
  - » Computational burden
- There is no single model fits all situations
  - » Physical insights are required when using different models
  - » Benchmark between different models are important
- Multi-scale modeling study on low power devices
  - » TFET
  - » PET
  - » CBRAM
  - » Grain boundary

Multi-scale simulation are critical for making predictive designs

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