COMPUTATIONAL MODELING AND SIMULATION STUDY OF ELECTRONIC AND THERMAL PROPERTIES OF SEMICONDUCTOR NANOSTRUCTURES

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TO MY FAMILY AND THE ALMIGHTY...

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ABBREVIATIONS AND SYMBOLS

BCM	Bond Charge Model
BTE	Boltzmann Transport Equation
BZ	Brillouin Zone
CB	Conduction Band
CBM	Conduction Band Minimum
CBCM	Charge Based Capacitance Method
CMOS	Complimentary Metal Oxide Semiconductor
CP	Cross-Plane
C_v	Constant Volume Specific heat
D, Drn	Drain
DFT	Density Functional Theory
DM	Dynamical Matrix
DOF	Degree of Freedom
DOS	Density of States
DIBL	Drain Induced Barrier Lowering
DIBT	Drain Induced Barrier Thinning
DUT	Device Under Test
E_b,ϕ_{sc}	Source to Channel barrier height
E_f,E_F	Fermi Level
EMA	Effective Mass Approximation
EOX	Electric Field in Oxide
EOT	Electrical Oxide Thickness
FET	Field Effect Transistot
FEM	Finite Element Method

GAA	Gate-All-Around
g_m	FET transconductance
$\hbar$	reduced Planck's constant
I_{ON}	ON state channel current
IP	In-Plane
J_G, J_g	Gate tunneling current
κ_l	Lattice thermal conductivity
κ_e	Electronic thermal conductivity
k_B	Boltzmann Constant
KVFF	Keating VFF model
λ	Mean free path
λ_{ph}	Phonon mean free path
λ_e	Electron mean free path
LANTEST	LANdauer ThermoElectric Simulation Toolkit
MD	Molecular Dynamics
ML	Mono Layers
MM	More Moore
MTM	More Than Moore
MVFF	Modified Valence Force Field
MOSFET	Metal-Oxide-Semiconductor FET
m_0	Free electron mass in vacuum
N_A	Number of atoms in a unitcell
NBTI	Negative Bias Temperature Instability
NEGF	Non-Equlibrium Green's Function
NEMO-3D	Nano-Electronic MOdeling tool
NWFET	Nanowire FET
NZ	Non-Zero
OOP	Object Oriented Programming
OMEN	Quantum Transport Simulator

PbSe	Lead Selenide
PF	Power-Factor (in Thermoelectricity)
PGF	Phonon's Green Function
PR	Participation Ratio
q,e	Electronic charge
RTA	Relaxation Time Approximation
R_{th}	Thermal Resistance
$\psi(V_G)$	Surface potential
Σ	Self Energy
S, Src	Source
S_{AA}	Channel active cross-section area
SCE	Short Channel Effects
SL	SuperLattice
SO	Spin-Orbit Coupling interaction
SS	Sub-threshold Swing
SiNW	Si Nanowire
SVR	Surface-to-Volume Ratio
T	Temperature
T_D	Debye Temperature
TB	Tight-Binding
TBR	Thermal Boundary Resistance
TB-VCA	TB based Virtual Crystal Approximation
TE	ThermoElectric
ToB	Top-of-the-Barrier
T_{ox}	Oxide thickness
UTB	Ultra-Thin-Body
VB	Valence Band
VBM	Valence Band Maximum
V_g,V_G,V_{gs},V_{GS}	Gate Bias

V_{GT}	Gate overdrive
V_d,V_D,V_{ds},V_{DS}	Drain Bias
V_{inj}	Electron Injection Velocity
V_{snd}	Sound Velocity
ZT	Thermoelectric Figure of Merit

ABSTRACT

Paul, Abhijeet, Purdue University, December 2011. Computational modeling and simulation study of electronic and thermal properties of semiconductor nanostructures. Major Professor: Gerhard Klimeck.

The technological progress in dimensional scaling has not only kept Silicon CMOS industry on Moore's law for the past five decades but has also benefited many other areas such as thermoelectricity, photo-voltaics, and energy storage. Extending CMOS beyond Si (More Moore, MM) and adding functional diversity to CMOS (More Than Moore, MTM) requires a thorough understanding of the basic electron and heat flow in semiconductors. Along with experiments computer modeling and simulation are playing an increasingly vital role in exploring the numerous possibilities in materials, devices and systems. With these aspects in mind the present work applies computational physics modeling and simulations to explore the, (i) electronic, (ii) thermal, and (iii) thermoelectric properties in nano-scale semiconductors. The electronic structure of zinc-blende and lead-chalcogenide nano-materials is calculated using an atomistic Tight-Binding model. The phonon dispersion in zinc-blende materials is obtained using the Modified Valence Force Field model. Electronic and thermal transport at the nano-scale is explored using Green's function method and Landauer's method. Thermoelectric properties of semiconductor nanostructures are calculated using Landauer's method.

Using computer modeling and simulations the variation of the three physical properties (i-iii) are explored with varying size, transport orientation, shape, porosity, strain and alloying of nanostructures. The key findings are, (a) III-Vs and Ge with optimized strain and orientation can improve transistors' and thermoelectric performance, (b) porous Si nanowires provide a lucrative idea for enhancing the thermo-

electric efficiency at room temperature, and (c) Si/Ge superlattice nanowires can be used for nano-scale tuning of lattice thermal conductivity by period control.

The present work led to the development of two new interface trap density extraction methods in ultra-scaled FinFETs and correlation of the phonon shifts in Si nanowires to their shape, size and orientation benchmarked against experimental Raman spectroscopy data, thereby enabling nano-scale metrology. Contribution of two research and six educational tools on nanoHUB.org forms an integral part of the work for global dissemination of semiconductor knowledge.

Atomic level manipulation holds the key to engineer material properties at the nano-scale. The findings of this work will hopefully open and guide new ways of engineering the electronic and thermal properties for better performance.

1. SEMICONDUCTOR NANOTECHNOLOGY: INNOVATIONS FOR FUTURE

Scaling of silicon transistors have continued for the last five decades due to the immense progress made in fabrication technologies keeping the transistor manufacturing industries on Moore law's path [1, 2]. A variety of technological innovations ranging from strain engineering, high-κ metal gates, gate last process and so on have pushed the Silicon performance far beyond than it was expected as reflected from the CMOS [1] scaling road-map of Intel shown in Fig. 1.1. The progress in CMOS fabrication methods has diffused into other technological areas as well such as thermoelectricity, photo-voltaics, and energy storage escalating the development of newer devices.

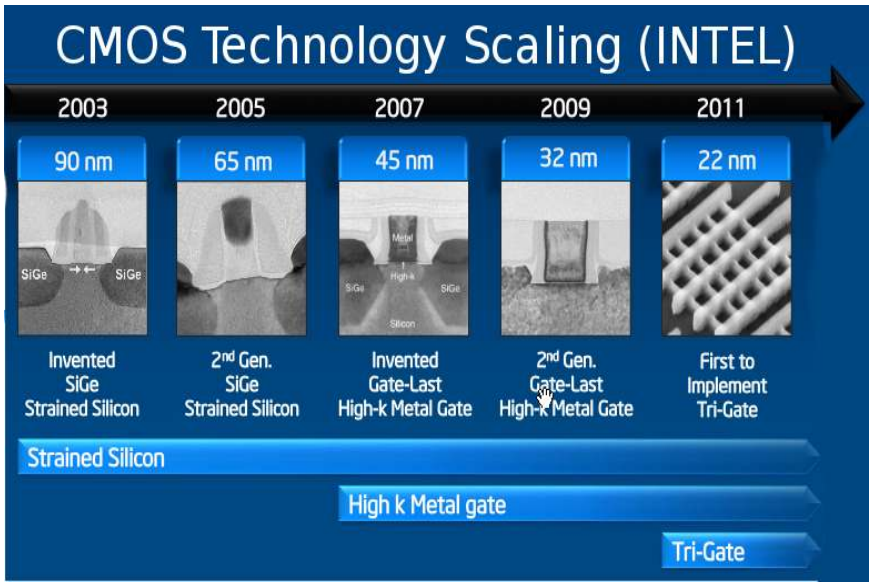

Fig. 1.1. The CMOS scaling trend in the last few years. The transistors changed from planar to 3D geometry to obtain higher benefit in terms of performance from Silicon. The image adapted from *http://www.intel.com/technology/silicon/tri-gate.htm.*

[1]Complimentary Metal Oxide Semiconductor

One of the areas where dimensional scaling has given a big performance boost is 'thermoelectricity', the interconversion of heat into electricity and vice-versa. Of all the renewable energy sources, thermoelectricity provides unique opportunity since it can be used as a generator deriving power out of waste heat as well as a quite efficient cooler/heater [3, 4]. Semiconductor materials are one of the most promising thermoelectric materials that allow separate engineering of electronic and thermal properties [5]. The ability to manipulate the materials at the atomic scale using structures such nanowires, thin films and quantum dots took the thermoelectric efficiency (ZT) beyond 1 after four decades of research [6]. The trends of scaling in thermoelectric (TE) materials is shown in Fig. 1.2.

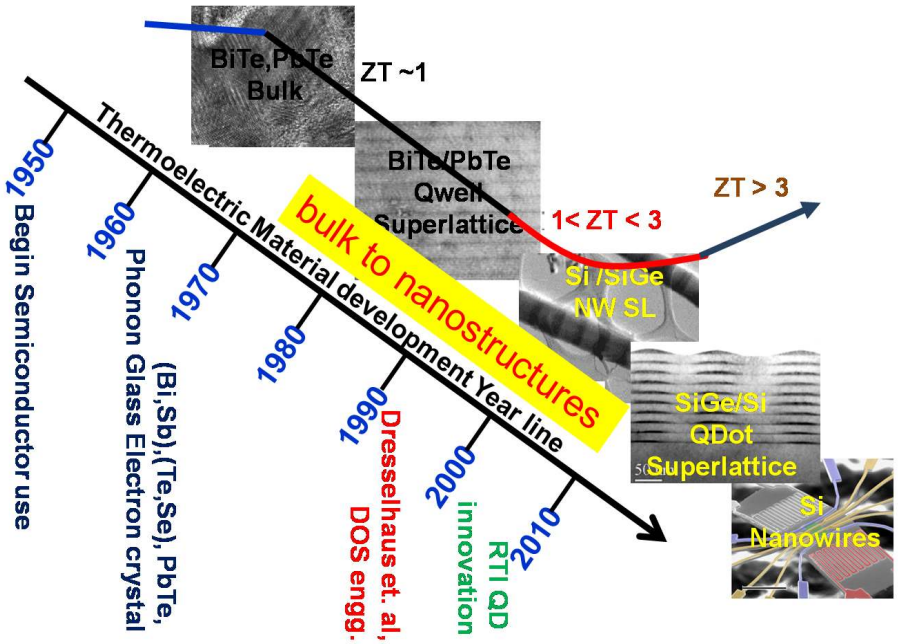

Fig. 1.2. The scaling of thermoelectric materials over the last six decades. The big boost in the ZT came only after nano-scale innovations such as nanowires, superlattices and quantum dots were used [6, 7]. The field sees a lot of technological innovation because of the advances made in CMOS fabrication processes.

Nanotechnology is playing a key role in these technological improvements by providing us the ability to manipulate matter at the atomic level, where conventional

physics breaks down, to impart new materials or devices with performance characteristics which are far better than the older approaches. For example, geometrical confinement can be used for manipulating electronic, thermal, optical and mechanical properties which can result in better transistors, thermoelectric devices, optical sensors, etc. Silicon has been pushed to its limit by nanotechnology and now questions are being asked if Silicon is running out of steam ? Is Si reaching its scaling limits ?

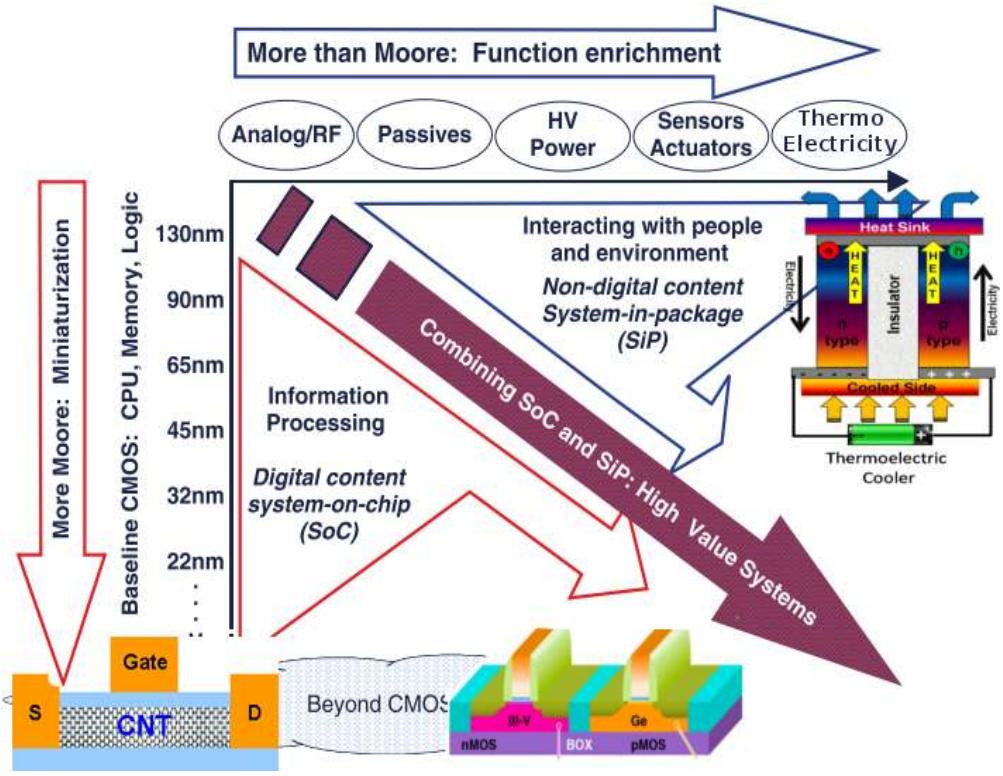

Fig. 1.3. The technological ways to extend the Moore's law. One branch explores new materials for making smaller transistors like III-V, Ge, Graphene, etc. This route is called the 'Moore Moore' (MM) path. The other branch extends to add more functional diversity to CMOS ranging from sensors to energy converters, etc. This route is called 'More Than Moore' (MTM) path. Part of the picture adapted from [8].

The answer seems to be yes for the questions asked above. It is getting harder to get more out of Silicon to meet the technological demands [8, 9]. This has put forth two very important questions now, which are, (i) What is next after Silicon

? and (ii) What more than just CMOS ? The first question is answered by the so called 'More Moore' (MM) [9, 10] concept and the second one is addressed by the 'More Than Moore' (MTM) [11] concept. The MM concept relies on using, (i) non-Si materials for the transistor channel such as III-V, Graphene, and Ge, and (ii) non-planar 3D transistor structures such as finFETs [12], trigates, and gate-all-around (GAA) FET [13]. The idea of MTM relies on adding more functional diversity to the existing electronic systems by including sensors, actuators, transducers, energy converters which is like adding eyes, ears, and nose to the brain [10, 11] (Fig. 1.3).

Extending the knowledge gained from CMOS technology to newer areas will require testing of ideas and concepts in the new setup. There are some very important issues which needs to be addressed for moving the technology forward. The next section talks about some of the relevant issues which are deterrent in the path of technology.

1.1 Challenges and Opportunities at the nano-scale

Some relevant technological challenges are presented in this section. The challenges are also opportunities to dwell into newer areas where the immense knowledge acquired from the CMOS technology will be useful. These technological challenges are:

1. CMOS performance: The performance of the Silicon transistors are being constantly pushed but then Si is hitting its fundamental limits. The planar transistors are replaced by non-planar Si structures like FinFETs [12], trigated FETs [14], etc. The non-planar technologies provide better gate to channel control and reduce Short Channel Effects (SCEs) [15, 16]. But 3D technology has many challenges like gate-stack integration, source/drain contacts, extremely high source drain resistances, integration with higher metal layers, bad semiconductor-oxide interface, lithography, etc. Even 3D geometry cannot push Si all the way to 8nm channel length devices.

2. Alternatives to Si FETs: There is a greater thrust to replace Si with other semiconductors. In this direction III-V and Ge are main contenders since these materials have better intrinsic electron and hole mobility, respectively compared to Si. However, newer materials also bring issues of process integration, gate-stacks and thermal budget. In the recent times a lot of progress in fabrication has been made which has allowed the manufacturing 3D-transistors using III-V [17] and Ge [18].

3. Nano-scale metrology: Another area which needs a lot of thrust is 'metrology'. Metrology deals with ability to obtain the details about the material and structure at the microscopic level. Method like SEM [2], NBD [3], Raman spectroscopy, etc, fall into this category. With shrinking device dimensions these methods need to be changed, upgraded and replaced by newer techniques. This area provides a lot of interesting and exciting opportunities.

4. Thermoelectric Efficiency: The large amount of waste heat is generated in the integrated chips, automobiles, boilers and industries. This opens up the exciting area of thermoelectric waste heat recovery. Nanotechnology is playing a key role in enhancing the ZT of such systems [3,6,19,20]. Semiconductor nanostructures are highly preferable materials but there are challenges in terms of process integration, material screening, assembly, etc., which have to be addressed for further progress.

5. Nano-scale thermal management: For computer chips, 'smaller and faster' just isn't good enough anymore. Power and heat have become the biggest issues for chip manufacturers and companies integrating these chips in everyday devices such as cell phones and laptops. The computing power of today's computer chips is provided mostly by operations switching at ever higher frequency. This physically induced power dissipation represents the limiting factor to a further

[2]Scanning Electron Microscope
[3]Nano-Beam Diffraction

increase of the capability of integrated circuits. Thus, heat management at the nano-scale is a big challenge and also provides lot of opportunities for research.

These challenges also bring a lot of opportunities with them. The improved fabrication methods [13,21–25] form an integral part to address these challenges. However, with endless possibilities, fabrication of every combination of material and structure is both impractical and economically unviable. To this end accurate computer modeling plays a significant role not just in explaining the experimental results using physics based modeling but also screening better technological options by predictive and evolutionary modeling [26–29].

1.2 Role of computer modeling

In the present work attempt is made to find solutions to the technological issues at the nano-scale using computer modeling and simulation. The importance of computer modeling can be understood from the fact that there are numerous possibilities of material, devices and systems which can be tried. An example is the use of complex materials for thermoelectricity as given here,

- Nano-composites, Ref. [30]
- Nanowires, Ref. [31–33].
- Superlattices, Ref. [34, 35].
- Complex materials, Ref. [36, 37].
- Hollow-porous materials, Ref. [38].
- Metal nitride superlattice, Ref. [39].

The list above shows the complexity in the materials and the dimensions with shrinking devices. It is important to switch to other methods for identifying better

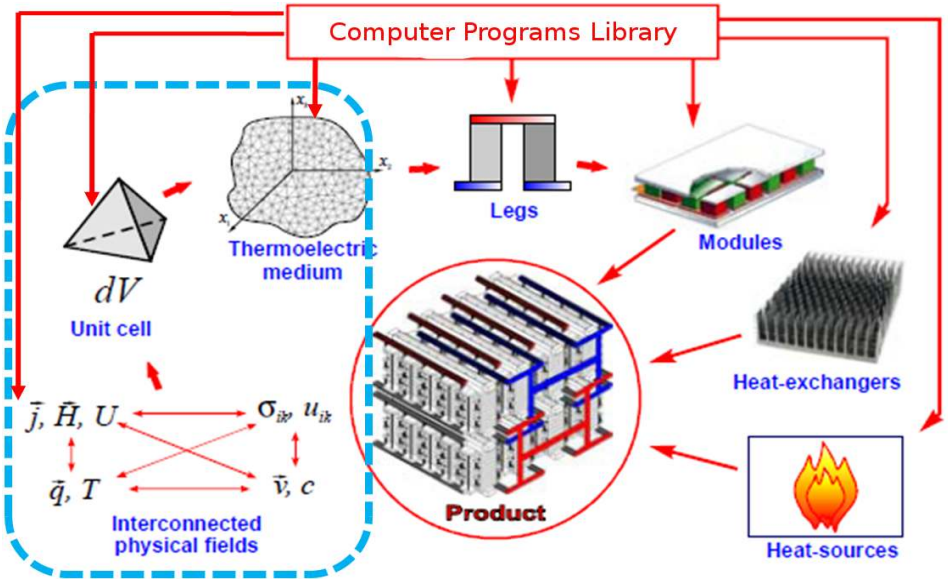

Fig. 1.4. TCAD modeling for thermoelectricity using object oriented approach of programming [26]. The present work focuses at the lowest level in material and device physics (shown by the dotted rectangle).

material combinations, which must be faster and cheaper than the original experiments and fabrication. To this end computer simulations serve the purpose. The central idea of this thesis is the judicious use of modeling and simulation, for determining the electrical, thermal and thermoelectric characteristics of the many device alternatives, that can serve as a cost-effective methodology to screen out the choices which are either difficult to manufacture or do not provide superior system-level performance [29].

As an example a broad idea for the complete thermo-electric-electric TCAD modeling is shown in Fig. 1.4 [26]. The method of object-oriented programming can be very useful for creating an hierarchy of computer modules with increasing complexity starting from a unit cell of a material to multicomponent devices. Thus, computer modeling and simulation will play a vital role in the development of future transistors and TE devices. The work in this thesis is around the lowest level to understand the physical, electronic and thermal aspects of materials under different conditions such

as geometrical confinement, application of potential and temperature gradient and alloying.

1.3 Main themes in the Thesis

The work in this thesis applies computational physics modeling and simulations to explore, (i) electronic, (ii) thermal, and (iii) thermoelectric properties in nano-scale semiconductors. A brief description of the three main themes is provided next.

1.3.1 Electronic Calculations

A semi-empirical atomistic Tight-binding (TB) model is used to obtain the electronic structure in semiconductor nanostructures [40–42]. The electronic transport analysis is mainly based on two models, (i) 'Virtual source' model [43], and (ii) Non-equilibrium Green's Function (NEGF) method [44, 45]. Atomistic electronic calculations in nanostructures helped in, (i) obtaining the validity range for the 'virtual source' model (Ch-2), (ii) calculating the electronic structure and conductivity in PbSe nanowires (Ch-3), (iii) scaling trends of SiGe nanowire transistors (Ch-3), (iv) development of 'Bandstructure Lab' tool on nanoHUB.org [46](Ch-3), (v) explaining the experimental C-V of gate-all-around Si nanowire transistors [47] (Ch-4), (vi) explaining the strain effects in biaxially strained SiGe bulk p-type transistors [48] (Ch-4), and (vii) understanding temperature based conductivity and interface trap extraction in undoped Si trigated transistors [16, 49] (Ch-4).

1.3.2 Lattice Thermal Calculations

An inter-atomic force constant model called the Modified Valence-Force-Field (MVFF) model [50] is used to calculate the 'phonons' or lattice vibrations in zinc-blende semiconductors. The phonon dispersion of nanowires is utilized to understand the thermal and mechanical properties of the nanostructures. Using the dynami-

cal matrix, Phonon Green's Function (PGF) is solved to obtain the heat flow in nanostructures. Inter-atomic force constant calculations in zinc-blende semiconductors allowed, (i) to obtain the phonon dispersion in bulk and nanostructures (Ch-5), (ii) calculation of thermal properties and their scaling trends in nanowires (Ch-6), (iii) calculation of Raman shifts and their scaling trends in nanowires (Ch-6), (iv) to understand the effect of strain and porosity on the thermal properties of Si nanowires (Ch-7), (v) to explore the thermal boundary resistance in Si/Ge interfaces (Ch-7), and (vi) thermal transport in ultra-short SiGe superlattice nanowires (Ch-7).

1.3.3 Thermoelectric Properties

Combining the learning and findings from Sec. 1.3.1 and 1.3.2, the nano-scale thermoelectric properties are analyzed within Landauer's model [51] using carrier scattering. This work encompasses the following, (i) a faster electronic and phonon mode counting method to calculate the transport parameters (Ch-8), (ii) ballistic thermoelectric analysis in GaAs and Si nanowires to understand the scaling trends (Ch-9), (ii) role of strain and orientation on improving the thermal efficiency (ZT) of n-type GaAs nanowires (Ch-10), (iii) role of porosity in improving ZT in Si nanowires (Ch-10), and (iv) developing thermoelectricity analysis tool called 'LANTEST' [4], on nanoHUB.org (Ch-10).

1.4 Contribution of the present work

The work outlined in the present work provides solutions to some of the technological challenges outlined in Sec. 1.1 as follows,

1. CMOS performance: Using careful simulation and modeling the performance of nano-scale SiNW FETs have been analyzed. The performance can be engineered using strain, channel and substrate orientation, and use of high-k gate dielectric.

[4]LANTEST is **LAN**dauer's **T**thermo**E**lectric **S**imulation **T**oolkit

The use of 3D geometry is important to obtain a better gate to channel coupling. The findings in this area are published in these Refs. [49, 52].

2. Alternatives to Si FETs: In this regard the feasibility of the SiGe nanowire FETs for both n- and p-type has been tested. There is an optimal design space which can beat Si CMOS technology. Also the feasibility of GaAs UTB pFETs are tested for the next generation transistors. The use of body scaling, high-k gate dielectric, strain, and orientation of substrate and channel can enhance their performance. These findings are published in Refs. [53, 54].

3. Nano-scale metrology: In this direction two main breakthroughs are made using the theoretical calculations. The first work enabled the extraction of interface trap density in the ultimate FinFETs using experiments and theory. The developed methods are completely new and will be extremely useful in the semiconductor industry. This work has been published in Ref. [49]. The second work enabled the calculation of phonon shifts in Si nanowires which allowed the determination of shape, size and orientation of the nanowires. This will immensely help in deciphering the observations from Raman Spectroscopy [55]. This work in under review in Journal of Applied Physics.

4. Thermoelectric Efficiency: Using atomistic modeling, the thermoelectric efficiency of n-type GaAs nanowires has been optimized using strain and orientation. The feasibility of using ultra-scaled GaAs nanowires as efficient thermoelectric materials is shown. This work is published in Ref. [56]. The use of porous Si nanowires for enhancing the thermoelectric efficiency is also proposed. The enhancement comes from the large reduction in the lattice thermal conductivity as pointed out by the simulations.

5. Nano-scale thermal management: In this direction various idea have been proposed. Careful simulation and modeling provides that strain and porosity can be used for tuning the specific heat and thermal conductivity of Si and Ge

nanowires. The phonon localization results in large reduction in the lattice thermal conductivity. These results are published in Ref. [57, 58].

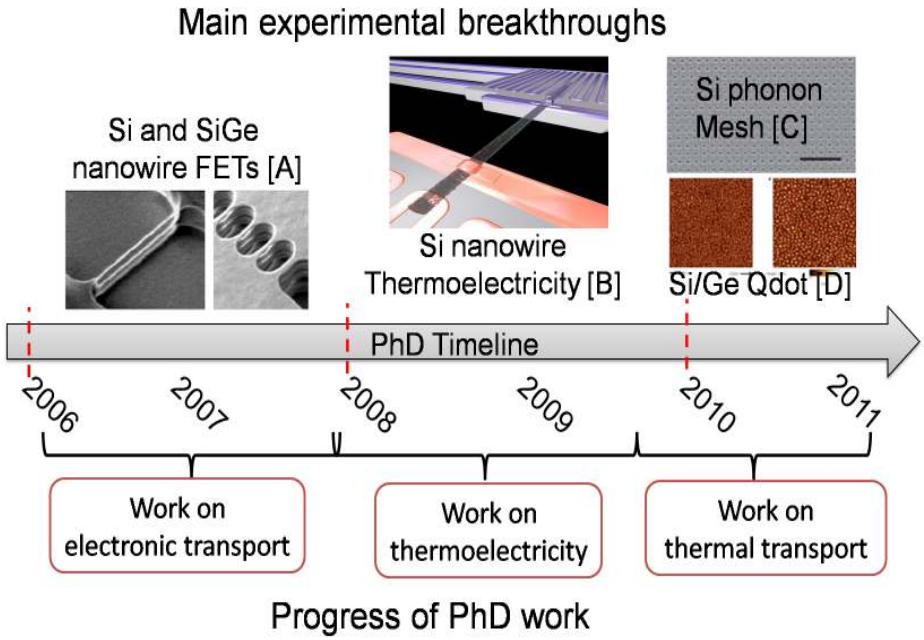

Fig. 1.5. The main experimental breakthroughs which inspired the work in this dissertation on a time-line. Image [A] is from Ref. [13], [B] is from Ref. [32], [C] is from Ref. [59], and [D] is from Ref. [60]. In 2006-2008 nanowire FETs set the trend for the next generation CMOS technology. Around 2008 Si nanowires showed the promise of better thermoelectricity. In 2010, thermal conductivity of Si were manipulated using nano-scale fabrication methods.

1.5 Thesis time-line and organization

The work on electronic structure started to address the 'MM' concept of going beyond Silicon. The breakthrough in harnessing waste heat of integrated-chips (IC) for electricity generation [32] extended the research towards exploring nano-scale thermoelectric properties along the lines of 'MTM' concept. Engineering thermoelectric properties necessitated a proper understanding of phonons and heat flow in nanos-

tructures which initiated the thermal study. The progress time-line of the PhD work is shown in Fig. 1.5.

A chapter-wise break-up of the dissertation is shown in Fig. 1.6. For each of the themes in this thesis, first theory is provided, followed by the scaling trends of the properties and then applications to realistic systems are shown. The chapters in the dissertation are organized as follows:

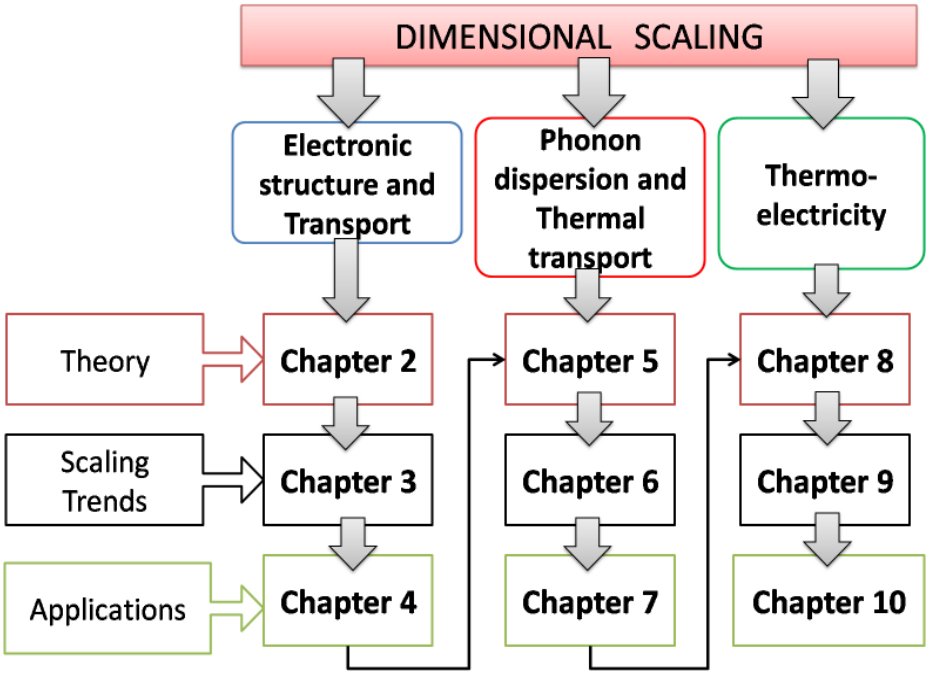

Fig. 1.6. The central themes in the dissertation and chapter-wise break-up.

- **Chapter 2:** This chapter provides a brief description of the atomistic nearest neighbor $sp^3d^5s^*$ Tight-binding (TB) theory [40]. The main focus of the chapter is on the implementation of the new bandstructure code in OMEN [45, 61], a parallel C++ code for quantum transport, called the 'OMEN-BSLAB' [46]. The short-comings of the older MATLAB codes and the important features of the new code are provided. The original OMEN code was developed by Dr. Mathieu Luisier. The OMEN-BSLAB code has been used for a variety of experimental and simulation based studies [47, 52, 53]. The simple 'Top-of-the-

barrier' (ToB) [43] model for transport in short channel MOSFETs is discussed. The comparison of ToB model with ballistic Non-Equilibrium Green's Function (NEGF) method provides the valid transistor regime where ToB model can be used with confidence. The pros and cons of using the ToB model are also discussed. The details on the 'Bandstructure Lab' tool on nanoHUB are also described in this chapter.

- **Chapter 3:** This chapter focuses on the scaling trends of electron transport properties in the ballistic regime under the influence of strain, orientation and dimensionality in non-Si material systems. Bandstructure calculation in SiGe bulk alloy using Virtual Crystal Approximation (VCA) within TB model (TB-VCA) is implemented. The bulk SiGe band-edge and effective mass results are benchmarked against experimental data. The TB-VCA model coupled with ToB model is used to study the performance of core/shell SiGe/Si nanowire FETs. A performance evaluation of p-type GaAs UTB FETs [5] is performed. The electronic bandstructure and conductance of Lead Selenide (PbSe) nanowires , an attractive material for TE and optical applications, are explored. The aim of this chapter is to explore the implications of bandstructure modification on the electronic transport in non-Si material devices.

- **Chapter 4:** With improved fabrication processes a variety of ultra-scaled Si transistors are manufactured. This chapter provides details on the application of atomistic self-consistent simulations to understand the, (i) experimental CV data of Gate-All-Around (GAA) Si nanowire FETs, (ii) performance and reliability of bulk SiGe on Si substrate p-MOSFETs, and (iii) the temperature dependent conductance measurements in ultra-scaled trigated undoped channel Si n-FinFETs. The experimental source-to-channel barrier height (E_b) and channel cross-section area (S_{AA}) are qualitatively explained by self-consistent simulations. The systematic mismatch led to the development of two novel

[5]FET=Field Effect Transistor

methods for extracting interface trap density in the ultimate FinFETs. The methods are outlined in detail in this chapter.

- **Chapter 5:** In this chapter the theory on the calculation of phonons in zinc-blende semiconductors using the Modified Valence Force Field (MVFF) model is developed. The model is used for the calculation of phonon dispersion in bulk and nanowire structures. Bulk phonon dispersions are bench-marked against experimental data. The phonon dispersion forms the basis for the calculation of lattice related physical properties such as specific heat (C_v), thermal conductivity (κ_l), sound velocity (V_{snd}), and phonon shifts useful for Raman Spectroscopy are provided in this chapter. Phonon Green's function (PGF) method for the evaluation of nano-scale heat transport is developed here. The Landauer's approach to obtain lattice thermal conductivity is also outlined.

- **Chapter 6:** The objective in this chapter is to understand the effect of nanowire size scaling, orientation and shape on the phonon shifts and thermal properties. The phonon shifts in nanowires allowed nano-scale metrology of these wires to determine their shape, size and orientation. These findings are bench-marked against experimental Raman Spectroscopy data and other theoretical calculations. The scaling of C_v and ballistic κ_l are studied in an effort to understand the ways to tune these quantities. Analytical expressions for the variation in these physical quantities with the nanowire features are proposed which may be beneficial for compact physical and thermal modeling [62].

- **Chapter 7:** This chapter proposes methods to engineer the C_v and κ_l in nanowires. These methods mainly rely on modifying the phonon dispersion of the wires by techniques such as strain, pores and alloying. The pore size, density and placement play a significant role in tuning κ_l. Uniaxial strain values $> 2\%$ provide an attractive way to modulate κ_l and C_v. Si/Ge superlattice nanowires are another alternate structures to engineer κ_l. These structures are studied using PGF method to understand the effect of orientation and atomic

disorder on the thermal boundary resistance (TBR). Furthermore, the in-plane and cross-plane heat transport in these superlattice nanowires are investigated.

- **Chapter 8:** This chapter combines the learning of Chapter 2 and 5 to understand and explore the thermoelectric properties in semiconductor nanostructures. The theory to calculate the linear transport parameters using Landauer's approach for electrons and phonons are developed in this chapter. Mode counting forms the central idea in Landauer's model. To this end an efficient algorithm is designed to obtain correct number of modes from a variety of dispersions even with sparse k-grids. Methods to include scattering mechanisms are also outlined.

- **Chapter 9:** The effect of material, size and orientation variation on the electronic contributions to the thermoelectric properties in nanowires are investigated in this chapter. The TE power-factor of GaAs and Si nanowires are compared. Si outperforms GaAs due to higher electronic density of states (DOS). The effect of strain on the TE PF is also investigated. Compressive strain improves the PF and the reason for this increase is also explained.

- **Chapter 10:** Ideas on engineering the thermoelectric PF and ZT in zinc-blende nanowires are outlined in this chapter. The use of optimal size, orientation and strain can enhance the PF and ZT in n-type GaAs nanowires even in the presence of scattering. It is further shown that porous Si nanowires provide a good way to increase the PF and ZT even in the presence of scattering. The enhancement comes from the drastic suppression of κ_l compared to the electronic PF. Discussion on the LANTEST, a tool on nanoHUB.org for exploring the thermoelectric properties in semiconductor bulk and nanostructures. tool is provided. This tool enables researchers to investigate the thermoelectric efficiency of nanostructures and new materials via nanoHUb.org.

- **Chapter 11:** The summary of the dissertation is provided in this chapter. A broad overview of the opportunities and challenges in the world of nanotechnology are given along with the possibilities for future work.

1.6 Reusability of published material

The work in this thesis is based on the papers published in different journals. Figures and contents have been reused from these publications in this work. The permission for the reuse of contents and figures from the publishers has been obtained which are present in the Appendix H.

2. THEORY OF ELECTRONIC STRUCTURE AND TRANSPORT IN SEMICONDUCTOR NANOSTRUCTURES

2.1 Introduction and Motivation

The shrinking physical dimension of nanostructures and the enhanced geometrical confinement, call for electronic structure models which are beyond effective mass approximation (EMA) [15, 63, 64] in evaluating the electron transport performance. Atomistic Tight-binding (TB) models [40, 41, 65] account for the (i) atomic positions, (ii) conduction and valence band interactions, (iii) strain, (iv) surfaces, and (v) arbitrary device orientations making them better than simple EMA models. The need for going beyond the simple EMA model for understanding the electronic properties at the nano-scale has been emphasized in multiple works [15, 63, 66, 67]. At the same time TB models can outperform first principle calculations like DFT [1], since TB models pack sufficient physics and are computationally must faster and capable of handling larger systems (>10 million atoms) which are not possible at present in the first principle models. These features make TB model highly suitable for investigating nano-scale devices.

This chapter outlines the implementation of the tools necessary for investigating nano-scale electron transport. The main components are, (i) electronic structure calculation, (ii) electronic transport calculation, and (iii) electrostatics solution using FEM based Poisson equation solver. In this chapter a brief description of the semi-empirical nearest neighbor atomistic 10 band $sp^3d^5s^*$ Tight-binding model (TB) for evaluating the bandstructure is nanostructures is provided in Sec. 2.2. The implementation of the electronic structure and the simple 'virtual source' [43] or Top-of-

[1] DFT = Density Functional Theory

the-Barrier (ToB) transport model as an extension in the parallel quantum transport simulator called 'OMEN' [45,61] is also provided in Sec. 2.3. A comparison of the ToB model with ballistic Non-equilibrium Green's Function (NEGF) quantum transport model is also provided to obtain the valid range of transistor dimensions where ToB can be used confidently (Sec. 2.4). A discussion on the implementation of the 'Band-structure Lab' tool [46] is provided in Sec. 2.5. Summary and outlook are provided in Sec. 2.6.

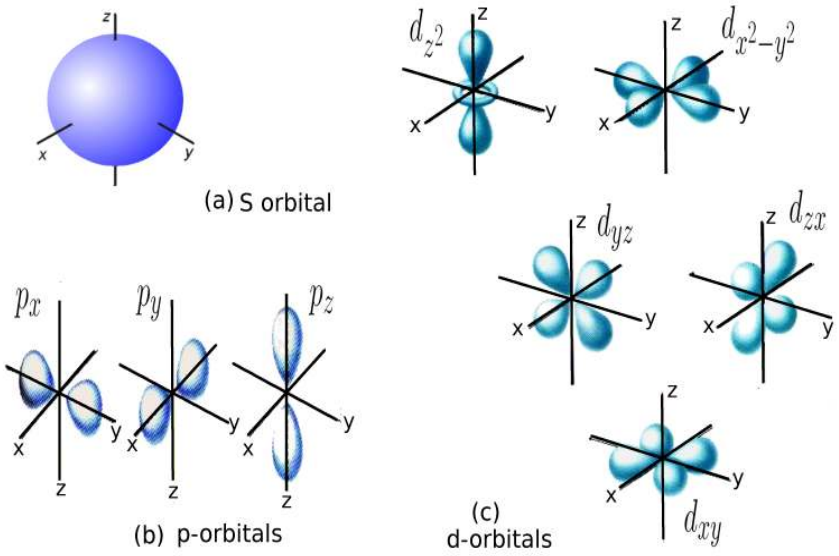

Fig. 2.1. The atomic orbitals used as the basis in the atomistic $sp^3d^5s^*$ TB model. (a) s-orbital which is non-directional and isotropic, (b) 3 p orbitals, and (c) 5 d orbitals. The p and d orbitals are directional.

2.2 Semi-empirical Tight-binding model

The nearest neighbor (NN) 10 band $sp^3d^5s^*$ TB model is composed of orthogonal orbitals [40,41] localized on atoms which form the basis set of the electronic structure calculation. The 10 orbitals, as shown in Fig. 2.1, are, (i)1 s, (ii) 2 p orbitals (p_x, p_y, p_z), (iii) 5 d orbitals (d_{xy}, d_{yz}, d_{zx}, $d_{x^2-y^2}$, d_{z^2}, and (iv) 1 fictitious orbital called s^* which accounts for all the other outer orbital interactions. The orbitals on one atoms

interact with the orbitals on the NN atoms. The resulting wave-functions are called the 'two-centered integrals' [41] as shown in Fig. 2.2.

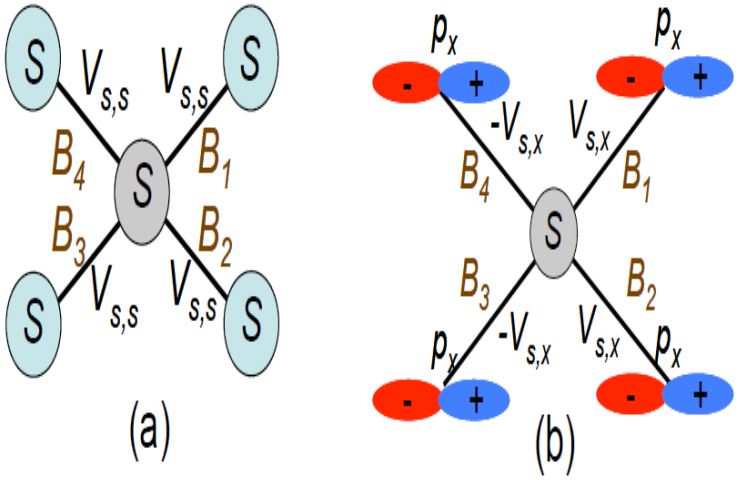

Fig. 2.2. The two-centered overlap integrals shown by the symmetry and parity of the orbitals when they interact. (a) The coupling between s,s orbitals is the same for all four bonds in zinc-blende. (b) The coupling between s, p_x orbitals is different for each bond. This is adapted from the PhD thesis of Dr. Neophytos Neophytou [15].

Within semi-empirical TB approach these two-centered integrals are used as fitting parameters [40]. The value of these parametrization are calculated using a genetic algorithm approach as pointed out in Ref. [40, 68]. The parameters extracted can reproduce the band edges, energy levels and effective masses at high-symmetry point in the complete first Brillouin Zone (BZ) for a given bulk semiconductor. An elaborate methodology of Tight-binding implementation in bulk and nanostructures is provided in the following Refs. [15, 40, 63–65].

2.3 Details of the computational tool: 'OMEN BSLAB'

Even though there are some older codes which solve the electronic structure using semi-empirical TB model like older MATLAB version of Bandstructure Lab and NEMO-3D [40], there are short-comings in these codes. The main drawbacks are,

1. *Serious limitation on the device size*: MATLAB [69] has serious memory constraints during execution. This puts a severe limitation on the size of devices that could be solved using the MATLAB codes. The largest possible Silicon nanowire that could be handled by the MATLAB based Bandstructure Lab code was roughly 12nm $\times$ 12nm. This limitation was mainly due to the large memory needed to store the TB Hamiltonian.

2. *Longer execution and turn-around time*: Another serious shortcoming is the very long execution time to solve the bandstructure for nanostructures. Since MATLAB is an interpreted language [69], it is inherently slow in executing the codes. This could be easily eliminated by using a lower level programming language. C/C++ is a good choice due to the fast acceptance of C/C++ in the scientific community and availability of many scientific libraries in C/C++.

3. *Limited MATLAB access on many super-computing clusters*: Most of the super-computing clusters do not allows MATLAB programs to run due to licensing issues. This limits the portability of large-scale MATLAB codes. However, C++ executables are highly portable and all supercomputing clusters support C++ programs. This is another reason to develop a C++ based code.

4. *Absence of a transport code*: NEMO-3D is good for solving electronic structure of large multi-million atomic systems [70]. However, it had a serious short coming in terms of the scalability of the code and solving transport in semiconductor systems [2]. This limitation was overcome in the new OMEN-BSLAB

[2]This limitation on NEMO-3D was solved by the new code called' OMEN3D-par' [71] which could do both electronic structure and transport calculations in multi-million atomic domains. This code

code where larger atomic domains (Silicon nanowire as large as 28nm × 28nm have been solved) could be solved both for electronic structure and transport.

2.3.1 Key Features of 'OMEN BSLAB'

The shortcomings presented in Sec.2.3 resulted in the development of 'OMEN-BSLAB' work. The target was to develop a faster code to enable electronic structure and transport simulation of larger structures in shorter time. This code also replaced the older MATLAB driven version of Bandstructure Lab on nanoHUB. This tool has been developed as an extension to another highly parallel and scalable quantum transport simulator called OMEN [45, 61, 63] developed by Dr. Mathieu Luisier at ETH, Zurich, Switzerland between 2005-2007. Some of the salient features of the OMEN-BSLAB code are:

1. *Highly parallel and scalable code:* OMEN-BSLAB successfully scaled up to 256 processors. OMEN itself has scaled up to 222720 cores[3]. This code has four levels of parallelization as shown in Fig. 2.3 which makes it fast and scalable. The parallelization utilized the classes implemented for parallel execution of commands using MPI (Message Passing Interface) in OMEN.

2. *Ability to handle larger device structures:* This code easily handles structures as large as 28nm × 28nm [100] Silicon nanowires for electronic structure calculations with 21425 atoms. For self-consistent calculations this code handles structures as large as $176nm^2$ with 4505 atoms and 36595 Poisson mesh points with ∼20000 triangular elements (more details on this in Sec.4.2 in Chapter 4).

3. *Modular code for easy extension:* This code has been developed based on object oriented paradigm (OOP). In fact one of the key features is the code re-usability

has better scalability compared to NEMO-3D. This code has been jointly developed by Sunhee Lee and Dr. Hoon Ryu of Purdue University. In fact this code was used for benchmarking experimental results as outlined in Refs. [16, 49].

[3]More details about the scaling of OMEN are present here https://engineering.purdue.edu/gekcogrp/software-projects/omen/scale_32768.php

in this software from OMEN via inheritance of the C++ classes (a kind of encapsulation) and polymorphism of functions (like virtual classes). For OO details see the contents at *www.cplusplus.com/doc/tutorial*. This allowed the code to be extended easily for thermoelectric and phonon calculations.

4. *Faster execution and turn-around time:* A big advantage of using C++ and multiple levels of parallelization [4] of the software was the faster calculation of results compared to the older MATLAB code.

5. *Highly portable:* This code is highly portable and has been successfully executed on many clusters such as Purdue clusters of Steele, Coates, Nanohub (see details here *http://www.rcac.purdue.edu/userinfo/resources/*) and Teragrid. Also this code has been compiled with different flavors of C++ compilers like g++, Intel and PGI.

6. *Powers tools on nanoHUB.org:* This code presently powers the Bandstructure Lab V2.0 tool [46] on nanoHUB.org. More details on this are provided in Section 2.5.

7. *Can handle many geometry and gate configurations:* This code has a flexible geometry handler (which uses qhull [5]) that allows it to treat many different geometries for electronic structure calculations and Poisson solution as shown in Fig. 2.4. Core-shell type of structures can be easily handled by this code as presented in Sec. 3.2 in Chapter 3 . Furthermore, different gate configurations such as GAA, tri-gate, and double gate can be easily handled for electrostatic calculations using FEM based Poisson solver [52, 72]. In fact geometry of the entire device can be sub-divided and fed to the code using its versatile input deck. This was done for the self-consistent simulation of silicon nanowire FET provided by IME Singapore [47] (discussed in Sec.4.2 in Chapter 4).

[4]Parallelization is achieved in OMEN-BSLAB using MPI (message passing interface). For more details see this link http://www.mcs.anl.gov/research/projects/mpich2/

[5]Details on qhull present here http://www.qhull.org/

8. *Better storage of Hamiltonian*: In the nearest neighbor TB approach the Hamiltonian generated is very sparse. To store such a sparse Hamiltonian many compressed formats like compressed row/column formats [73] can be used. This has been successfully implemented in the code.

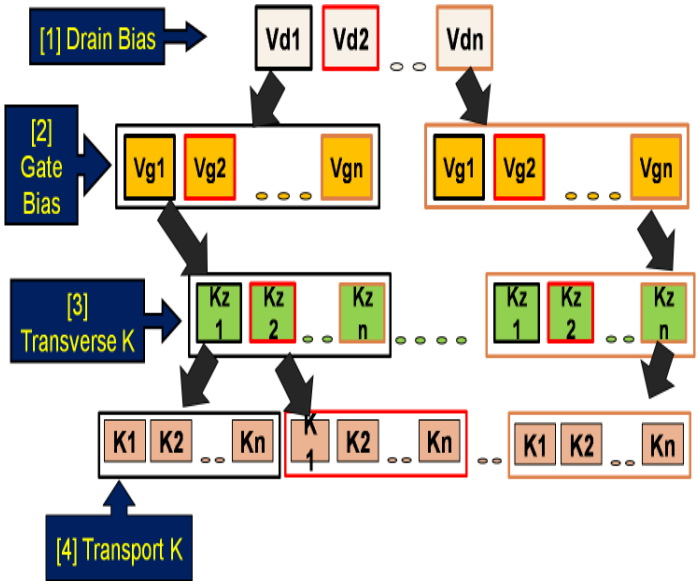

Fig. 2.3. Parallelization scheme for OMEN-BSLAB. First the drain bias (V_D) is divided into MPI groups. The each V_D group is provided all the gate biases V_G. The electronic structure calculation at each V_G is further broken down into two sub-groups, (i) first the transverse momenta (kz) (present only in 2D ultra-thin-body case), and (ii) each kz is given the transport momenta (k) which are further distributed on many CPUs.

2.3.2 Main themes in OMEN-BSLAB

The core of the code consists of solving the Schrodinger equation using atomistic TB method. The filling of electronic eigen states is done using Fermi-Dirac distribution. The electrostatic solution is provided by the Poisson solver [66,67]. The detailed description is provided as follows:

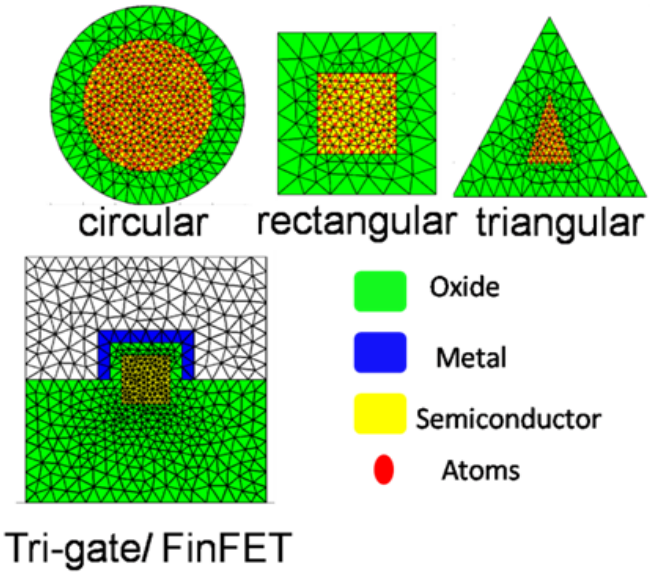

Fig. 2.4. Some of the many possible geometries that can be handled by OMEN-BSLAB. The finite element mesh is created using *qhull*[5]. These elements are composed of triangles and tetrahedrons in 2D and 3D, respectively. Regions with different material properties can be defined.

1. *Electronic Structure*: Electronic structure calculation is based on the atomistic 10 band $sp^3d^5s^*$ orthogonal Tight-binding (TB) model with spin orbit coupling (SO). The details of the method are in the following papers [40, 41, 66, 74–77] and the references therein. In broad this method is based on the wave-functions (s,p,d type) localized on each atom which linearly combine to generate the wave function for the entire system. Details on the construction and solution of the TB Hamiltonian are provided in detail in Refs. [15, 63, 64].

2. *Transport*: For ballistic [66, 67] and back-scattering dominated [78] FETs, 'Virtual Source' or ToB model [43, 66, 67, 79] provides an adequate description. The electronic eigen states are filled at the virtual source (Fig. 2.5) to obtain the total charge in the transistor at a given V_G and V_D. In ballistic (and back-scattering dominated) FETs it is assumed that the most important physical

phenomena occur at the virtual source (Fig. 2.5). More elaborate description is available in Ref. [15]..

3. *Electrostatics*: For solving the potential distribution in the atomistic channel as well as in the surrounding continuum dielectric, finite element based 2D/1D Poisson solvers have been implemented in the code. This has been successfully applied to obtain self-consistent charge and potential solutions in a variety of devices [52, 53].

The self-consistent method for obtaining charge and potential in the gated FETs is shown in Fig. 2.5. Once the self-consistency is achieved the ballistic (or back-scattering dominated) terminal characteristics like electron current (I), conductance (G), and injection velocity (V_{inj}) can be calculated using the Landauer's approach [51] as discussed in Refs. [15, 66, 67, 79].

2.4 The 'ToB' model

The 2D top of the barrier atomistic quantum transport model [53, 66, 67, 80] has been used for speedy simulation and analysis of Silicon Nanowire (SiNW) FET device characteristics. However, to use the ToB model reliably, it is essential to understand the device regime where this model is valid. This section provides an elaborate discussion on the ToB model in terms of (i) valid transport regime, and (ii) computational advantage. The comparison is done against full 3D ballistic NEGF simulations obtained using OMEN.

2.4.1 Approach and device details

Simulation Procedure: First full 3D atomistic ballistic simulations are performed using OMEN for rectangular GAA n-type SiNW FETs with a given cross-section width (W) and height (H), keeping W/H = 1 for different channel lengths (Lc). The channel orientation of [100] and [110] are used for the FETs. 3D $I_D - V_G$ simulations

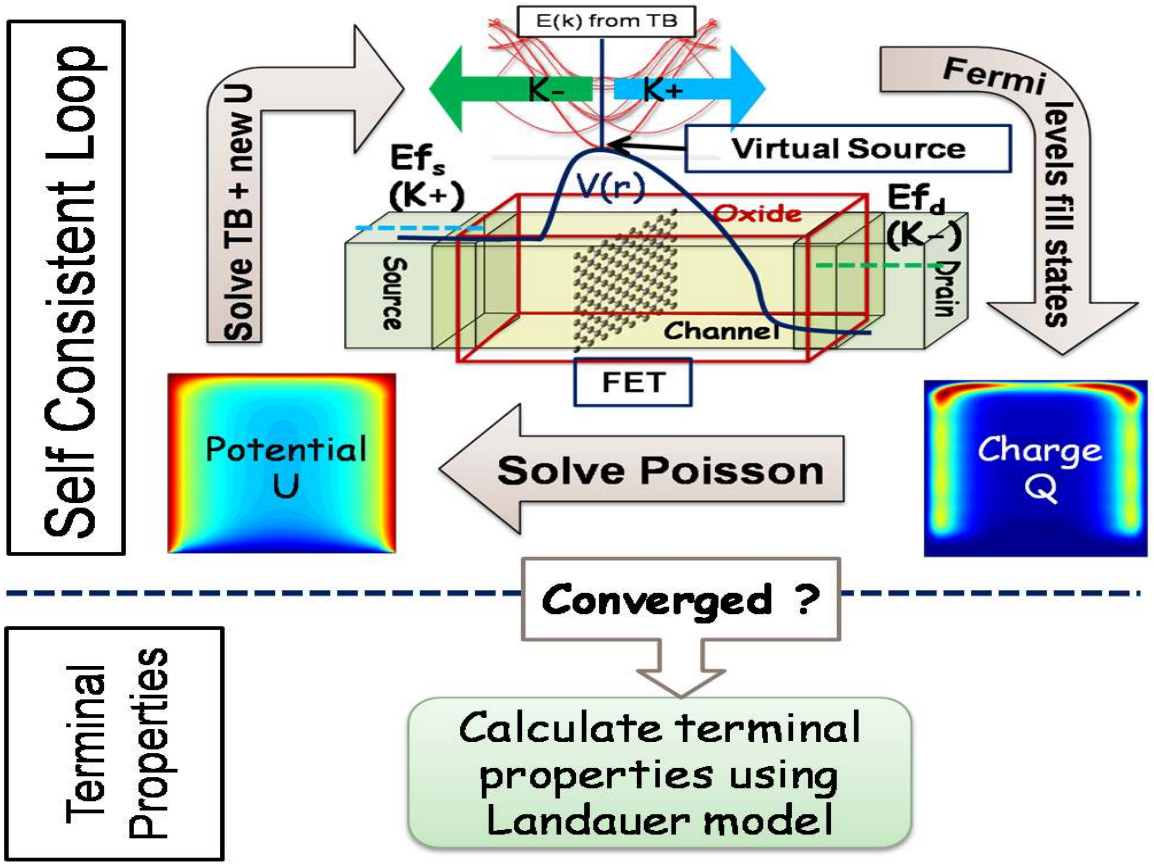

Fig. 2.5. The self-consistent loop for the calculation of charge and potential in ballistic FETs. The electronic eigen states are calculated at the 'virtual source' which are then filled by the source (E_{fs}) and drain (E_{fd}) Fermi levels. This charge is then passed to a FEM based 2D/1D Poisson equation solver which provides the potential distribution in the device. After the charge and potential are obtained self-consistently the ballistic terminal characteristics are calculated using the Landauer's method [51].

are done for low and high drain biases (V_{DS}). From these $I_D - V_G$ curves DIBL [6] is extracted. Using this DIBL value 2D $I_D - V_G$ are simulated for the exact same devices, using the ToB model to account for different "channel lengths".

[6]DIBL = Drain Induced Barrier Lowering

Simulation environment and devices: Square SiNW FETs with cross-section size of 3.1 nm (W) × 3.1 nm (H) and oxide thickness (T_{ox}) of 2nm are simulated using the 3D model at two drain biases: V_{DS} = 0.05V (low) and 0.6V (high). Channel lengths of 4, 7, 10, and 15 nm have been simulated with [100] and [110] channel orientations.The source/drain extension is 10nm with $10^{20} cm^{-3}$ n-type doping. The same exact devices are then simulated using the 2D ToB model in OMEN-BSLAB.

2.4.2 Terminal characteristics

The Lc dependent $I_D - V_G$ curves obtained from OMEN and ToB models are shown in Fig. 2.6. An important observation is that the 2D model completely underestimates the sub-threshold current for the smaller Lc FETs. For the Lc = 10nm device the sub-threshold current from 3D and 2D models are close. This sheds light on a very important phenomenon which is missing in the ToB model. This phenomenon is the 'Source to Drain' (S/D) tunneling [81]. Since ToB is a thermionic model it cannot capture the carriers going below the potential barrier and hence it underestimates the drain current (I_D).

2.4.3 Two conditions for ToB to match 3D $I_D - V_G$

There are two important conditions that must be met so that ToB can successfully replicate the results of 3D simulation. These two conditions are:

1. *Reduced S/D tunneling current*: Figure 2.6 shows that $I_D - V_G$ from ToB is in good agreement with the 3D OMEN result at low V_{DS}, without any DIBL compensation, for Lc = 10nm. The deviation at shorter Lc is attributed to S/D tunneling current [81, 82] under ballistic condition, which is not included in the ToB model. Table 2.4.3 shows that the sub-threshold swing (SS) becomes considerably larger than 60mV/dec (ideal ToB result) with decreasing Lc for both [100] and [110] SiNW FETs, reflecting strong S/D tunneling current in the OFF-state. Also [100] wires show larger SS and tunneling rate (Fig. 2.7)

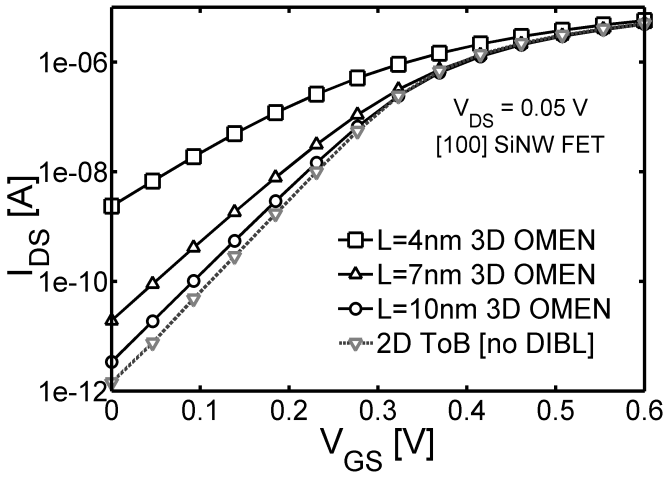

Fig. 2.6. $I_D - V_G$ plot obtained for a 3.1 nm × 3.1 nm, [100] square SiNW with GAA oxide using 3D OMEN [45] for different Lc and ToB (without DIBL adjustment). At Lc=10nm, results from the two methods are in close agreement.

compared to [110] wires [82], hence making them less scalable. *Thus, increased S/D tunneling current causes 2D ToB to deviate from 3D $I_D - V_G$ results for shorter Lc devices.*

2. *Source to channel barrier (ϕ_{sc})*: Figure 2.8 and insets of Fig. 2.9 and Fig. 2.10 show that ϕ_{sc} reduces as V_{GS} increases. This decrease is stronger for smaller Lc devices (Fig. 2.8). ToB result shows a strong deviation from 3D $I_D - V_G$ results since ϕ_{sc} becomes much smaller than the k_BT/q limit which causes an excessive S/D tunneling current to flow. *Thus, existence of proper source to channel barrier is important for ToB to match 3D results.*

2.4.4 Comparison of the two models for different Lc FETs

To obtain the device regime where ToB provides reliable results, it is important to understand the effect of gate and drain electrostatics on the source to channel barrier. In this part we analyze the two models for different Lc FETs and point out

Table 2.1
Short-channel characteristics (SCE) for [100] and [110] SiNW FETs obtained from OMEN [45] and the valid simulation regime for ToB.

Lc (nm)	SS (mV/dec)		DIBL (mV/V)		ToB Valid ?	
	[100]	[110]	[100]	[110]	[100]	[110]
4	106.4	158.2	175.4	201.2	No	No
7	69.71	80.1	70.92	80.27	No	No
10	62.80	63.6	11.58	13.69	Partly	Partly
15	60.19	60.89	4.17	4.04	Yes	Yes

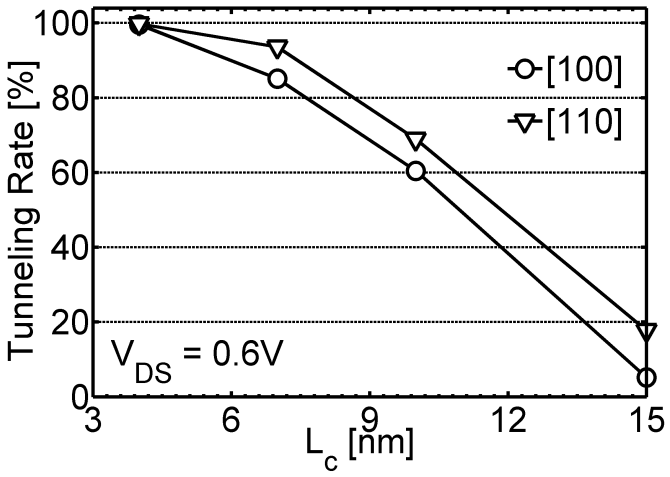

Fig. 2.7. Tunneling current rate percentage in the OFF-state for [100] and [110] SiNW FETs for different Lc. Tunneling current decreases in the OFF state, as Lc increases for both [100] and [110]. [110] wires have larger tunneling component hence worse SCEs.

the reasons why the two models agree or disagree with each other. These FETs can be broadly classified into two groups namely, (i) long Lc FETs and (ii) short Lc FETs. Each of these device regimes are discussed.

1. *Longer Lc devices:* Figure 2.9 shows that ToB provides good agreement to 3D results for Lc = 15nm (long channel) in the OFF-state since the S/D barrier is well defined at low V_{GS} and high V_{DS}. The S/D tunneling current is minimal

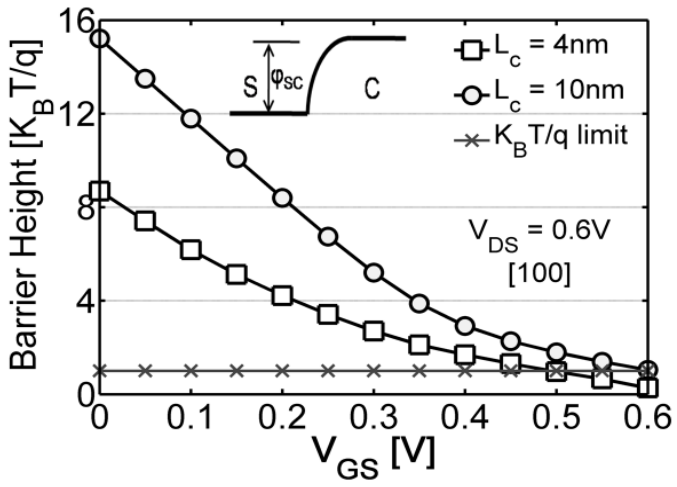

Fig. 2.8. Reduction in source to channel barrier height for different channel length in ⟨100⟩ SiNW FETs. Shorter channel device shows more reduction in the barrier height.

due to a longer Lc. However, in the ON-state ToB current is smaller compared to 3D under high V_{GS} and V_{DS}. As V_{GS} increases, the S/D barrier decreases. As a result carriers injected at the source side are no more reflected by the barrier. To ensure charge neutrality in the source, the electrostatic potential on the source side (ϕ_{sc}) decreases allowing more carrier injection which causes an artificial increase in the ON-current in the 3D ballistic model. This is an artifact of the ballistic approximation that is not captured in ToB model and explains why the full 3D OMEN ON-current is larger at high V_{GS} (Fig. 2.9 and 2.10).

2. *Shorter Lc devices:* As Lc decreases the drain bias starts to reduce the S/D barrier width (DIBT[7] [81], Fig. 2.10 inset) causing excessive S/D tunneling current to flow. For Lc = 4nm (short channel), ToB results are not in good agreement with full 3D OMEN anywhere (Fig. 2.10) since the S/D barrier is not well defined and is below the thermal k_BT/q limit (Fig. 2.8). Absence of a

[7]DIBT = Drain Induced Barrier Thinning

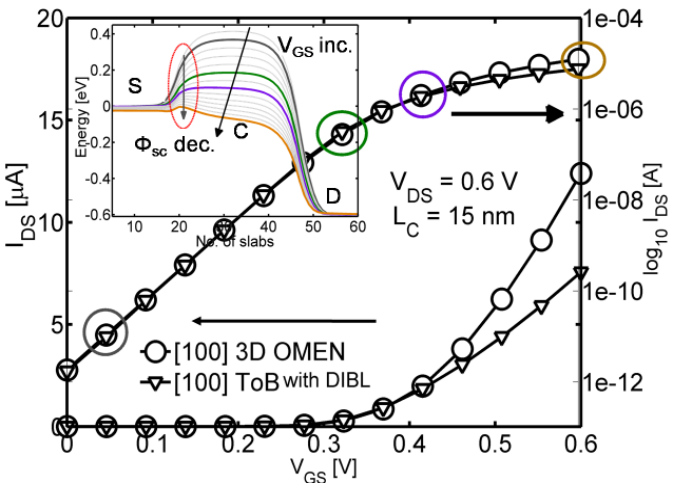

Fig. 2.9. Long Lc $I_D - V_G$ characteristics for ToB (with DIBL) vs. 3D OMEN for [100] SiNW, Lc = 15nm, at $V_{DS} = 0.6$V. Inset shows the variation in the S/D barrier at 4 different V_{GS} computed using 3D OMEN. I_{OFF} shows very good agreement; however, I_{ON} is higher for 3D.

clear S/D barrier makes ToB inapplicable to short Lc devices. As a quantitative estimate for tunneling current rate (R_{TUN}) (in the OFF-state) Eq. (2.1) is used:

$$R_{TUN} = 100 \times \frac{J_{3D} - J_{TOB}}{J_{3D}} \tag{2.1}$$

where, J_{3D}, J_{TOB} are currents from 3D and ToB simulations, respectively. Figure 2.7 shows that at I_{OFF}, tunneling rate (R_{TUN}) increases dramatically with decreasing Lc , with [110] devices showing worse SCEs compared to [100] devices [82].

2.4.5 Computational Speedup of ToB

One advantage of using the ToB lies in the reduced compute time compared to the full 3D OMEN atomistic quantum transport simulations. For square (W/H = 1) SiNW FETs, with longer Lc (Lc $\leq$ 5×W) devices 1 self-consistent Schrodinger-Poisson iteration time for 3D simulation goes as W^{n3D}, with $n3D = 5.63$, whereas

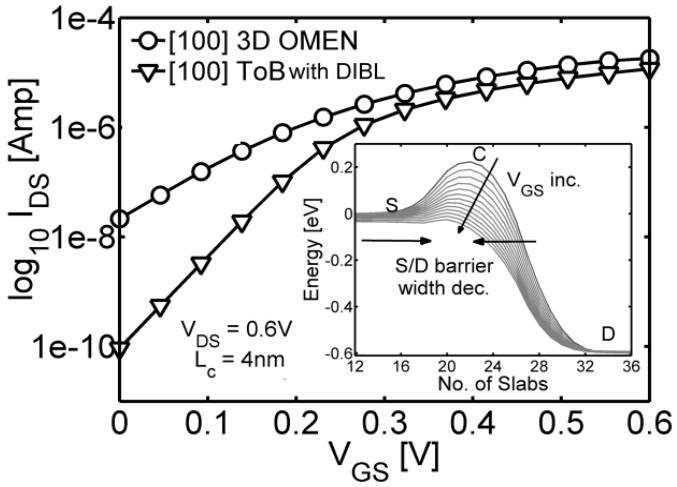

Fig. 2.10. Short Lc comparison of $I_D - V_G$ from ToB (with DIBL) with 3D OMEN, for $\langle 100 \rangle$ SiNW FET, Lc = 4nm. Inset shows the S/D barrier for the device which decreases in width and height as V_{GS} increases.

for 2D ToB it goes as W^{n2D} ,with $n2D = 2.82$, on a single CPU (Intel dual core processor) as shown in Fig. 2.11. The simulated devices have 1nm GAA oxide. For the performance comparison of the two models 'Speedup' term is defined as,

$$Speedup = C_{rat} W^{(n3D-n2D)} \tag{2.2}$$

$$\lambda = C_{3D}/C_{2D} \tag{2.3}$$

where, C_{rat} is the ratio of time intercepts for 3D (C_{3D}) and 2D (C_{2D}) simulation time (Fig. 2.11). Value of C_{rat} in Fig. 2.11 is ~ 51.

Table 2.4.5 shows the actual compute times for both the models and the speedup obtained as a function of W for SiNW FETs. Speedup of 2D ToB simulations increases rapidly as W increases making it a very attractive model for device simulation. Also the memory storage needed for ToB device simulation is much smaller compared to 3D simulation.

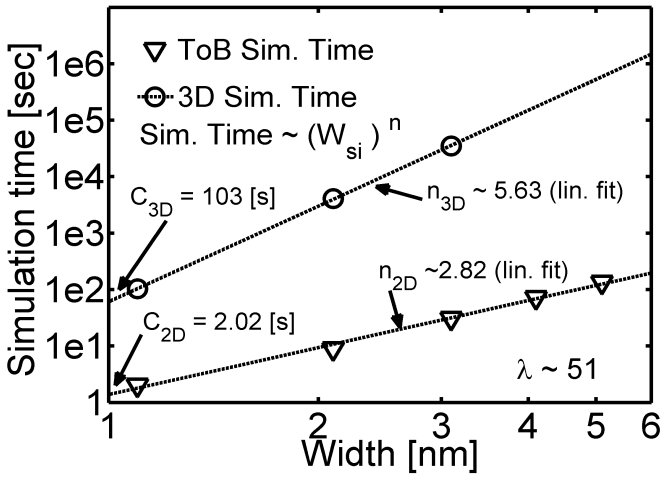

Fig. 2.11. Simulation time for 1 self-consistent iteration for 3D OMEN vs. 2D ToB for a square SiNW with 1nm GAA oxide on 1CPU. ToB simulates $\sim (W_{Si})^2\times$ faster compared to 3D OMEN, where W_{Si} is the silicon body thickness.

Table 2.2
Comparison of actual simulation time (for 1 self-consistent iteration) for full 3D and 2D model with Speed-up achieved from 2D ToB model for different cross-section width (W) Silicon nanowire FETs with 1nm Gate all around oxide.

Width (W)[nm]	Time (secs) [1CPU]		Speedup
	3D	2D	($\lambda \sim 51$)
1.1	103	2.02	66.6
2.1	4080	8.92	410.13
3.1	35200	30.63	1225.2
4.1	205000	71.52	2688

2.4.6 Summary of the work

The presence of a proper Source/Drain barrier in the device is an important criterion for the applicability of ToB model. Long channel devices can be accurately

modeled under low and high drain bias after DIBL adjustment. Two factors are important in defining the valid device regime for ToB,

1. The presence of proper source to channel barrier ($\phi_{sc} \geq k_B T/q$)

2. A small source to drain tunneling current.

Due to these reasons ToB compares well with 3D model for longer Lc devices. *For a ratio of Lc/W $\geq$ 5, the ToB model can be used to obtain accurate 3D results.* ToB is a suitable model for SiNW FETs where channel electrostatics is controlled mostly by the gate. In this regime, DIBL from experiments can be fed to ToB, to obtain accurate terminal characteristics. Computational speedup as well as smaller memory storage requirements make ToB a very attractive model for typical device simulation. The ToB model also provides significant insight into the importance of atomistic bandstructure effects in nanowires [66, 67].

2.5 Tool development - Bandstructure Lab

One of the main impact of the development of the OMEN-BSLAB tool was faster and much more capable Bandstructure Lab [46] deployed on nanoHUB.org (fig.2.12). Bandstructure Lab uses the sp^3d^5s* Tight binding method [40, 65] to compute E(k) for bulk, planar UTBs, and nanowire semiconductors. This tool computes and visualizes the bandstructure of bulk semiconductors, thin films, and nanowires for various materials, growth orientations, and strain conditions. Physical parameters such as the bandgap and effective mass can also be obtained from the computed E(k). The bandedges and effective masses of the bulk materials and the nanostructures structures can be analyzed as a function of various strain conditions. Some of the main improvements after the new C++ engine replaced the older MATLAB code are as follows:

1. *Parallelization of the tool*: The back end code is parallel which makes the tool faster.

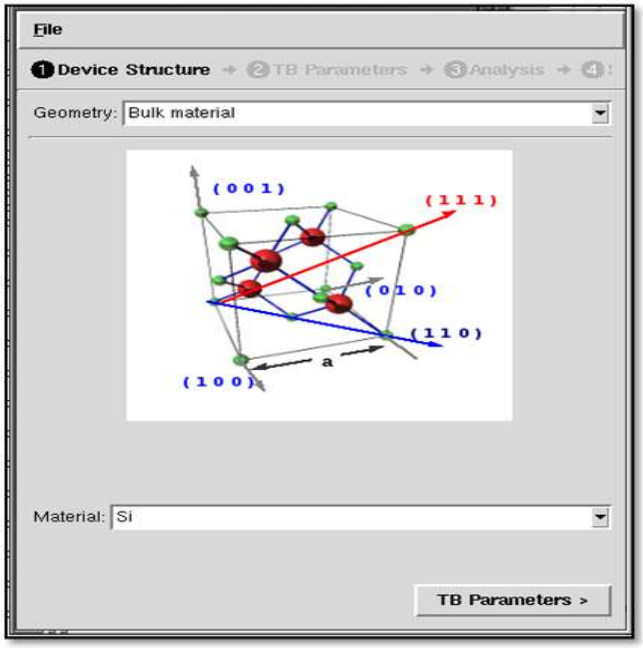

Fig. 2.12. Rappture [9] based Graphical User Interface (GUI) of Band-structure Lab V2.0 [46] on nanoHUB.org.

2. *Multi threading for faster job submission*: Now a lot of jobs can be submitted in a short span of time. This has been enabled due to the multi-threaded job submission procedure. The older serial job submission method has been replaced.

3. *Multi cluster job submission*: Now the tool can run on many clusters such as nanoHUB, Steele, Coates, and Teragrid.

4. *High Impact*: This tool is one of the most used tools on nanoHUB with a users all over the globe (fig.2.13).

A detailed usage statistics of the tool is provided in the Table 2.5

Fig. 2.13. Global locations of the user of Bandstructure Lab. Source:http://nanohub.org/resources/bandstrlab/usage

Table 2.3
Detailed usage statistics of Bandstructure Lab

Item	Average	Total
Simulation Users	-	3238
Interactive Sessions	-	12035
Simulation Sessions	-	34881
Simulation Runs	-	45871
Wall Time	1.65 hours	2394 days
CPU Time	15.43 minutes	373.67 days
Interaction Time	46.92 minutes	1136 days

Source: http://nanohub.org/resources/bandstrlab/usage

2.6 Summary and Outlook

This chapter sets the background for electronic calculations and self-consistent simulations of charge and potential in nano-scale FETs. Details of the OMEN-BSLAB

tool are provided since most of the FET work in the present thesis are done using this code. This code also powers Bandstructure Lab V2.0 on nanoHUB. The details of the ToB model are provided along with the pros and cons of the model. It is essential to know the limitations and the strength of the model to correctly identify the realms where the simulations make sense and where they may fail. The inclusion of scattering and S/D tunneling in the ToB model based on experimental observations can make it a very powerful tool in analyzing the future generations of ultra-scaled transistors. Some noticeable work in this direction are outlined in Refs. [78, 83].

3. ELECTRON TRANSPORT IN NON-Si NANOSTRUCTURES

3.1 Introduction and Motivation

This chapter applies the electronic transport theory implemented in OMEN-BSLAB [46] as discussed in Chapter 2 to study the impact of scaling on the electronic parameters of non-Si materials. This chapter brings out the vast capabilities of TB theory [40] and ToB model [72] in estimating the transistor performance even for non-Si materials such as SiGe and GaAs. The effect of strain, channel and substrate orientation, etc., are analyzed in an effort to obtain the combinations that can out-perform Si to meet the future ITRS targets [9]. Electronic structure and conductance of PbSe nanowires are investigated using TB model and Landauer's approach for future TE applications.

The present chapter is organized as follows. Section 3.2 outlines the application of virtual crystal approximation (VCA) in the TB model (TB-VCA) for calculating SiGe bandstructures. The TB-VCA model coupled with ToB model is used for predicting the performance of SiGe/Si core/shell nanowire MOSFETs which is outlined in Sec. 3.3. The performance analysis of p-type GaAs UTB FETs under strain and orientation is provided in Sec. 3.4. The calculation of electronic structure of bulk PbSe is given in Sec. 3.5. The calculations of electronic band-structure and ballistic conductance in PbSe nanowires to understand the size and orientation effects are provided in Sec. 3.6. Summary and outlook is provided in Sec. 3.7.

3.2 Electronic structure of SiGe alloys

This section outlines the procedure to calculate the electronic structure of SiGe alloy using the VCA method within TB theory (called as TB-VCA). The simulated results are further benchmarked against the experimental data to establish the correctness of the method.

3.2.1 Approach for Electronic-structure calculation

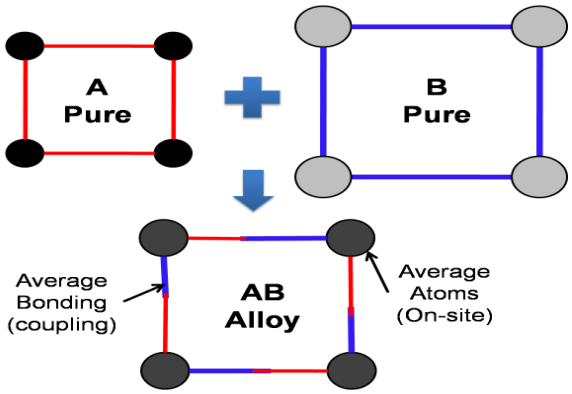

Fig. 3.1. Cartoon showing the basic concept of virtual crystal approximation (VCA) applied to an alloy AB. In TB-VCA model the onsite and the bonding elements are averaged in a non-linear fashion.

A general atomistic TB electronic structure calculation method to solve a SiGe systems is provided. The bandstructure of SiGe is based on a virtual crystal representation of the binary alloy (A_xB_{1-x}) as shown in Fig. 3.1. Its TB coefficients are calculated as the weighted mean of the coefficients of the individual materials A and B,

$$E_\sigma^{AB} = x \cdot E_\sigma^A + (1-x) \cdot E_\sigma^B \tag{3.1}$$

$$V_{\sigma_1\sigma_2}^{AB} = x \cdot V_{\sigma_1\sigma_2}^A + (1-x) \cdot V_{\sigma_1\sigma_2}^B \tag{3.2}$$

where E_σ and $V_{\sigma_1\sigma_2}$ are the onsite energies for an orbital σ and the nearest-neighbor coupling elements between two orbitals $\sigma_{1,2}$, respectively. Si and Ge atoms are replaced by fictitious SiGe atoms as shown in Fig. 3.1 whose TB parameters are linearly interpolated between those of Si and Ge taken from Ref. [77].

Si and Ge have a lattice mismatch of 4.2%, which gives rise to a large strain field in SiGe systems. This effect is taken into account by first adjusting the coupling matrix elements $V^A_{\sigma_1\sigma_2}$ and $V^B_{\sigma_1\sigma_2}$ in Eq. (3.2) according to Harrison's scaling rule [77] and then by linearly interpolating them

$$V^{AB,strain}_{\sigma_1\sigma_2} = \\ x \cdot V^A_{\sigma_1\sigma_2}(\frac{d_A}{d_{AB}})^{\eta_A} + (1-x) \cdot V^B_{\sigma_1\sigma_2}(\frac{d_B}{d_{AB}})^{\eta_B} \tag{3.3}$$

In Eq. (3.3) the η's are taken from Ref. [77] and the average bond length d_{AB} is calculated using Vegard's law [84],

$$d_{AB} = x \cdot d_A + (1-x) \cdot d_B, \tag{3.4}$$

where d_A and d_B are the individual bond lengths for material A and B, respectively. The internal strain at the SiGe/Si (AB/A) interface is accounted by averaging the bond length at the interface (d_{int}) over two atomic mono-layers,

$$d_{int} = (d_{AB} + d_A)/2 \tag{3.5}$$

The scaling of the nearest-neighbor coupling elements $V_{\sigma_1\sigma_2}$ leads to an energy shift (Δ_σ) of the diagonal elements E_σ ($E_\sigma \rightarrow E_\sigma + \Delta_\sigma$) [76]. This is accounted for in Eq. (3.1) as,

$$E^{AB,strain}_\sigma = x \cdot (E^A_\sigma + \Delta^A_\sigma) + (1-x) \cdot (E^B_\sigma + \Delta^B_\sigma) \tag{3.6}$$

A previous study [85] derived an approximate, atomic disorder dominated band-structure of SiGe nanowires and showed that the standard VCA, which simply averages the Si and Ge TB parameters, cannot reproduce the bandgaps of the disordered

system. The improved VCA model presented here includes the nonlinear effects of bond deformation in Si and Ge as a function of bond length separately before the material is homogenized. Comparison of the new model against experimental material data shows that the new model can now reproduce critical design elements such as bandgaps and effective masses. It does, however, not include the atomistic disorder that could be captured with a full 3D representation. A recent study showing the atomistic analysis of SiGe alloys is presented in Ref. [86].

3.2.2 Benchmarking Against Bulk Bandstructure

The $E(k)$ dispersion along the principle Brillouin Zone axes ($L \rightarrow \Gamma \rightarrow X \rightarrow U/K \rightarrow \Gamma$) is calculated for relaxed and biaxially strained bulk SiGe structures with different Ge concentrations. Figure 3.2a shows the relaxed conduction (CB) and valence (VB) bandedges. The TB-VCA model agrees well with the available experimental data [87,88] for all the Ge compositions. The crossover of the conduction band (CB) edge from the X-valley to the L-valley at around 85% Ge is correctly captured in the relaxed system (Fig. 3.2 a).

Biaxially strained SiGe structures are obtained by growing SiGe on a thick silicon layer [93]. Pure Ge grown pseudomorphically on a (100) Si substrate produces a compressive strain of 4.2% due to lattice mismatch. Figure 3.2b shows the bandedge variation as a function of Ge% for compressively strained SiGe on (100) Si. The bandgap variation for relaxed and biaxially strained bulk SiGe is shown in Fig. 3.2c. The strained CB varies only weakly with varying Ge% resulting in a larger bandgap reduction compared to the relaxed system. The valence band (VB) shift is similar in the both systems.

Biaxial compressive stress only weakly affects the electron transverse and longitudinal masses at the X and the L valley compared to the relaxed case as shown in Fig. 3.2d.

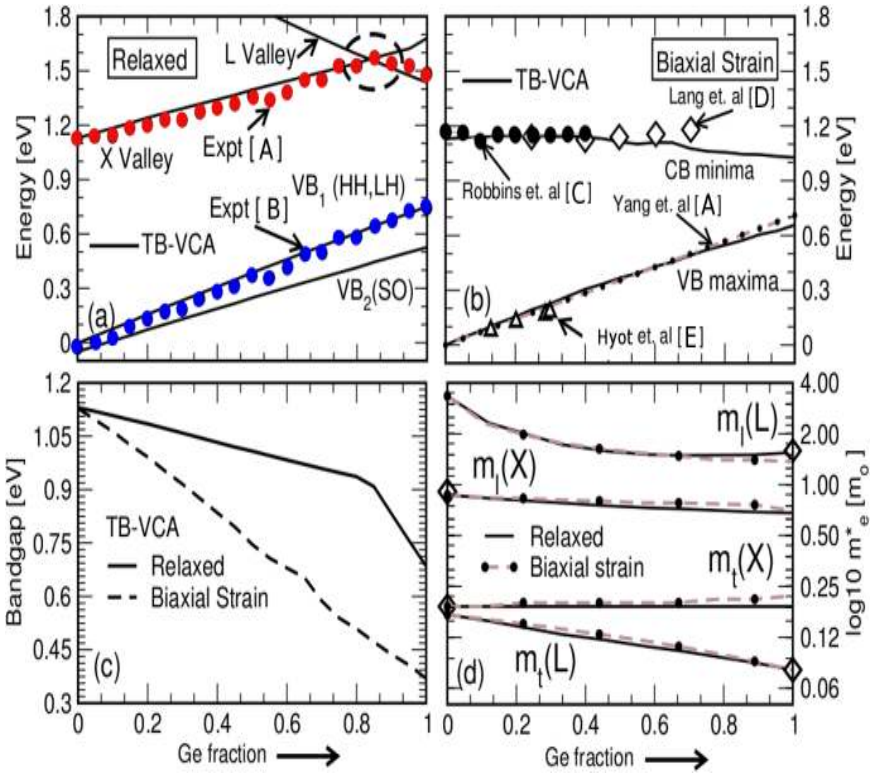

Fig. 3.2. **(a)** Comparison of bandedges for relaxed bulk SiGe. Experimental data [A](○) for CB is from [87]. VB values [B] are obtained by subtracting the bandgap (Eg) values in [88] from the CB values obtained from the TB-VCA model. **(b)** Comparison of bandedges for biaxially strained SiGe bulk structure. Experimental data for CB [C] is from [89] (○) and [90] (◊) [D] and for VB, values are from [91] (△)[E] and [88] (dotted line). The TB-VCA results show good agreement with the experimental values.**(c)** Bandgap variation in relaxed and biaxially strained SiGe bulk structure calculated using TB-VCA. **(d)** Electron effective masses in transverse (m^*_{te}) and longitudinal (m^*_{le}) directions for relaxed and biaxially strained SiGe bulk with varying Ge%. Experimental data (⋄) in (d) is from [92].

3.2.3 Summary of the work

An improved bandstructure model for both relaxed and strained SiGe structures are presented. The complete method to obtain the bandstructure is outlined. The simulated results for bandedges and effective masses compare very well with the ex-

perimental results. This method opens up ways to analyze the nano-scale transistors made of SiGe.

3.3 Performance analysis of SiGe NWFETs

High performance (HP) CMOS technology improvement are pursued by increasing the hole mobility through the use of SiGe by various experimental groups [93–95]. Improvements in the process technology enabled the fabrication of high Ge concentration, ultra-scaled SiGe channel NWFETs. These NWFETs can be divided into two categories: (a) SiGe/Si core/shell channels with SiO_2/High-κ as gate dielectrics [93, 94] (Type A), and (b) SiGe channels with High-κ (HfO_2 or ZrO_2) gate dielectrics [95] (Type B), as shown in Fig. 3.3. The performance analysis of SiGe NWFETs with nanoscale dimensions is possible using TB and ToB models since they can simultaneously handle the material and strain variation, the quantum confinement properties, and electron-hole band coupling of the devices.

3.3.1 Device details and analysis approach

SiGe/Si core/shell structures represent an attractive FET design due to their low defect channel/gate-dielectric interface and improved performances for both n and p FETs [93, 94] over their Si counterparts. Here Type A and B NWFETs with n- and p-doped contacts and [100] oriented channels are considered. The total wire diameter (W) is set to 9nm with a 1.5nm gate oxide ($SiO_2, \epsilon_r = 3.9$). The core diameter (CD) is varied from 0 (pure Si), 3, 4, 6, 8 to 9 nm (no Si-shell,Type B). The self-consistent calculation of the charge and potential is done using the scheme outlined in Sec. 2.3.2 in Chapter 2.

The performance comparison is done using a constant over-drive voltage ($V_{OD} = 2V_{DD}/3$) method as proposed in [96]. The ON-state gate bias (V_{GS}^{ON}) is defined as, $V_{GS}^{ON} = V_{Tlin} + V_{OD}$, where V_{Tlin} is the linear threshold voltage of the FET. A V_{DD} of 0.5V has been used according to the ITRS [9].

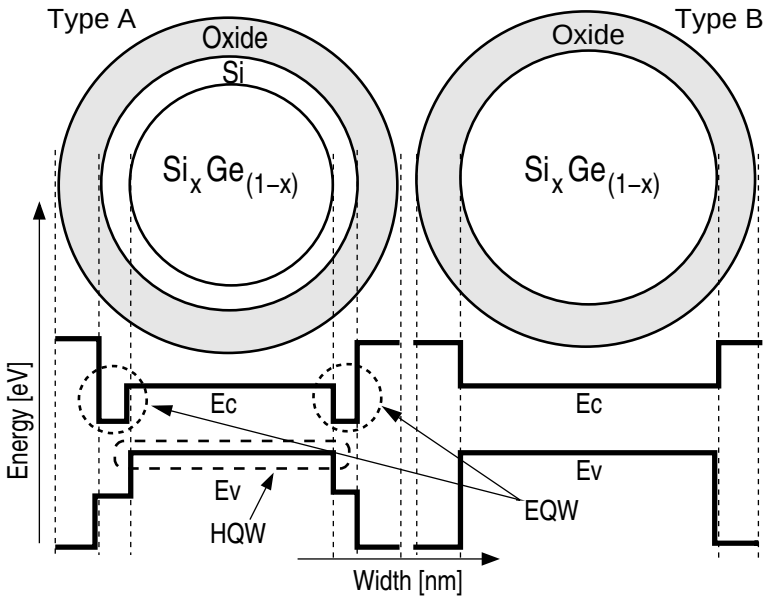

Fig. 3.3. Schematic of Type A and B SiGe NWFETs. Cross-sectional material variations are shown for the two structures. Shown below is the variation in the conduction band minimum (E_c) and the valence band maximum (E_v) along the cross-section of the NWFETs. EQW and HQW represent the electron and hole quantum-well respectively, formed due to the bandedge mismatch at SiGe and Si interface. This figure is from Ref. [53].

The ON-state drain current, I_{ON} and the intrinsic device delay, $\tau_D = C_g V_{GS}^{ON}/I_{ON}$, where C_g is the gate capacitance, are two important metrics for performance comparison [96]. In 1D-ballistic FETs, I_{ON} and τ_D are a direct function of the 'virtual source' carrier velocity (v_{inj}^{ON}),

$$I_{ON} = C_g \cdot V_{OD} \cdot v_{inj}^{ON} \tag{3.7}$$

$$\tau_D = (C_g \cdot V_{OD})/(C_g \cdot V_{OD} \cdot v_{inj}^{ON}) \tag{3.8}$$

3.3.2 Results and Discussion

SiGe vs. Si, v_{inj}^{ON} comparison

Figure 3.4 a shows that for n-FETs v_{inj}^{ON} improves by ∼1.07× for 90% Ge and CD(Core Diameter)/W = 2/3. For a given CD, the CB edge mismatch increases with increasing Ge% in the core hence forming deeper EQW (Electron Quantum Well) in the Si-shell (Fig. 3.3). The inversion charge preferably stays in this Si EQW where electron velocity (v_{inj}) is higher than Ge [97]. As the CD increases the EQW becomes thinner and the inversion charge moves back to the slower SiGe core. This explains the oscillation in v_{inj}^{ON} with shell thickness reduction. Type B NWFETs show decreasing v_{inj}^{ON} with increasing Ge%. Figure 3.4b shows that in p-FETs a higher Ge% and reduction in Si-shell thickness improves v_{inj}^{ON} ∼1.2× compared to Si.

SiGe vs. Si, I_{ON} comparison

Figure 3.4c shows that in n-FETs for 90% Ge with CD/W ∼ 2/3, the I_{ON} improves by ∼1.33× since the inversion charge is pushed inside the high velocity Si shell [97]. In n-FETs, I_{ON} also shows an oscillatory nature for the same reason as v_{inj}^{ON}. The p-FETs show improvement in I_{ON} with an increasing Ge% and CD (Fig. 3.4d). This benefit can be attributed to the higher Ge% in the core (higher v_{inj}^{ON}) and very thin Si shell (larger C_g). In p-FETs, I_{ON} shows a dip when going from pure Si channel to SiGe channel (Fig. 3.4(d)), since the charge build-up is mostly inside the SiGe core (HQW, Fig. 3.3) which is buried under a thick Si shell resulting in smaller C_g and hence smaller I_{ON} according to Eq.(3.7).

SiGe vs. Si, τ_D comparison

The gate delay (τ_D) is determined by the interplay of the inversion charge build-up and its velocity in the channel. For n-FETs, an improvement of ∼1.1× is observed for 90% Ge core with CD/W ∼70% (Fig. 3.5a). In p-FETs, the minimum τ_D is

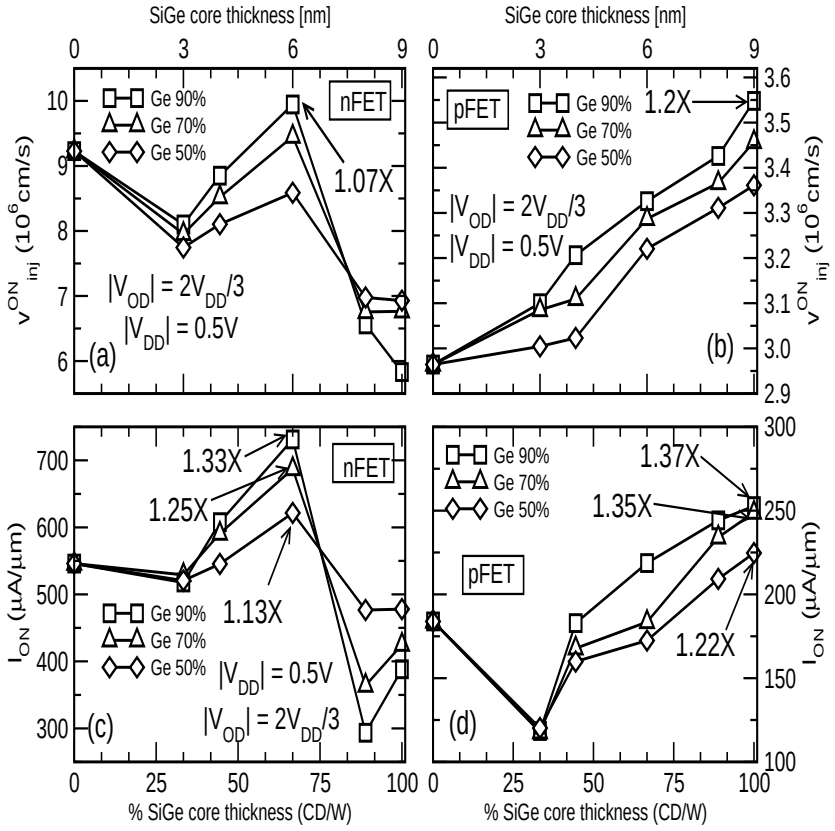

Fig. 3.4. On-state virtual source velocity (v_{inj}^{ON}) for the **(a)** n-FETs and **(b)** p-FETs. I_{ON} is shown for the **(c)** n-FETs and **(d)** p-FETs. The device metrics, calculated at $V_{OD} = 2V_{DD}/3$ and $|V_{DD}| = 0.5V$, are plotted for three different Ge concentrations (90%, 70% and 50%) in the channel with varying SiGe core thickness (0, 3, 4, 6, 8, 9 nm). Channel orientation is [100]. Rightmost FETs on all the plots are 'Type B' devices. This figure is from Ref. [53].

obtained for the devices with CD/W ∼66% (Fig. 3.5b). For p-FETs the maximum improvement is obtained for 90% Ge core which has higher v_{inj}^{ON}. Thus, the core/shell structures can be designed to speed up both the n and p FETs compared to their Si counterparts.

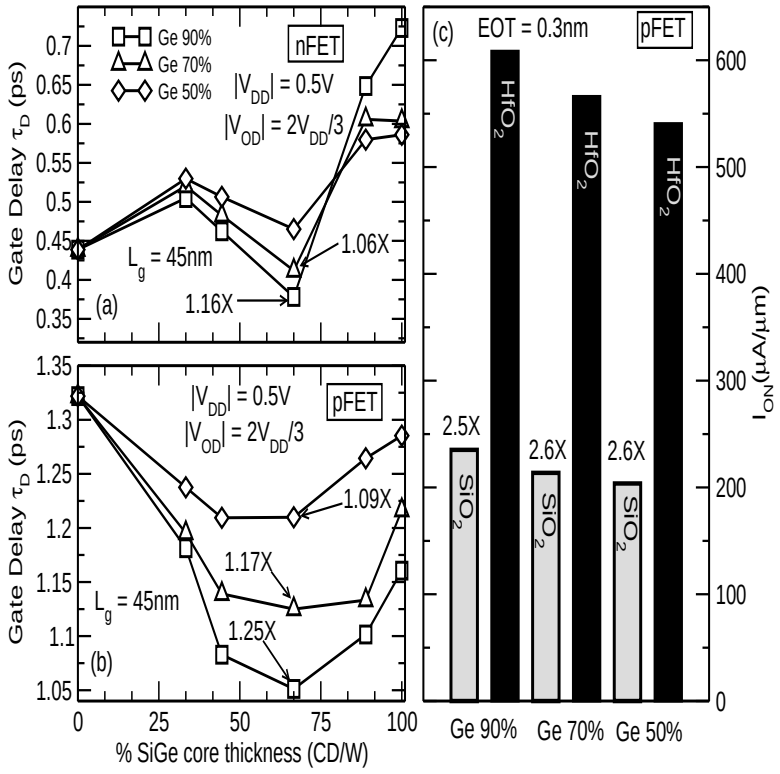

Fig. 3.5. Calculated intrinsic gate delay (τ_D) in pico-seconds (ps) for different SiGe **(a)** n-FETs and **(b)** p-FETs. The fastest n-FET (90% Ge channel, CD = 6nm) is ∼2× faster than the fastest p-FET (90% Ge channel, CD = 6nm). **(c)** I_{ON} in the p-FETs improve by ∼2.5× after replacing SiO_2 by HfO_2, for 9nm diameter SiGe channel. The figure is from Ref. [53].

Comparison of SiGe n and p FETs

Figure 3.5a and b show that the p-FETs are ∼ 2× slower as compared to the n-FETs ($\frac{\tau_n}{\tau_p} \sim \frac{0.4}{1.05}$). The p-FETs can be enhanced by improving the gate control on the channel. This can be achieved in two ways, (**a**) by reducing the Si shell thickness and (**b**) by using a high-κ gate dielectric material. $I_D - V_G$ simulation for three Ge% (90,70 and 50) channels with no Si shell and 1.5 nm thick HfO_2 as gate-dielectric (EOT∼0.3nm, $\epsilon_r \sim 21$) have been performed. The I_{ON} improves as much as ∼2.5× bringing the p-FET performance closer to the n-FET as shown in Fig. 3.5(c).

However, this increases the fabrication complexity and the need for good NW/oxide interface quality [93, 95].

3.3.3 Summary of the work

Design for 9nm SiGe NWFETs are explained. The n-FETs can be improved by $\sim$1.3$\times$ in I_{ON} and the p-FETs by $\sim$1.37$\times$ compared to the Si FETs. Both n and p-type SiGe FETs show an improvement of $\sim$1.2$\times$ over their Si counterparts in terms of the gate delay for a high Ge% and an optimally thick Si shell. SiGe p-FETs will require a thinner Si shell and a High-κ gate dielectric material to make them comparable to SiGe n-FETs. Alloy and interface roughness scattering have been neglected in this study which are expected to reduce the channel currents [98].

3.4 GaAs UTB p-FETs: Impact of strain, orientation and body thickness on performance

III-V semiconductors can provide a viable option for continuous scaling of future CMOS technology [9,99,100]. A significant enhancement in the I_{ON} of UTB GaAs intrinsic channel p-MOSFETs using biaxial compressive strain can be obtained. Atomistic TB investigation shows that VBs become hyperbolic under compressive strain in GaAs rendering effective mass approximation (EMA) invalid. Thus, a full-band approach can provide correct directions for enhancing the performance of these p-type GaAs UTB FETs.

3.4.1 Theory and Approach

The ballistic I_{ON} ($\sim$ Q_{inv} (hole density) $\times$ V_{inj} (injection velocity)) is governed mainly by the asymptotic group velocity (V_{grp} $\sim$K $\cdot V_{inj}$) of the hyperbolic VBs. These bands can be engineered using GaAs body thickness (T_{ch}) scaling, compressive strain and wafer orientation. The analysis of I_{ON} involves the following steps. VB E(k) is

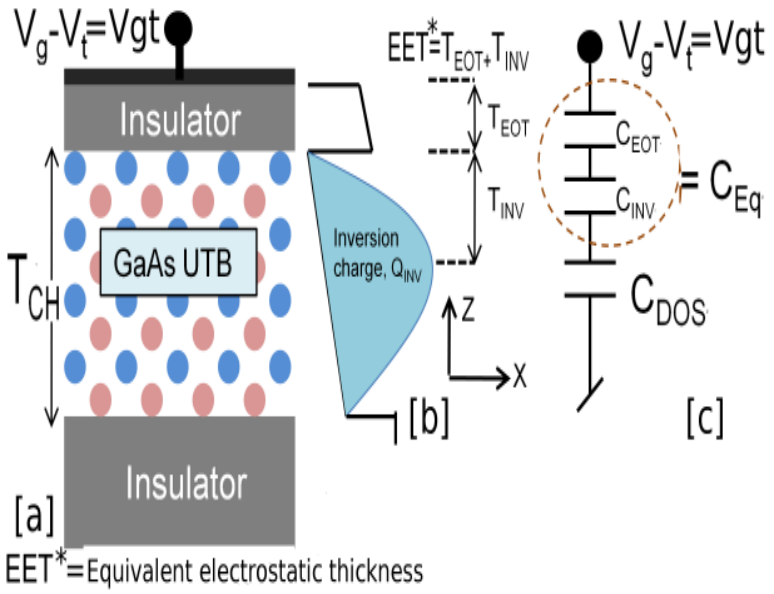

Fig. 3.6. Schematic of an atomic GaAs UTB p-FET channel along with inversion hole density. The value of T_{inv} is calculated using SCHRED [101]. Gate electrostatics is taken into consideration using Eq. (3.9).

calculated using an atomistic $sp^3d^5s^*$ TB model with spin orbit (SO) coupling [40] under the action of biaxial compressive strain (0 to 4%) for the following [transport]/(wafer) orientations: [100]/(100), [110]/(110) and [110]/(111) (Fig. 3.6a), for T_{ch} varying from 2 nm to 5 nm. DOS and modes (M(E)) are calculated numerically using the VB E(k) which are eventually used to calculate the Q_{inv} and drain current (I_{ds}), respectively. The V_{inj} value is calculated using I_{ds}/Q_{inv}. Gate electrostatics is accounted for by considering a gate oxide of thickness T_{ox}. Quantum hole charge density correction (T_{inv}) is obtained using SCHRED [101]. The entire procedure and the equation to calculate gate over drive (V_{GT}) is similar to the method in Ref. [99]. The V_{GT} is given by,

$$V_{GT} = E_f + \frac{C_{Eq} + C_{DOS}}{C_{Eq} \cdot C_{DOS}} \cdot Q_{inv}(E_f), \tag{3.9}$$

where the terms of the equation are shown in Fig. 3.6

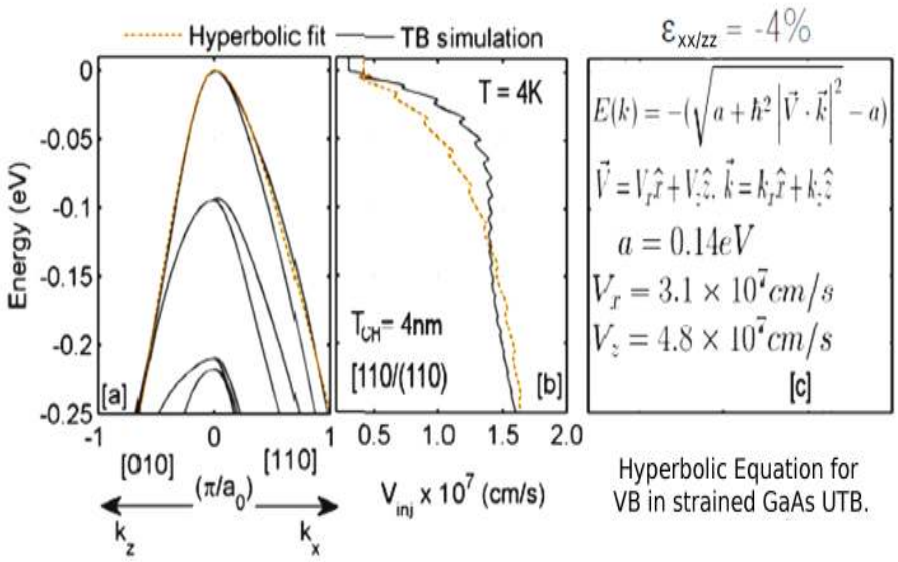

Fig. 3.7. (a) TB calculated (grey solid) and hyperbolic fitted (brown dot line) E(k) along kx (at kz=0) and kz (at kx=0). (b) Comparison of injection velocity obtained from hyperbolic E(k) to the simulated value at T = 4K. Constant V_{inj} vs. E_f is a signature of hyperbolic band. (c) Hyperbolic E(k) expression and the parameter values used for fitting the TB E(k).

3.4.2 Results and Discussion

With III-V n-FETs, the density of states (DOS) is low, the bands are approximately parabolic, and electron velocity varies as the square root of kinetic energy; the channel effective mass, m^* , is selected for highest drive current by balancing its opposing effects on charge density and on injection velocity [99, 100]. In marked contrast, over the range of Fermi energies expected in p-FET operation, the computed VB E(k) fits closely to a hyperboloid as shown in Fig. 3.7 b, with carrier group velocity approaching an asymptotic maximum with increased kinetic energy. The calculated VB E(k) for a 4nm thick GaAs UTB under 4% strain fits very well to hyperbolic bands (Fig. 3.7a), and the injection velocity shows little variation with energy (Fig. 3.7b). Further, because the state density is high, highest current is obtained by designing the channel for highest group velocity, and by selecting a thin

body and dielectric for high charge density. Approximating the hyperbolic bands as E(k) = $\hbar v_0 \parallel k \parallel$, the injection velocity is constant, $V_{inj} = \frac{2}{\pi} \cdot v_0$ and the sheet hole density, $Q_{inv}(k) = \frac{\|k^2\|}{\pi} = \frac{E(k)^2}{(\hbar v_0)^2 \pi}$, is large and varies as the inverse square of the asymptotic velocity (v_0). Strained VBs in GaAs can be well represented by hyperbolic bands where the velocity, rather than the effective mass, is constant with energy which is huge deviation from EMA.

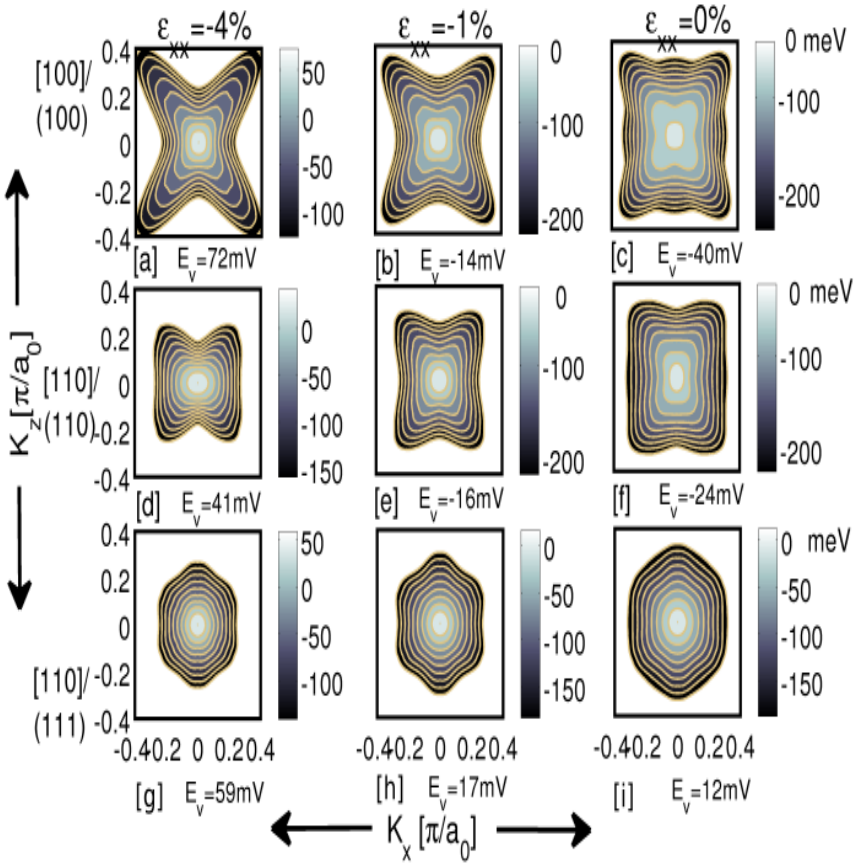

Fig. 3.8. 2D E(k) of the highest VB in the 4nm thick strained GaAs UTB for (a-c) [100]/(100) high V_{grp} (d-f) [110]/(110) low V_{grp} and (g-i) [110]/(111) high V_{grp}. Strain value is -4%, -1% and 0% for left, middle and right column, respectively. The VB max values (Ev) are shown. Energy range is from Ev to $8k_BT$ below Ev. K_x is the transport direction.

The valence bands are highly anisotropic and respond very differently to strain applied in different directions. Figure 3.8 shows the VB E(k) for 4nm thick GaAs UTB

channel for -4%, -1% and 0% biaxial strain. Strain causes an isotropic compression of VB E(k) for [100]/(100) (Fig. 3.8 a-c) and [110]/(111) (Fig. 3.8 g-i) channels. However, for [110]/(110) channel the strain causes anisotropic compression in VB E(k) (Fig. 3.8 d-f) which affects the final terminal characteristics of the GaAs p-FETs.

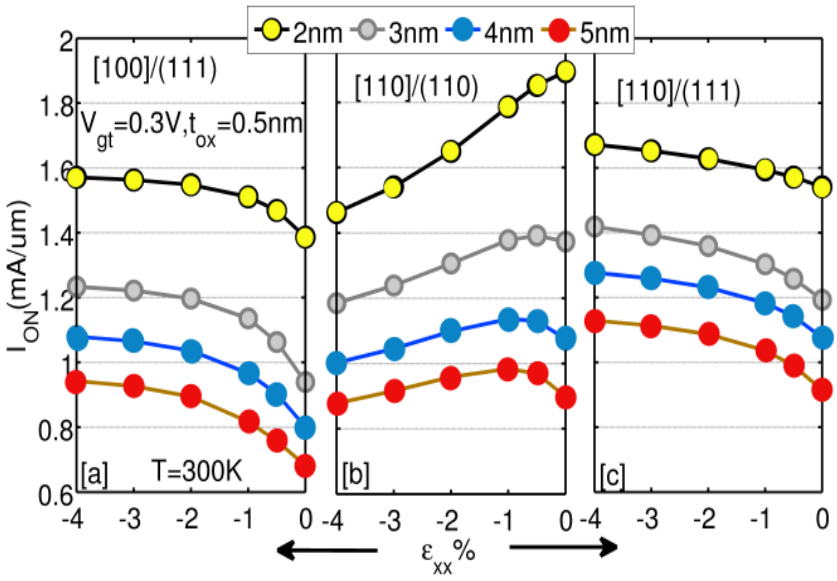

Fig. 3.9. I_{ON} variation with strain for (a) [100]/(100), (b) [110]/(110) and (c) [110]/(111) oriented GaAs p-FETs for 4 different body thickness. [100]/(100) and [110]/(111) devices show improvement with strain and body thickness scaling, whereas [110]/(110) degrades with strain. In [100]/(100) I_{ON} improves a maximum of 38% (5nm,-4%) with strain and $\sim$2$\times$ with body scaling. [110]/(110) I_{ON} degrades by 29% (2nm,-4%) but improves by $\sim$ 2$\times$ with body scaling. In [110]/(111) I_{ON} improves a maximum of 23%.

The calculated I_{ON}, under strain at V_{GT} =0.3V and T_{ox} = 0.5nm (low-operating-power devices [9]) are shown for various GaAs body thickness. The I_{ON} improves $\sim$2$\times$ for all the orientations with body scaling from 5nm to 2nm under 0% strain (Fig. 3.9a-c). The anisotropic strain effect on VB E(k) reveals itself in the computed I_{ON} vs. strain. [100]/(100) and [110]/(111) p-FETs improve monotonically with strain (Fig. 3.9 a and c) showing a maximum improvement of 38% and 23%, respectively for 5nm

thick GaAs channel under -4% biaxial strain. This is an outcome of the compression of the VB E(k) under strain which increases the V_{inj} (Fig. 3.8). The highest I_{ON} is obtained in the [110]/(110) orientation among all the orientation combinations, though strain provides no benefit as shown in Fig. 3.9 b.

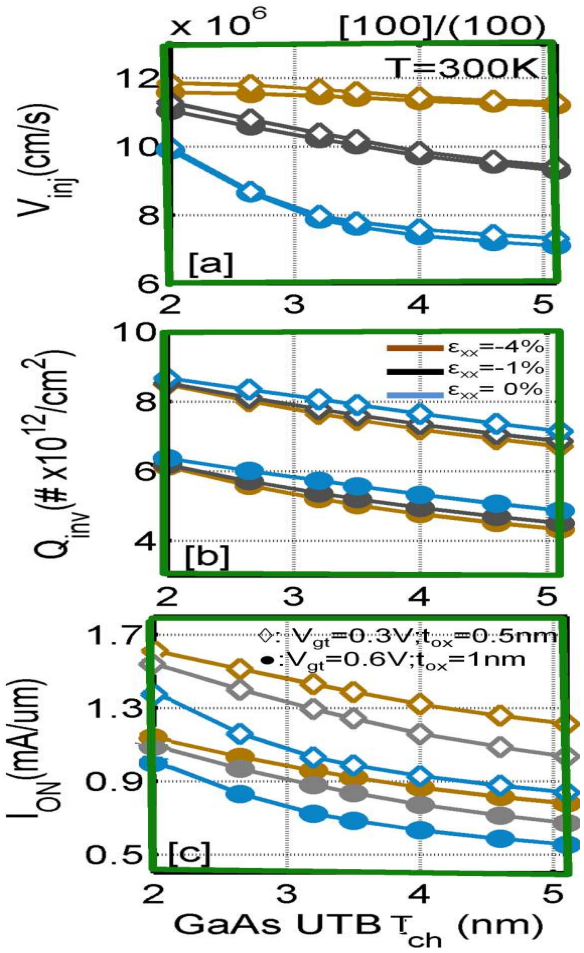

Fig. 3.10. Variation in (a) V_{inj}, (b) Q_{inv} and (c) I_{ON} with GaAs body thickness for 3 strain values (-4%, -1% and 0%) and two gate overdrive biases (V_{GT}). Filled (open) symbol represents V_{GT} = 0.6V (0.3V) for T_{ox} = 1nm (0.5nm). The inversion charge is governed by the gate electrostatics while the injection velocity is governed mainly by strain.

A crucial aspect for designing III-V p-FETs is the action of strain and gate electrostatics on the drive current. As an example the V_{inj}, Q_{inv} and I_{ON} for [100]/(100)

p-FETs with T_{ch} for two different V_{GT} are shown in Fig. 3.10. An important observation is that V_{inj} is primarily enhanced by strain (Fig. 3.10 a) whereas Q_{inv} is dominated by the gate electrostatics. This behavior is observed in all the orientations. The independent control of Q_{inv} and V_{inj} can essentially allow us to design III-V p-FETs with required I_{ON}.

3.4.3 Summary of the work

A proper choice of wafer/transport orientation and strain, providing a high hole group velocity, along with an optimal gate oxide thickness can lead to better III-V p-FETs for the future CMOS technology. V_{inj} is primarily controlled by strain and T_{ch} whereas, Q_{inv} is governed mainly by the gate electrostatics, thus providing two separate design parameters to control I_{ON}. Isotropic strain enhances V_{inj} which gives a maximum improvement in I_{ON} of ∼23-40% for [100]/(100) and [110]/(111) pMOSFETs for 5 nm body thickness at 4% compressive biaxial strain. Scaling body thickness from 5nm to 2nm improves I_{ON} by ∼2× for all the device orientations considered in this study.

3.5 Lead Selenide (PbSe): Bulk electronic structure

Lead Selenide (PbSe) is a narrow, direct band gap semi-conductor material ($\sim Eg^{bulk} = 0.16$eV at 4K [42, 102]) with useful electrical, optical and lattice properties [103–105]. It is used extensively in optical devices [103, 106], lasers [107, 108] and thermoelectric devices [104, 109, 110]. The large Bohr exciton radius of about 46nm in PbSe makes it a suitable system to study quantum confinement effects on electrons and holes [106, 111–113]. Recent progress in multiple exciton generation (MEG) in PbSe with higher optical efficiency has renewed interest in the optical properties of PbSe [105]. Extremely low thermal conductivity of PbSe ($\sim$ 2 W/m-K in bulk [114] to $\sim$ 0.8 W/m-K in NWs [115]) also makes it a suitable thermoelectric material

[104, 110]. PbSe can become a preferable material over Lead Telluride due to the higher availability of selenium (Se) compared to tellurium [116].

Bulk PbSe has a stable rocksalt structure with a co-ordination number of six at room temperature (300K) and normal atmospheric pressure [102, 116]. The lattice constant is 0.6121 nm [102] at T = 4K, which is also utilized in the bandstructure calculations. The PbSe NWs are constructed using the same bulk structure with three different wire axis orientations of [100], [110] and [111] (Fig. 3.11).

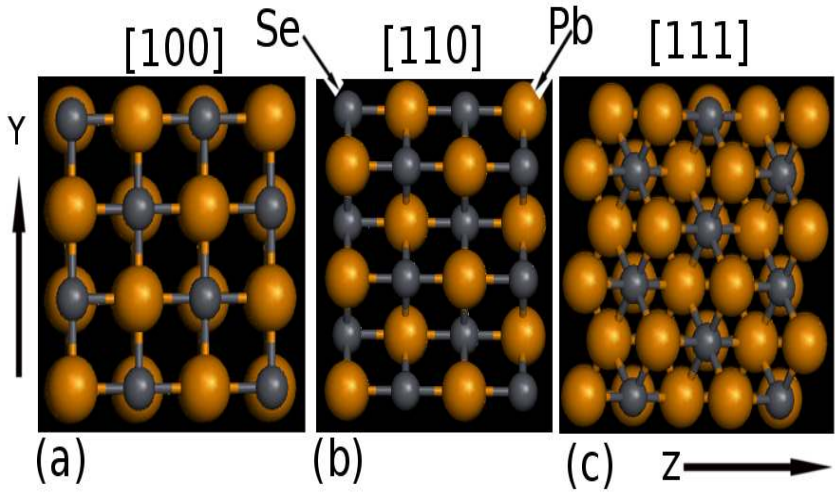

Fig. 3.11. Projected PbSe unitcell with wire axis orientations (X) along (a) [100], (b) [110] and (c) [111]. The cross-section size is of 2.5nm (Y) × 2.5nm (Z). Lead (Pb) and selenium (Se) atoms are also marked.

The main methods for analyzing the lead salt structures are (1) continuum method like 4/8-band k·p [106], (2) semi-empirical atomistic methods like tight-binding (TB) [42, 117], pseudo-potential approaches [118] or (3) first principles methods [113, 116, 119, 120]. The 4/8-band k·p method captures some quantum confinement effects, however, it fails to capture the interaction of various valleys present along the *L*-*K* and *L*-*X* directions, the band anisotropy and the correct frequency dependent dielectric function [113, 117, 118]. The first principle calculations are highly accurate but the demand for computational power is very high and these methods are limited

to solving only small structures with few thousand atoms [70,117]. The semi-empirical methods are versatile in terms of the involved physics and can handle a large number of atoms ($\geq$ 10 million atoms [70]) making them suitable for electronic structure and transport calculation in realistic device structures. However, an integral part of these methods is the requirement of correct semi-empirical parameter sets to properly represent the electronic structure properties like bandgaps, effective masses, wave-function symmetry, etc.

3.5.1 Methodology

The present work utilizes a semi-empirical atomistic TB method based on sp^3d^5 formulation with spin orbit coupling (SO) optimized for bulk Pb salts by *Lent et al* [42] to calculate the electronic structure in NWs. The inclusion of SO is important in PbSe since both CB and VB have strong p-contributions from Pb and Se atoms, respectively [113, 117].

3.5.2 Benchmarking the TB calculations

The routine to calculate the bandstructure was benchmarked using the data provided in Ref. [42] as shown in Fig. 3.12. This provided the confidence to calculate the bandstructure in the nanowires made of PbSe.

The bulk effective masses calculated using the TB parametrization in Ref. [42] is obtained for (i) electrons as $m_e^{\parallel}/m_e^{\perp} = 0.087(0.07)/0.036(0.04) = 2.4$ (1.85) and (ii) holes as $m_h^{\parallel}/m_h^{\perp} = 0.094(0.068)/0.031(0.34) = 2.9$ (2.0). The values in the parenthesis are from Ref. [102]. The TB parametrization in Ref. [42](TB_A) is preferred over the parametrization in Ref. [117] (TB_B) since the TB_A model captures the mass anisotropy quite well, an important requirement for TB models as pointed in Ref. [118].

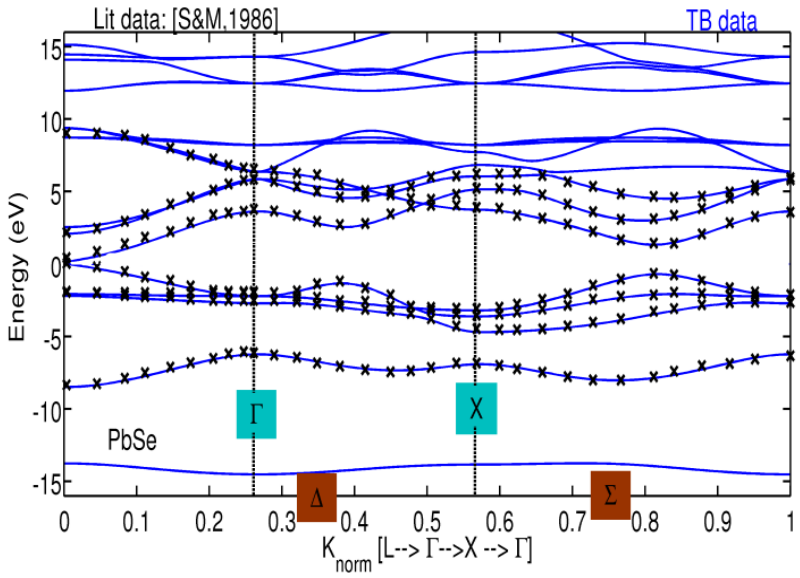

Fig. 3.12. The electronic bandstructure of bulk PbSe calculated using the atomistic sp^3d^5 TB model with spin orbit coupling. The markers are from Ref. [42] and the lines show the TB implementation of this work. A good agreement is obtained between the two calculations.

3.5.3 Summary of the work

A bandstructure implementation for the calculation of PbSe and other lead-chalcogenides using TB model is provided and benchmarked with other theoretical calculations. This lays a good foundation for the atomistic analysis of PbSe nanowires.

3.6 PbSe Nanowires: Electronic structure and conductance

One dimensional nanostructures of PbSe like nanowires (NW) and nanorods (NR) combine the interesting bulk material properties as well as the quantum confinement effects which can lead to better thermoelectric [110,114,115] and optical [103] devices. The analysis of the physical properties in PbSe NWs will require proper understanding of the electronic structure, which is the theme of this section.

With recent advances in the growth and process technology, the fabrication of PbSe NWs have become very efficient and controlled. PbSe NWs are developed using

a variety of methods like, chemical vapor transport (CVT) method [109], oriented nano-particle attachment [111], electro-deposition without catalyst [112] and with catalyst [25], hyper-branching [121], growing PbSe structures on phosphate glass [122], etc. These methods enable PbSe NWs fabrication with a variety of growth directions and surfaces.

3.6.1 Methodology

The electronic structure of PbSe nanowires is calculated using the TB model outlined in Sec. 3.5. To solve for the eigen states of finite structures the surface atoms must be handled correctly. The surface atoms are not passivated for Pb salt nanostructures. It has been previously shown that surfaces do not introduce states in the energy gaps of the bulk band structure, even though they are not passivated [117] and the same is obtained in the present study. The surface states are mainly p-like for Pb salts which are strongly coupled with orbitals of atoms at the interior unlike the zinc-blende semiconductors where atoms are described by hybrid sp^3 orbitals which remain uncoupled at surfaces, forming dangling bonds [123]. The lack of surface passivation has also been pointed out by the first principle calculations in stoichiometric Pb salt nanostrutures [113, 120].

3.6.2 Results and Discussion

The bandstructure of CB and VB for PbSe nanowires are shown in Fig. 3.13 for 3 different wire orientations. For all the wires the conduction band minima (CBM) and valence band maxima (VBM) are normalized to zero to enable a better comparison of the valleys. Some important points to observe are, (i) bulk L valleys are projected at the BZ edge at X for all orientations (Fig. 3.13). The [110] wire has an additional projected valley at the Γ position (Fig.3.13 b, e), (ii) [100] NW show a degeneracy (D) of 1 for both CB and VB due to strong valley splitting, however [110] and [111] NWs show a D of nearly 2 (extremely small valley splitting) for the positive 'k' states.

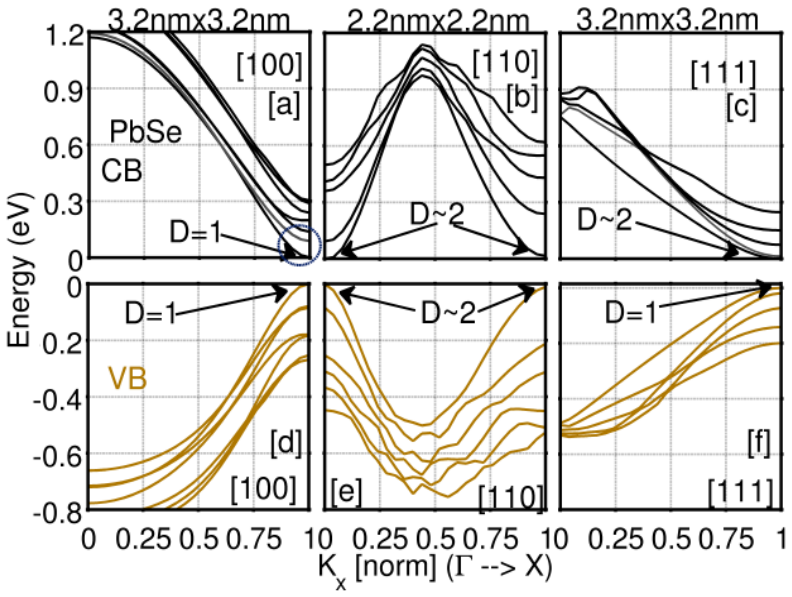

Fig. 3.13. Bandstructure of PbSe NWs for (a) [100], (b) [110] and (c) [111] oriented channels. The CB minima and VB maxima are normalized to zero for simplified band comparison. Only the first 5-10 sub-bands are shown.

The CBM and VBM variation with cross-section size (W) and orientation are shown in Fig. 3.14 a. All the orientations show quite similar band-edge variation with W. As the cross-section size decreases the geometrical confinement increases which pushes the CBM (VBM) higher (lower) in energy. The variation in the bandedges with W also compare surprisingly well with a previous 4-band k·p calculation done for [111] cylindrical PbSe NWs [124]. The bandgap variation with W in PbSe NWs can be fitted to the following analytical expression,

$$Eg = \beta/(W)^{\alpha}, \tag{3.10}$$

where α represents the power law dependence on W.

For [111] NWs the value of $\beta, (\alpha)$ is 1.726 (0.8734). For [110] NWs these values are $(\beta, (\alpha))$ 1.564 (0.8592) and for [100] NWs these values are $(\beta, (\alpha))$ 1.87(1.072). The bandgap values (Fig. 3.14 b) roughly show an inverse relation with W for all the NW orientations which is very different from the prediction of EMA (Eg $\propto W^{-2}$).

Similar results for Eg have been obtained by other independent calculations carried out in PbSe nanostructures using first principle calculations [113] as well as TB calculations [117]. This justifies the application of TB electronic structure calculation which correctly captures the quantum confinement effects in ultra-scaled PbSe NWs.

The transport properties of PbSe NWs are revealed by the electronic conductance which is calculated using Landauer's formula [51]. Figure 3.15 shows the normalized 1D ballistic conductance for electrons in the PbSe NWs for 3 different orientations. [110] and [111] oriented wires show higher G value for both the CB and the VB compared to [100] NWs. A larger valley splitting in the CB and the VB in [100] NWs decrease the conductance compared to the other two orientations. The normalized conductance increases in steps of 2 for [100] NWs for the CB but not for the VB (Fig. 3.15) which shows that the CB and the VB are not entirely symmetric in energy, a result similar to the one given in Ref. [118]. Thus, transport characteristics show the effect of geometrical confinement and channel orientation.

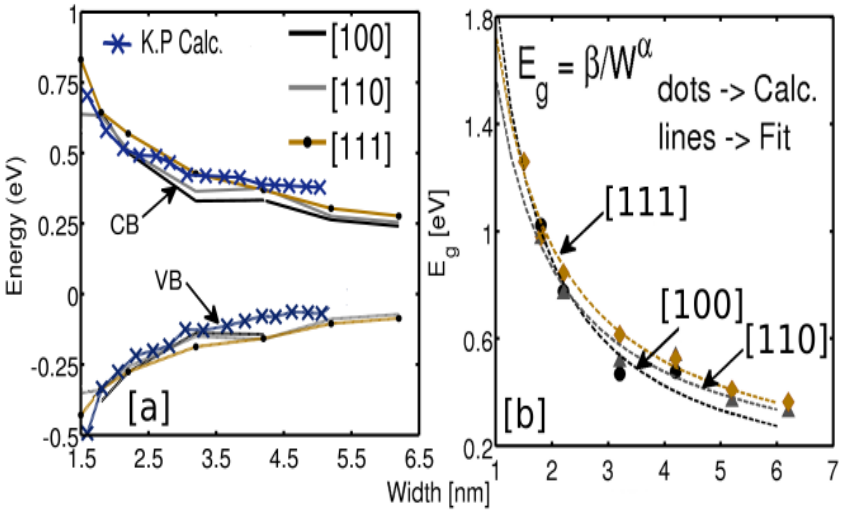

Fig. 3.14. (a) Bandedges for square PbSe nanowires with [100], [110], and [111] channel orientations. Bandedge result using 4-band k·p calculation for cylindrical PbSe nanowires from Ref. [124]. (b) Bandgap variation for all the nanowires. Dots represent calculated TB values and lines represent analytical fitting w.r.t the cross-section size.

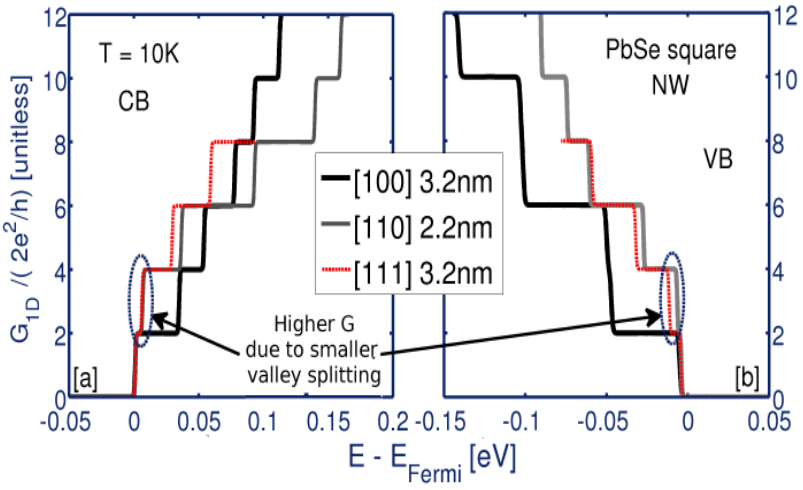

Fig. 3.15. Ballistic conductance in PbSe NWs for (a) CB and (b) VB for 3 different wire orientations at T = 10K. The temperature comes from the Fermi-Dirac distribution of the carriers.

3.6.3 Summary of the work

PbSe NWs have tremendous potential of becoming the next generation thermoelectric and optical devices. The proper understanding of the physical properties of these ultra-scaled PbSe nanowires will depend strongly on the correct electronic structure calculation. The application of semi-empirical tight-binding theory to these NWs to understand the variation of conduction and valence bands and the position of the important energy valleys have been presented. The variation of the bandgap and the bandedges with NW cross-section size is strongly influenced by the cross-section size and channel orientation. Simple EMA theory cannot predict the bandgap variation. The amount of valley splitting is strongly dependent on the type of geometrical confinement as reflected in the ballistic conductance of the PbSe NWs. [110] NWs provide the maximum ballistic conductance for both the CB and VB. The tight-binding analysis of electronic structure opens door to explore the optical and thermoelectric effects in PbSe NWs.

3.7 Summary and Outlook

The versatile nature of the TB model is revealed by the ease with which non-Si materials are analyzed for the future CMOS and TE applications. The impact of strain, size and orientation of the nanostructures on the electronic properties are explored. It is shown that with optimal Si capping SiGe nanowire FETs can be tuned to outperform Si nanowire FETs. The application of compressive biaxial strain to ultra-thin body GaAs p-FETs can improve their drive currents making them a feasible contender for replacing Si p-FETs at the nano-scale. PbSe nanowires show interesting quantum mechanical effects on their electrical characteristics which can be used for thermoelectric devices. The highly non-parabolic nature of the energy bands again shows the need to go beyond EMA. In all these analysis, scattering has been neglected since the main motive was to understand if bandstructure itself results in some fundamental limitations on the performance. An extended analysis including scattering effects such as surface roughness [98], and phonons [125] will play a crucial role in determining the best possible future device combinations.

4. ELECTRON TRANSPORT IN EXPERIMENTAL ULTRA-SCALED Si TRANSISTORS

4.1 Introduction

The aim of this chapter is to apply TB theory coupled with ToB model to investigate real transistors. It is essential to match experimental data using simulations as it gives confidence in the models as well as calibrates the models for predicting the electronic properties of the next generation transistors. In this chapter the electron transport theory has been applied to calculate the electrostatics of Si nanowire FETs and bulk p-type SiGe MOSFETs. The models are also used to understand the experimental source to channel barrier height (E_b) and active channel cross-section area (S_{AA}) in trigated undoped channel Si FinFETs. The key message of this chapter is that TB-ToB model gives insight which is helpful in understanding the experimental results in ultra-scaled FETs.

Much of the work in this chapter has been done in collaboration with experimental groups from all over the world. The collaboration details are provided in the respective sections. The present chapter is organized as follows. Match with experimental capacitance-voltage (C-V) data is provided in Sec. 4.2. The work on p-type bulk SiGe MOSFETs is outlined in Sec. 4.3. The estimation of E_b and S_{AA} in trigated Si n-FinFETs is outlined in Sec. 4.4. The procedure of the new interface trap extraction methods are provided in Sec. 4.5. Summary and outlook are provided in Sec. 4.6.

4.2 Matching experimental CV for [100] SiNW FETs

This project involved understanding the experimental CV obtained from a new technique called CBCM [1] using the quantum mechanical simulations in OMEN-BSLAB [46]. This work has been published in Ref. [47]. The details of the project are:

- Collaborating Institutes: Purdue University, USA and Institute of Micro-Electronics (IME), Singapore.
- Collaborators: (1) Purdue University: Mark Lundstrom, Gerhard Klimeck, Abhijeet Paul, Raseong Kim, and Mathieu Luisier.
  (2) IME Singapore: Subash Rustagi, Hui Zao, Fa-jun Ma

4.2.1 Device details

For the fabrication of SiNW FETs, the process flow in Ref. [126] is modified by introducing the local release of the SiNW to prevent the formation of a gate poly-Si stringer around the S/D region. This significantly reduces the gate-to-source/drain parasitic capacitance. The DUT[2] has a gate length of $0.85\mu m$ and a rounded triangular cross section with base of width (W) $\sim$ 22nm and height (H) of $\sim$ 9nm as shown in Fig. 4.1. The gate oxide (SiO_2) thickness (T_{ox}) is $\sim$ 9 nm, as seen from the TEM image (Fig. 4.1).

The detailed capacitance measurement method is provided in the Ref. [47].

4.2.2 Simulation procedure

There were two tasks that needed to be done for obtaining the CV for this SiNW FET. First was the determination of the parasitic capacitance(C_{par}) of the structure and second was the calculation of the voltage dependent intrinsic capacitance (C_{int})

[1] charge-based capacitance measurement
[2] DUT = Device Under Test

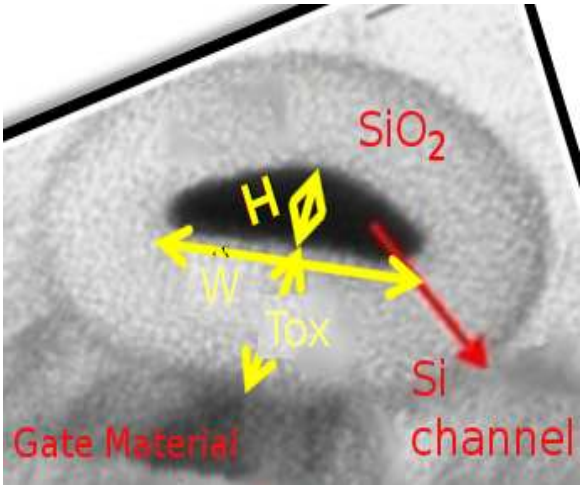

Fig. 4.1. TEM image of SiNW FET fabricated at IME Singapore. Details in Ref. [47]. W $\sim$ 22nm, H $\sim$ 9nm and Tox $\sim$ 9nm.

of the device. First task was done by Dr. Raseong Kim (Purdue University) using COMSOL[3]. The details are given in Ref. [47]. The value of C_{par} is provided in the Fig. 4.5. The second task is discussed in more detail next.

Calculation of C_{int}

The first step to perform a CV simulation was to obtain the device description. This was extracted from the coordinates of the TEM image for the device (Fig.4.1). This information was fed to the OMEN-BSLAB tool. The oxide and the atomistic channel were broken into 12 and 23 triangular pieces, respectively to completely match the device size. The Si channel was represented atomistically for solving the Schrodinger equation using the TB model. The Si channel unitcell consisted of 4505 atoms as shown in Fig. 4.2a. To obtain the electrostatic potential, the entire device cross-section is meshed using 36595 points ($\sim$20000 triangles making the mesh) as shown in Fig. 4.2 b. The self-consistent calculation for charge and potential is the same as described in section 2.3.2 (Fig.2.5).

[3]More details on COMSOL Multiphysics tool can be found on http://www.comsol.com

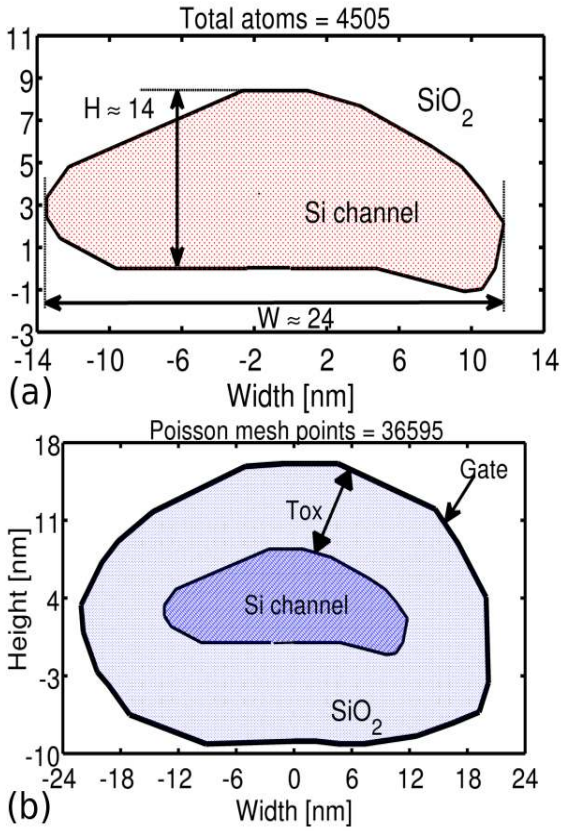

Fig. 4.2. (a) Atomic mesh for the Silicon channel oriented along [100] direction. There are 4505 atoms in the unitcell used for solving the Schrodinger equation. (b) The FEM mesh is used for solving the Poisson equation to obtain the potential distribution. The region was discretized into 36595 mesh points with $\sim$ 20000 triangles.

The value of C_{int} was calculated from the self-consistent charge ($Q_{TB}(V_G)$) and potential (V_{GS}) as,

$$C_{int}(V) = \frac{\partial Q_{TB}(V)}{\partial V_{GS}} \tag{4.1}$$

where, the unit of Q_{TB} is in col/m. V_{GS} is the gate bias. The results for charge and potential at $V_{GS} = 1$V are shown in Fig. 4.3 and 4.4, respectively. An important point to note in the charge distribution is the piling of electrons at the sharp corners, an effect known as the 'corner-effect' [127]. However, this does not result in any double turn-on in the channel as reflected by the single turn-on smooth C-V curve of

the device (observed both experimentally and in simulation, Fig. 4.5). This indicates that these SiNW FETs are volume inverted due to their extremely small cross-section size. The potential distribution is smooth as shown in Fig. 4.4.

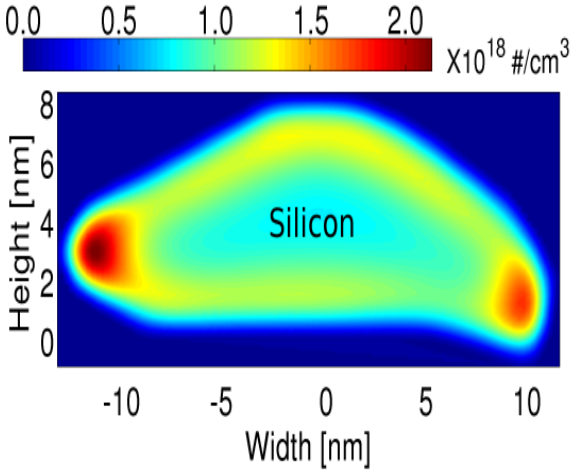

Fig. 4.3. Electron density in the device at $V_{GS} = 1$V. Unit is $\#/cm^3$.

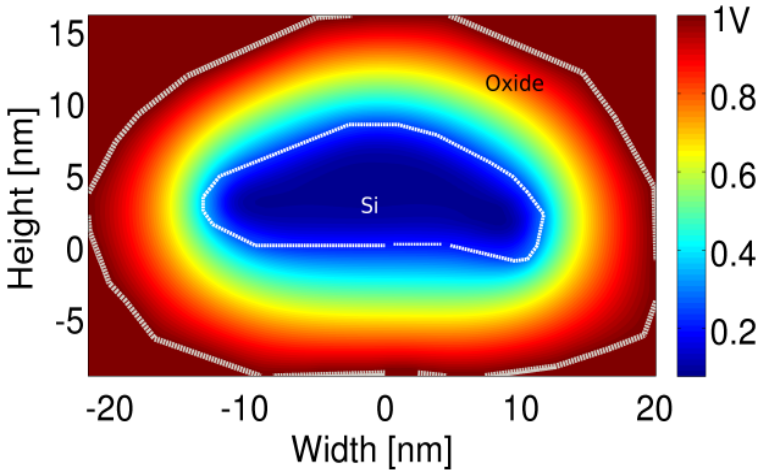

Fig. 4.4. Potential distribution in the device at $V_{GS} = 1$V.

4.2.3 Comparison of the simulated and experimental CV

The measured gate capacitance (C_{DUT}) of the single-channel SiNW transistor measured by CBCM is shown in Fig. 4.5 (black thick line). As the S/D contacts are n-type, any significant capacitance on the accumulation side ($V_{GS} < 0$) is not expected. However, a capacitance floor of ∼0.72 fF[4] can be seen in the $C_{DUT}V_{GS}$ curve. It was further observed that the minimum capacitance increased linearly with the length of the S/D region suggesting that the origin of this minimum capacitance is parasitic related to the contact pads of the S/D regions as outlined in Ref. [47].

Figure 4.5 shows a very good agreement of the measured C_{DUT} with the sum of the simulated C_{int} and C_{par}. The simulated gate capacitance in inversion (∼0.261 fF) from the self-consistent simulation is about 90% of the measured value (∼0.29 fF, measured from the minimum), and the sum of the self-consistent and parasitic capacitance is about 95.8% of the measured capacitance. A little larger value of the measured inversion capacitance is inferred to be due to the bottom-gated portion of the channel that extends from the gate all-around region by 75 nm to both source and drain contact regions. The oxide capacitance increases by 3.6% when the bottom gate is considered in 3-D electrostatic simulations, as seen in Fig. 4.5. Thus, a very close agreement with the experimental CV is obtained after taking into account the parasitic and overlap capacitance.

4.2.4 Summary of the work

Top of the barrier model is indeed very useful in analyzing the device properties at the ultra-scaled regime. The successful matching of the experimental CV of the ultra-scaled device shows the importance of the quantum mechanical effects in these devices. There is a need to shift from the conventional EMA models to more sophisticated full band methods like Tight-Binding for device simulations. This project also showed the wide applicability of OMEN-BSLAB code.

[4]fF = femto Farad = 10^{-15}F

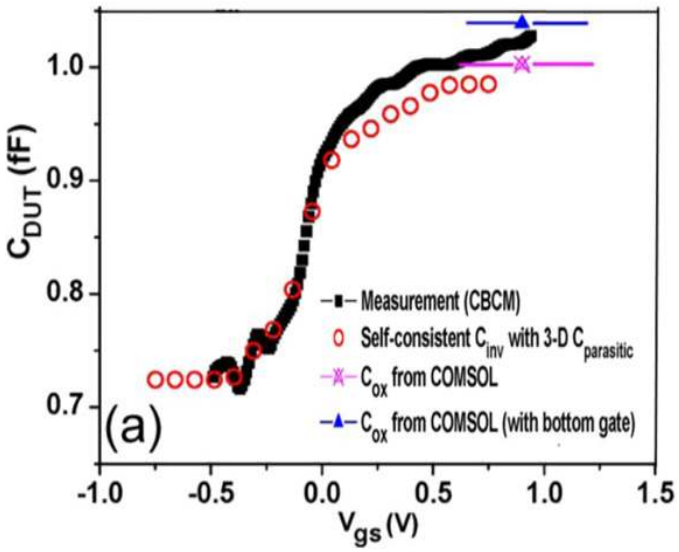

Fig. 4.5. CV curves of the single-channel SiNW transistor measured by the CBCM technique (black) and self-consistent intrinsic SiNW gate capacitance (circular dots) simulated with the $sp^3d^5s^*$ Tight-binding model (in OMEN-BSLAB) added with the 3-D electrostatic capacitance without considering the SiNW in the COMSOL simulation.

4.3 Performance and Reliability study in SiGe pMOSFETs

High hole mobility (μ_h) and CMOS process compatibility makes SiGe an attractive p-MOSFET channel material [128]. This project involved matching the experimental CV in bulk p-SiGe MOSFETs, with strained SiGe layers grown on Si bulk, and to understand the impact of the strain on the overall device performance and reliability. This work has been published in Ref. [48]. The details of the project are:

- Collaborating Institutes: (1) Purdue University, USA, (2) Sematech, USA, and (3) Indian Institute of Technology (IIT), Bombay, India.

- Collaborators: (1) Purdue University: Abhijeet Paul, and Gerhard Klimeck.
  (2) Sematech: G. Bersukar, J. Huang, and R. Jammy.
  (3) IIT: Shweta Deora, and R. Bijesh.

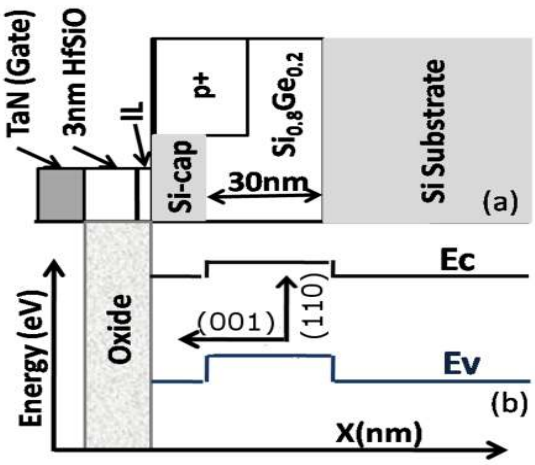

Fig. 4.6. Schematic of a bulk p-type strained SiGe layer MOSFET.

4.3.1 Device Details

Experiments were performed on epitaxial 30nm thick SiGe (20%Ge) grown on (001) Si surface with [110] channel orientation, and with and without Si cap p-MOSFETs [3] (see Table 4.1). The substrate doping is $\sim 10^{18} cm^{-3}$. The surface was cleaned with HF chemistry, which was immediately followed by a ∼3nm thick HfSiO deposition. The gate dielectric was grown by atomic layer deposition. Subsequent processing included a conventional gate-first metal gate (MG) process with 950C source/drain annealing for 10s. Gate material used was 70nm thick TaN with metal gate work-function (ϕ_m) of ∼4.6eV. A Si cap of 3nm thickness was used. The device schematic is shown in Fig. 4.6. The SiGe layer grown on Si is biaxially compressive strained due to lattice mismatch. These devices were fabricated at Sematech, Austin, TX, USA.

4.3.2 Simulation Procedure

The experimental findings and trends are further supported by the theoretical calculation of hole bandstructure (E(k)) in bulk Si and biaxially strained SiGe bulk

Table 4.1
Bulk SiGe p-MOSFETs used in the performance and reliability study.
The substrate orientation is (001) and channel orientation is [110].

Wafer	Substrate	Dielectric	Si-cap	PVD metal
Si	Si only	3nm HfSiO	none	TaN 70nm
SiGe	30nm SiGe on Si (20% Ge)	3nm HfSiO	none	TaN 70nm
Si/SiGe	30nm SiGe on Si (20% Ge)	3nm HfSiO	3nm	TaN-70nm

using the TB-VCA model outlined in Sec. 3.2 [40, 53, 65] along with self-consistent charge and potential calculation using the effective masses (m*), band-edges and band-gaps extracted from the full E(k). The use of EMA is justified here because of the large size of the system (Si substrate > 500nm) and using strain modified effective masses [129]. The results for simulations and their effect on the experimental observations are explained in the next part.

4.3.3 Results and discussion

Strained Valence Bands:

Due to the compressive strain the heavy hole (HH) bands in SiGe (with 20% Ge) become lighter whereas the light-hole (LH) bands become slightly heavier as shown in Fig. 4.7. The large reduction in HH effective mass and increased separation between the HH and LH (shown in Fig. 4.10) plays a significant role in increasing the hole mobility in strain SiGe p-MOSFETs [130].

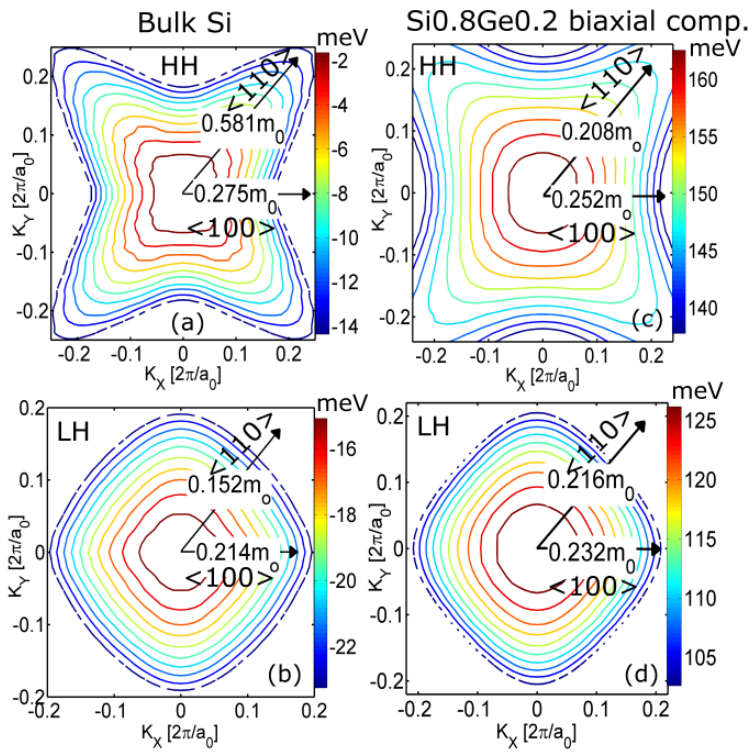

Fig. 4.7. Comparison of hole transport mass along [110] in Si and biaxially compressed $Si_{0.8}Ge_{0.2}$ channel obtained using full-band atomistic TB simulations. The Heavy hole shows a reduction of ∼2.8× in hole effective mass while the light hole shows an increase of ∼1.42× in SiGe compared to Si. Bandstructure is calculated using atomistic TB-VCA method outlined in Sec. 3.2.

Matching with experimental CV:

The self-consistent calculation of CV using the effective masses, barrier height and band separation obtained from the TB calculations provide a very good match with experimental CV for all the three MOSFETs as shown in Fig. 4.8. This reflects the importance of using correct masses and band separation for matching the experimental CV. Once the CV is matched the oxide electric field (EOX) and the effective oxide thickness (EOT) can be extracted from the simulations which allow for further analysis of the experimental data [48].

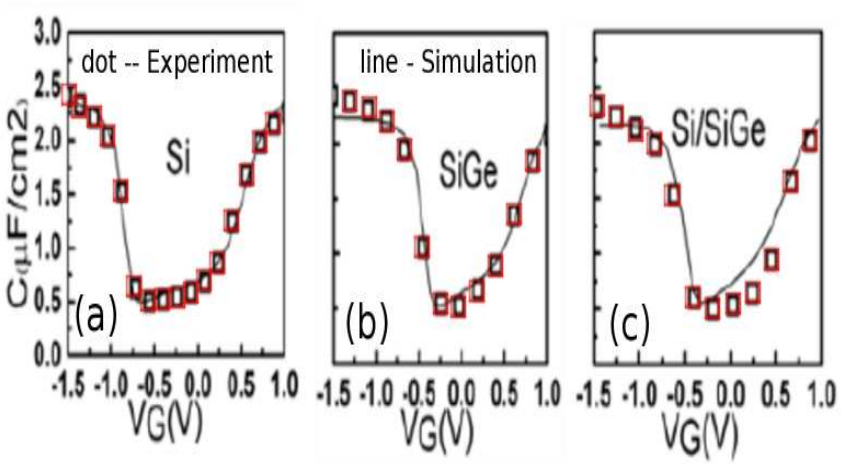

Fig. 4.8. Matching of experimental CV using self-consistent simulation for p-type MOSFETs with (a) Si channel and substrate, (b) SiGe channel with Si substrate, and (c) Si-cap/SiGe channel with Si substrate. Ge concentration is 20% in SiGe layer. A very good match is obtained in these devices.

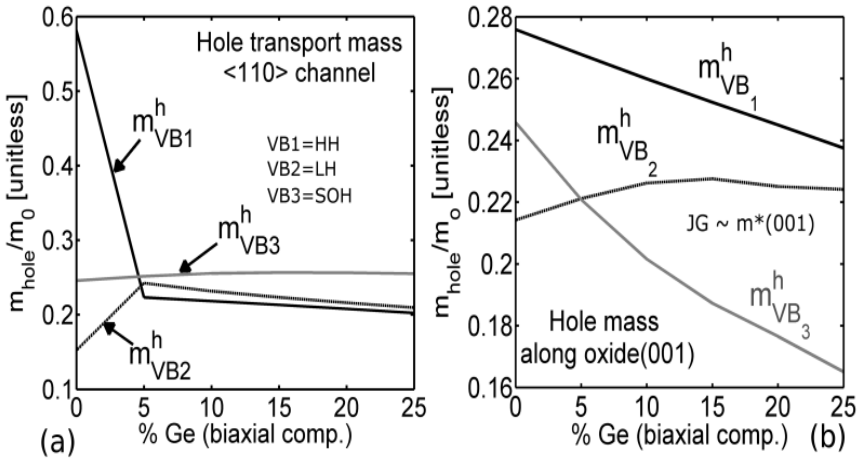

Fig. 4.9. Hole effective masses calculated using the 10 band TB model with spin orbit coupling for three hole bands along two different directions. (a) [110] direction along the channel transport, and (b) [100] direction along the oxide direction. The oxide tunneling current (J_G gate leakage component) is proportional to the effective mass along the oxide direction.

Performance improvement:

SiGe and Si/SiGe devices show ∼1.4× and ∼1.7× improvement in drain current and g_m over Si devices [48]. SiGe shows ∼1.5× improvement in hole mobility over Si which gets better with Si-cap (∼2×) due to better oxide-semiconductor interface quality. These improvements can be attributed to (i) the reduction in hole transport mass (Fig. 4.7) in biaxially strained SiGe compared to Si by ∼2.8× (Fig. 4.9a), and (ii) the suppression of inter-band phonon scattering due to the large strain field splitting of HH and LH [130] in SiGe (Fig.4.10, ΔVB ∼36meV at 20% Ge concentration).

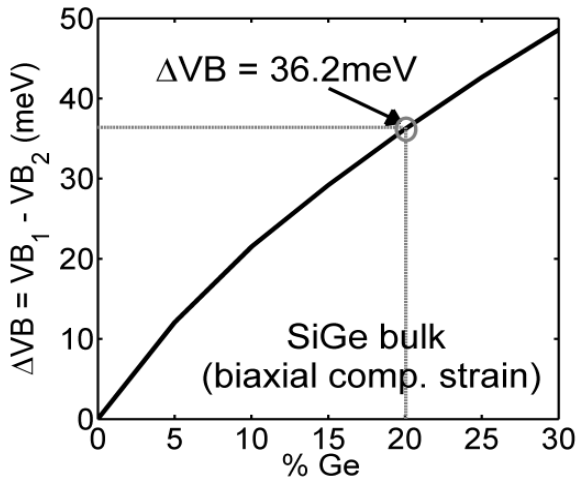

Fig. 4.10. Energy band separation (ΔVB) between heavy-hole and light-hole for various Ge compositions. At 20% Ge ΔVB ∼36meV. This large energy splitting improves hole mobility due to the reduction in inter-valley phonon scattering [130].

Reliability improvement:

The reliability of the SiGe p-MOSFETs is better than Si MOSFETs in terms of NBTI[5] and 1/f noise [48]. This is due to two probable reasons, (i) large increase in the hole effective mass (Fig. 4.9b) along the oxide direction which reduces the J_G,

[5]NBTI = Negative Bias Temperature Instability

and (ii) increase in the oxide and VB hole barrier in compressive strained SiGe (Fig. 4.11) which again suppresses hole tunneling. The experimental observations are well supported by the simulation results.

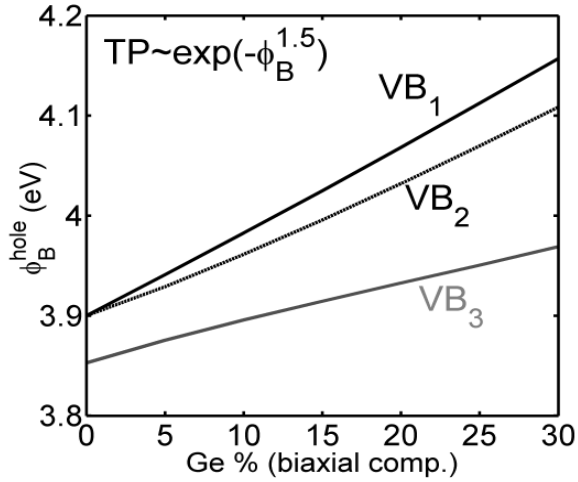

Fig. 4.11. Hole tunneling barrier height (ϕ_B^{hole}) for HH, LH and split-off bands in strained SiGe with Ge concentration. The hole barrier height increases in SiGe channel with increasing Ge%. At 20% Ge, ϕ_B^{hole} increases by 0.154eV compared to Si. This increase in ϕ_B^{hole} reduces the tunneling probability (TP) and hence the gate tunneling current.

4.3.4 Summary of the work

Biaxially strained SiGe channel shows improvement in performance due to the reduction in the hole transport mass and valance band splitting. There is a significant reduction in degradation in SiGe compared to Si. Si-cap on SiGe further improves performance and reliability, but at an added process complexity. The correct estimation of EOX and EOT is provided using the self-consistent calculation by using the hole masses from TB calculations. Hence, a multi-scale simulation setup enabled the understanding of performance and reliability improvement in SiGe p-MOSFETs.

4.4 Sub-threshold transport in undoped trigated Si n-FinFETs

This project spanned over two years (2009-2011) which led to the following key achievements:

1. Understood the sub-threshold transport in undoped channel Si trigated n-FinFETs. The results of this work are published in Ref. [16].

2. Developed two new interface trap extraction methods in these Si n-FinFETs. The results of this work are published in Ref. [49].

The details of the project are:

- Collaborating Universities: Purdue University, USA and Technical University, Delft (TUDelft), Netherlands.

- Collaborators: (1) Purdue University: Gerhard Klimeck, Abhijeet Paul, Sunhee Lee, and Saumitra Mehrotra.
  (2) IME Singapore: Sven Rogge and Giuseppe Tettamanzi

This part of the project discussed in this section dealt with understanding thermally activated sub threshold transport in undoped triple-gate MOSFETs (Fig. 4.12).

4.4.1 Device and Experimental details

Device details: In this work, seven different FinFETs (labeled A-G) with two different channel orientations of [100] ((FinFETs A-C and G)) and [110] ((FinFETs D-F)) have been used [24] (see Table 4.2). All the FinFETs have the same channel length ($L = 40$nm). The channel height (H) is either 40nm or 65nm (Table 4.2). The channel width (W) varies between 3 to 25nm. All the FinFETs consist of one or more Si channel(s) (fins) running between the same source and drain contacts. These fins are etched on an intrinsic Si film with wrap-around gates covering the three faces of each of the channel fins (Fig. 4.12 a) [24]. An HfSiO (high-κ) layer isolates a TiN layer from the intrinsic Si channel [24]. In particular the FETs used in this study,

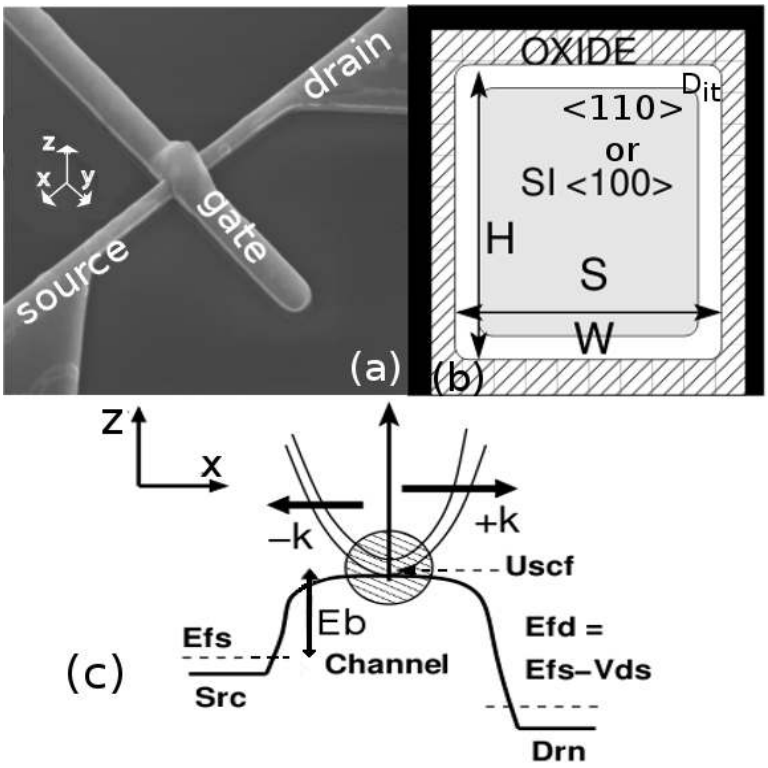

Fig. 4.12. (a) Scanning-electron-microscope (SEM) image of a Si n-FinFET with [100] channel orientation and single fin. (b) The schematic of the cross-sectional cut in the Y-Z plane of a typical tri-gated FinFET. The active cross-section (S_{AA}) is in gray, H and W are the physical height and width, respectively. (c) Ballistic top of the barrier model employed for calculating the thermionic current in the FinFETs.

have either one fin (FinFETs A-C and G) or ten fins (FinFETs D-F) between a given source and drain. The measured drain current is normalized by the number of fins in the channel to obtain the current per fin which allows a fair comparison between different types of FinFETs. These devices have two different surface treatments (with or without H_2 annealing) as shown in Table 4.2.

Measurement procedure: The experimental value of E_b and S_{AA} are obtained using a differential conductance ($G = \partial I_D/\partial V_{ds}$) method. The conductance data are taken at $V_{ds} = 0$ V using a lock-in technique. The full experimental method and the required ambient conditions have been outlined in detail in Ref. [16].

Table 4.2
Si n-FinFETs used in this study along with their labels. The surface hydrogen annealing detail is also shown. The channel is intrinsic Si, while the source and the drain are n-type doped for all the FinFETs.

Label	H [nm]	W [nm]	L [nm]	Channel Orientation	H_2 anneal
A	65	25	40	[100]	Yes
B	65	25	40	[100]	No
C	65	∼5	40	[100]	No
D	40	18	40	[110]	Yes
E	40	18	40	[110]	Yes
F	40	∼3-5	40	[110]	Yes
G	65	∼7	40	[100]	Yes

4.4.2 Modeling Approach

Self-consistent calculation

The bandstructure for the Si channel is calculated using TB [45, 66, 72]. The TB calculation is coupled self-consistently to a 2D Poisson solver to obtain the charge and the potential [66, 72]. Once the convergence between the charge and the potential is achieved the thermionic current in the FinFETs is obtained using the semi-classical ballistic ToB model as shown in Fig. 4.12c [43, 66, 72]. Due to the extensively large cross-section of the devices that combines up to 44,192 atoms (for H = 65nm, W = 25nm FET) in the simulation domain, a new NEMO-3D code has been integrated in the top of the barrier analysis [71]. Since the FinFETs studied here show (i) negligible source-to-drain tunneling current and (ii) reduced SCEs [16], the ToB model is applicable to such devices [72]. All the FinFETs are n-type doped in the source and drain to a value of $5{\times}10^{19} cm^{-3}$. A 1.5nm SiO_2 cover is assumed for simulations.

The ballistic ToB model has been chosen for simulations due to the following reasons. The FinFETs used in the study have undoped channels [16] which reduce impurity scattering. Also a small channel length of 40nm along with a small signal drain bias ($V_{ds}^{dc} = 0V$,$V_{ds}^{ac} \sim 1mV$ coming from the lock in technique) [16] further suppresses back-scattering in the sub-threshold operation regime.

As it is difficult to extract the gate work-function (WF) from the experimental results, a mid-gap gate WF value of 4.5eV is utilized in the simulations for all the FinFETs. The simulated $I_D - V_G$ curves are then shifted such that the simulated and the experimental V_T overlap. Then the V_{GS} range is chosen from the matched V_T point (V_2 in Eq.(4.15)) down to a constant gate under-drive, $(V_{gs} - V_T) \sim 1/3V_{dd}$ (V_1 in Eq.(4.15)), where $V_{dd} = 0.9$V (according to Ref. [9]). This analysis method is outlined in detail in Ref. [96].

4.4.3 Calculation of E_b and S_{AA}

For pure thermionic emission any carrier energetic enough to surmount the barrier from the source to the channel (Fig. 4.12c) will reach the drain provided the transport in the channel is close to ballistic [43]. Typically S/D in FETs are close to thermal and electrical equilibrium (since heavy scattering in the contacts is assumed which leads to instantaneous carrier relaxation). This allows us to make the assumption that most of the carriers in the S/D are thermalized at their respective Fermi-levels (E_{fs}, E_{fd} in Fig. 4.12 c). Also the channel potential (U_{scf}) can be determined under the application of V_{gs} using the self-consistent scheme (discussed in Sec. 4.4.2). Hence, for the source-to-channel homo-junction inside a FET, E_b can be determined as a function of V_{gs},

$$E_b(V_{gs}) = U_{scf}(V_{gs}) - E_{fs}. \tag{4.2}$$

This definition of E_b implicitly contains the temperature dependence since the simulations are performed at different temperatures (T) which enters through the

Fermi-Dirac distribution of the S/D. In a later section it is shown that the temperature dependence of E_b in the sub-threshold region is very weak (Sec. 4.4.4). Therefore, all the theoretical E_b results shown in this work are at T = 300K.

The study of thermionic emission model is applicable when the barrier height is much larger than the thermal broadening ($E_b \gg k_BT$ [131]). For this reason, Eq. (4.2) works only in the sub-threshold region where E_b is well defined [72]. Once the FinFET is above the threshold, E_b ($\leq k_BT$) is not a well defined quantity [72]. Using the E_b value, S_{AA} can be extracted using the conductance (G) in the thermionic emission regime for a 3D system [16, 131] as,

$$G_{3D} = S_{AA}A^*T\frac{e}{k_B}exp\Big(-\frac{E_b(V_{gs})}{k_BT}\Big) \tag{4.3}$$

where A^* is the effective 3D Richardson constant ($A^*_{Si,3D} = 2.1 \times 120\, Acm^{-2}K^{-2}$) [131], and e is the electronic charge. This will hold only when the cross-section size of the FinFET is large enough (i.e.: W, $H >$ 20nm) to be considered a 3D bulk system. For a very narrow width FinFET, S_{AA} cannot be extracted using Eq.(4.3) since the system is close to 1D. For a 1D system the G, under a small drain bias (V_{ds}) at a temperature T, is given by the following relation (for a single energy band [132]),

$$G_{1D} = \frac{2e^2}{h} \cdot \Big[1 + exp(\frac{E_b(V_{gs})}{k_BT})\Big]^{-1} \tag{4.4}$$

where h is the Planck's constant. Since Eq.(4.4) lacks any area description, G for 1D systems is no more a good method to extract S_{AA}.

The conductance measurement are performed at low temperature (T$\sim$ 40K-220K) [49] where phonon scattering is negligible. The undoped FinFET channel also results in negligible impurity scattering. Due to these experimental conditions and the devices, scattering has been neglected in the simulations. As a future work the effects of scattering could be investigated.

4.4.4 Results and Discussion

In this section the theoretical results as well as their comparison with the experimental data are provided.

3D vs. 1D system

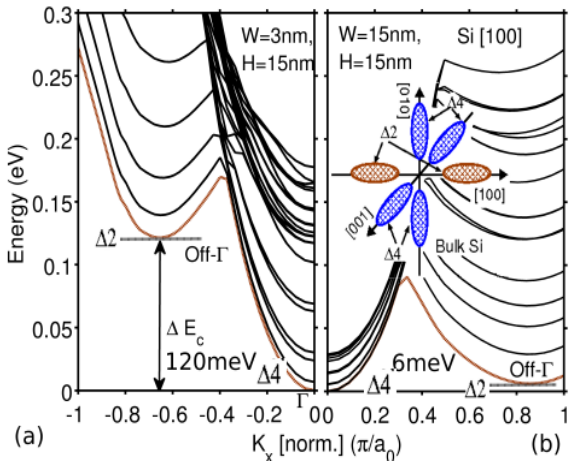

Fig. 4.13. Simulated conduction band E(k), using TB, for [100] Si channel with $H = 15$nm for (a) $W = 3$nm and (b) $W = 15$nm. The inset shows 6 equivalent bulk Si conduction band ellipsoids. The Δ_2 valleys (brown cigars) are along the transport direction [100] whereas the Δ_4 valleys (blue cigars) are in the quantized plane.

The conduction band structure (E(k)) can be utilized to distinguish a 1D system from a 3D system. The bulk silicon conduction band (CB) has 6 degenerate valleys (Δ_6) (see inset of Fig. 4.13 and Fig. 4.14) which split into 2 sets of degenerate valleys called the '$4-2$ *configuration*' ($\Delta_4 - \Delta_2$) for [100] and [110] 1D nanowires (NWs) due to the geometrical confinement [66]. In Si bulk the Δ_2 valleys are along the [100] direction. For a [100] Si nanowire channel the bulk Δ_2 valleys are projected along the channel axis away from the Γ point due to the folding of the Brillouin Zone (Fig. 4.13 a and b) [66]. The bulk Δ_4 valleys are projected at the Γ point [66]. The bandstructure of conduction band for silicon channel with $W = 3$nm and $H = 15$nm, and $W = H$

= 15nm is shown in Fig. 4.13 a and b, respectively. For [110] oriented Si channel the valley projection is different compared to the [100] channel. The CB minima is at the Off-Γ position as shown in Fig. 4.14. This happens due to the different atomic positions and geometrical confinement in [100] and [110] channels [66].

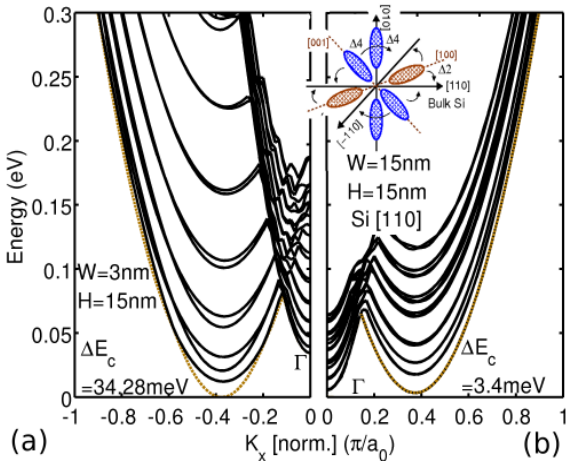

Fig. 4.14. Simulated conduction band E(k), using TB, for [110] Si channel with H = 15nm for (a) W = 3nm and (b) W = 15nm. The CB minima is at Off-Γ position for the thinner [110] Si channel. Inset shows the bulk Si 6 equivalent conduction valleys.

The energy separation between the Γ and Off-Γ valleys is given by,

$$\Delta E_c = E(\Gamma) - E(Off - \Gamma), \tag{4.5}$$

which gives a measure of how close (or far) a 1D NW system is from a 3D bulk system. The observation of a large ΔE_c value strongly points towards a 1D system, whereas a value close to zero points to a bulk system. Tight-binding simulations predict a ΔE_c value of around 120 meV for a [100] Si nanowire channel with W = 3nm and H = 15nm (Fig.4.13 a) while this value reduces to 6 meV for a Si nanowires channel with $W = H$ = 15nm (Fig. 4.13 b). For a [110] Si channel the ΔE_c value is around 34 meV for W = 3nm and H = 15nm (Fig.4.14 a) which reduces to 3.4 meV for W = 15nm and H = 15nm (Fig.4.14 b). This indicates that larger cross-section silicon channels are closer to the 3D bulk system for both [100] and [110] oriented channels.

The conduction band minimum (CBM) decreases with increasing channel width for both [100] and [110] SiNWs (Fig. Fig. 4.15 a). Also the ΔE_c value decreases with silicon channel width for a fixed height of 15nm ((Fig. 4.15 b). The ΔE_c value is negative for [110] channel since the Off-Γ valley is lower in energy compared to Γ valley. For $W > 15$nm the ΔE_c is less than 5 meV ($\leq k_b T_{300K}$) for both [100] and [110] Si channels. *This suggests that silicon channels with $W \geq 15$nm, and $H = 15$nm behave electrically close to the bulk Si system at room temperature.*

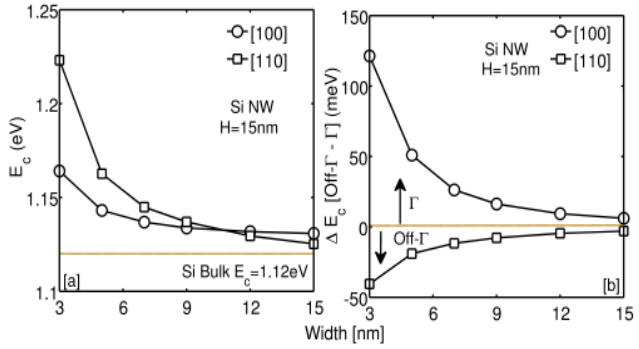

Fig. 4.15. (a) Variation of the conduction band minimum (E_c) for [100] and [110] oriented Si channels with width for a fixed height of 15nm. (b) The separation of the Δ_2-Δ_4 valleys with width (W) for rectangular [100] and [110] Si channel for a fixed height of 15nm.

Temperature dependence of E_b

The source-to-channel barrier height has been assumed to be temperature independent in the sub-threshold region. Figure 4.16 shows the results of a temperature dependent ToB calculations and proves that the barrier height (E_b) is only weakly temperature dependent. In the sub-threshold region, the E_b value for a device identical to FinFET C, is same at four different temperatures (T=140K, 200K, 240K and 300K). The variation with temperature becomes more prominent when the FinFET transitions into the ON-state. Thus, E_b has a weak temperature dependence in the sub-threshold region enabling the evaluation of E_b from the 300K simulations only.

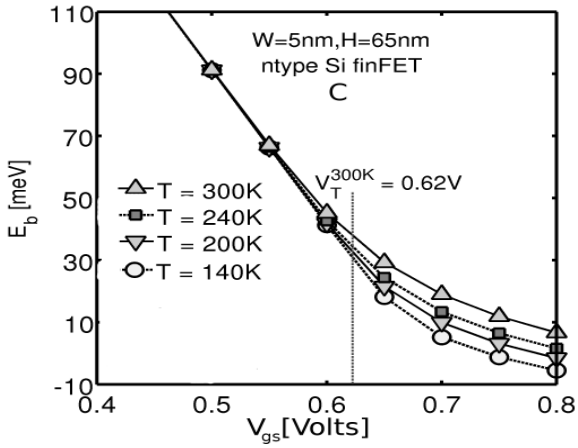

Fig. 4.16. Temperature dependence of the simulated barrier height (E_b) in n-FinFET C. At T=300K, V_T of the FinFET is 0.62V. The overlap of the curves at different temperatures with V_{gs}, below V_T at 300K, shows a weak temperature dependence of E_b in the sub-threshold region. The impact of temperature becomes prominent after V_{gs} goes above V_T.

Evolution of E_b and S with V_{gs}

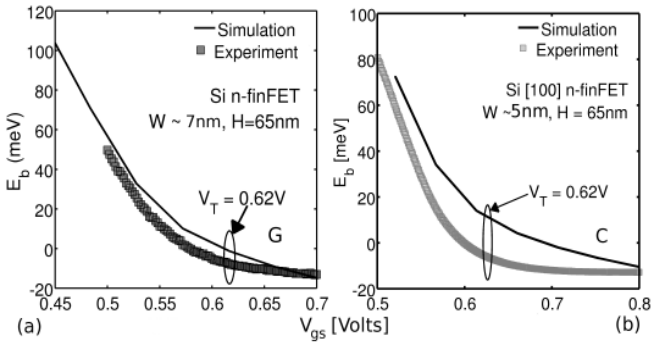

Fig. 4.17. Experimental and simulated barrier height (E_b) in n-FinFET (a) G and (b) C. Both the devices have same V_T. Both experiment and simulation show a decreasing value of E_b with V_{gs}, but the absolute values are different.

Experimentally, it has been shown that, for undoped silicon n-FinFETs [16], E_b reduces as V_{gs} increases. Theoretically, the E_b value is determined using Eq. (4.2) which

depends on the self-consistent channel potential (U_{scf}). As the gate bias increases, the channel can support more charge. This is obtained by pushing the channel CB lower in energy to be populated more by the source and drain Fermi level [66]. Figure 4.17 and 4.18 show the experimental and theoretical evolution of E_b in FinFETs G, C and D, E, respectively. Theory provides correct qualitative trend for E_b with V_{gs}. Few important observations here are, *(i) the theoretical E_b value is always higher than the experimental value and (ii) [110] Si devices (D and E) show a larger mismatch to the experimental values.* The reason for the first point is suggested to be the presence of interface traps in the FinFETs which screen the gate from the channel [16, 49]. The second observation can be understood by the fact that [110] channels with (110) sidewalls have higher interface trap density due to the higher surface bond density [131] and poor anisotropic etching of the (110) sidewalls [133, 134].

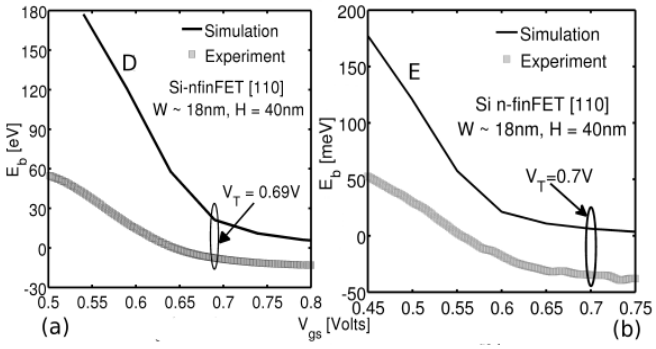

Fig. 4.18. Experimental and simulated barrier height (E_b) in n-FinFETs (a) D and (b) E. The devices have different V_T which is attributed to process induced variations. Both experiment and simulation shows a decreasing value of E_b with V_{gs}, but the absolute values are different.

The active channel area (S_{AA}) represents the part of the channel where the charge flows [16]. Experimentally S_{AA} is shown to be decreasing with gate bias since the inversion charge moves closer to the interface which electro-statically screens the inner part of the channel from the gate [16]. This gives a good indication of how much channel area is used for the charge transport. Figure 4.19 a and b show the

experimental evolution of S_{AA} in FinFET B and E, respectively. The theoretical value of S_{AA} decreases with V_{gs} which is in qualitative agreement to the experimental observation [16, 49]. However, the absolute values do not match. In fact theory over-estimates the experimental S_{AA} value (Fig. 4.19) which is attributed to the interface traps.

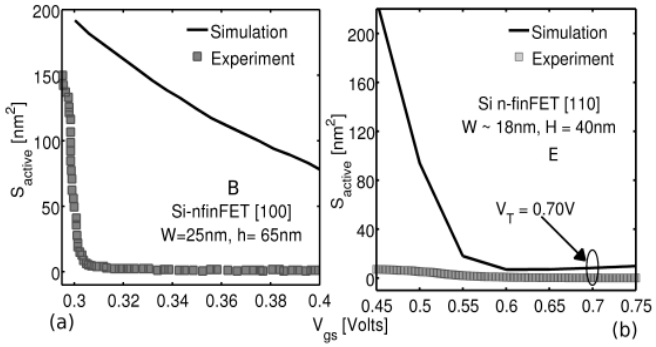

Fig. 4.19. Experimental and simulated channel active cross-section (S_{AA}) in n-FinFETs (a) B and (b) E. Both experiment and simulation show a decreasing value of S_{AA} with V_{gs}, but the absolute values are different. The simulated graph is for the same FinFET in both the cases, however, the V_{gs} ranges are different due to the different V_T of the experimental devices.

4.4.5 Summary of the work

The Top-of-the-barrier model, combined with Tight-binding calculations, explains very well the thermally activated sub-threshold transport in state-of-the-art Si FinFETs. The qualitative evolution of E_b and S with V_{gs} are well explained by the theory. The simulated values over-estimate the experimental values. The reason for this over-estimation could be due to the presence of interface traps in these Si n-FinFETs.

4.5 Interface trap extraction in undoped trigated Si n-FinFETs

Channel conductance measurements can be used as a tool to study thermally activated electron transport in the sub-threshold region of state-of-art FinFETs. Together with theoretical Tight-Binding (TB) calculations, this technique can be used to understand the dependence of the source-to-channel barrier height (E_b) and the active channel area (S_{AA}) on three important parameters, (i) the gate bias (V_{gs}), (ii) the temperature, and (iii) the FinFET cross-section size. The quantitative difference between experimental and theoretical values that was observed in the previous section can be attributed to the interface traps present in these FinFETs. Therefore, based on the difference between measured and calculated values of (i) S_{AA} and (ii) $|\partial E_b/\partial V_{gs}|$ (channel to gate coupling), two new methods of interface trap density (D_{it}) metrology are outlined. These two methods are shown to be very consistent and reliable, thereby opening new ways of analyzing in situ state-of-the-art multi-gate FETs down to the few nm width limit. Furthermore, theoretical investigation of the spatial current density reveal volume inversion in thinner FinFETs near the threshold voltage. The quantum mechanical simulations were done in OMEN-BSLAB and OMEN3D-par [71].

Qualitatively, similar theoretical and experimental trends for S_{AA} versus gate bias (V_{gs}) and E_b versus V_{gs} [16] are obtained. However, the theoretically obtained S_{AA} and E_b values quantitatively over-estimated the experimental values. The reduced experimental values can be attributed to the presence of interface traps in these FinFETs [16, 133–135]. The effect of interface traps on channel property are even more dominant in the extremely thin FinFETs [49]. This difference in S_{AA} and E_b has been utilized to directly estimate the interface trap density (D_{it}) in these FinFETs, thereby eliminating the need to implement special FinFETs geometries to determine D_{it} [133]. These methods now enable the direct implementation of interface trap density metrology in state-of-the-art undoped Si n-FinFETs.

The trap extraction method outlined in this section is new and different from the older trap extraction techniques such as C-V, charge pumping and inductance methods [133,136]. The older methods rely of special structures like the gated diodes [133] and large capacitors. However, the final FinFETs used in the circuits undergo different process steps like extra etching, deposition, higher thermal budgets, etc. These processes result in different interface quality in the final FETs compared to the test structures. Thus, older methods cannot provide correct D_{it} information in the final FETs. The methods presented in this work overcome this limitation by carefully analyzing the experimental measurements and comparing the data with simulation, thus, enabling the extraction of the trap density in the final FET structures.

4.5.1 Trap extraction methods

In Ref. [16] it was observed that the active cross-section area ($S_{AA,sim}$) obtained theoretically was an over-estimation of the experimental value ($S_{AA,exp}$). In the results section it will be further shown that also the theoretical E_b value can over estimate the experimental E_b value. These mismatches can be attributed to the presence of traps at the oxide-channel interface of multi-gate FETs where these traps can enhance the electrostatic screening and suppress the action of the gate on the channel [16,49,133,134]. This simple idea is a powerful tool used for the estimation of interface trap density (D_{it}) in these undoped Si n-FinFETs.

Method I: D_{it} from active area

Based on the difference between the simulated and the experimental active area (S_{AA}) values, a method to calculate the density of interface trap charges, σ_{it}, in the FinFETs is outlined. The method is based on the assumption that the total charge in the channel at a given V_{gs} must be the same in the experiments and in the simulations. This requirement leads to the following,

$$S_{AA,sim} \cdot L_{ch} \cdot \rho_{sim} = S_{AA,expt} \cdot L_{ch} \cdot \rho_{expt} + e \cdot \sigma_{it} \cdot L_{ch} \cdot P \tag{4.6}$$

where $S_{AA,sim}$ ($S_{AA,expt}$) is the simulated (experimental) active area, P is the perimeter of the channel under the gate ($P = W + 2H$) and ρ_{sim} (ρ_{expt}) is the simulated (experimental) charge density. By applying Gauss's law at the oxide channel interface, ρ_{expt} is obtained from ρ_{sim} and σ_{it} as,

$$\rho_{expt} = \rho_{sim} - \rho_{it} = \rho_{sim} - (e \cdot \sigma_{it} \cdot P)/(W \cdot H) \tag{4.7}$$

Using (4.6) and (4.7) the final expression for σ_{it} is obtained as,

$$\begin{aligned} \sigma_{it}(V_{gs}) &= \frac{\rho_{sim}(V_{gs}) S_{AA,sim}(V_{gs})}{e \cdot P} \\ &\times \left[\frac{\left[1 - \frac{S_{AA,expt}(V_{gs})}{S_{AA,sim}(V_{gs})}\right]}{\left[1 - \frac{S_{AA,expt}(V_{gs})}{W \cdot H}\right]} \right] \quad [\#/cm^2] \end{aligned} \tag{4.8}$$

This method is useful for wider devices for which Eq.(4.3) is valid. For very thin FinFETs (close to a 1D system) this method cannot be utilized .

Assumptions in Method I: The extra charge contribution completely stems from the interface trap density (D_{it}) and any contribution from the bulk trap states has been neglected. All the interface traps are assumed to be completely filled which implies $\sigma_{it} \cong D_{it}$. The interface trap charges are assumed to be situated very close to the oxide-channel interface for Eq.(4.7) to be true. Also the interface trap density is assumed to be constant and identical for the top and the side walls of the FinFET which is generally not the case [133, 134]. This method of extraction works best for undoped channel since any filling of the impurity/dopant states is neglected in the calculation. Surface orientation dependent D_{it} for different surfaces could be included as a further refinement.

Method II: D_{it} from barrier control

The second method does not utilize the E_b value directly but its derivative w.r.t V_{gs}. The term $\alpha = |\partial E_b/\partial V_{gs}|$ represents the channel to gate coupling [16]. The presence of interface traps weakens this coupling due to the electrostatic screening. This method of trap extraction is based on the difference in the experimental and the simulated α value. The α value can be represented in terms of the channel and the oxide capacitance. The equivalent capacitance model for a MOSFET with and without interface traps (D_{it}) is shown in Fig.4.20.

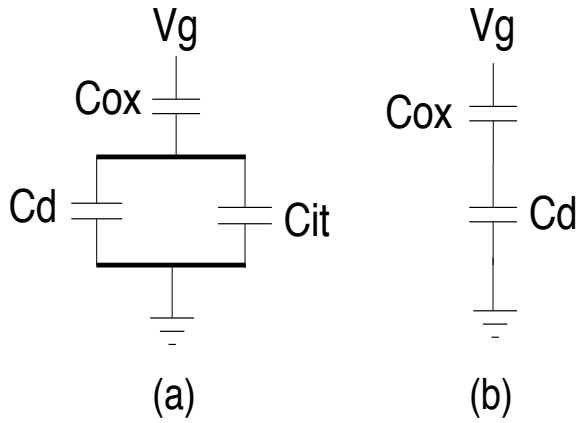

Fig. 4.20. Equivalent circuits (a) with interface-trap capacitance (C_{it}) and (b) without interface capacitance. C_d and C_{ox} are the depletion and the oxide capacitance, respectively. The idea for this equivalent circuit is obtained from page 381 in Ref. [131].

The α value can be associated to the oxide, interface and semiconductor capacitance which is given in Eq.(38) on page 383 in Ref. [131]. This leads to the following relation,

$$|\frac{\partial E_b}{\partial V_{gs}}| = 1 - \frac{C_{tot}}{C_{ox}}, \tag{4.9}$$

where C_{tot} is the total capacitance. For the two cases, as shown in Fig.4.20, the total capacitance is given by,

$$C_{tot}^{exp} = \frac{C_{ox} \cdot (C_d + C_{it})}{C_d + C_{ox} + C_{it}}, \tag{4.10}$$

$$C_{tot}^{sim} = \frac{C_d \cdot C_{ox}}{C_d + C_{ox}}, \tag{4.11}$$

where C_{it}, C_{ox} and C_d are the interface trap capacitance, the oxide capacitance and the semi-conductor capacitance, respectively. Eq. (4.10) represents the capacitance in the experimental device and Eq. (4.11) represents the capacitance in the simulated device under ideal conditions without any interface traps. Combining Eq. (4.9), (4.10) and (4.11) and after some mathematical manipulations, results in,

$$\frac{1}{\alpha_{exp}} = \frac{1}{\alpha_{sim}} + \frac{C_{it}}{C_{ox}}, \tag{4.12}$$

Manipulating Eq. (4.12) gives the following relation for C_{it},

$$C_{it} = C_{ox} \cdot \Big(\frac{1}{\alpha_{sim}}\Big) \cdot \Big[\frac{\alpha_{sim}}{\alpha_{exp}} - 1\Big] \tag{4.13}$$

Also C_{it} can be related to the interface charge density (σ_{it}) as [131],

$$C_{it} = e \cdot \frac{\partial \sigma_{it}}{\partial V_{gs}}. \tag{4.14}$$

In Eq. (4.13) all the values are dependent on V_{gs} except C_{ox}. Combining Eq. 4.13 and 4.14 and integrating w.r.t V_{gs} yields the final expression for the integrated interface charge density in these FinFETs as,

$$\sigma_{it} = \frac{C_{ox}}{e} \cdot \int_{V1}^{V2=V_T} \Big(\frac{1}{\alpha_{sim}(V_{gs})}\Big) \times \Big[\frac{\alpha_{sim}(V_{gs})}{\alpha_{exp}(V_{gs})} - 1\Big] dV_{gs} \;\; [\#/cm^2], \tag{4.15}$$

where V_T is the threshold voltage of the FinFET and V1 is the gate under-drive. Thus, V1 and V2 is the integration range for Eq. (4.15) in the sub-threshold region. The second method derived from barrier control has the advantage that it is independent of the dimensionality of the FinFET. Hence, Eq. (4.15) can be used for wide as well as thin FinFETs.

Assumptions in Method II: The most important assumption is that the rate of change of the surface potential ($\Psi(V_{gs})$) is the same as E_b w.r.t V_{gs}. The extra charge contribution completely originates from the density of interface trap charges (σ_{it}) and any contribution from the bulk trap states have been neglected. Also all the interface traps are assumed to be completely filled which implies $\sigma_{it} = D_{it}$. This method works best when the change in the DC and the AC signal is low enough, such that the interface traps can follow the change in the bias sweep [131] .

4.5.2 Limitations of the methods

It is important to understand the limitations of the new trap metrology methods to apply them properly. One of the main limitation is how closely the simulated FinFET structure resembles the experimental device structure. This depends both on the SEM/TEM imaging as well the sophistication of the model. In the present case the FinFET cross-section structure was created using the TEM image making the simulated structure as close to the experimental device as possible. With the development of better TCAD tools, the proximity of the simulated structure to experimental structure has increased. The physical device model needs to comprehend the crystal directions, atomistic details, strain and gating realistically to realize the working of the nano-scale FETs. Effective mass models fail to properly represent the bandstructure in these type of ultra-scaled nanowires/FinFETs [137]. The model enables the calculation of theoretical conductance value with good confidence to be used in the trap calculation. Furthermore, the calculated G is assumed as close to ideal as possible and all the difference between the ideal and experimental G is attributed to the traps which may not be true always. An important difference between the two methods is that they are calculated over different V_{gs} ranges. This is important since the trap filling and their behavior changes with V_{gs} range which should be taken into account accurately. One must also be aware of the embedded assumption of complete interface trap filling and the neglect of the bulk traps in the gate dielectric.

4.5.3 Results and Discussion

In this section the results on the interface trap density (D_{it}) in the undoped Si n-FinFETs are presented.

D_{it} using S_{AA}: Method I

The calculated D_{it} values for FinFET B and E are 1.02e12cm^{-2} and 1.81e12cm^{-2} (Fig.4.21 a and b, respectively). The D_{it} values compare quite well with the experimental D_{it} values presented in Ref. [133] and also shown in Table 4.3. As expected the D_{it} value for FinFET E (with [110] channel and (110) sidewalls) is higher than FinFET B ([100] channel with (100) sidewalls). This is attributed to the higher D_{it} ($\sim 2\times$) on the (110) surfaces [133, 134]. The results show $\sim 1.8\times$ more D_{it} for (110) sidewalls, in close agreement to the experiments. This method allows to obtain the D_{it} in the actual FinFETs rather than custom made FETs.

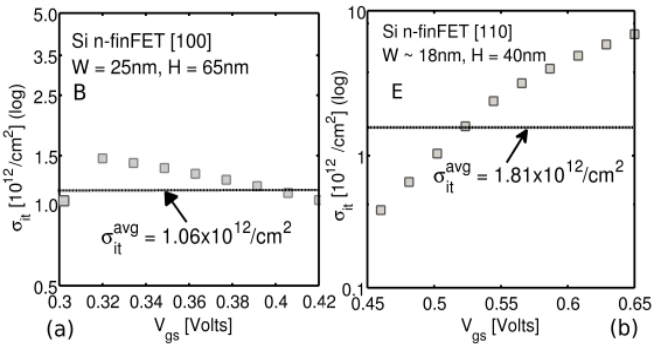

Fig. 4.21. Extracted trap density using the difference in active device area (method I) for n-FinFETs (a) B and (b) E.

D_{it} using $|\partial E_b/\partial V_{gs}|$: Method II

The C_{ox} value needed in this method is taken as $\sim$0.0173 F/m^2 which is assumed to be the same for all the devices since these FinFETs have similar oxide thickness.

The calculated D_{it} values for FinFET C and D are 9.26e11cm^{-2} and 1.563e12cm^{-2} (Fig.4.22 a and b, respectively). These calculations also show that the [110] channel device (FinFET E) shows a higher D_{it} compared to the [100] channel device (FinFET C), again consistent to the observations made in Ref. [133]. The advantage of this method is that it can be used to obtain D_{it} in extremely thin FinFETs (close to 1D system) unlike method I which is applicable only to wider FinFETs (due to the reasons discussed in Sec. 4.4.3).

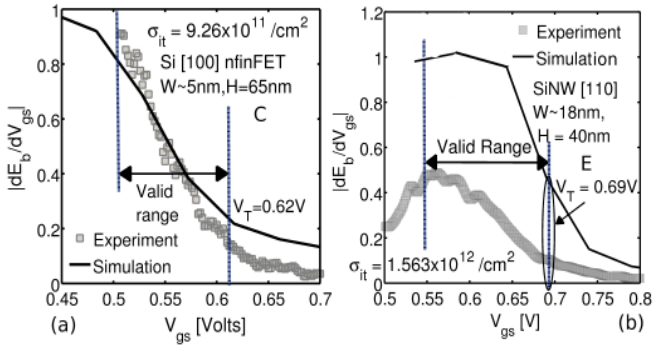

Fig. 4.22. Experimental and simulated value of α in n-FinFETs (a) C and (b) E.

Discussion on the two methods and D_{it} trends

The D_{it} values for all the FinFETs used in this study are shown in Table 4.3. The important outcomes about the two methods are outlined below:

- The D_{it} values obtained by the two methods compare very well with the experimental measurement in Ref. [133] for similar sized FinFETs (A and B), demonstrating the validity of these new methods.
- The D_{it} values calculated using method I and II (for B and E) compare very well with each other which shows that the two methods are complimentary [49] for large cross-section devices.

- The D_{it} values calculated for the two similar FinFETs (D and E) compare very well showing the reproducibility of the methods [49].

The calculated D_{it} values also reflect some important trends about the FinFET width scaling and surfaces (Table 4.3). The central points are :

- Hydrogen passivation considerably reduces D_{it} [135]. This is observed for FinFETs A and B where H_2 passivation results in $\sim 2\times$ less D_{it} in FinFET A [49].
- Width scaling requires more etching which also increases D_{it} [133, 134]. The same trend is observed in devices A to C and D to F (decreasing W).
- (110) sidewalls show higher D_{it} compared to (100) sidewalls [133]. The same trend is also observed for FinFETs A, B, C, G ((100) sidewall) compared to FinFETs D, E and F ((110) sidewall).

Table 4.3
Values of D_{it} obtained from all the n-FinFETs as well as from Ref. [133].

Device	Method	D_{it} ($10^{11} cm^{-2}$)	FET type	Observations
L=140nm [133]	Charge	1.725	Special body	–
L = 240nm [133]	Pumping	2.072	tied FET	–
A	I	5.560	Std. FET	H_2 anneal, reduces D_{it}
B	I	10.60	Std. FET	
	II	8.860	Std. FET	
C	II	9.26	Std. FET	Thin fin, more D_{it}
D	II	18.31	Std. FET	(110) side-wall, thin fin, more etching, more D_{it}
E	I	18.1	Std. FET	
	II	15.3	Std. FET	
F	II	36.3	Std. FET	
G	II	4.33	Std. FET	H_2 anneal, less D_{it}

4.5.4 Summary of the work

The systematic mismatch in the experimental and theoretical values of E_b and S_{AA} led to the development of two new interface trap density metrology schemes. The advantage of these schemes is that they do not require any special MOSFET structure as needed by the present experimental methods allowing to probe the interface quality of the ultimate channel. These methods are shown to provide consistent and reproducible results which compare very well with the independent experimental trap measurement results. The calculated trends of interface trap density with channel width scaling, channel orientation and hydrogen passivation of the surfaces show a good correlation with the experimental observations.

4.6 Summary and Outlook

The ToB model with Tight-binding is very useful in describing the experimental results in the ultra-scaled transistors. The CV calculations in gate-all-around Si nanowire MOSFETs and in bulk SiGe pMOSFETs shows the strength and the expansive nature of the modeling provided by these models. The use of accurate atomistic modeling is reemphasized by the correct trends of E_b and S_{AA} in ultra-scaled Si trigated n-FinFETs. Two new trap charge density metrology methods in ultra-scaled Si n-FinFETs are also presented which will be very useful for future generation transistors.

5. THEORY OF THERMAL TRANSPORT AT THE NANO-SCALE

5.1 Introduction

Many of the modern day semiconductor applications are based on the miniaturized devices. An integral part of the design is to understand the impact of dimensional scaling and nano-alloying on thermal transport. Lattice thermal conductivity (κ_l) is an important design parameter for new materials and devices [138]. Depending on the type of application the required value of κ_l can be either large or small. For example, in scaled MOSFETs heating is becoming a major problem since heat flow gets obstructed by small dimensions [139–141]. At the same time the thermoelectric devices require smaller κ_l in order to reduce the heat flow leading to larger thermal gradients which can allow for better interconversion of heat and electricity [142] (Fig. 5.1).

The work in this chapter mainly focuses on the thermal transport in semiconductor systems, where heat is carried by the lattice vibrations known as 'phonons' [143–145]. The phonons show a variation in energy based on the system frequency which results in the phonon-dispersion of the solids [146]. Depending on the temperature and system size the mean-free path of the phonons (λ_{ph}) may vary from 1-300nm [142,147]. Present fabrication methods can be used to manufacture devices which are 10 to 100nm in size, thus, making them comparable to λ_{ph}. This clearly requires looking beyond the classical heat flow such as Fourier law since the heat transport can change from the particle nature to wave nature, from diffusive to radiative in these length scales. The present chapter focuses on two themes, (i) an atomistic way of capturing the phonons using an inter-atomic potential method [50, 146, 148], and (ii) using

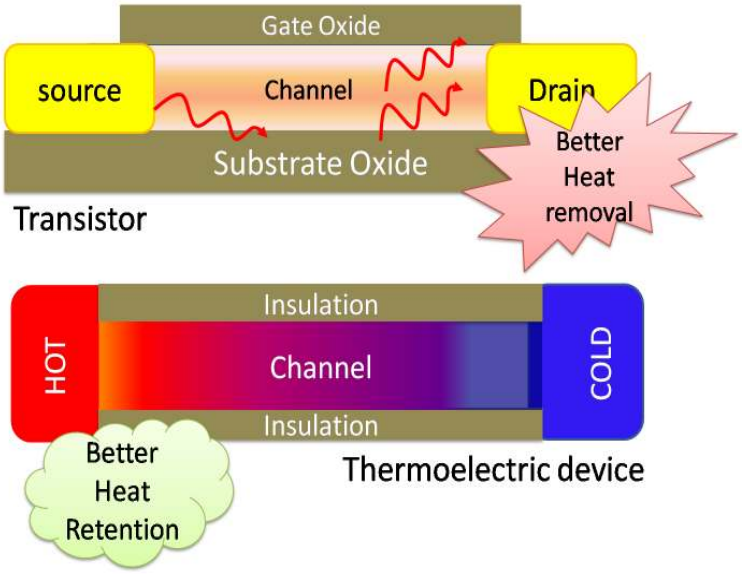

Fig. 5.1. The contrasting requirement of thermal management in nano-scale devices. Transistors need better heat removal for faster operation whereas thermoelectric devices require lower thermal loss to maintain temperature gradient for better inter-conversion of heat and electricity.

Landauer's [51, 138] and Green's function [149–153] method to calculate the thermal transport in nano-scale devices such as nanowires and superlattices.

This chapter is arranged in the following sections. The first half of the chapter deals with the calculation of phonons using Modified Valence Force Field (MVFF) model in zinc-blende semiconductors while the second half solves thermal transport using the dynamical matrix (DM) obtained in the first half. The MVFF theory for calculating the phonon dispersion in zinc-blende semiconductors is covered in Sec. 5.2 which encompasses the details on the total potential energy (U) of the crystals in the MVFF model, construction of the DM and salient features of the DM. The computational details for the calculation of phonon dispersion are presented in Sec.5.3. Details on the thermal transport using Green's function is covered in Sec. 5.4.1. Details on the Landauer's model is presented in Sec. 5.4.2. The details on the calculation of physical and thermal properties in solids using phonons are outlined

in Sec. 5.5. Section 5.6 provides the results on the application of the MVFF model to bulk and nanowires. Numerical comparison of Landauer's model with Green's function is given in Sec. 5.7. Summary and outlook are in Sec.5.8.

5.2 Modeling of phonon dispersion

Phonons are crucial in determining many important properties in semiconductors such as, (1) the determination of the phonon limited low field carrier mobility in MOSFETs [154], (2) the knowledge of the lattice thermal conductivity in semiconductors which plays an important role in thermoelectric design [138, 153, 155], and (3) the structural stability of ultra-thin semiconductor nanowires which have a variety of applications [156]. Thus, a proper method to calculate the phonon dispersion in semiconductors is required. A complete and elaborate description of the MVFF phonon model [50, 157] is presented in this section along with applications to bulk and nanowire structures.

A variety of methods have been reported in the literature for the calculation of the phonon spectrum like the Valence Force Field (VFF) method and its variants [50,146,157,158], Bond Charge Model (BCM) [148,159], Density Functional Methods [151, 156], etc. The main reasons for using the VFF model are, (a) in crystals where covalent bonding is important (like Si, Ge, GaAs), simple VFF potentials are sufficient to match the experimental data [158,160], (b) valence coordinates depend only on the relative positions of the atoms and is independent of rigid translations and rotations of the solid which makes the potential energy (U) invariant, and (c) it is easy to extend the model to ultra-scaled structures made of few atoms with surfaces since the interactions are at the atomic level.

5.2.1 Modified VFF theory

The starting point for modeling the phonons is to obtain the equation of motion for atomic vibrations in the system. Since MVFF is a crystalline model, the dynamical equation for each atom 'i' can be written as,

$$m_i \frac{\partial^2}{\partial t^2}(\Delta R_i) = F_i = -\frac{\partial U}{\partial(\Delta R_i)} \tag{5.1}$$

where, ΔR_i, F_i and U are the vibration vector of atom 'i', total force on atom 'i' in the crystal, and the potential energy of the crystal respectively. Eq. (5.1) indicates that the calculation of the vibrational frequencies requires the estimation of the potential energy in the system. The MVFF method [50,146,157] approximates U based on nearby atomic interactions (short-range) [50, 157] as shown for a zinc-blende (or diamond) crystal,

$$\begin{aligned} U \approx \frac{1}{2}\sum_{i\in N_A}\Bigg[& \sum_{j\in nn(i)} U_{bs}^{ij} + \sum_{j,k\in nn(i)}^{j\neq k}\big(U_{bb}^{jik} \\ & + U_{bs-bs}^{jik} + U_{bs-bb}^{jik}\big) + \sum_{j,k,l\in COP_i}^{j\neq k\neq l} U_{bb-bb}^{jikl}\Bigg] \end{aligned} \tag{5.2}$$

where N_A, $nn(i)$ and COP_i represent the total number of atoms in one unitcell, number of nearest neighbors for atom 'i' and the coplanar atom groups for atom 'i' respectively. The first two terms in Eq.(5.2) are from the original KVFF model [146]. The other interaction terms are needed for the accurate matching of the phonon dispersion in the entire BZ. U_{bs}^{ij} and U_{bb}^{jik} represent the elastic energy from bond stretching and bending between the atoms connected to each other (Fig. 5.2a,b). U_{bs-bs}^{jik}, U_{bs-bb}^{jik} and U_{bb-bb}^{jikl} represent the cross bond stretching [50], cross bond bending-stretching [157] and coplanar bond bending [50] interaction respectively (Fig. 5.2 c,d,e).

The functional dependence of each interaction term on the atomic positions are given by,

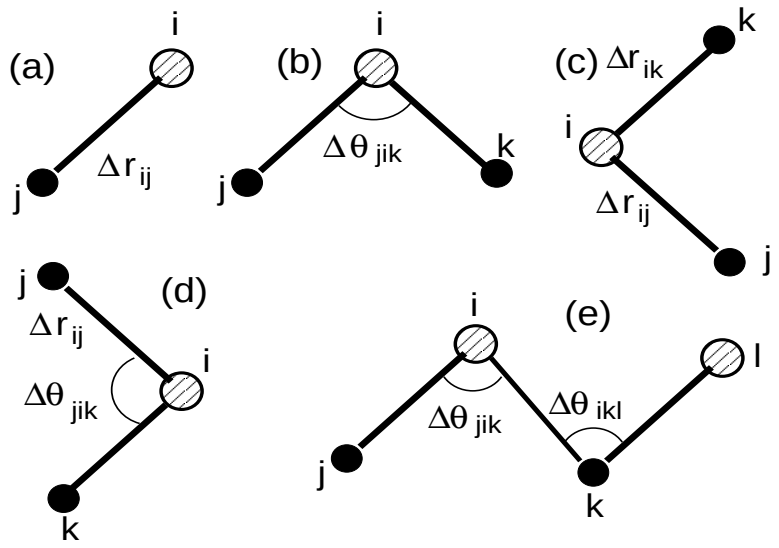

Fig. 5.2. The short range interactions used for the calculation of phonon dispersion in zinc-blende semiconductors.(a) bond stretching (b) bond bending (c) cross bond stretching (d) cross bond bending-stretching, and (e) coplanar bond bending interaction.

$$U_{bs}^{ij} = \frac{3}{8}\alpha_{ij}\frac{(r_{ij}^2 - d_{ij,0}^2)^2}{\|d_{ij,0}^2\|} \tag{5.3}$$

$$U_{bb}^{jik} = \frac{3}{8}\beta_{jik}\frac{(\Delta\theta_{jik})^2}{\|d_{ij,0}\|\|d_{ik,0}\|} \tag{5.4}$$

$$U_{bs-bs}^{jik} = \frac{3}{8}\delta_{jik}\frac{(r_{ij}^2 - d_{ij,0}^2)(r_{ik}^2 - d_{ik,0}^2)}{\|d_{ij,0}\|\|d_{ik,0}\|} \tag{5.5}$$

$$U_{bs-bb}^{jik} = \frac{3}{8}\gamma_{jik}\frac{(r_{ij}^2 - d_{ij,0}^2)(\Delta\theta_{jik})}{\|d_{ij,0}\|\|d_{ik,0}\|} \tag{5.6}$$

$$U_{bb-bb}^{jikl} = \frac{3}{8}\sqrt{(\nu_{jik}\nu_{ikl})}\frac{(\Delta\theta_{jik})(\Delta\theta_{ikl})}{\sqrt{\|d_{ij,0}\|\|d_{ik,0}^2\|\|d_{kl,0}\|}} \tag{5.7}$$

where $\Delta\theta_{jik} = r_{ij} \cdot r_{ik} - d_{ij,0} \cdot d_{ik,0}$. The term r_{ij} ($d_{ij,0}$) are the non-ideal (ideal) bond vectors from atom 'i' to 'j'. The terms α, β, δ, γ and ν determine the strength of the interactions used in the MVFF model (like spring constants). These are used as parameters optimized to reproduce the bulk phonon dispersion [50, 157, 160]. The value of these strength parameters also change according to the deviation of the bond

length and bond angle from their ideal values. This allows to capture the anharmonic properties of the lattice vibrations [161] (hence, MVFF is sometimes referred to as the 'quasi-harmonic' model). The empirical functional dependence of each strength parameter on the bond length and bond angle are provided in Ref. [50].

Interaction Terms: The bulk primitive unitcell used for phonon calculation is made of two atoms (anion-cation pair for zinc-blende and 2 similar atoms for diamond lattice). The black dotted box with atom 1 and 2 represent the bulk unitcell in Fig. 5.3. The total number of terms in each interaction (Eq.(5.3-5.7)) for a bulk unitcell are provided in Table 5.1. Except for the coplanar bond bending interaction [50] all the other terms involve the nearest neighbor interactions . There are 24 coplanar (COP) groups present in a bulk zinc-blende unitcell which are needed for the calculation of the phonon dispersion. For clarity some of the representative COP groups in a bulk unitcell are shown in Fig. 5.3. Each group consists of 4 atom arranged as anion(A)-cation(C)-anion(A)-cation(C) (eg. 1(A)-2(C)-3(A)-4(C) in Fig. 5.3). The details of the coplanar interaction groups are provided in Appendix A.

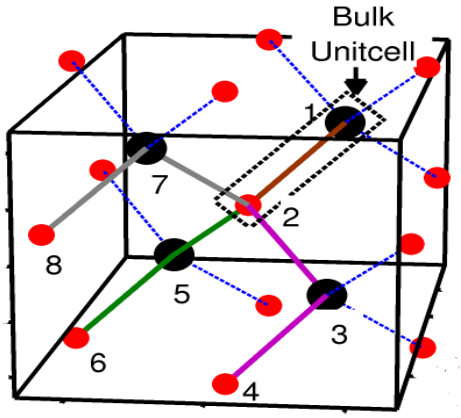

Fig. 5.3. Three co-planar atom groups (out of 24) shown in a bulk zinc-blende unitcell. The groups are (i) 1-2-3-4, (ii) 1-2-5-6, and (iii) 1-2-7-8. Atoms 1 and 2 make the bulk unitcell used in the calculations. Red (black) atoms are cations (anions).

Table 5.1
Number of terms in different interactions of MVFF model in a bulk zinc-blende unitcell (anion-cation pair)

Interaction Type	Total terms (anion+cation)
Bond stretching (bs)	8
Bond bending (bb)	12
Cross bond stretching (bs-bs)	12
Cross bond stretch-bend (bs-bb)	12
Coplanar bond bending (bb-bb)	24

5.2.2 The Dynamical Matrix (DM)

The dynamical matrix captures the dynamics of the atoms in a given system. In this section the structure of this matrix is discussed. The derivation of the DM from the equation of motion (Eq. (5.1)) is given in Appendix B. The DM calculation is based on the harmonic approximation (see Appendix B). For the interaction between two atoms 'i' and 'j', the DM component at atom 'i' is given by,

$$D(ij) = \begin{bmatrix} D^{ij}_{xx} & D^{ij}_{xy} & D^{ij}_{xz} \\ D^{ij}_{yx} & D^{ij}_{yy} & D^{ij}_{yz} \\ D^{ij}_{zx} & D^{ij}_{zy} & D^{ij}_{zz} \end{bmatrix} \tag{5.8}$$

where, any component of $D(ij)$ is given by,

$$\begin{aligned} D^{ij}_{mn} &= \frac{\partial^2 U}{\partial r^i_m \partial r^j_n} \\ & \quad i, j \in N_A \quad \text{and} \quad m, n \in [x, y, z], \end{aligned} \tag{5.9}$$

where N_A is the total number of atoms in the unitcell. For each atom the size of $D(ij)$ is fixed to 3×3. For N_A atoms in the unitcell the size of the dynamical matrix is $3N_A \times 3N_A$. However, the matrix is mostly sparse. The details of sparsity pattern, fill factor, etc. are discussed in Sec. 5.3.

Symmetry considerations in the DM: Under the harmonic approximation the dynamical matrix has special symmetry in its calculation which can be readily utilized to reduce the assembly time. From software development point of view this will be crucial in optimizing both storage and compute time. The continuous nature of the potential energy U leads to,

$$D^{ij}_{mn} = \frac{\partial^2 U}{\partial r^i_m \partial r^j_n} = \frac{\partial^2 U}{\partial r^j_n \partial r^i_m} = D^{ji}_{nm} \tag{5.10}$$

A closer look at Eq.(5.10) shows the following symmetry relation,

$$D(ij) = D(ji)' \quad \forall i \neq j \tag{5.11}$$

This reduces the total number of calculations required for constructing the dynamical matrix and speeds up the calculations. Also if the matrix is stored for repetitive use, then only one of the symmetry blocks need to be stored. This will reduce the memory requirement in the software. Further reduction in construction time of DM can be achieved depending on the type of interaction being solved, the implementation details of the software and the symmetry of the crystal (not covered in this work, see Ref. [162] for discussion).

5.2.3 Boundary conditions (BC)

To calculate the eigen modes of lattice vibration it is important to apply proper boundary conditions to the DM. In the case of bulk material, the unitcell has periodic (Born-Von Karman) boundary condition along all the directions (x,y,z) [50, 159] since the material is assumed to have infinite extent in every direction. However, for nanostructures the boundary conditions are different due to the finite extent of the material along certain directions. The boundary conditions vary depending on the dimensionality of the structure (1D, 2D or 3D see Table 5.2) for which the dynamical matrix is constructed. Boundary conditions are typically of two types; (i) Periodic Boundary condition (PBC) and (ii) Clamped/Free boundary conditions (CBC) (de-

pends how freely the surface atoms move). Table 5.2 provides the boundary condition details depending on the dimensionality of the structure used for phonon calculation.

Table 5.2
Boundary condition (BC) in DM based on the dimensionality of the structure

Dimensionality	Periodic BC	Clamped/Free BC
Bulk (3D)	3	0
Thin Film (2D)	2	1
Wire (1D)	1	2
Quantum Dot (0D)	0	3

Application of PBC has been provided in many papers [50,157,159]. The boundary conditions associated with geometrically confined nanostructures other than PBC are discussed here. The vibrations of the surface atoms can vary from completely free (Free BC) to damped oscillations (damped BC). It is shown next that all these cases can be handled within one single boundary condition.

Boundary conditions for nanostructures: The surface atoms (Fig. 5.4, hollow atoms) of the nanostructures can vibrate in a very different manner compared to the inner atoms (Fig. 5.4, filled atoms) since the surface atoms have different number of neighbors and ambient environment compared to the inner atoms. The degree of freedom of the surface atoms can be represented by a direction dependent damping matrix Ξ, defined in Eq.(C.1.1). In such a case the dynamical matrix component between atom 'i' and 'j' ($D(ij)$) modifies to,

$$\tilde{D}(ij) = \Xi^i D(ij) \Xi^j \tag{5.12}$$

The details of the calculation are provided in Appendix C.

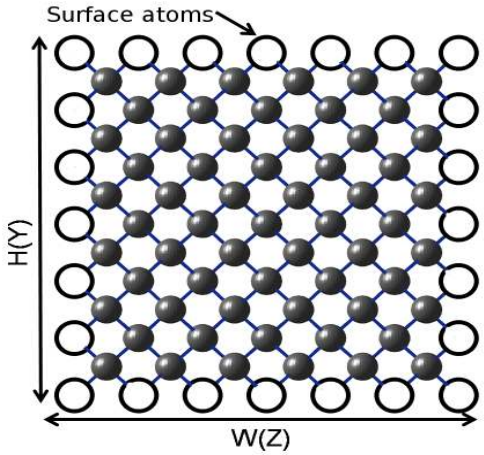

Fig. 5.4. Projected unitcell of a [100] oriented rectangular SiNW shown with surface (hollow) and inner (gray filled) atoms.

5.2.4 Diagonalization of the dynamical matrix

After setting up the dynamical matrix with correct boundary conditions the following eigen value problem is solved,

$$DQ(p,q) = M\omega^2(p,q)Q(p,q), \tag{5.13}$$

where, M is the atomic mass matrix. The terms p and q are the phonon polarization and momentum vector, respectively. The term $Q(p,q)$ is the column vector comprising of phonon eigen displacement modes ($u(p,q)$) associated with polarization p and momentum q. Modifying Eq.(5.13) slightly for numerical calculations leads to,

$$\overline{D}Q(p,q) = \omega^2(p,q)Q(p,q) \tag{5.14}$$

The details for obtaining $\overline{D}$ is outlined in Appendix D. To obtain Eq.(5.14) another step is needed. Time dependent vibration of each atom ($\Delta R(t)$) can be represented by the linear combination of phonon eigen modes of vibration $u(p,q)$ (a complete basis set) as,

$$\Delta R_i(t) = \sum_P u_P(p,q)e^{i(q\cdot R_i - \omega t)} \tag{5.15}$$

where, P is the size of the basis set. The term ω is the vibration frequency of the modes. Using the result of Eq.(5.15) in the LHS of Eq.(5.1) yields,

$$m_i \frac{\partial^2}{\partial t^2} \Delta R_i(t) = -\omega^2 \sum_P u_P(p,q) e^{i(q \cdot R_i - \omega t)} \tag{5.16}$$

After some mathematical manipulation and using Eq.(5.13) the final eigen value problem is obtained as given in Eq.(5.14).

5.2.5 Summary of the work

A detailed theoretical development of the MVFF model is presented. The present model is different from the Keating's VFF model due to the extra terms used. These terms are needed for the correct representation of the phonon dispersion in the entire BZ.

5.3 Computational Details of the MVFF model

This section provides the computational details involved in obtaining the phonon dispersion in semiconductor structures. Details about bulk and nanowire (NW) structures are provided.

5.3.1 Dynamical matrix details

A primitive bulk zinc-blende unitcell has 2 atoms. This fixes the size of the DM for the bulk structure to 6 $\times$ 6 ($3N_A \times 3N_A$) as reported in Sec.5.2.2). However, for the case of nanowires, N_A varies with shape, size and orientation of the wire [151]. In the present work, all the results are for square shaped SiNW with [100] orientation. Figure 5.5 shows the variation in N_A with the width (W) of SiNW. The number of atoms increase quadratically with W. For a 6nm $\times$ 6nm SiNW, N_A is 1013 which means the size of DM is 3039 $\times$ 3039. Extrapolating the N_A data gives around 7128 atoms for a 16nm $\times$ 16nm SiNW resulting in a DM of size 21384 $\times$ 21384 (details

in Appendix E). So, the dynamical matrix size increases rapidly with the increase in the width.

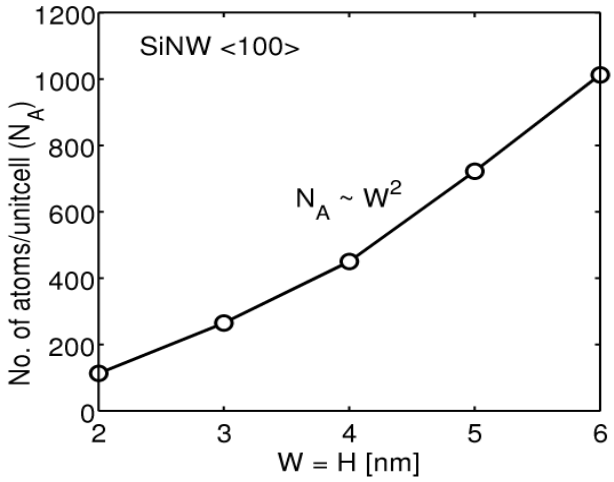

Fig. 5.5. Number of atoms per unitcell (N_A) with width (W) of [100] oriented square SiNW.

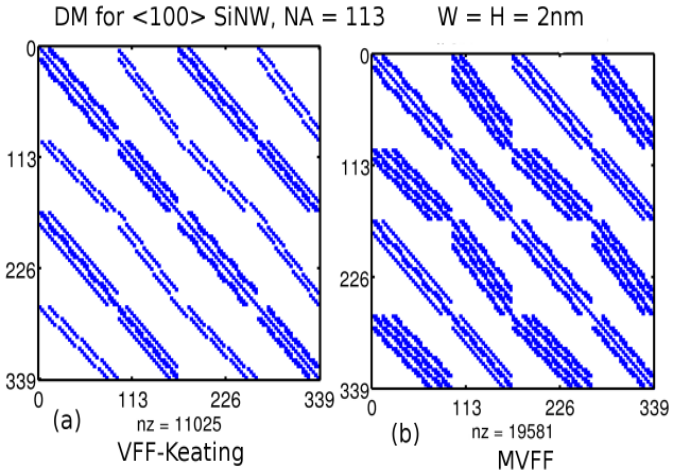

Fig. 5.6. Sparsity pattern of the dynamical matrix used in (a) the Keating VFF model, and (b) the MVFF model. SiNW has W = H = 2nm with 113 atoms in the unitcell.

Increasing DM size with wire cross-section puts constraint on the structure size which can be solved using the atomistic MVFF method. However, the entire matrix

is quite sparse. The qualitative idea about the filling can be observed from the sparsity pattern for a 2nm × 2nm SiNW dynamical matrix as shown in Fig. 5.6. The quantitative idea about the fill fraction of the DM and the number of non-zero elements (NZ) in the DM are shown in Fig. 5.7. The non-zero elements in the DM increase quadratically with W of SiNW. An estimate for 16nm × 16nm SiNW gives about 800117 non-zero elements (details in Appendix E). However, to get an idea about the absolute filling of the DM, a term called the 'fill-factor' is defined as,

$$\begin{aligned} fillfactor &= Total\ nonzero\ elements/Size\ of\ DM \\ &= \frac{NZ}{(3 \times N_A)^2} \end{aligned} \tag{5.17}$$

The percentage fill factor of the DM reduces with increasing W of SiNW (Fig. 5.7). This value is $\sim 0.1\%$ for a SiNW with W $\sim$ 25nm (Appendix E) . So even though the non-zero elements increase with W, DM becomes sparser which allows to store the DM in special compressed format like compressed row/column format (CRS/CCS) [73] enabling better memory utilization.

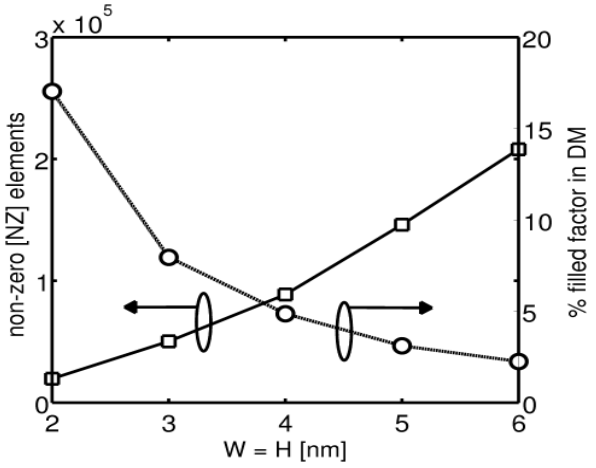

Fig. 5.7. Non zero elements in the dynamical matrix and fill factor in DM. Fill factor reduces as the wire unitcell size increases even though the non-zero elements increase.

5.3.2 Timing analysis for the computation of DM

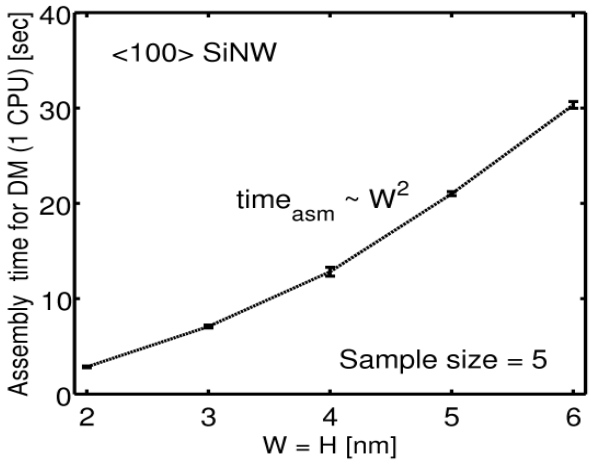

Fig. 5.8. Variation in time to assemble the DM ($time_{asm}$) with width (W) of [100] oriented SiNW.

The assembly of dynamical matrix takes a considerable time due to the many interactions calculated in the MVFF model. The assembly time ($time_{asm}$) increases as N_A increases. To give an idea about the timing, dynamical matrix for SiNW with different W are constructed on a single CPU (Intel). The assembly time is calculated for each width 5 times to obtain a mean value for the $time_{asm}$. The error bar at each W is the standard deviation from the mean $time_{asm}$ (Fig. 5.8).

Extrapolating the data for the computational and timing requirement obtained for the smaller SiNWs, can provide some estimates about the size and time requirement for larger SiNWs (table 5.3). Analytical expressions for the various parameters have been provided in Appendix E.

5.3.3 Summary of the work

A detailed computational analysis of the MVFF model is provided. The memory and computation time increases as the cross-section size of the nanowires increase.

Table 5.3
Resource and timing estimate for larger [100] square SiNW

W (nm)	N_A	NZ	% fill factor	$\overline{time_{asm}}$ (sec)
16	7128	800117	0.423	238.48
20	11120	1252490	0.224	370.73
25	17346	1.96×10^6	0.101	576.91

However, the sparsity of the DM allows its storage using special compressed formats. These details will be useful for the implementation of the phonon calculation codes.

5.4 Heat transport calculation in nanowires

Traditionally computational approaches to thermal-transfer problems spanned from numerical solutions of Fouriers law to calculations based on the Boltzmann Transport Equation (BTE) [163] to atomistic simulations such as Molecular Dynamics (MD) [164–166] and Green's function method [149, 150, 152]. The BTE based approaches are mainly based on explicit calculation of the physics of heat transfer and phonon scattering. This leads to reliable calculation method but requires a fairly sophisticated understanding of the fundamental phonon processes. These methods work well to explain anharmonic phonon effects, isotopic defects, and point defects [142], however, interface currents are poorly explained. The MD simulations solve the Newtons equations of motion in time for an ensemble of atoms interacting with each other through a, usually empirical, inter-atomic potential [164]. The MD approaches do no require any a-priori understanding of heat transport, which makes these methods ideal for investigating the fundamental heat-transfer mechanisms. However, MD methods are completely classical, where all the phonons are equally excited; thus making them only rigorously applicable to solids above the Debye temperature (T_D).

The nano-scale heat transport requires quantum corrections which cannot be treated well within BTE or MD [167]. Two very successful methods to handle transport for mesoscopic systems are, (i) Green function methods, and (ii) Landauer's method based on transmission. The typical structure where thermal transport is solved, in this thesis, consists of a channel sandwiched between two leads (Fig. 5.9). One lead is kept hot and the other one is kept cold. Heat flows between these two leads. In this section both these methods are discussed.

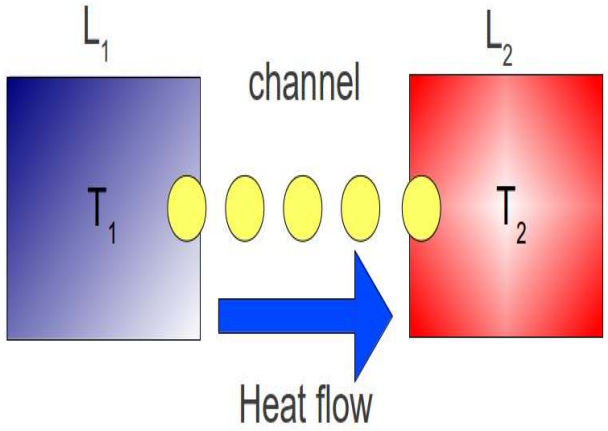

Fig. 5.9. Schematic of a two terminal device. Lead L_1 is maintained at temperature T_1 and lead L_2 is maintained at temperature T_2, such that $T_1 > T_2$. Heat is flowing from terminal L_1 to L_2.

5.4.1 Green's Function Formalism for thermal transport

Green's function formalism provides a very useful method to handle transport of particles in mesoscopic systems [44]. It has been very successfully used in treating quantum electron transport at the nano-scale in various works [45, 168]. Recently atomistic Phonon Green's Function (PGF), both in equilibrium and non-equilibrium form, has been used for understanding thermal transport at the nano-scale [149, 150, 152, 169].

Numerical approach

The main idea of implementing the Green's function formalism is provided here. For more theoretical details on the Green's function methods and motion of equation refer to the work of Supriyo Datta and the references therein [44]. The starting point for solving the heat transport is to describe the system using the dynamical matrix. The details on implementing DM using the MVFF model have been provided in the first half of this chapter. Once the DM of the channel, K_D is calculated (Fig. 5.11) the closed channel Phonon retarded Green's function ,PG_0^R, for an n-dimensional (nD) system is obtained as,

$$PG_0^{R,nD}(\omega) = [(\omega^2 + i\eta)I - K_D(q_\perp^{nD})]^{-1}, \tag{5.18}$$

where nD describes the same dimensionality as mentioned in Table 5.1, η is the energy broadening in the system due to noise [44] and I is the identity matrix. The value $q_\perp^{nD}$ is the transverse momenta degree of freedom (DOF) as shown in Fig. 5.10. The $q_\perp^{nD}$ value is given as,

$$q_\perp^{3D} = [q_\perp^1, q_\perp^2], \tag{5.19}$$

$$q_\perp^{2D} = [q_\perp^1], \tag{5.20}$$

$$q_\perp^{1D} = \text{none}, \tag{5.21}$$

Once this closed system is connected to the external system via leads (L1, L2 in Fig. 5.9), the leads inject states into the channel thereby changing this closed system to an open system. The injection from the external sources is calculated using the self-energy of the leads ($\Sigma_{L,R}$) as shown in Fig. 5.11 [150, 152, 168]. The retarded $\Sigma_{l/r}^R$ can be calculated using the unperturbed surface retarded Green's function of the leads ($pg_0^{l/r}$) by assuming semi-infinite leads. This is given by [149, 152],

$$\Sigma_{l/r}^R(\omega, q_\perp^{nD}) = H_{LR}(q_\perp^{nD}) \cdot pg_0^{l/r}(\omega) \cdot H_{RL}(q_\perp^{nD}), \tag{5.22}$$

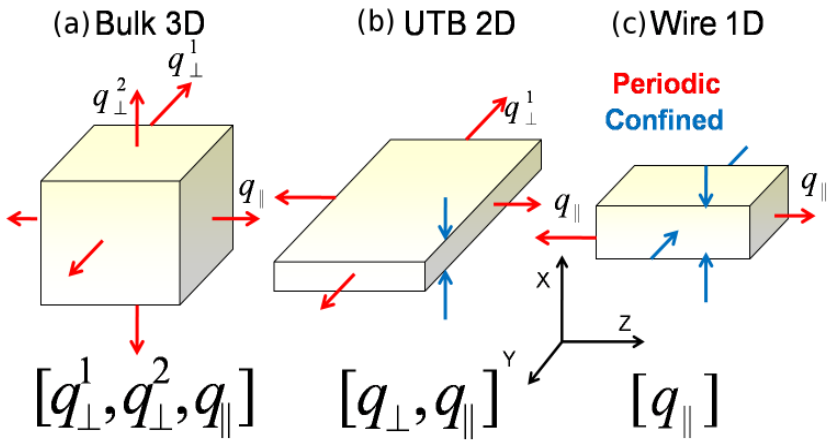

Fig. 5.10. Momentum space of phonons depending on the dimension of the structure. (a) Bulk 3D structure with all three directions periodic. (b) 2D Ultra-thin body (UTB) structure with 2 periodic and 1 confined direction, and (c) 1D Nanowire structure with 1 periodic and 2 confined directions. The transport direction is along $q_{\parallel}$ where as the remaining periodic directions are denoted by $q_{\perp}$.

where $H_{LR/RL}$ represents the coupling of the left(right) device layer to the right(left) layer as shown in Fig. 5.11. The surface Green's function is calculated using Eq. (5.18) with $\eta \rightarrow 0$. Calculation of the self-energy is a computationally expensive process especially for realistic structures. This calculation can be sped up by using the Sancho-Rubio process which has a fast convergence rate [170]. Once the contacts are taken into account the open system retarded Green's function can be calculated as,

$$PG^{R,nD}(\omega) = [(\omega^2 + i\eta)I - K_D(q_{\perp}^{nD}) - \Sigma_l(\omega, q_{\perp}^{nD}) - \Sigma_r(\omega, q_{\perp}^{nD})]^{-1}. \tag{5.23}$$

From Eq. (5.23) the phonon transmission ($\mathcal{P}(\omega, q_{\perp}^{nD})$) is calculated as,

$$\mathcal{P}(\omega, q_{\perp}^{nD}) = Tr(\Big[\Gamma_l(\omega, q_{\perp}^{nD})PG^{R,nD}(\omega)\Gamma_r(\omega, q_{\perp}^{nD})PG^{A,nD}(\omega)\Big]), \tag{5.24}$$

where Tr() represents the trace of the matrix, and the term $\Gamma_{l/r}(\omega, q_{\perp}^{nD}) = Im(\Sigma_{l/r}^{R}(\omega, q_{\perp}^{nD}) - \Sigma_{l/r}^{A}(\omega, q_{\perp}^{nD}))$. The term $\Sigma_{l/r}^{A}(\omega, q_{\perp}^{nD})$ represents the advanced lead self-energy. Simi-

larly $PG^{A,nD}(\omega)$ represents the advanced Green's function of the channel. Using this transmission the spectral thermal current, $J_h(\omega)$ can be calculated as,

$$\begin{aligned}\langle J_h(\omega)\rangle &= \frac{\hbar}{(2\pi)^{nD}}\int_0^{\omega_{max}}\int_{q_\perp^{nD}} \mathcal{P}(\omega, q_\perp^{nD})\cdot\omega\cdot \\ &\Big[\mathcal{F}_{BE}^{L1}(\omega(q_\perp^{nD})) - \mathcal{F}_{BE}^{L2}(\omega(q_\perp^{nD}))\Big]\cdot\partial q_\perp^{nD}\cdot\partial\omega \;\; [m^{nD-1}W/K],\end{aligned} \tag{5.25}$$

where the term $\mathcal{F}_{BE}^{L1/L2}(\omega, q_\perp^{nD})$ is the Bose-Einstein distribution providing the equilibrium phonon density for leads 1 and 2, respectively. This term is given by,

$$\mathcal{F}_{BE}^{L1/L2}(\omega, q_\perp^{nD}) = \Big[exp(\frac{\hbar\omega(q_\perp^{nD})}{k_B T_{1/2}}) - 1\Big]^{-1} \tag{5.26}$$

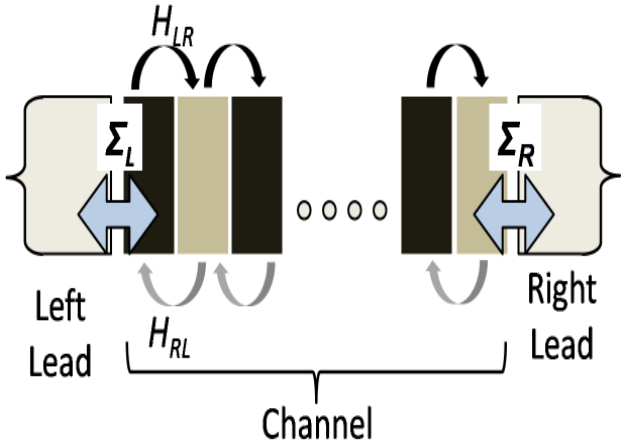

Fig. 5.11. Schematic of a two terminal device. The coupling of the lead with the channel is represented by the self-energy, $\Sigma_{L/R}$. The inter-layer coupling inside the channel is represented by the matrices H_{LR} or H_{RL} which represent left (right) to right (left) coupling.

The Green's function solution can be computationally very expensive and may require special numerical techniques like recursive Green's function method and parallel integration routines [171–173]. Also the elastic and in-elastic scattering mechanisms like anharmonic phonon decay can be included in this method by using scattering self-energies [125] and then solving the Green's function using the Born self-consistent approach [125, 149].

5.4.2 Landauer's Approach to heat transport

For periodic systems within the Landauer's approach one simply thinks of transport as a transmission problem and the current across the system is obtained directly using this picture. In the simplest set-up one thinks of one-dimensional reservoirs (leads) filled with non-interacting phonons (Fig. 5.9) at different chemical potentials. On connecting the system in between the reservoirs, phonons are transmitted through the system from one reservoir to the other. The net current in the system is then the sum of the currents from left-moving and right-moving phonon states from the two reservoirs, respectively.

The flow of heat in nano-scale structures with two leads maintained under a temperature difference of ΔT can be measured using the Landauer's approach [51, 138]. In Landauer's model the transport is viewed in terms of transmission from lead L1 to lead L2 (Fig. 5.9). In this model the thermal current, J_h, between L1 and L2 is given by,

$$\begin{aligned}\langle J_h \rangle &= \frac{\hbar}{(2\pi)^{nD}} \int_0^{\omega_{max}} \int_{q_\perp^{nD}} \Pi(\omega, q_\perp^{nD}) \cdot \mathcal{P}(\omega, q_\perp^{nD}) \cdot \omega \cdot \\ &\quad \left[\mathcal{F}_{BE}^{L1}(\omega(q_\perp^{nD})) - \mathcal{F}_{BE}^{L2}(\omega(q_\perp^{nD}))\right] \cdot \partial q_\perp^{nD} \cdot \partial\omega \;\; [m^{nD-1}W/K],\end{aligned} \tag{5.27}$$

where $\Pi(\omega, q_\perp^{nD})$ is the phonon modes and $\mathcal{P}(\omega, q_\perp^{nD})$ is the phonon transmission at phonon frequency ω and transverse momenta $q_\perp^{nD}$. The dispersion of $\omega(q^{nD})$ is obtained using the MVFF model in these nanostructures as described in the first half this chapter.

5.5 Calculation of physical and thermal properties in solids

A lot of important physical and thermal properties can be obtained using the phonon information in solids. This section describes some of the important physical properties calculated in bulk and nano-structures.

5.5.1 Sound Velocity (V_{snd})

One important parameter is the group velocity (V_{grp}) of the acoustic branches of the phonon dispersion which gives the velocity of sound (V_{snd}) in the solids. Depending on the acoustic phonon branch used for the calculation of V_{grp}, sound velocity can be either, (a) longitudinal ($V_{snd,l}$) or (b) transverse ($V_{snd,t}$). V_{snd} in solids is obtained near the BZ center (for q $\rightarrow$ 0) where $\omega \sim q$. Thus, V_{snd} is given by,

$$V_{snd} = \frac{\partial \omega(p,q)}{\partial q}\Big|_{q\rightarrow 0} \tag{5.28}$$

where p is the polarization of the phonon frequency.

5.5.2 Phonon shifts

The vibrational spectra of the solids are strongly influenced by, (i) the finite size of the structures, (ii) the mismatch with the matrix material (by the surrounding atoms), (iii) defects [55,174,175], and (iv) strain. The optical and the acoustic phonon energies are shifted compared to the bulk values (around $q \propto 0$) in these nanostructures. Nanostructures are very sensitive to this phonon shift. Raman spectroscopy reveals the decrease of the optical frequency with down-scaling of the nanostructures (called the optical softening or optical red shift) [176, 177] and the increase of the acoustic frequency (called the acoustic hardening or acoustic blue shift) [174, 176]. These phonon shifts are estimated using the following relation [176, 178, 179],

$$\Delta\omega_0^{ac/opt} = \omega_{NS}^{ac/opt} - \omega_{bulk}^{ac/opt}, \tag{5.29}$$

where $\omega_{bulk/NS}^{ac/opt}$ is the bulk (nanostructure) acoustic (optical) phonon frequency at the Γ point. Using a series of Raman spectroscopy measurement for a sample of nanostructures the size and the dimensionality of the nanostructures can be predicted [55, 176, 180], thus making it a very important tool for device metrology.

5.5.3 Thermal Conductance (K_l)

The phonon spectrum also provides information about the lattice thermal conductance (K_l). The thermal conductance (K_l), for a two lead device maintained at temperature T1 and T2 (T1 > T2), can be obtained using the thermal current, $\langle J_h \rangle$ (see Sec. 5.4) as [138, 151, 153],

$$K_l = \frac{\langle J_h \rangle}{\Delta T \ \rightarrow \ 0}, \tag{5.30}$$

where ΔT = T1-T2.

5.5.4 Constant Volume Specific heat (C_v)

From the calculated phonon dispersion the constant volume specific heat (C_v) at a given T, can be calculated [144] as,

$$C_v(T) \quad = \quad (\frac{k_B}{m_{uc}}) \cdot \sum_{n,q} \Big[\frac{(\frac{E_{n,q}}{k_B T}) \cdot \exp(\frac{-E_{n,q}}{k_B T})}{[1 - \exp(\frac{-E_{n,q}}{k_B T})]^2} \Big] \quad [J/kg.K], \tag{5.31}$$

where m_{uc} is the mass of the SiNW unitcell in kg. The quantity $E_{n,q}$ is the phonon eigen energy associated with the branch 'n' and crystal momentum vector 'q' given as $E_{n,q} = \hbar\omega_{n,q}$.

5.6 Results on the MVFF Phonon model

In this section results for the phonon spectrum in bulk and confined semiconductor structures using both the MVFF and KVFF models are shown. Also some of the physical properties extracted from the phonon dispersions are reported.

5.6.1 Experimental Benchmarking

The first step to check the correctness of the MVFF model is to compare the simulated results against the experimental data. Figure 5.12 shows the simulated and experimental [181] bulk phonon dispersion for (a) Silicon and (b) Germanium. The

value of the strength parameters are provided in Table 5.4. A very good agreement between the experimental and simulated data is obtained. To further support the correctness of the MVFF model, V_{snd} is calculated in bulk Si and Ge along [100] direction (Table 5.5). The extracted sound velocity compares very well with the experimental sound velocity data [182] (max error $\leq$ 10%). Hence, MVFF model captures the experimental phonon dispersion in bulk zinc-blende material very well.

Table 5.4
Force constants (N/m) used for phonon dispersion calculation

Material	Model	α	β	δ	γ	ν
Si [50]	MVFF	49.4	4.79	5.2	0	6.99
Si [146]	KVFF	48.5	13.8	0	0	0
Ge [50]	MVFF	44.32	3.68	4.95	0	6.13

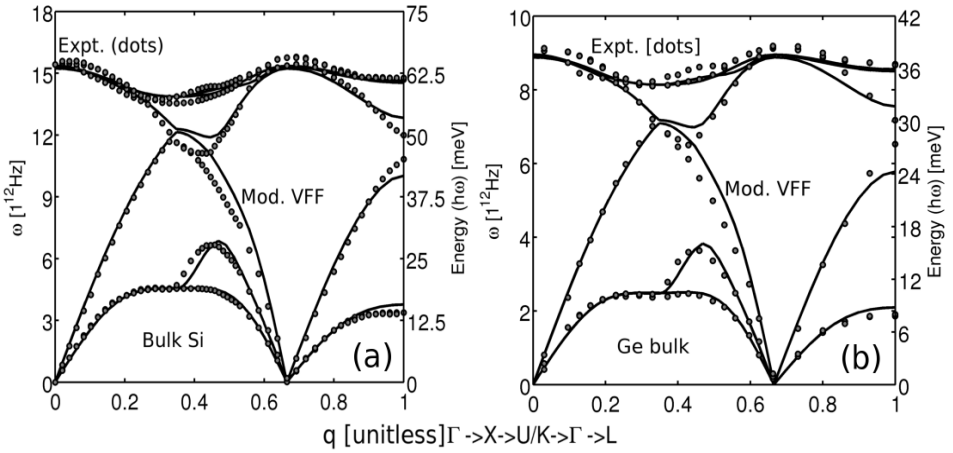

Fig. 5.12. Benchmark of simulated bulk phonon dispersion with experimental phonon data for (a) Si, and (b) Ge. Experimental data is obtained using neutron scattering at 80K [181].

Table 5.5
Sound Velocity in km/sec in semiconductor structures

Material	Structure	V_{snd} calc.	V_{snd} [182]
Si	Bulk V_l [100] [1]	9.09	8.43 (∼8%)
	Bulk V_t [100] [2]	5.71	5.84 (∼2%)
	NW V_l (W=H=6nm)	6.51	–
	NW V_t (W=H=6nm)	4.46	–
Ge	Bulk V_l [100]	5.13	4.87 (∼5%)
	Bulk V_t [100]	3.36	3.57 (∼6%)
	NW V_l (W=H=6nm)	3.70	–
	NW V_t (W=H=6nm)	2.61	–

5.6.2 Comparison of VFF models

In this section comparison of the original Keating VFF model [146] with the MVFF model is given to show the need for the more elaborate MVFF model. From computational point of view the DM for both the models are quite different as shown in Fig. 5.6. The difference in the sparsity pattern arises because of the coplanar interaction present in the MVFF model which takes into account interactions beyond the nearest neighbors. The quantitative comparison of DM for the two models for same SiNW is shown in Fig. 5.13. The KVFF model has lesser non-zero elements compared to the MVFF model. The increase in non-zero elements in MVFF model goes up as the wire cross-section size increases (Fig. 5.13). MVFF model can take upto 85% more space compared to KVFF model for a 5nm × 5nm SiNW. Thus MVFF model demands more storage space.

Comparison of the bulk Si phonon dispersion from the two models is shown in Fig. 5.14. The parameters for both the models are provided in Table 5.4. Qualitatively MVFF shows a better match to the experimental data compared to the KVFF model. There are few important points to be noted in the bulk phonon dispersion. The KVFF

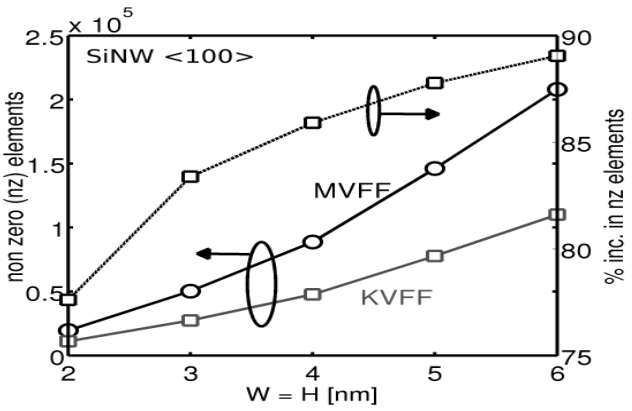

Fig. 5.13. Matrix size and number of non zero elements required by the two models. MVFF has more elements needed for accurate phonon dispersion.

model reproduces the acoustic branches very well near the BZ center but overestimates the values near the zone edge (at X and L point in the BZ, Fig. 5.14). The MVFF model overcomes this shortcoming and reproduces the acoustic branches very well in the entire BZ. Comparison of sound velocity along the [100] direction for bulk Si obtained from both the models show a very good match to the experimental data (Table 5.6).

The KVFF model overestimates the optical phonon branch frequencies where as the MVFF model produces a very good match to the experimental data (Fig. 5.14). The comparison of the optical frequency at the Γ point reveals that the KVFF model overshoots the experimental value by $\sim 7\%$ whereas the MVFF model is higher by only $\sim 0.6\%$. The MVFF model captures the optical branches very well compared to the KVFF model. The correct representation of bulk phonons is very important since this will affect the phonon spectrum of the confined structures. At the same time the physical properties like lattice thermal conductivity, phonon density of states (Ph-DOS), etc. are also affected. Hence, MVFF model is more accurate in capturing the experimental bulk phonon data, though it comes at the expense of additional calculations and storage.

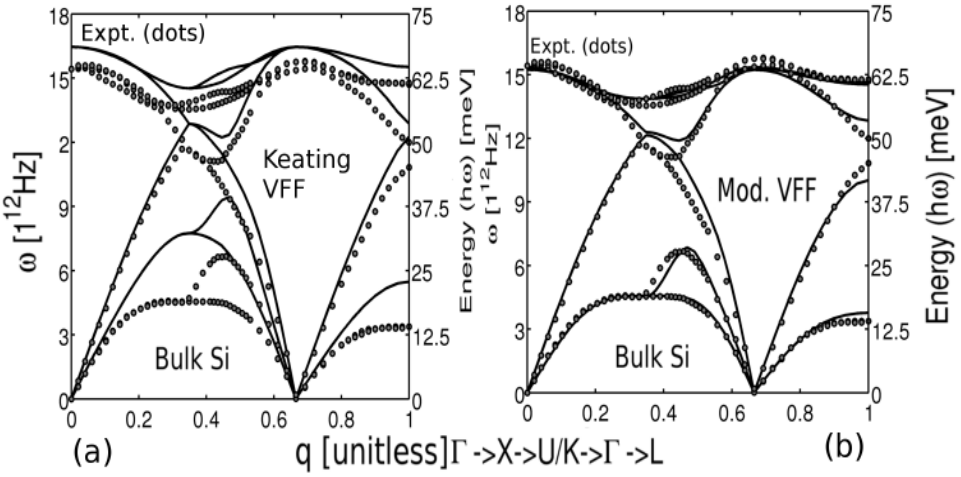

Fig. 5.14. Simulated bulk phonon dispersion for Si using (a) Keating VFF and (b) modified VFF compared with experimental phonon data. MVFF shows a very good match compared to KVFF

5.6.3 Phonons in nanowires

After benchmarking the bulk phonon dispersion, the same strength parameters (Table 5.4) are used to obtain the phonon spectrum in [100] square SiNW (Fig. 5.15). The result for a 2nm × 2nm free-standing SiNW is shown in Fig. 5.15(a). Some of the key features to notice in the phonon dispersion are, (i) presence of two acoustic branches ($\omega(q) \sim$ q, 1,2 in 5.15(a)), (ii) two degenerate modes (3,4 in 5.15(a)) with $\omega(q) \sim q^2$, which are called the 'flexural modes', typically observed in free-standing nanowires [151, 156, 183] , and (iii) heavy mixing of the higher energy sub-bands leaving no proper optical mode. So, the features are quite different from the bulk phonon spectrum. This will strongly affect the other physical properties of nanowires extracted using the phonon dispersion.

Using the boundary condition method discussed in sec.5.2.3, the phonon spectrum in a 2nm × 2nm [100] SiNW are calculated with different damping values ($\Xi = 1$ (free standing), 0.5 and 0.1) as shown in Fig. 5.15(b). Only the bottom surface of the SiNW is clamped whereas the other three sides have free boundary condition. The effect of damping is very prominent at the BZ edge compared to the zone center. Zone edge

Table 5.6
Comparison of bulk parameters in Si for two models

Model	$V_{l,100}^{bulk}$ (km/sec)	$V_{t,100}^{bulk}$ (km/sec)	$\omega_{opt}(\Gamma)$ (THz)
MVFF	9.09	5.71	15.49
KVFF	8.35	5.75	16.46
Expt. [182]	8.43	5.84	15.39

frequencies decrease in energy as the damping increases. A reduction of $\sim 1.07\times$ and $\sim 2.11\times$ are observed for the zone edge frequency for 1st branch at $\Xi = 0.5$ and $\Xi = 0.1$ respectively (Fig. 5.15(b)). This shows that the system vibrational energy is decreasing especially for higher momentum 'q' values. First four branches are very strongly affected, however, the higher phonon branches are less affected.

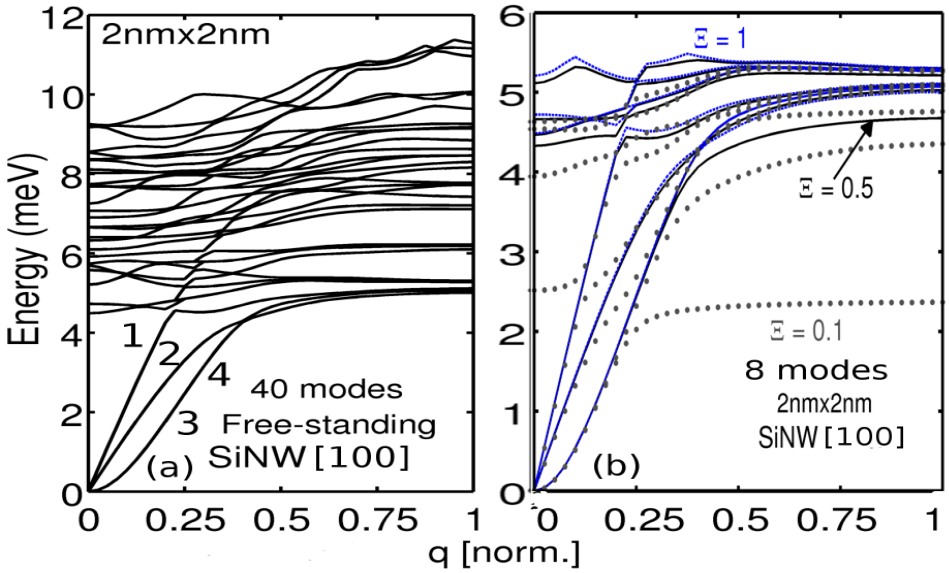

Fig. 5.15. (a) Phonon dispersion in ⟨100⟩ oriented SiNW with W = H = 2nm. For clarity only the lowest 40 sub-bands are shown. (b) Dependence of phonon dispersion on the damping of vibration of the bottom surface atoms for Ξ = 1,0.5 and 0.1. Reduction of phonon energy at the Brillioun zone boundary is stronger compared to the zone center.

5.6.4 Ballistic lattice thermal conductance (K_l^{bal}) in SiNWs

In this part the ballistic K_l^{bal} for square SiNW calculated using their phonon dispersions are presented. The conductance is calculated using the 1D form of Eq. (5.30). Clamping the bottom surface affects the K_l^{bal} stronger at higher temperature compared to the lower temperature value(Fig. 5.16). Inset of Fig. 5.16 shows the K_l^{bal} at 300K. The reduction in K_l^{bal} from free-standing wire to a clamped wire ($\Xi = 0.1$) is $\sim 13\%$. Hence, fixing the surface atoms have a strong impact of the lattice thermal conductance in SiNW.

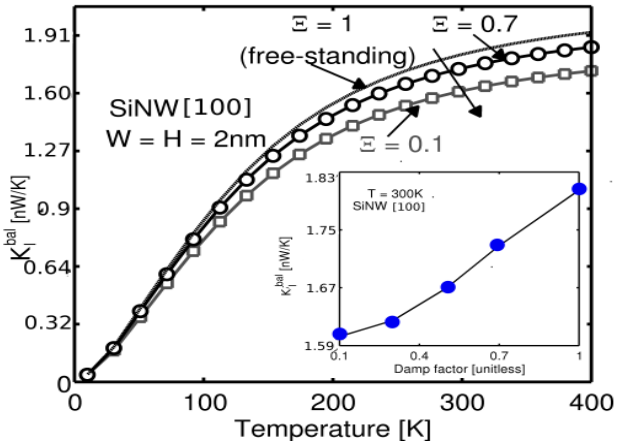

Fig. 5.16. Ballistic lattice thermal conductivity (K_l^{bal} for a 2nm $\times$ 2nm [100] SiNW with different bottom surface damping. K_l^{bal} drops as damping increases. Inset shows K_l^{bal} at 300K. As the bottom surface changes from free-standing to clamped ($\Xi = 0.1$), K_l^{bal} reduces by about 13%.

5.6.5 Summary of the work

The need for using an advanced VFF method compared to the Keating's method has been shown. The MVFF model provides a better match with the experimental phonon dispersion as well as other physical quantities. Furthermore the MVFF model is applied to SiNWs with both free and clamped surfaces showing the wide applicability of the model.

5.7 Comparison of PGF and Landauer's method

For non-interacting systems, the formal expressions for current obtained from the PGF approach is in terms of transmission coefficients (Eq. 5.24) of the phonons across the system (Fig. 5.9), with appropriate weight factors corresponding to the population of modes in the reservoirs. These expressions are basically what one also obtains from the Landauer formalism. As a comparison the ballistic thermal conductance for a [100] 3nm X 3nm SiNW is calculated using Landauer's method and PGF as a function of temperature. Results from both the calculations match each other perfectly as shown in Fig. 5.17. For uniform non-interacting systems Landauer's approach is computationally much faster compared to Green's function method. However, when there are non-uniformities along the channel like alloying and roughness or in-elastic scattering processes then PGF provides a better way to handle such systems.

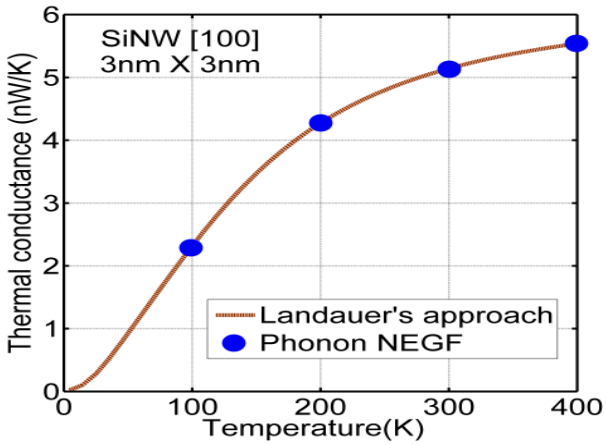

Fig. 5.17. Ballistic lattice thermal conductance (K_{th}^{bal} for a 3nm × 3nm [100] SiNW calculated using Landauer's approach and PGF. Both the results are equal when the channel and the contacts are made of same material without any defect.

5.8 Summary and Outlook

The details for calculating phonon dispersion in zinc-blende semiconductor structures using the modified Valence Force Field method have been outlined. The procedure to calculate the thermal transport in nanostructures using Green's Function method as well as the Landauer's approach are provided. MVFF method has been applied to calculate the phonon spectra in confined nanowire structures with varying boundary conditions. The methodology and the computational requirements for the method has been provided. Comparison of Keating VFF with MVFF shows that, MVFF provides accurate phonon dispersion but at the expense of more computational power.

Formulation for the extraction of the physical and thermal properties of semiconductors using the phonon dispersion and thermal transport will act as important tools for the analysis of physical properties in real devices in the next chapter. Accurate modeling of phonons cannot be undermined which is revealed in the correct calculation of physical quantities like sound velocity and lattice thermal conductance.

6. FROM PHONONS TO STRUCTURAL AND THERMAL PROPERTIES OF Si NANOWIRES

6.1 Introduction

Nanowires have the potential of becoming useful for structures for CMOS transistors [13], thermoelectric devices [32] and many other applications. Extensive application of nanowires to various technologies requires an adequate understanding of the structural [156], electrical [154], thermal [153], and optical [184] properties which arise from the strong geometrical confinement, atomic positions and increased surface-to-volume ratio (SVR). The phonon spectra of nanowires hide a lot of vital information about the structural and thermal properties of the wires.

The present chapter concentrates on understanding the effects of geometrical confinement, orientation, cross-section shape and size on the phonon dispersion and the associated phonon shifts (useful for Raman Spectroscopy [55]) and thermal properties of silicon nanowires (SiNWs). Most of the work in this chapter is based on SiNWs but the general aspects of nanowire scaling on the structural and thermal properties hold for other 1D nanowires too.

This chapter is organized as follows. The influence of shape, size and orientation on the phonon shift in SiNWs is described in Sec. 6.2 whereas the influence of the same factors on the thermal properties is outlined in Sec. 6.3. The scaling of these properties with cross-section size and the concept of bulk material is discussed in Sec. 6.4. Conclusions and outlook are provided in Sec. 6.5.

6.2 Phonon shifts in Si Nanowires

This section theoretically explores the effect of the cross-section geometry, size and orientation of ultra-scaled SiNWs on the phonon shifts. Engineering the structural properties of nanowire based on their cross-section size has been studied extensively [174, 179, 183, 185] along with the impact of semiconductor (GaAs, GaP, ZnS, etc) nanowire shape on their structural properties has been observed [180, 186, 187]. The amount of the optical and acoustic phonon shift along with phonon line width broadening is utilized in Raman spectroscopy which provides a valuable, non-destructive method to analyze the physical properties of nanostructures (NS) like cross-section size [174, 185], degree of crystallinity [175], dimensionality of confinement [185, 188], etc.

The first satisfactory theoretical model for explaining Raman shifts and line width broadening was proposed by Richter et al [189] and improved by Campbell and Fauchet [190]. These phenomenological continuum models are based on the choice of the phonon weighting function as well as the boundary conditions of the phonon vibrations [189,190] which are chosen rather arbitrarily and hence do not provide correct phonon shift in nanostructures [191]. Arora et al. experimentally [55] reported that phonon shifts are very different from bulk in nanostructures with size less than 20nm. Tanaka et al [192] also pointed out the failure of continuum models to predict the Raman shift in nanostructures with size < 7.5nm due to the arbitrary parameter sets used in continuum models. The continuum models can match the experimental Raman spectroscopy data using fitting parameters. However, they lack the predictive capability for estimating the phonon shifts and line widths in extremely small nanostructures with different shapes and compositions [176, 191, 192].

Many efforts to explain the phonon shifts in nanostructures have been reported. They are based on models like the VFF approach [183,193], partial density approach [191], BCM model [178,179], bond order model [176], etc. In all these approaches the importance of taking into account the atomic positions and the atomic surrounding to

understand the Raman shift has been stressed which most of the continuum models lack [189, 190]. The Modified Valence Force Field (MVFF) phonon model is utilized, as discussed in Chapter 5, to study the phonon shifts in SiNWs.

6.2.1 Approach

The vibrational spectra of the nanostructures are strongly influenced by, (i) the finite size of the nanostructures, (ii) the mismatch with the matrix material (by the surrounding atoms), (iii) defects [55, 174, 175], (iv) heating by laser [180], and (v) wire orientation. The acoustic and optical phonon shifts are calculated using Eq.(5.29) of Chapter 5. The phonon shifts show the following functional dependence on the nanostructure cross-section size (W) [176, 178, 185],

$$\Delta\omega_0^{ac/opt} = A_{ac/opt}(\frac{a_0}{W})^{d_{ac/opt}} \ \ [cm^{-1}], \tag{6.1}$$

where a_0 is the lattice constant of the material. For A>0 the phonon shift is positive (or blue shift) and for A<0 the shift is negative (or red shift) [176]. The exponent value 'd' indicates the dimensionality of the geometrical confinement. For 1D nanowires/nanorods a variety of 'd' values have been reported in the literature like 0.67 [178], 0.95 [156], 1.44 [185], etc. Atomistic phonon modeling correctly takes surface boundary conditions into account depending on the cross-section shape of the wire which reflects in the overall phonon spectrum. The surface and inner atomic movements vary with different cross-section shapes and therefore affects the phonon shifts. Equation 6.1 captures the nanostructure size effect in the exponent value 'd' and the shape effect in the pre-factor 'A'. Thus, a combination of A and d can be useful for the determination of size and shape of the SiNWs.

6.2.2 Si Nanowire details

Four cross-section shapes for [100] oriented SiNWs have been considered in this study, (a) circular, (b) hexagonal, (c) square and (d) triangular cross-section shapes

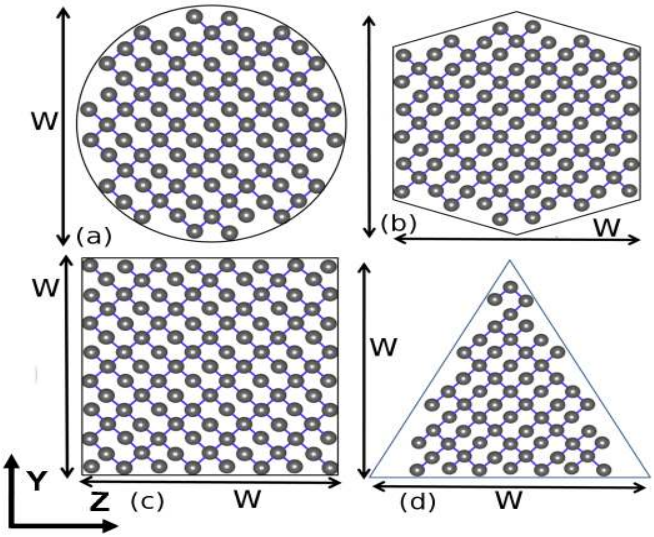

Fig. 6.1. Projected unit cell structures of free-standing [100] oriented silicon nanowires with (a) Circular, (b) Hexagonal, (c) Square, and (d) Triangular cross-section shapes. Width and height of the cross-section are defined using a single width variable W (width = height). These structures are at W = 2nm.

(Fig. 6.1). SiNWs with [110] and [111] channel orientation studied here are of square cross-section only as shown in Fig. 6.2. The feature size is determined by the width parameter W. The value of W is varied from 2 to 6 nm. The surface atoms are allowed to vibrate freely without any passivating species. The wires are still assumed to have a tetrahedral geometry. It has been shown that wires with diameter below 2nm tend to lose the tetrahedral structure [194, 195] due to surface pressure and internal strain.

6.2.3 Results and Discussion

In this section the effect of cross-section on the phonon dispersion and phonon shifts of [100] SiNWs are discussed. There is a lack of proper channel orientation information in the literature. However Adu et al. [180] reported [100] channel orientation due to which the [100] SiNWs is chosen for shape study. Furthermore, the impact of channel orientation on the phonon shifts is also investigated.

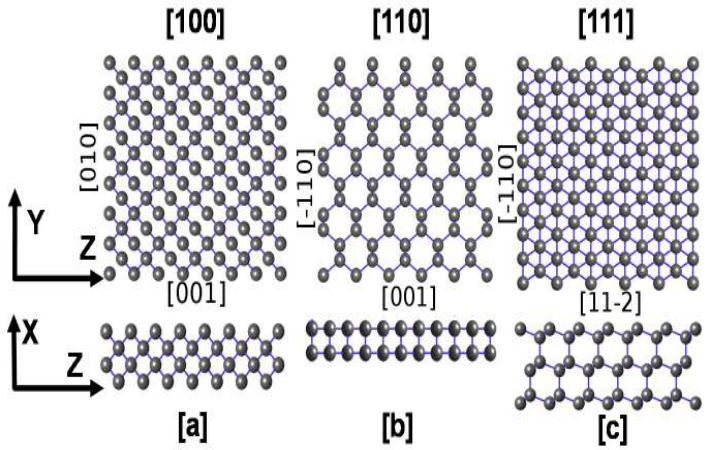

Fig. 6.2. Projected unit cells of square free-standing SiNWs with (a) [100], (b) [110], and (c) [111] wire axis orientation. Width and height of the SiNWs are defined using W. These structures are at W = 2nm.

Phonon dispersion: Shape effect

The phonon dispersion of SiNWs for all the cross-section shapes with [100] channel are shown in Fig. 6.3. While the full phonon dispersion extends up to ∼65meV, phonon modes till 9 meV energy range are shown for clarity. All the wires exhibit two flexural branches [196] ($\omega_{q\leftarrow 0} \propto q^2$). These modes are double degenerate in all the shapes except the triangular wire. In the triangular wires these modes split due to the reduced structural symmetry (Fig. 6.3 d). The next two phonon branches in all the structures show $\omega_{q\leftarrow 0} \propto q$. These branches determine the sound velocity in these structures [196] (Table 6.1). The triangular wire has the lowest longitudinal and transverse sound velocity ($V_{snd,l}$) whereas other shapes have very similar sound velocities. *The splitting of the degenerate flexural modes and the reduced sound velocity show that triangular wires have the least structural symmetry.*

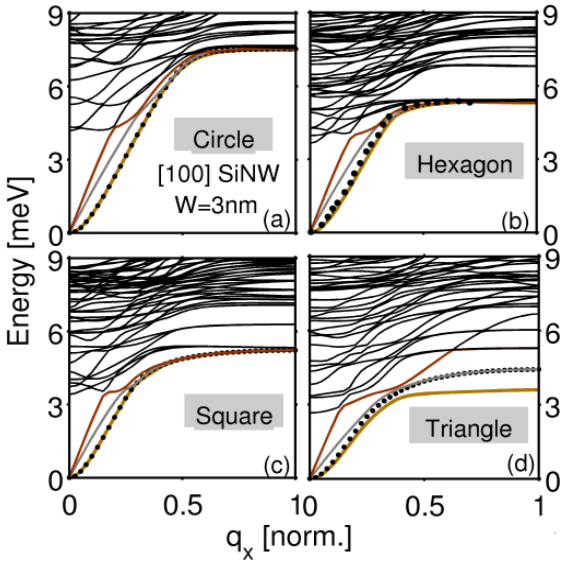

Fig. 6.3. Phonon dispersion in free-standing [100] oriented, W = 3nm, SiNWs with (a) Circular, (b) Hexagon, (c) Square, and (d) Triangular cross-section shapes. The first two branches (brown and black dot) are the flexural modes [196]. The next two branches (gray and brown) are the acoustic branches [196].

Table 6.1
Cross-section shape dependence of longitudinal and transverse sound velocity in W= 3nm, [100] SiNW

Shape	$V_{snd,l}(km/sec)$	$V_{snd,t}(km/sec)$
Circular	6.23	4.50
Hexagon	6.18	4.37
Square	6.26	4.37
Triangular	5.79	3.12

Experimental Benchmark of Phonon shifts

Both the experimental acoustic and optical phonon shifts in Si nanocrystals are compared.

Acoustic shift: Acoustic phonon shift obtained in square [111] SiNWs using the MVFF model compares very well with other theoretical values [179, 183] as shown in Fig. 6.4. The acoustic shift is caused due to the geometrical confinement present in SiNWs which breaks the crystal symmetry [176] providing frequency shifts between 20 to 100 cm^{-1}. Similar acoustic hardening is also reported in Ref. [183] for [111] SiNWs utilizing the Keating VFF model [146] (Si-1, Si-2 in Fig. 6.4) and in Ref. [179] which uses the Bond Charge Model (Si-3 in Fig. 6.4). The phonon shifts calculated using MVFF show a power law of $W^{-0.78}$ which is close to the BCM result of $W^{-0.71}$ for square SiNWs [179]. Thus, the acoustic phonon shifts from the MVFF model compare well with other theories.

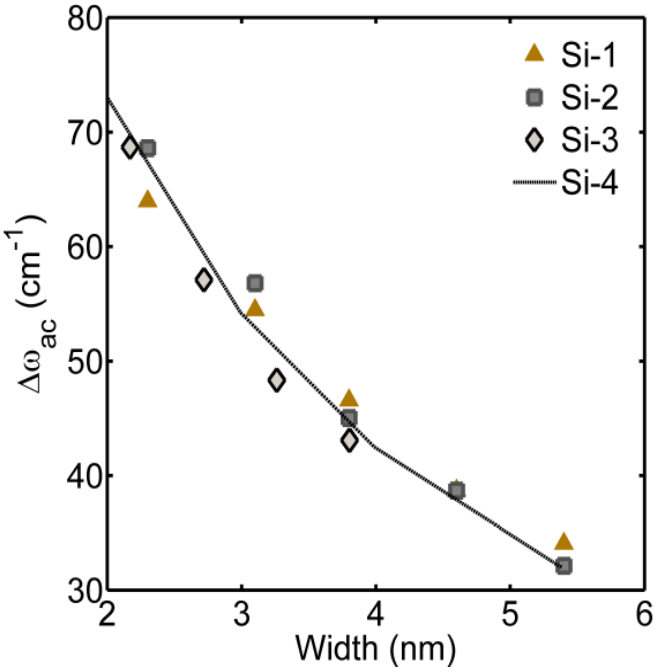

Fig. 6.4. Comparison of theoretical acoustic phonon frequency shift (line) obtained for square [111] SiNWs using MVFF model with other theoretical calculations. The Si-1 and Si-2 results are for [111] SiNW for two light polarizations from Ref. [183], Si-3 is for square SiNW from Ref. [179] and Si-4 represents the MVFF calculation.

Optical shift: The optical phonon shift is experimentally measured using Raman spectroscopy [180]. With decreasing cross-section size the optical red-shift in-

creases [176]. The theoretical optical phonon shift is calculated for free-standing [100] circular SiNWs using the MVFF model (Si-8 in Fig. 6.5). The theoretical values of the optical shift agree well with the experimental data [180] (Si-2 in Fig. 6.5). Comparison of the MVFF calculation (Si-8) with other theoretical models (see Fig. 6.5) like the Si-1 result based on BCM from Ref. [179], Si-3 [176] based on bond order length strength correlation method (BOLS), Si-4 obtained by empirical fitting using Gaussian function [190] , Si-5 [185] based on bond polarizability model (BPM), Si-6 [197] based on theoretical size dependence of root-mean-square average amplitude of atomic thermal vibration, and Si-7 [198] obtained from a modified phonon confinement model (Heisenberg's uncertainty principle), is very good. The mismatch in the phonon shifts at extremely small dimensions ($W \sim 2nm$) may be due to the structural relaxation in small cross-section wires [194, 195] which is not taken into account in this study. Hence, the MVFF model correctly captures the optical phonon shifts in SiNWs for W$\geq$2nm. However, for $W < 2nm$ the MVFF phonon values without structural relaxation are not very accurate. Though the optical shift is well captured by the Richter model [189] (Si-4 in Fig. 6.5), the fitting parameters are chosen arbitrarily which removes the predictive capability from the model.

In the next few sections the predictions on the structural properties of ultra-scaled SiNWs with different cross-section shapes, orientation and sizes are discussed.

Acoustic Phonon shift in SiNWs

Influence of cross-section shape and size: The acoustic phonon shifts are calculated using the MVFF model for different cross-section shaped SiNWs. All the wire geometries show a blue shift of the acoustic mode (this mode closely resembles the 'radial breathing mode' observed in perfectly circular wires [183]) as the wire cross-section size is reduced (Fig. 6.6 a). There is a clear cross-section shape dependence of the blue shifts where the blue shift follows the order $\Delta\omega_{tri} < \Delta\omega_{sq} < \Delta\omega_{hex} < \Delta\omega_{cir}$.

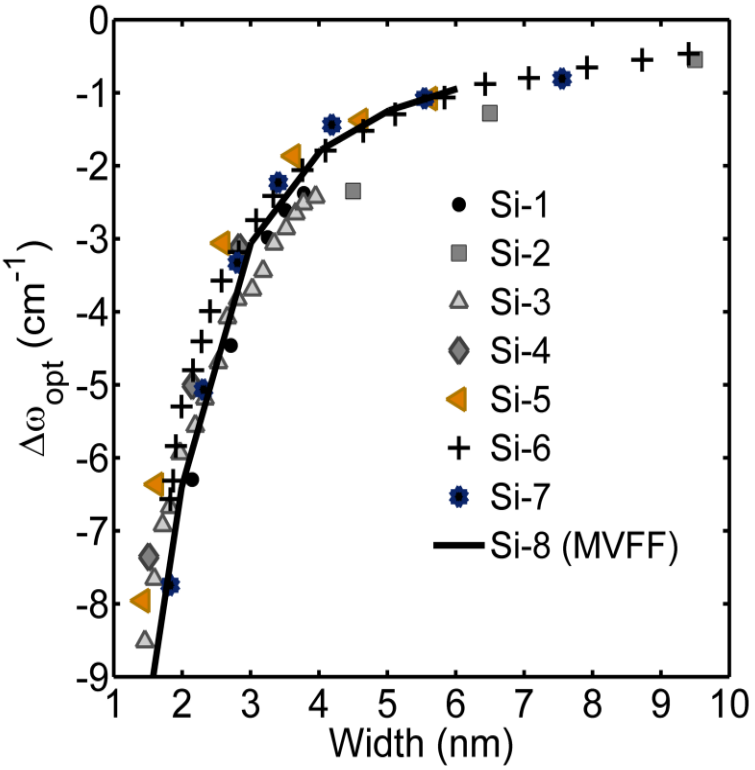

Fig. 6.5. Comparison of theoretical optical phonon frequency shift (Si-8), obtained for circular SiNWs using the MVFF model with other experimental data and theoretical models. The Si-1 result is from Ref. [179] using BCM. The Si-2 is experimental data from Ref. [180], Si-3 is from Ref. [176] based on theoretical bond order length strength correlation method (BOLS), Si-4 is from Ref. [199] obtained by empirical fitting using Gaussian function [190] , Si-5 is from Ref. [185] based on bond polarizability model (BPM), Si-6 is from Ref. [197] based on theoretical size dependence of root-mean-square average amplitude of atomic thermal vibration, Si-7 is based on a modified phonon confinement model (Heisenberg's uncertainty principle) provided in Ref. [198]. The Si-8 results are from the present MVFF calculation.

The power exponent (d_{ac}), for the SiNWs in this study, varies between 0.6 and 0.87 (Table 6.2). The order of the pre-factor (A_{ac}) in Eq.(6.1) value (Table 6.2) also shows the order of the acoustic blue shift for [100] SiNWs.

Similar trends for acoustic blue shift are observed in other theoretical works [179, 183]. The power exponent and the pre-factor are shown in Table 6.2. The values

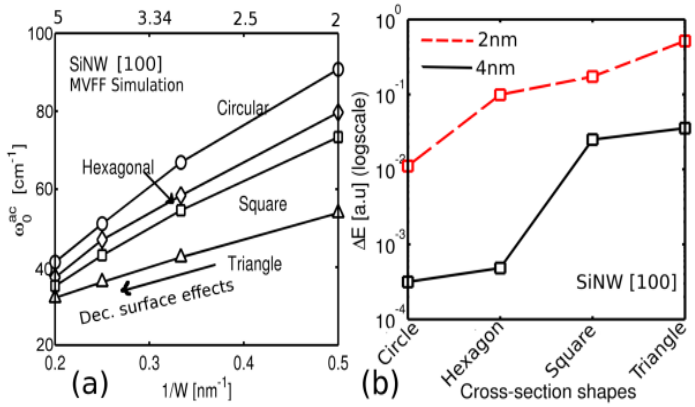

Fig. 6.6. (a) Effect of cross-section shape on the acoustic phonon shift in [100] SiNWs. (b) Difference in the average vibrational energy density of the inner and the surface atoms in 4 cross-section shape [100] SiNWs for W = 2nm and 4nm.

Table 6.2
Width parameters for acoustic phonon shift in [100] SiNWs and other theoretical calculations (see Fig. 6.4).

Shape	A_{ac} (cm^{-1})	d_{ac}
Circular	286.3	0.87
Hexagon	230.1	0.81
Square	210.4	0.79
Triangular	111.6	0.6
SiNW (YY, Si-1) [183]	255.9	0.89
SiNW (ZZ, Si-2) [183]	272.7	0.92
SiNW square (Si-3) [179]	196.66	0.72

of d_{ac} and A_{ac} for Si-1, and Si-2 indicate that the SiNWs used in Ref. [183] are almost circular which is indeed the case as presented in that work. Similarly the d_{ac} and A_{ac} values obtained for Si-3 (based on BCM) represent a square SiNW which is corroborated by the structure shape used in Ref. [179]. Thus, the combination of d_{ac}

and A_{ac} values can clearly correlate to the shape of the SiNWs and these combinations are very well calculated using the MVFF model.

With the increase in wire cross-section size two important things happen, (i) the geometric confinement on the phonons reduces, and (ii) the vibrational energy deviation between the surface and the inner atoms decreases (Fig. 6.6). First point explains the reduction in the blue shift with increase in cross-section size for all the SiNWs while the second point explains the order of blue-shift with shape.

As the SiNW cross-section is reduced lots of low velocity phonon sub-bands start to appear above the acoustic branches (Fig. 6.3) which are normally absent in bulk. These relatively flat bands cause phonon confinement. These zone center low energy phonon sub-bands cause acoustic blue shift. The surface atom vibrations become comparable to the inner core atom vibrations with size reduction. The blue shift is more pronounced when surface modes are less dominant. If the surface atoms vibrations are more than inner atoms then blue shift is suppressed [176].

The acoustic blue shift order can be explained by the difference between the vibrational energy density [200] of the surface atoms and the inner atoms (ΔE). Surface atoms are the ones with dangling bonds. The spatial vibrational energy density can be calculated as [200],

$$E_{i,q}^{den} = \sum_{NA} \sum_{j\in[x,y,z]} [F_{BE}(\omega_{i,q}) + 0.5]\hbar\omega_{i,q}\phi_{i,q,j}\phi_{i,q,j}^{*}, \tag{6.2}$$

where NA is the total number of atoms in the unit cell, 'i' is the phonon sub-band, 'q' is the phonon wave-vector, 'j' is the polarization, F_{BE} is Bose-Einstein distribution for phonon population, $\omega_{i,q}$ is the phonon eigen frequency for sub-band 'i' and wave-vector 'q' and $\phi_{i,q,j}$ is the phonon eigen vibration mode.

Figure 6.6b shows that the triangular wire exhibits the maximum difference between the surface and inner atom vibrational energy density for W = 2nm and 4nm, followed by the square, the hexagonal, and the circular wire. Figure 6.7 shows the spatial distribution of the energy density for the acoustic phonon branch for 2nm cross-section SiNWs. The surface atoms vibrate more intensively compared to the

inner atoms. In circular and hexagonal nanowires all atoms vibrate with a similar intensity as indicated by the small ΔE value. However, in square and triangular wires the surface atoms vibrate more compared to the inner atoms leading to a larger ΔE value.

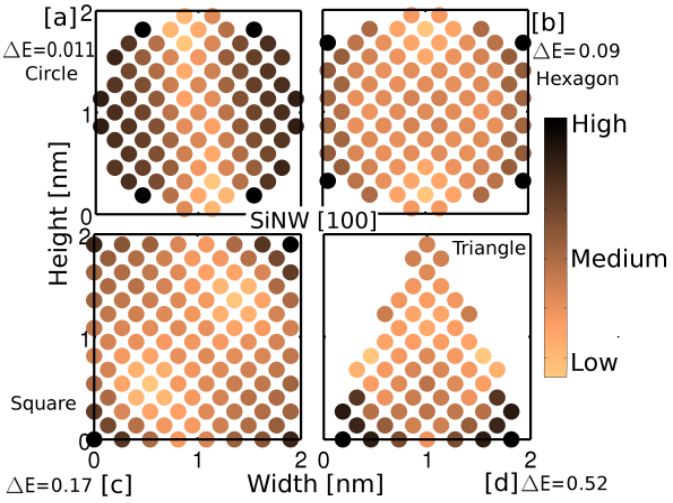

Fig. 6.7. Phonon energy density for the confined acoustic mode in 2nm × 2nm [100] SiNWs with (a) circular, (b) hexagonal, (c) square and (d) triangular shapes. Surface atoms vibrate more compared to the internal atoms. The difference in the energy of the surface and inner atoms is represented by ΔE. Triangular wires have largest ΔE which results in minimum acoustic phonon confinement (see Fig. 6.6).

The low frequency acoustic phonon modes are very similar to the breathing mode found in larger circular wires [183]. These eigen frequencies follow a $1/W^d$ law (Fig. 6.6), with d = 1 for a perfectly concentric circular wire [183]. The value of 'd' deviates from 1 as the cross-section shape deviates from the ideal circular geometry.

Influence of cross-section shape and size: The acoustic phonon shifts are calculated using the MVFF model for different cross-section shaped SiNWs. All the wire geometries show a blue shift of the acoustic mode (this mode closely resembles the 'radial breathing mode' observed in perfectly circular wires [183]) as the wire cross-section size is reduced (Fig. 6.6 a). There is a clear cross-section shape dependence of the blue shifts where the blue shift follows the order $\Delta\omega_{tri} < \Delta\omega_{sq} < \Delta\omega_{hex} < \Delta\omega_{cir}$.

The power exponent (d_{ac}) varies between 0.6 and 0.856 (Table 6.2). The order of the pre-factor (A_{ac}) in Eq.(6.1) value (Table 6.2) also shows the order of the acoustic blue shift for [100] SiNWs.

With the increase in wire cross-section size two important things happen, (i) the geometric confinement on the phonons reduces, and (ii) the vibrational energy deviation between the surface and the inner atoms decreases (Fig. 6.6. First point explains the reduction in the blue shift with increase in cross-section size for all the SiNWs while the second point explains the order of blue-shift with shape.

As the SiNW cross-section is reduced lots of phonon sub-bands start to appear above the acoustic branches (Fig. 6.3) which are normally absent in bulk. These relatively flat bands cause phonon confinement. These zone center low energy phonon sub-bands cause acoustic blue shift. The surface atom vibrations become comparable to the inner core atom vibrations with size reduction. The blue shift is more pronounced when surface modes are less dominant. If the surface atoms vibrations are more than inner atoms then blue shift is suppressed [176].

The observed acoustic blue shift order can be explained by the difference between the vibrational energy density [200] of the surface atoms and the inner atoms (ΔE). Surface atoms are the ones with dangling bonds. Figure 6.6 b shows that the triangular wire exhibits the maximum difference between the surface and inner atom vibrational energy density for W = 2nm and 4nm, followed by the square, the hexagonal, and the circular wire. Figure 6.7 shows the spatial distribution of the energy density for the acoustic phonon branch for 2nm cross-section SiNWs. The surface atoms vibrate more intensively compared to the inner atoms. In circular and hexagonal nanowires all atoms vibrate with a similar intensity as indicated by the small ΔE value. However, in square and triangular wires the surface atoms vibrate more compared to the inner atoms leading to a larger ΔE value.

The low frequency acoustic phonon modes are very similar to the breathing mode found in larger circular wires [183]. These eigen frequencies follow a $1/W^d$ law (Fig.

6.6), with d = 1 for a perfectly concentric circular wire [183]. The value of 'd' deviates from 1 as the cross-section shape deviates from the ideal circular geometry.

Optical Phonon shift in SiNWs

Table 6.3
Width parameters for optical phonon shift in [100] SiNWs and in other experimental and theoretical models (see Fig. 6.5).

Shape	A_{opt} (cm^{-1})	d_{opt}
Circular (Si-8)	-72.49	1.85
Hexagon	-62.59	1.82
Square	-74.47	2.1
Triangular	-106.05	1.79
Si-1 [179]	-78.84	1.98
Si-2 [180]	-96.9	1.76
Si-3 [176]	-39.6	1.40
Si-4 [190]	-46.5	1.64
Si-5 [185]	-39.1	1.58
Si-6 [197]	-39.2	1.52
Si-7 [198]	-96.9	2.03

Influence of cross-section shape and size: For optical phonon shift the MVFF model predicts a width exponent factor d_{opt} between 1.8 and 2 (Table 6.3) for all the cross-section shapes. The [100] triangular SiNWs show the maximum optical red shift (d_{opt} = 1.795) whereas the square SiNWs show the minimum optical red shift (d_{opt} = 2.06, close to the prediction in Ref. [179]) (Fig. 6.8). Furthermore, with decreasing cross-section size (W) all the wires show an increasing optical red-shift (Fig. 6.8).

The d_{opt} and A_{opt} values for optical phonon frequency shift in SiNWs from other experimental data and theoretical models are provided in Table 6.3. The combination (d_{opt}, A_{opt}) for Si-1 indicates a roughly square SiNW which is indeed the structure used in Ref. [179]. The (d_{opt}, A_{opt}) combination for Si-2 directs towards triangular SiNWs. Experimentally the cross-section shapes are not very clear since the fabricated SiNWs are all bunched up together [180]. The value of d_{opt} and A_{opt} for Si-3 [176], Si-5 [185], and Si-6 [197] are smaller compared to the values obtained from MVFF model. This can be due to the use of (i) surface reconstruction (neglected in present study), and (ii) bulk phonon dispersion in these theoretical models. The d_{opt}, A_{opt} combination for Si-7 indicates a square SiNW which is indeed the case as provided in Ref. [198]. Thus, the optical coefficients provide a good correlation to the SiNW shapes as corroborated from other theoretical and experimental works. Hence, MVFF provides a reliable indicator for the SiNW shapes using the optical phonon red-shift.

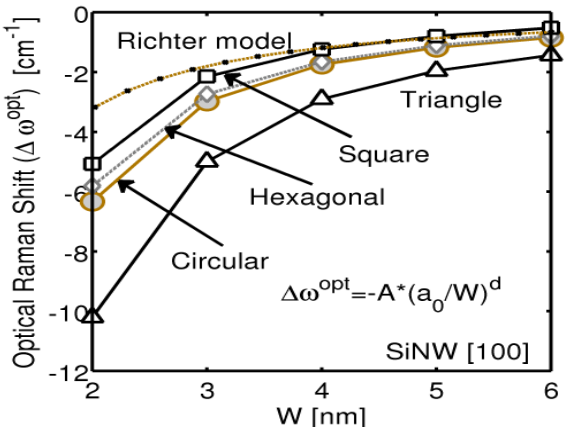

Fig. 6.8. Effect of cross-section shape on the optical phonon shift in [100] SiNWs.

Many explanations have been reported in the literature for the optical red-shift in nanostructures like, the increasing surface-to-volume ratio (SVR) [176,188], compressive strain [175], surface defects [201] and optical phonon confinement [188–190, 202]. In the present study of free-standing SiNWs the observed shape and size dependence can be explained using the vibrational energy density [200] of the optical mode as well as the optical phonon group velocity (V_{grp}^{ph}) [196].

Figure 6.9 shows the spatial distribution of the vibrational energy density for the optical mode in SiNWs with W = 4nm. The structure with the maximum spatial spread of the energy density has the most active optical modes [176] since surface atom vibrations contribute to the optical modes. The symbols in Fig. 6.9 show the FWHM extent of the energy density. The square wire has the maximum energy spread while the triangular wire has the minimum energy spread which explains the highest red-shift in the triangular wires (least active optical modes). As the SiNW dimensions decrease, the energy spread also decreases which increases the red shift for all the shapes.

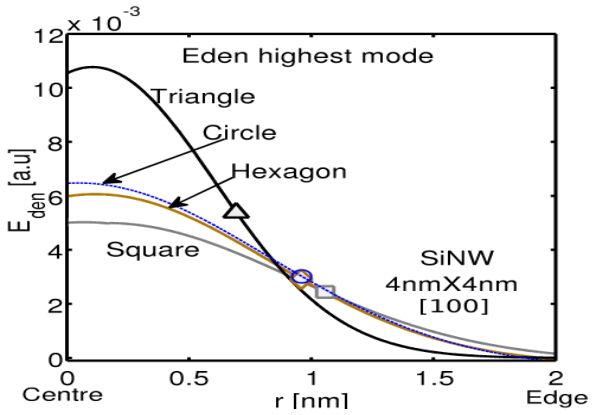

Fig. 6.9. Spatial vibrational energy density for optical modes in different cross-section shaped 4nm × 4nm [100] SiNWs. The symbols show the full width half maximum (FWHM) of energy density which reflect how active the optical mode is. A larger spatial spread indicates more active optical modes. Optical modes in square wires are the closest to the bulk ones and triangular wires are the farthest.

Another reason for the red-shift can be attributed to the phonon group velocity. Figure 6.10 shows that the triangular wire has the smallest group velocity whereas the square wire has the highest group velocity. A smaller group velocity implies higher phonon confinement [202]. Thus, the phonon group velocity gives the following order of optical phonon confinement; triangular > circular > hexagonal > square. Higher phonon confinement results in more red-shift. This again explains the observed shape dependence of optical red-shift in [100] SiNWs.

Orientation effect on phonon shifts

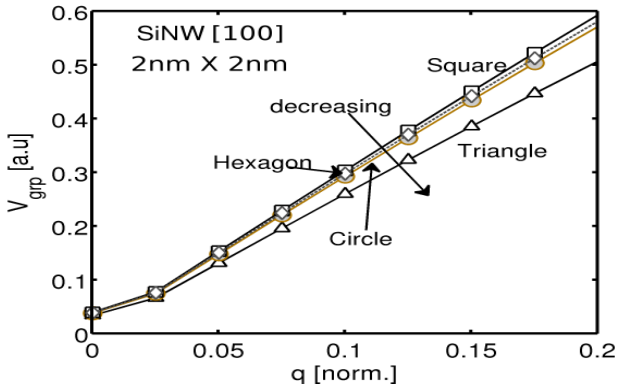

Fig. 6.10. Optical phonon group velocity in [100] SiNWs with 2nm × 2nm cross-section.

Along with the shape and size of the SiNWs, the wire axis direction can also produce different phonon shifts. This indicates that the confined phonon dispersion is anisotropic. For brevity the orientation effects for square SiNWs are only presented, however, these trends are also valid for other shapes. The acoustic phonon shift and the optical phonon shifts are shown in Fig. 6.11 a and b, respectively. The acoustic phonon blue shift exhibits a strong anisotropy (Fig. 6.11 a), however, the optical red shift has a very weak orientation dependence (6.11 b). This observed behavior of phonon shift can be explained by the phonon dispersion anisotropy in Si. In Si the maximum phonon frequency of the acoustic branch along [100], [110] and [111] directions are highly anisotropic [50, 151], whereas the maximum frequency of the optical branches are isotropic (∼519.3 cm^{-1}). The acoustic blue shift show the following behavior $\Delta\omega_{ac}^{100} > \Delta\omega_{ac}^{111} > \Delta\omega_{ac}^{110}$. The cross-section size dependence for both kind of phonon shifts are provided in Table. 6.4. The acoustic phonon shift exponent of [110] wires is 0.89 which compares reasonably to the exponent of 0.95 observed for [110] SiNWs in Ref. [156] (see Fig. 6.4).

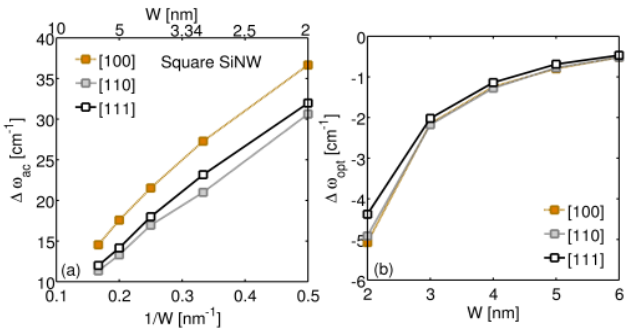

Fig. 6.11. Effect of SiNW orientation on (a) acoustic phonon shift and (b) optical phonon shift.

Table 6.4
Width parameters for acoustic and optical phonon shift in square SiNWs with different orientations

Channel Or	A_{ac} (cm^{-1})	d_{ac}	A_{opt} (cm^{-1})	d_{op}
[100]	106	0.81	-74.62	2.06
[110]	98.34	0.89	-66.47	2.00
[111]	100.7	0.87	-57.17	1.97

6.2.4 Summary of the work

At the nanometer scale the acoustic phonon shift is quite sensitive to the (i) wire cross-section size and shape, and (ii) wire channel orientation whereas the optical phonon shift is mainly controlled by the wire cross-section shape and size. The different width exponents and the pre-factors from the acoustic and optical phonon shifts can become a useful tool in predicting the size and shape of the SiNWs. Triangular wires show the highest optical phonon confinement and the least structural symmetry.

6.3 Thermal properties of Si Nanowires

Thermal transport measurements using techniques like 3ω method [203] and thermo-reflectance [204] have led to a good understanding of the heat flow in large nanowires

(diameter > 30nm). However, the physics of heat flow for ultra-scaled SiNWs is still not well understood [151]. The phonon spectra of SiNWs can provide a theoretical estimate about the heat transport in the ultra-scaled regime since phonons (lattice vibrations) are responsible for carrying most of the heat in semiconductors [138, 151, 153, 200].

This section explores the effect of (i) cross-section geometry, (ii) cross-section size, and (iii) wire orientation of ultra-scaled SiNWs on the thermal properties like ballistic thermal conductance (κ_l^{bal}) and specific heat (C_v). Furthermore the analytical expressions for the variation in these quantities with size for each cross-section shape and orientation are provided enabling a compact modeling representation of thermal properties which can be used in simulators like Thermal-Spice [62] and Thermoelectric module simulator [205].

Thermal properties of SiNWs differ considerably from bulk Si [151, 206]. The transition from the particle to wave nature of heat transport with structural miniaturization also calls for improved heat transport models. The traditional continuum models for thermal conductivity by Callaway [207] and Holland [208] are based on the Debye limit for phonons, sound velocity and many other parameters, which render these models quite cumbersome at the nano-scale, as discussed by Mingo et al [138]. Dependence of continuum models on too many open fitting parameters make them unsuitable for predicting the thermal properties with dimensional scaling. This is overcome by the atomistic MVFF model (see Chapter 5) which can automatically take into account the effects of structural miniaturization like geometrical confinement, orientation effects, cross-sectional shape and surface-to-volume ratio effects.

The complete phonon dispersion of SiNWs are used for obtaining the, (i) constant volume temperature (T) dependent specific heat ($C_v(T)$), and (ii) the thermal conductance (κ_l^{bal}) as described in Sec. 5.5 of Chapter 5. This section also uses the same SiNW unitcells for study as used in Sec. 6.2.2.

The SiNWs used in this section are the same as used in Sec. 6.2.2.

6.3.1 Results and Discussion

In this section the results on the effect of cross-section shape, size and orientation on the thermal properties of SiNWs are presented and discussed. All the thermal quantities are calculated at 300K. However, the analysis holds for any temperature (T) where the anharmonic phonon effects are small. For T < T_{Debye} the anharmonic interactions are quite small [200]. For bulk Si, T_{Debye} ~725K [209] and it further increases for SiNWs [194].

Specific heat in SiNWs

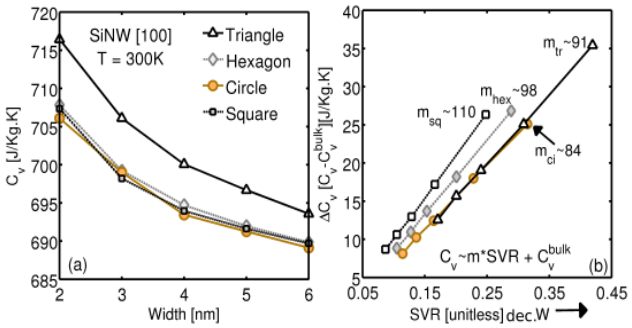

Fig. 6.12. (a) Dependence of the specific heat (C_v) on cross-section shape and size in [100] SiNWs. (b) Variation in ΔC_v ($= C_v - C_v^{bulk}$) with SVR for all the [100] SiNW shapes. C_v^{bulk} for each shape is provided in Table. 6.6.

Influence of the shape and size on C_v: The C_v of SiNWs increases with decreasing cross-section size for all wire shapes (Fig. 6.12a). The size dependence of C_v can be approximated by the following relation [210],

$$C_v(W) = C_v^{bulk} + \frac{A}{W}. \tag{6.3}$$

Table 6.6 shows the value of C_v^{bulk} and A for each geometry. As W $\rightarrow \infty$ (increasing cross-section size), the C_v of all the SiNWs converges to a fixed value of ~681 J/kg.K which is in reasonably close to the experimental bulk Si C_v value (as provided in

Refs. [210, 211]). The triangular wires show the maximum C_v for all the W value, whereas the other shapes show similar C_v values at any given cross-section size (Fig. 6.12a).

Table 6.5
Width Parameter for C_v in [100] SiNWs at T = 300K.

Shape units →	C_v^{bulk} $(J/kg \cdot K)$	A $(J \cdot nm/kg \cdot K)$
Circular	681.4	47.82
Hexagon	681.2	53.58
Square	680.9	52.66
Triangular	681.0	73.43

The plot of ΔC_v $(=C_v^{wire} - C_v^{bulk})$ vs. SVR (SVR = Total surface Atoms/Total atoms in unit cell) shows a linear behavior (Fig. 6.12b), which can be represented as,

$$C_v^{wire} \approx m_c \times \text{SVR} + C_v^{bulk}, \tag{6.4}$$

where m_c represents the additional contribution to the C_v of the SiNWs with increasing surface-to-volume ratio. The value of m_c is positive for all the wire shapes (Fig. 6.12b) which corroborates the fact that specific heat increases with increasing surface area [210]. The atomistic effects no the C_v variation in the ultra-scaled SiNWs is clearly illustrated here. As the wire size increases the SVR $\rightarrow$ 0 and C_v^{wire} converges towards the bulk value.

The C_v increase with decreasing W can be attributed to two reasons, (i) phonon confinement due to small cross-section size and (ii) an increased surface-to-volume ratio (SVR) in smaller wires [196, 210]. With increasing geometrical confinement (smaller cross-section size) the phonon bands are separated more in energy [196] which makes only the few lower energy bands active at a given temperature (see Eq.(5.31)). Thus, more energy is needed to raise the temperature of the smaller wires.

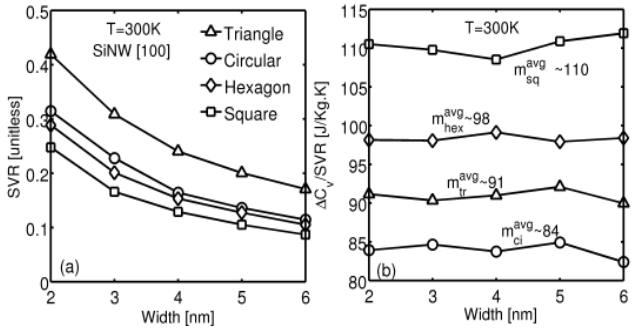

Fig. 6.13. (a) Surface-to-volume ratio (SVR) for different cross-section shape and size [100] SiNWs. (b) Incremental contribution to the specific heat with SVR for different cross-section shape [100] SiNWs.

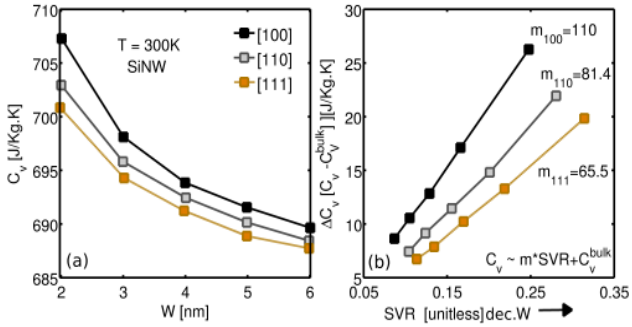

Fig. 6.14. (a) Dependence of the specific heat (C_v) on the orientation of square SiNWs. (b) Variation in ΔC_v ($= C_v - C_v^{bulk}$) with SVR for all the SiNW orientations. C_v^{bulk} are taken from the Table. 6.6.

The shape dependence of the C_v can be understood from Eq.(6.4). The variation of (i) SVR, and (ii) m_c with W for different shapes decide the eventual C_v order. Figure 6.13(a) shows that triangular wires have the maximum SVR while the other shapes have similar SVR at a fixed W. The increasing SVR results in a higher partial phonon DOS associated with the wire surface, which further enhances the specific heat with decreasing wire cross-section [210]. The variation in m_c (ΔC_v/SVR) shows that square wires provide the largest surface contribution to C_v (Fig. 6.13b). An optimal value of SVR and m_c in SiNWs will maximize the C_v. The product $SVR \times m_c$, show the following order, triangle (∼36) > hexagonal (∼29) > square (∼27) > circular

(∼26). Thus, triangular wires show the highest C_v due to the highest SVR. However, other shapes show opposite trends for SVR ($SVR_{sq} < SVR_{hex} < SVR_{ci}$) and m_c ($m_c^{sq} > m_c^{hex} > m_c^{ci}$) thus, showing almost similar C_v values. The C_v values shows the following shape order in [100] SiNWs: *triangular* > *hexagonal* ≈ *square* ≈ *circular.*

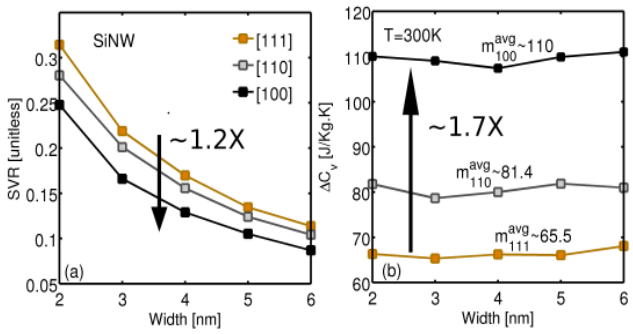

Fig. 6.15. (a) Surface-to-volume ratio for different wire orientations of square SiNWs. (b) Incremental contribution to the specific heat with SVR for different orientations of SiNWs.

Influence of orientation on C_v: The specific heat also shows variation with SiNW orientation (Fig. 6.14a). The C_v varies inversely with W, similar to the trend calculated for different shapes (Eq.(6.3)). The width parameters (Eq.(6.3)) for the variation in C_v with orientation are provided in Table 6.6. The ΔC_v value again shows a linear variation with SVR for different wire orientations (Fig. 6.14b). The C_v trend shows the following order with size, $C_v^{100} > C_v^{110} > C_v^{111}$. This trend can be explained again by looking at the impact of (i) SVR and (ii) m_c (Eq.(6.4)) on the overall C_v value. The SVR shows the following order with W, $\text{SVR}^{111} > \text{SVR}^{110} > \text{SVR}^{100}$ (inc. of ∼1.2× from [100] to [111]) as shown in Fig. 6.15a. However, m_c shows the following order with W, $m_c^{100} > m_c^{110} > m_c^{111}$ (dec. of ∼1.7× from [100] to [111]) (Fig. 6.15b). *The larger incremental surface contribution to the C_v plays a more crucial role over total available surface area in deciding the C_v trend for SiNWs with different orientations.*

Table 6.6
Width Parameter for C_v in [100] SiNWs at T = 300K.

Shape units →	C_v^{bulk} $(J/kg \cdot K)$	A $(J \cdot nm/kg \cdot K)$
Circular	681.4	47.82
Hexagon	681.2	53.58
Square	680.9	52.66
Triangular	681.0	73.43

Ballistic thermal conductance in SiNWs

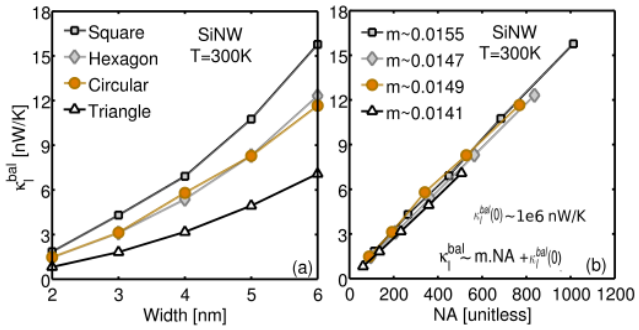

Fig. 6.16. (a) Effect of cross-section shape and size on the ballistic thermal conductance of [100] SiNWs. (b) Variation in κ_l^{bal} with the total number of atoms in the unit cell (NA) for different cross-section shapes.

Influence of shape and size on κ_l^{bal}: The ballistic thermal conductance (κ_l^{bal}) for 4 different shapes (Fig. 6.1) of [100] SiNWs are calculated as shown in Fig. 6.16a. The κ_l^{bal} can be fitted according to the following size (W) relation,

$$\kappa_l^{bal}(W) = \kappa_0 \left(\frac{W}{a_0}\right)^d, \tag{6.5}$$

where a_0 is the silicon lattice constant (0.5431 nm), d is a power exponent and κ_0 is a constant of proportionality. The values of 'd' and κ_0 for different wires shapes are

shown in Table 6.9. The value of d varies between 1.92 and 2.011 which implies that κ_l^{bal} shows a similar size dependence for all the wire shapes. However, the pre-factor value (κ_0) reflects the shape dependence. This pre-factor has the same ordering as the thermal conductance ordering (Fig. 6.16a).

Table 6.7
Width Parameter for κ_l^{bal} in [100] SiNWs at T = 300K.

Shape	κ_0 (nW/K)	d
Circular	0.133	1.92
Square	0.141	1.96
Triangular	0.062	1.97
Hexagon	0.097	2.01

The ballistic thermal conductance shows a linear behavior with the number of atoms in the unit cell (NA) as shown in Fig. 6.16b. This linear relation can be approximated by the following equation,

$$\kappa_l^{bal} \approx m_k \times NA + \kappa_l^{bal}(0), \tag{6.6}$$

where, the slope m_k represents the average contribution from each atom in the unit cell to κ_l^{bal} and $\kappa_l^{bal}(0)$ is the thermal conductance at NA = 0. The value of $\kappa_l^{bal}(0)$ is almost close to zero which is expected for NA = 0. The value of m_k takes into account the surface, shape and atomic effects since the calculation procedure involves the complete phonon dispersion. This relation shows a direct correlation of the atomistic effects to the ballistic thermal conductance.

The size dependence can be explained by the fact that the larger wires have, (i) more phonon sub-bands resulting in more number of modes ($M(\omega)$ in Eq.(5.30)) and (ii) a higher acoustic sound velocity which is responsible for larger heat conduction in these SiNWs [196].

The shape dependence can be explained as an interplay of the two effects, (i) the total number of atoms (NA) present in the unit cell of SiNWs, and (ii) the average

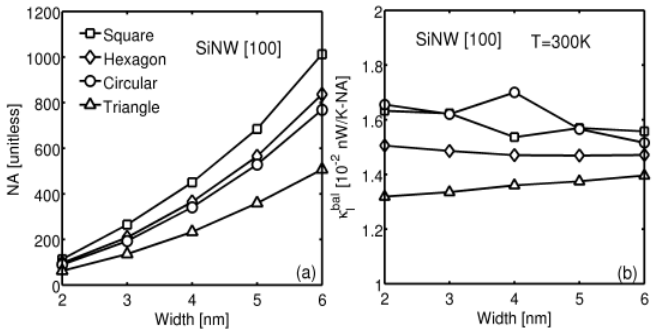

Fig. 6.17. (a) The number of atoms (NA) in [100] SiNW unit cell for different cross-section size and shapes. (b) Contribution to κ_l per atom for different cross-section shapes.

contribution of every atom towards κ_l^{bal}. For a fixed cross-section size W, the NA ordering is; $NA_{sq} > NA_{ci} > NA_{hex} > NA_{Teri}$ (Fig. 6.17a). The total number of phonon branches are 3×NA, due to the three degrees of freedom associated with each atom [212]. The number of phonon modes ($M(\omega)$) is directly proportional to the phonon energy sub-bands. The per atom contribution to thermal conductance (m_k) stays almost constant with wire cross-section size for a given shape (Fig. 6.17b). *Since, the values of m_k are quite similar for all the cross-section shapes , the ordering of NA with shape governs the dependence of κ_l^{bal} on the cross-section shape.*

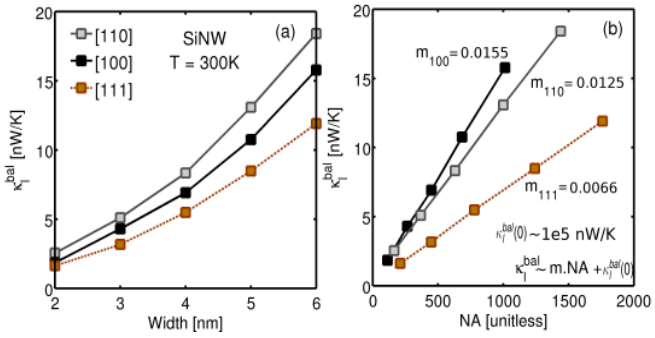

Fig. 6.18. (a) Effect of size on the ballistic thermal conductance in SiNWs with different orientations. (b) Variation in κ_l^{bal} with the total number of atoms in the unit cell (NA) for different wire orientations.

Table 6.8
Width Parameter for κ_l^{bal} in SiNWs at T = 300K.

Orientation	κ_0 (nW/K)	d
[100]	0.141	1.96
[110]	0.204	1.87
[111]	0.129	1.88

Influence of wire orientation on κ_l^{bal}: The thermal conductance is anisotropic in SiNWs with the following order, $\kappa_l^{110} > \kappa_l^{100} > \kappa_l^{111}$ (Fig. 6.18a). This result is similar to the one reported in Ref. [151]. The κ_l value shows linear variation with NA for all the wire orientations (Fig. 6.18b). The width parameters for the thermal conductance (Eq.(6.5)) for different wire orientations are provided in Table 6.8. The order of the ballistic thermal conductance with W for different orientations can be understood by the product of NA$\times m_k$ (P_{nm}). The NA shows the following variation, $NA^{111} > NA^{110} \; NA^{100}$ (Fig. 6.19a), whereas m_k shows the following order $m_k^{100} > > m_k^{110} > m_k^{111}$ (Fig.6.19b). These two orders are reverse of each other. However, the product shows the following order, $P_{nm}^{110} > P_{nm}^{100} > P_{nm}^{111}$). Thus, [110] wires show highest κ_l due to the optimal value of NA and m_k.

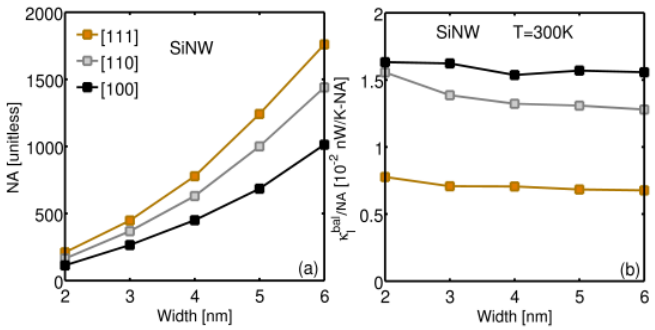

Fig. 6.19. (a) The number of atoms (NA) with W in one SiNW unit cell for different orientations. (b) Contribution to κ_l per atom for different SiNW orientations.

An important point to note here is that κ_l^{bal} is expected to decrease further in smaller wires due to phonon scattering by other phonons, interfaces and boundaries [138,153] which is neglected in the present study. The main idea here is to understand the geometrical effects on the phonon dispersion and the thermal properties of these small nanowires which is attributed to (i) the modification of the phonon dispersion, and (ii) phonon confinement effects in the coherent phonon transport regime.

6.3.2 Universal scaling of thermal properties

All the thermal properties are shown to scale with W. Also NA depends on W as follows,

$$NA \propto W^{\gamma}, \tag{6.7}$$

where $\gamma > 0$. So using Eq.(6.7), Eq.(6.3) and Eq.(6.5) can be re-casted in terms of NA as,

$$\begin{aligned} \Delta C_v(NA) &= C_0 \cdot (NA)^{\frac{-1}{\gamma}} \qquad (6.8) \\ &= C_0 \cdot (NA)^{-\eta} \\ \kappa_l^{bal}(NA) &= K_0 \cdot (NA)^{\frac{d}{\gamma}} \qquad (6.9) \\ &= K_0 \cdot (NA)^{\rho}, \end{aligned}$$

where, C_0 and K_0 are the pre-factors. Thus, a universal power law can be derived for the thermal properties depending on the number of the atoms in the unit cell which represents the pure atomistic effect on the thermal quantities. In these SiNWs, $1.98 \leq \gamma \leq 2.1$ which provides the limits for ρ and η,

$$\rho \in [0.93\ ,\ 1.03] \tag{6.10}$$

$$\eta \in [0.48\ ,\ 0.50] \tag{6.11}$$

The variation in the thermal conductance with NA is shown on a log-log scale in Fig. 6.20a. All the SiNWs show almost the same power law with an average exponent value of ∼0.97, which is in the limit derived in Eq.(6.10). Similarly the variation in C_v with NA is shown on a log-log scale in Fig. 6.20b. All the SiNWs used in this study show the same power law (Eq.(6.8)) with average exponent as -0.51, which is in the limit derived in Eq.(6.11). Thus, the thermal quantities show a universal power law behavior with the number of atoms in the unit cell (NA) irrespective of the details of the unit cell. The details of shape and orientation are embedded in the pre-factors C_0 and K_0 (Eq.(6.8) and (6.9)).

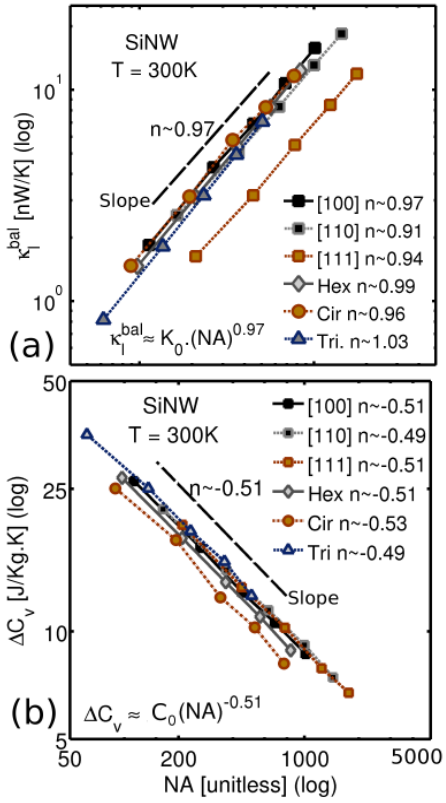

Fig. 6.20. (a) The number of atoms (NA) in one [100] SiNW unit cell for different cross-section size and shapes. (b) Contribution to κ_l per atom for different cross-section shapes.

The relationship of C_v and κ_l to the shape, size and orientation of SiNWs have been provided. The explicit equations for the same have been provided (Eq.(6.3),

(6.4), (6.5), and (6.6). These closed form analytical expressions are very handy for compact modeling of thermal and thermoelectric properties of SiNWs [62,205]. Since, these expression are derived from physics based model, they capture the important geometrical and atomistic effects thus, enabling fast modeling of realistic systems. This proves the utility of the present work from a thermal compact modeling point of view.

6.3.3 Summary of the work

The thermal properties are sensitive to the wire cross-section size, shape and orientation. The thermal properties follow a universal power law with the number of atoms in the unitcell in SiNWs revealing the atomistic effects on the thermal properties reveals the direct atomistic impact on these properties at the nanometer level. Triangular SiNWs show higher C_v and low κ_l, thus making them good candidate for thermoelectric devices whereas the [110] oriented square Si nanowires are better in terms of heat dissipation due to their higher thermal conductance.

6.4 Evolution of structural and thermal properties in Si Nanowires

An important aspect of all the physical properties in these ultra-scaled SiNWs is that as the wire cross-section size increases the these properties are expected to move towards the bulk values. This allows to check the correctness of the theory and how large SiNWs can be used effectively for shape engineering of the physical properties.

6.4.1 Impact on phonon shifts

The acoustic and optical phonon shifts are expected to vanish as the wire cross-section size increases. With increasing size the geometrical confinement and the surface effects on the phonons are expected to reduce. Acoustic phonon blue shift shows very weak shape dependence for W $>$ 7nm (Fig. 6.21) and optical phonon red

shift shows diminished shape dependence for W > 10nm (Fig. 6.21). For wires larger than these critical size limits it will be harder to distinguish between the shapes by just analyzing the phonon shift data.

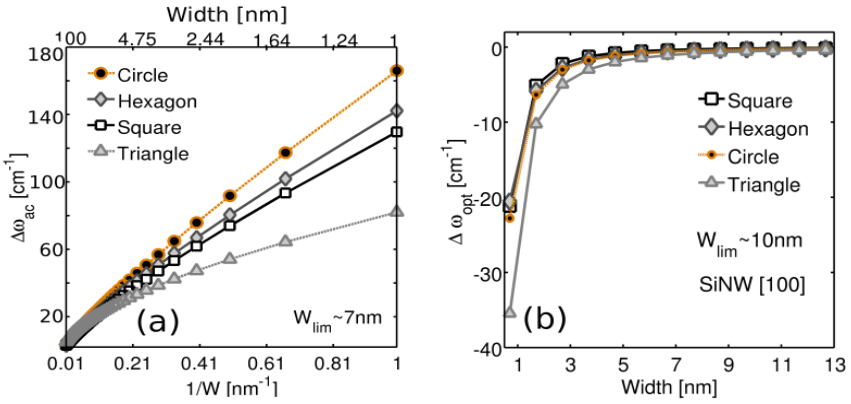

Fig. 6.21. Diminishing shape effect on (a) acoustic phonon shift, (b) optical phonon shift.

6.4.2 Impact on thermal properties

The thermal properties also move towards bulk values with increasing cross-section size for different wires shapes. Wire specific heat does not show much shape dependence for W beyond 30nm (Fig. 6.22). For thermal conductance this limiting size is much larger, around 200nm (Fig. 6.23). Similar diminishing shape effect for κ_l has been also observed in another theoretical work [209]. Thus, κ_l can be tuned for much larger wires using shape compared to C_v.

6.4.3 Summary of the work

All the structural and thermal properties move towards the bulk values as the cross-section size of the SiNWs increase. This points out the correctness of the MVFF model. Every physical property evolve at a different rate with cross-section size and hence have a very different meaning for the bulk material.

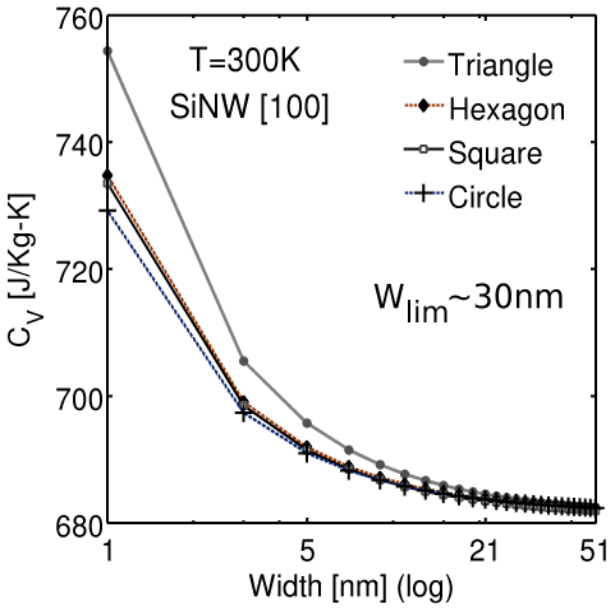

Fig. 6.22. Diminishing shape effect on C_v in [100] SiNW. All the wires converge to the bulk C_v value of $\sim$ 690 J/kg.K

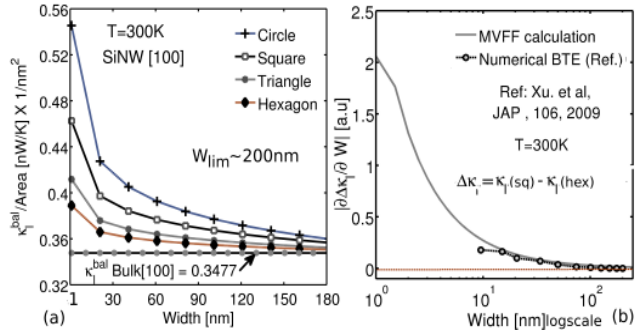

Fig. 6.23. (a) Diminishing shape effect for the normalized lattice thermal conductance (κ_l/area of wire cross-section). All the SiNWs converge to the bulk value of 0.3477 $nW/K.nm^2$. For bulk Si the effective area is taken to be $a_0^2/4$ nm^2, where a_0 is the Si lattice constant. (b) MVFF provides similar shape diminishing effect as provided in Ref. [209].

6.5 Summary and Outlook

The MVFF phonon model provides an adequate method to calculate the phonon shifts as well as thermal properties in SiNWs. The phonon shift results from theory

Table 6.9
Bulk Size for each physical property [100] SiNWs

Property	Temp (K)	W_{lim}
Ac. shift	300	7
Opt. shift	300	10
Cv	300	30
κ_l	300	200

agrees quite well with the experimental Raman shift data. An experimentally benchmarked phonon shift provided by the MVFF model correlates very well with the SiNW shape, size and orientation. This provides a good metrology method to identify the nano-scale structures. The thermal properties are also sensitive to the wire cross-section size, shape and orientation. The atomistic effect on thermal properties is revealed by the universal dependence on the number of atoms in the unitcell of a SiNW. Analytical expressions for the shape and size dependence of the phonon shifts and thermal properties are useful for compact modeling of physical properties of ultra-scaled SiNWs [62, 205]. The meaning of bulk material for different physical properties are quite different. Phonon shifts evolve very rapidly to move towards the bulk values compared to the thermal properties. The inclusion of phonon scattering in the study of thermal properties can form a useful future work.

7. ENGINEERING LATTICE THERMAL PROPERTIES IN NANOWIRES

7.1 Introduction and Motivation

Modulation of the lattice thermal conductivity (κ_l) in semiconductor devices has received a lot of focus in the recent times due to its vast engineering potential [166, 213]. Lower thermal conductance is beneficial for thermoelectric devices whereas higher thermal conductivity ensures better heat evacuation from the MOSFETs. The main techniques used for tuning thermal conductivity are, (i) nanostructuring such as making thin films [34] and nanowires [214], (ii) nanocomposities [5, 19], (iii) superlattice structures [215], (iv) porous nanostructures [59, 200, 216], and (v) strain [217, 218].

Along with these experimental methods, a proper theoretical development for understanding the ways to engineer κ_l in nanostructures is also necessary. The MVFF phonon model and the thermal transport models, outlined in Chapter 5, provide a very good starting point to understand the implications of porosity, strain and superlattice structures at the nano-scale. This chapter investigates the effects of strain, porosity and superlattices on the thermal properties of silicon and germanium nanowires. These materials are studied since these materials are compatible to the present CMOS process flows making them technologically more favorable to be used for different applications.

This chapter is organized as follows. Section 7.2 discusses the utility of porous Si and Ge nanowires for tuning thermal conductivity for making better thermoelectric devices. The investigation on the effect of strain on the phonons and thermal properties in Si are provided in Sec. 7.3. Thermal transport in SiGe superlattice nanowires is discussed in Sec. 7.4. Summary and outlook are provided in Sec. 7.5.

7.2 Tuning κ_l^{bal} by porosity control in ultra-scaled Si and Ge nanowires

Recent experimental works [32, 33] reveal that the nanowire geometry can greatly enhance the ZT of Si (upto 1 at 200K [33]) from its bulk value of 0.06 at 300K [219] by suppressing κ_l. The lattice thermal conductivity in bulk Si can be suppressed, as shown both experimentally [59, 220] and theoretically [38], by creating pores in the crystalline material. More recently the fabrication of a phonon 'nano-mesh' [59] showed a 100 fold reduction in κ_l from the bulk Si value of 148 W/m-K to 1.9W/m-K. Recent technological developments enable the fabrication of hollow nanowire arrays using sacrificial templates [21], hollow spinel wires using the 'Kirkendall effect' [22], electrochemical anodic dissolution [221] and template based hollow wire fabrication [222]. Surface scattering affects phonons and the associated thermal conductivity (κ_l) more drastically than electrons, due to the smaller coherent phonon wavelength than electrons [38].

In this section the ballistic thermal conductance (κ_l^{bal}) in hollow Si and Ge nanowires with various channel orientations ([100], [110] and [111]) are theoretically explored. A systematic study to understand the impact of (i) pore size, (ii) pore density and (iii) pore distribution on κ_l^{bal} of ultra-scaled nanowires is carried out. This allows us to identify ways to better tune l and hopefully guide the improved fabrication methods [21, 22, 221, 222] to obtain better TE structures made of Si and Ge. Furthermore the reasons for the reduction in κ_l^{bal} are also discussed.

7.2.1 Nanowire details

Rectangular NWs are studied with width (W) and height (H) varying from 3nm to 5nm with three channel orientations of [100], [110] and [111]. The number of pores varies from 1 to 4 as shown in Fig. 7.1. The pore radius R_h varies from 0 to 0.8nm. The separation between the pores (d_{sep}) is varied from 0 to 1nm in steps of 0.2nm each. The meaning of d_{sep} for each case is shown in Figure 7.1. There are multiple ways to create separation among the pores. The idea is to understand the impact

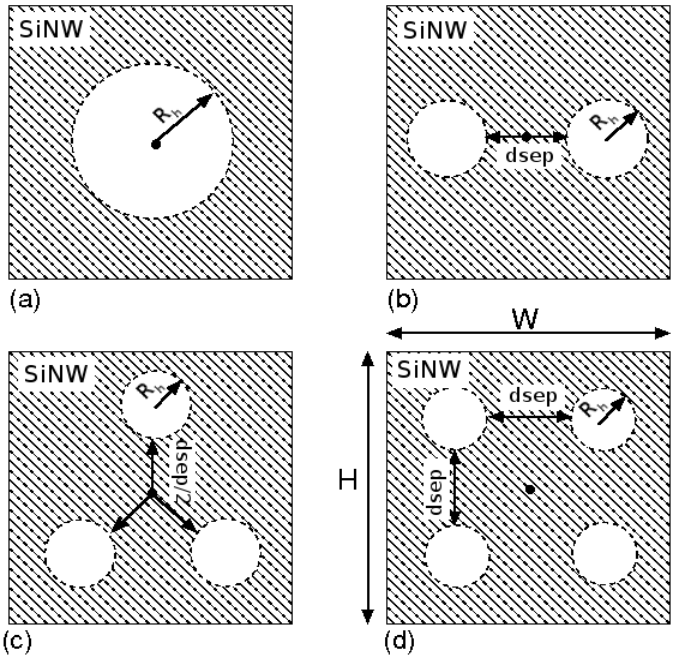

Fig. 7.1. Schematic of SiNWs with different pore density, (a) 1 pore, (b) 2 pores, (c) 3 pores and (d) 4 pores. The width (W) and height (H) of the SiNWs vary between 3nm to 5nm. To understand the impact of pore density on the ballistic thermal conductance (κ_l^{bal}) a similar percentage of atoms (12 %) are removed for all the cases (a-d) The separation between the holes (d_{sep}) is also changed from 0 to 1nm in steps of 0.2nm to study the impact of pore distribution on κ_l^{bal}.

of pore separation in an ordered manner. These pores could be generated randomly too (close to experiments). The R_h value has been chosen such that not more than 12-13% of the total atoms (Fig. 7.2) have been removed from the unitcell to ensure structural stability of these wires (no negative phonon dispersion is obtained [156]). The inner and outer surface atoms in these NWs are allowed to vibrate freely (Fig. 7.2). Extremely small SiNWs ($W \leq 1nm$) have been excluded from the present study since significant atomic reconstruction can take place in such wires [195].

7.2.2 Results and Discussion

The effect of pores on the phonon dispersion and κ_l^{bal} are provided in this part.

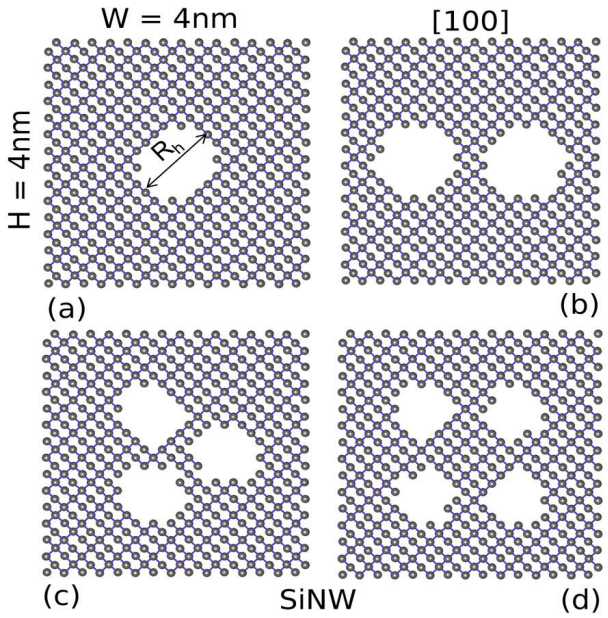

Fig. 7.2. Projected atomic structure of hollow Si unitcells with [100] channel orientation.(a) 1 pore case, (b) 2 pores, (c) 3 pores, and (d) 4 pores. SiNW has cross-section size of 4nm(W) × 4nm(H).

Phonon spectra of hollow SiNWs

Hollow nanowires have fewer atoms per unitcell compared to the solid nanowires which results in a reduced number of total phonon sub-bands. Figure 7.3 shows the phonon spectra of a 4nm × 4nm [100] SiNW with different pore densities. In the hollow NW a lot of flat phonon sub-branches appear in the lower energy portion of the phonon spectra (Fig. 7.3a and b) indicating slower phonons. The presence of 3 and 4 pores in a 4nm X 4nm SiNW brings down 14 and 18 sub-bands below 7 meV, (this energy value is chosen arbitrarily) respectively (Fig. 7.3a and b). However, a same sized filled (solid) SiNW has only 10 phonon sub-bands below 7meV (Fig. 7.3c). The sound velocity in these hollow wires reduce by ∼30% compared to the solid nanowires showing the presence of slow moving phonons in porous nanowires.

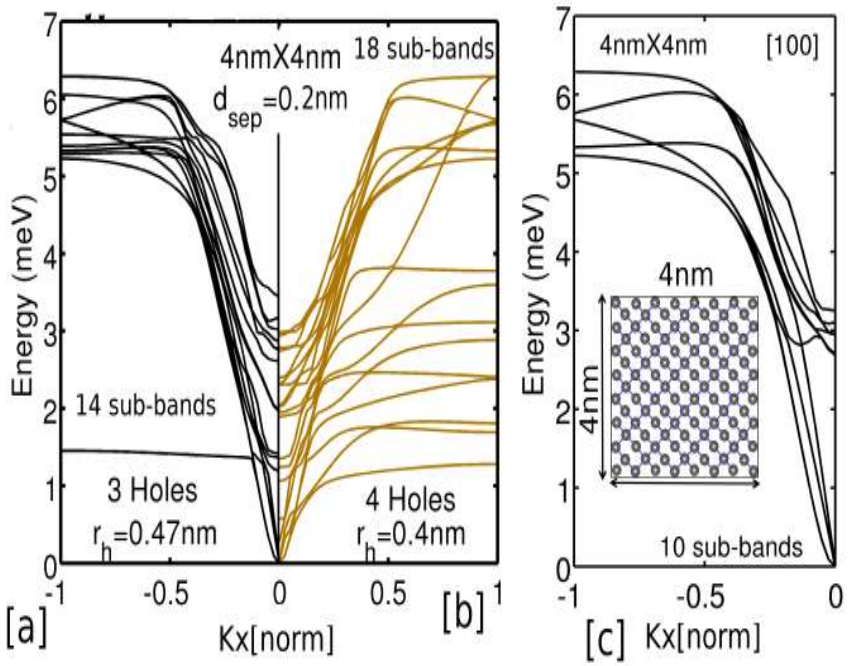

Fig. 7.3. Phonon dispersion for 4nm × 4nm hollow [100] SiNW with (a) 3 pores (Rh=0.47nm) and (b) 4 pores (Rh = 0.4nm) with a separation of 0.2 nm among the pores. (c) Phonon dispersion for 4nm × 4nm filled square SiNW. Inset shows the projected atomic unitcell of the filled SiNW. Only the first 10 sub-bands are below 7meV for the filled SiNW where as 14 and 18 sub-bands are within 7meV for 3 and 4 pores, respectively.

Ballistic thermal conductance κ_l^{bal}

In all the nanowires κ_l^{bal} is calculated using Eq.(5.30) in Chapter 5. The impact of three main factors on κ_l^{bal} are studied below,

1. Effect of porosity size (R_h): The size of the pore has a direct influence on the thermal conductance. As a general trend, κ_l^{bal} reduces in hollow nanowires compared to the solid nanowires (Fig. 7.4). Comparison of κ_l^{bal} in Si and Ge NW show a similar amount of reduction in thermal conductance (Fig. 7.4a and b). This indicates a weak material dependence of the reduction mechanisms. A 3nm × 3nm Si(Ge) NW shows a reduction of ∼37%(38%) for r_h = 0.8nm. This reduction decreases as the wire cross-section size increases due to the reducing surface-to-volume ratio. The phonons

feel the surface less in larger cross-section NWs compared to the smaller wires. Thus, creating pores in smaller cross-section wires can reduce κ_l^{bal} more drastically compared to larger cross-section size NWs.

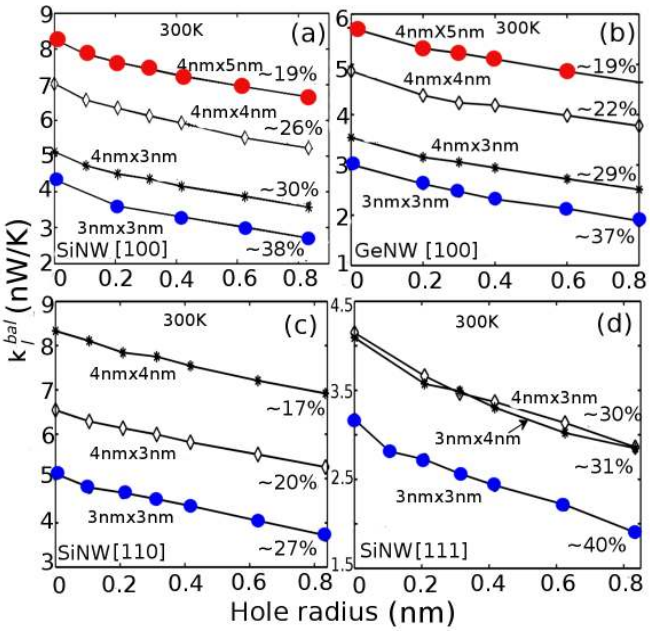

Fig. 7.4. Ballistic κ_l^{bal} in small cross-section rectangular nanowires. (a) [100] SiNW, (b) [100] GeNW, (c) [110] SiNW and (d) [111] SiNW. The percentage reduction in κ_l^{bal} for all the wires for $r_h = 0.8$nm is also indicated.

2. Effect of wire orientation: The κ_l^{bal} reduction is wire orientation dependent as revealed in Fig. 7.4a, c and d. For a 3nm × 3nm SiNW with $r_h = 0.8$nm, a [100] wire shows a reduction of ∼38% (Fig. 7.4a), a [110] wire shows a reduction of ∼27% (Fig. 7.4c) and a [111] wire shows a reduction of ∼40% (Fig. 7.4d). The κ_l^{bal} reduction shows the following order [111] $\approx$ [100] $>$ [110] for all the wire cross-section sizes considered here. Thus, κ_l^{bal} can be tuned by three ways, (i) wire cross-section size, (ii) hole radius and (iii) channel orientation.

3. Effect of porosity density and separation: The reduction in κ_l^{bal} shows a strong dependence on the number of pores in the SiNW (Fig. 7.5). At $d_{sep} =$ 0nm, all the pore cases show very similar reduction in κ_l^{bal} ($\sim$ 22% -23%) (Fig. 7.5).

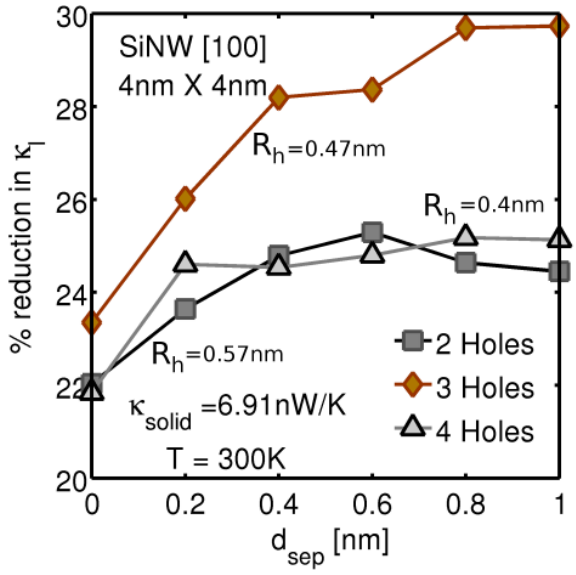

Fig. 7.5. Percentage reduction in κ_l^{bal} with hole density and their separation (d_{sep}) in a 4nm × 4nm [100] SiNW at 300K. Hole radius for 2 holes, 3 holes and 4 holes case is 0.57nm, 0.47nm and 0.4nm, respectively Approximately 12.5% atoms are removed in all the cases. The reduction in κ_l^{bal} increases with the separation in holes and also shows maximum reduction for the 3 holes case.

This is expected since at d_{sep} = 0nm all the cases coincide with the 1 pore case. As the separation between the pores increases, the κ_l^{bal} reduction shows different results for different pore density. The 2 and 4 pore cases show a reduction of $\sim$ 22% to 24% when the pore separation changes from 0nm to 1nm (Fig. 7.5). However, the 3 pore case shows a much higher reduction from $\sim$ 24% to 30% for the same change in pore separation (Fig. 7.5). This non-monotonic behavior of κ_l^{bal} reduction with pore density can be explained using phonon localization (discussed later). It turns out that the phonon mode reduction and mode participation reduction is higher for the 3 pores case. Hence, the pore density and their separation can be an effective way for tuning κ_l^{bal} as shown in Fig. 7.6. As a comparison, for the removal of $\sim$12% atoms 3 pore case can further decrease the κ_l^{bal} by $\sim$5-6% compared to the 1 pore case (Fig. 7.6).

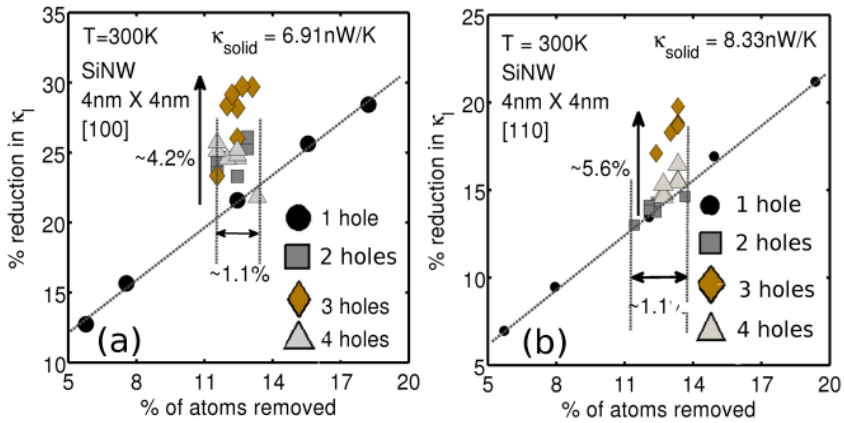

Fig. 7.6. Effect of higher pore density on κ_l^{bal} of SiNWs for (a) [100] oriented wires, (b) [110] oriented wires. Larger pore density with same number of atoms removed create at least 4 to 5% extra reduction in κ_l^{bal}

Even though there are larger number of phonon sub-bands in hollow nanowires (Fig. 7.3), these sub-bands are mostly flat and do not contribute a lot to the κ_l^{bal}. As shown in Fig. 7.7, higher number of phonon bands in hollow wires contribute more to κ_l^{bal} in the lower energy regime but soon the filled SiNW shows higher contribution due to the larger number of modes in higher energy range (Fig. 7.7 a and b). Thus, hollow wires still show an overall reduction in κ_l^{bal} compared to filled wires.

Reasons for the reduction in κ_l^{bal}

Creation of pores in SiNWs breaks the crystal symmetry which affects the phonon dispersion and causes a drop in l. In the coherent phonon limit, there are three main reasons responsible for the reduction in κ_l^{bal} :

1. Increased phonon localization in hollow nanowires.
2. Anisotropic modes which is orientation dependent.
3. Mode reduction in hollow nanowires.

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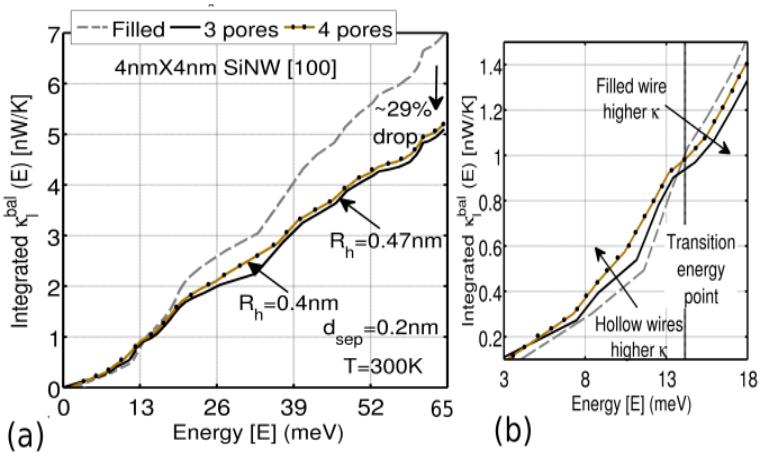


Fig. 7.7. (a) Sub-band contribution to the lattice thermal conductance for the three cases, (i) solid (ii) 3 pores (R_h=0.47nm) and (iii) 4 pores (R_h = 0.4nm) with a separation of 0.2 nm among the pores for a 4nm × 4nm hollow [100] SiNW with, at 300K. (b) A closer look at the variation in κ_l^{bal} for smaller energy range. Initially hollow wires show higher contribution but filled wire overtakes as sub-bands beyond 14meV start contributing.

1. Phonon localization: As the nanowire size reduces the geometrical confinement increases which results in increased phonon confinement [200]. All the phonon modes in hollow nanowires do not propagate well and become localized which reduces κ_l^{bal} compared to the solid Si and Ge NWs [200, 223]. The extent of localization of phonon modes can be calculated using a 'participation ratio' (PR) [223]. The participation ratio measures the fraction of atoms participating in a mode. This ratio can be calculated for each phonon mode as [223],

$$PR^{-1} = N\Sigma_i(\Sigma_{n,j\in[x,y,z]}\psi^*_{i,n,j}\psi_{i,n,j})^2, \tag{7.1}$$

where N is the total number of atoms in the unitcell, n and j represent the number of sub-bands and directional vectors, respectively and $\psi_{i,n,j}$ is the eigen vector associated with atom 'i', sub-band 'n' and direction 'j'. The eigen vectors are calculated from the MVFF dynamical matrix formulation as described in Chapter 5. The participation

ratio value varies between $O(1)$ for delocalized states to $O(1/N)$ for localized states and effectively indicates the fraction of atoms participating in a given mode.

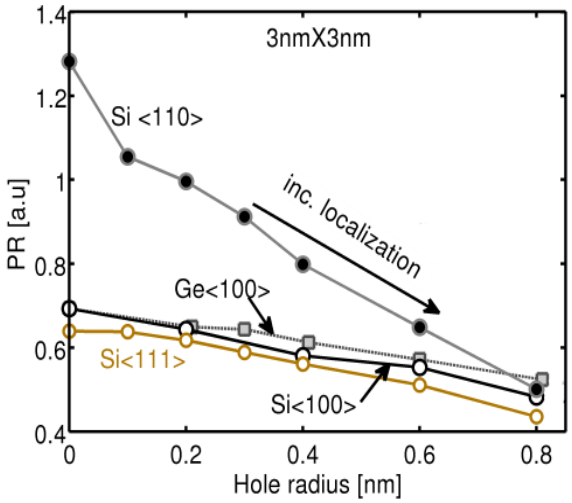


Fig. 7.8. Average participation ratio (PR) in Si and Ge NWs. PR reduces with increasing hole radius indicating increasing phonon localization in hollow NWs. This figure is adapted from Ref. [58].

The average PR in 3nm × 3nm, [100] Si and Ge NW shows a reduction with increasing r_h as shown in Fig. 7.8. The solid NWs have PR close to 0.7, showing delocalization, which gradually decreases indicating phonon localization. Thus, both Si and Ge show similar phonon localization and hence similar κ_l^{bal} reduction as shown in Fig. 7.4a and b. Therefore, a weak material dependence is predicted.

The PR value, for different pore densities, reduces more for 3 pores case as the pore separation increases compared to the 2 and 4 pore cases as shown in Fig .7.9. This explains the larger reduction in κ_l^{bal} for the 3 pores case (Fig.7.5) which has a higher phonon localization. This indicates that the 3 pores case breaks the crystal symmetry strongly.

2. Anisotropic phonon modes: The reduction in κ_l^{bal} with channel orientation shows anisotropy due to different propagating modes (M(E)) for each orientation. Figure 7.10 (a) shows that [110] wires have the largest number of modes while [100] and [111] wires have fewer modes [151]. The [100] and [111] wires show similar

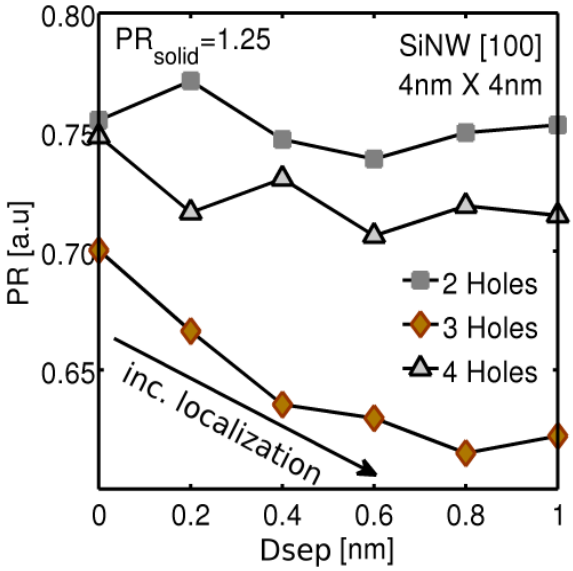


Fig. 7.9. Participation ratio (PR) indicating the localization of phonons in SiNWs. PR value for different types of pores in a 4nm × 4nm size SiNW. 3 pore case shows the maximum phonon localization.

decrease in total M(E) with R_h (Fig. 7.10a) which explains the similar reduction in κ_l^{bal}. The energy resolved modes (M(E)) for 3nm × 3nm SiNWs with $R_h = 0.4$nm (Fig. 7.10b) clearly shows higher number of modes in [110] orientation thus resulting in smaller reduction in κ_l^{bal}. Phonon localization also reflects that a [111] SiNW shows similar localization as [100] SiNW whereas, [110] SiNW shows less localization (Fig. 7.8). This further corroborates the anisotropic reduction of κ_l^{bal} in SiNWs.

3. Reduction in phonon modes (M(E)): The total number of phonon modes has a direct impact on κ_l^{bal} (Eq.(5.30), Chapter 5). The total number of phonon modes reduces with increasing pore size as shown in Fig. 7.10. A ∼7% reduction in modes with pore size (Fig. 7.11) reduces κ_l^{bal} by ∼ 30% for 3 pore case in a 4nm × 4nm [100] SiNW as shown in Fig. 7.5. Again the 3 pore case shows a higher reduction in total number of modes due to larger symmetry breaking which corroborates the larger reduction in κ_l^{bal}.

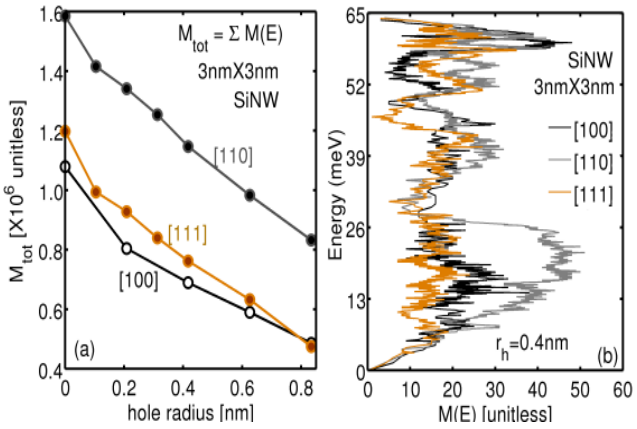


Fig. 7.10. (a) Total modes in hollow SiNWs for three channel orientations with hole radius. [110] has maximum modes. [111] and [100] are very close.(b) Modes distribution in energy for three channel orientations. Both plots are for 3nm × 3nm SiNWs. This figure is taken from Ref. [58].

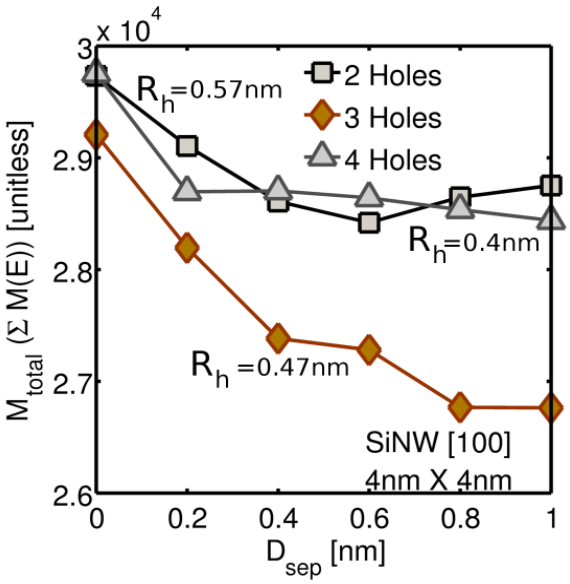


Fig. 7.11. Variation in the total number of modes with pore density in 4nm × 4nm [100] SiNW

7.2.3 Summary of the work

It has been shown that the presence of holes in Si and Ge NWs can be used for tuning their thermal conductance. Increased phonon confinement, phonon localization

due to increased surface-to-volume ratio and phonon mode reduction are the reasons for such drastic reduction in κ_l^{bal}. Thus, variation of nanowire cross-section size, pore radius, channel orientation, pore density and pore separation provide attractive ways to tune the thermal conductance. [100] and [111] nanowires show maximum reduction in κ_l^{bal} for Si. Similar trends are also expected in GeNWs. This can pave the way to make better TE devices using these nanowires.

7.3 Effect of strain on phonons and thermal properties

Semiconductor properties can be engineered [224,225] through the introduction of built-in stress by process engineering and by external forces like wafer bending [226]. The presence of strain changes the bond lengths and bond angles at the atomic scale which in turn affects the total crystal potential U (Chapter 5, Sec. 5.2.1). This crystal potential is composed of many individual contributions coming due to bond length (b_r) and angle (b_θ) change from the ideal values. Each individual contribution, U_{int}, can be expressed in the following form,

$$U_{int}(b_r, b_\theta) = \mathcal{S}(b_r, b_\theta) \cdot \mathcal{U}(b_r, b_\theta), \tag{7.2}$$

where $\mathcal{S}$ and $\mathcal{U}$ represent the interaction strength and form, respectively. The effect of the stress in U_{int} can be included in three following ways,

1. Change only $\mathcal{S}$ keeping $\mathcal{U}$ constant as provided in the work of Sui et. al. [50].
2. Change only $\mathcal{U}$ keeping $\mathcal{S}$ constant as provided in Ref. [146].
3. Change both $\mathcal{S}$ and $\mathcal{U}$ as adopted in the works [157, 160, 161].

All the three methods provide reasonable results when compared with the experimental Grüneisen values ($\gamma_{i,q}$) [50]. Under the action of hydrostatic strain the crystal is compressed without changing its symmetry. With pressure (P) the phonon frequency shifts, which is measured by $\gamma_{i,q}$ given as,

$$\gamma_{i,q} = -\frac{\partial(ln(\omega_{i,q})}{\partial ln(V)}, \tag{7.3}$$

$$= \frac{B}{\omega_{i,q}} \cdot \frac{\partial \omega_{i,q}}{\partial P}, \tag{7.4}$$

where, $\omega_{i,q}$ is the eigen frequency for the ith branch at a momentum q. The terms B, P, and V are the volume compressibility factor, pressure on the system, and volume of the crystal, respectively. This parameter is extracted by calculating the eigen frequencies at ambient conditions (P = 0) and at a small hydrostatic pressure ($\epsilon = \pm 0.02$) and then taking the difference in the calculated frequencies. The value of this parameter at high symmetry points (Γ, X, etc.) in the BZ can be measured experimentally by Raman scattering spectroscopy [227]. In this thesis method 1 is adopted for including the strain for phonon calculations. The details of the calculations are outlined in Ref. [50].

Branch name →	**TA1**	**TA2**	**LA**	**LO**	**TO1**	**TO2**	**Source**
K point ↓	**Bulk Silicon**						
Γ	NaN	NaN	NaN	0.979	0.979	0.979	MVFF
	--	--	--	0.98±0.06	0.98±0.06	0.98±0.06	Sui *et. al.*
X	-1.401	-1.401	0.987	1.071	1.498	1.498	MVFF
	-1.4±0.3	-1.4±0.3	1.03	1.03	1.5±0.2	1.5±0.2	Sui *et. al.*
L	-1.404	-1.404	0.486	1.546	1.208	1.208	MVFF
	-1.3±0.3	-1.3±0.3	0.45	1.62	1.24	1.24	Sui *et. al.*

Fig. 7.12. Grüneisen parameters for Bulk Si calculated using the MVFF model and bench-marked with other experimental and theoretical results provided in Sui et al. [50]. The calculated values compare very well with other calculations.

7.3.1 Verification of strain implementation in MVFF model

To ensure the strain model for MVFF works correctly the Grüneisen parameters are calculated for bulk Si and Ge using the MVFF model and bench-marked against other experimental data and theoretical models. These values are shown below. The references for the experimental data and theoretical results are provided in Ref. [50].

Branch name →	TA1	TA2	LA	LO	TO1	TO2	Source
K point ↓	Bulk Germanium						
Γ	NaN	NaN	NaN	0.959	0.959	0.959	MVFF
	--	--	--	0.96±0.05	0.96±0.05	0.96±0.05	Sui *et. al.*
X	-1.523	-1.523	1.037	1.12	1.487	1.487	MVFF
	-1.53±0.1	-1.53±0.1	1.17	1.17	1.49	1.49	Sui *et. al.*
L	-1.515	-1.515	0.552	1.57	1.19	1.19	MVFF
	-1.4	-1.4	0.55	1.67	1.28	1.28	Sui *et. al.*

Fig. 7.13. Grüneisen parameters for bulk Ge calculated using the MVFF model and bench-marked with other experimental and theoretical results provided in Sui et al. [50]. The calculated values compare very well with other calculations.

The Grüneisen parameters are calculated for the 6 bulk phonon branches namely, (i) Transverse acoustic 1 and 2 (TA1 and TA2), (ii) Longitudinal acoustic (LA), (iii) Transverse optical 1 and 2 (TO1 and TO2), and (iv) Longitudinal optical (LO). The close match of the results from other published results [50] show that the strain models for phonons have been implemented correctly and can be used for analyzing the effect of strain on other physical properties like the thermal properties in nanowires.

7.3.2 Effect of strain on the thermal properties of Si nanowires

Tuning thermal properties using strain can be beneficial for cooling and increasing gain of lasers [213, 226] or improving the efficiency of TE devices [213]. Strain/stress

effects on the thermal conductivity of doped bulk zinc-blende (ZB) semiconductors at low temperatures has been well studied [228, 229]. Most of the bulk studies in ZB semiconductors found decrease in thermal conductivity with tensile strain which is qualitatively attributed to (i) a decrease in the phonon mean free path [217], (ii) an increase in the Debye temperature [217, 226], and (iii) a change in the material stiffness [209]. The few experimental [218] and theoretical [209, 213, 226, 230] efforts that have focused on the strain effects on the thermal properties in nanostructures, are either limited to single crystal orientation (mostly [100]) or diffusive phonon transport even in small nanostructures. This work investigates the external strain effects on the thermal properties in ultra-scaled SiNWs in the coherent phonon transport regime where the wire cross-section sizes are comparable to the phonon wavelengths [231] ($\lambda_{ph} = hV_{snd}/k_BT_{300K} \approx 1nm$ at $V_{snd} = 6.5$ km/sec for a 3nm X 3nm [100] SiNW [196], where k_B and h are the Boltzmann constant and Planck's constant, respectively).

Theoretical details

Free-standing SiNWs' phonon dispersion are studied using the MVFF model (Chapter 5). In the previous section the stress behavior of phonons in bulk Si and Ge using the MVFF model has been bench-marked too. The SiNW phonon dispersion under hydrostatic and uniaxial stress are studied. The ballistic thermal conductance (κ_l^{bal}) and constant volume specific heat (C_v) are calculated using Eq.(5.30) and Eq.(5.31), respectively from Chapter 5. A modified representation of the κ_l^{bal} is used in this section given by,

$$\kappa_l(\epsilon, T) = \frac{1}{\hbar} \sum_{i \in [1,N]} \kappa_l^i(\epsilon, T), \text{ where} \tag{7.5}$$

$$\kappa_l^i(\epsilon, T) = \int_{E_{i,min}}^{E_{i,max}} M(\epsilon, E_i) \cdot E_i \cdot \frac{\partial}{\partial T} \Big[\frac{1}{(exp\big(\frac{E_i}{k_BT}\big) - 1)} \Big] dE_i \tag{7.6}$$

where N is the number of energy bins in the entire phonon dispersion energy range.The terms ϵ, M(E), T, and e are the strain percentage, the number of modes

at phonon energy E, the temperature, and the electronic charge, respectively. The term $\kappa_l^i(E,T)$ is the contribution to the total κ_l of SiNW for $E_{i,min} \leq \mathrm{E} < E_{i,max}$. This energy resolved representation in Eq.(7.5) allows for better understanding of the variation in κ_l due to strain.

Silicon nanowire details

Square SiNWs with width (W) and height (H) = 3nm with two channel orientations of [100] and [110] are studied (inset of Fig. 7.14a,b). Hydrostatic deformation (equal deformation along all the directions) and uniaxial deformation (along the wire axis) are applied to these wires varying up to ±2%. The outer surface atoms in these NWs are allowed to vibrate freely. Extremely small SiNWs may show significant surface and internal atomic reconstruction [195, 213] or phase change [213] under strain leading to larger changes in C_v and κ_l have been neglected in the present study.

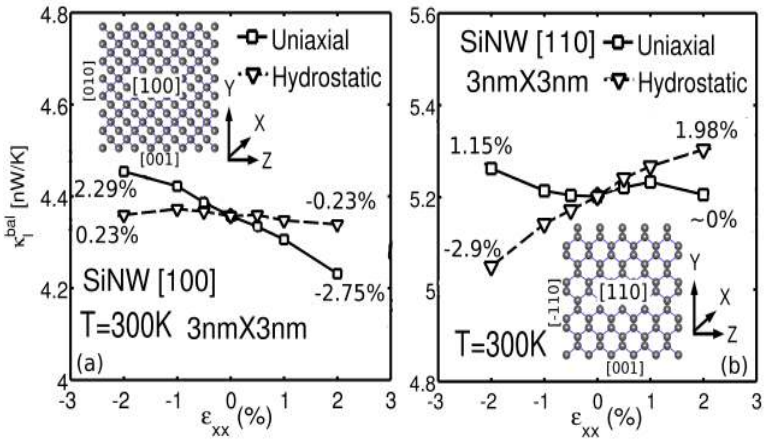


Fig. 7.14. Variation in κ_l with hydrostatic and uniaxial stress in 3nm × 3nm SiNW with (a) [100] and (b) [110] orientation. The uniaxial stress is applied along the wire axis. Insets also show the atomic structures of both the SiNWs with the coordinate axes. This figure is taken from Ref. [57].

7.3.3 Results and Discussion

1. Ballistic thermal conductance κ_l

In all the SiNWs κ_l is calculated using Eq.(7.5) at 300K. κ_l increases (decreases) under uniaxial compression (tension) for both the wire orientations. Similar variations in κ_l for [100] SiNWs are also observed by Li. et al [213] using non-equilibrium molecular dynamics (NEMD) calculations. The [100] SiNW shows larger variation in κ_l under tensile uniaxial deformation compared to the [110] SiNW (Fig. 7.14a,b). κ_l shows a weak hydrostatic stress dependence in [100] SiNW in contrast to the [110] SiNW which shows a decrease (increase) of 2.9% (1.98%) in κ_l under 2% compressive (tensile) strain from the unstrained value (Fig. 7.14a,b). Similar strain behavior is obtained in SiNWs with W=H up to 5nm, which are not shown here for the sake of brevity. *Thus, ultra-scaled SiNWs show an anisotropic variation in κ_l under hydrostatic deformation.*

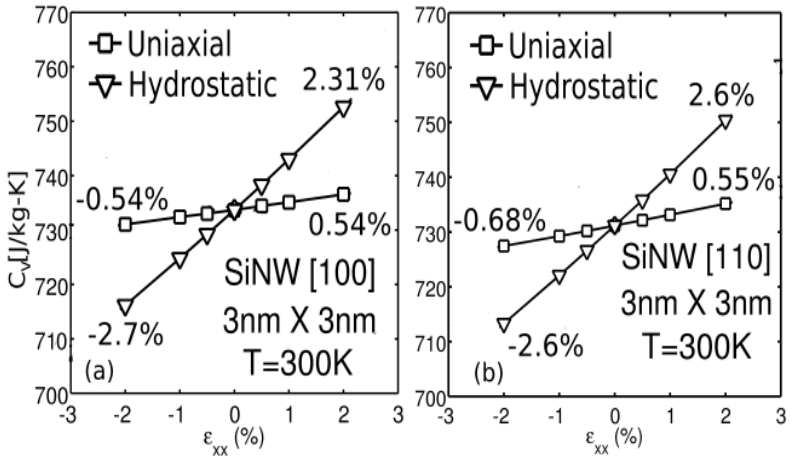


Fig. 7.15. Variation in the C_v with stress in 3nm × 3nm SiNW with (a) [100] and (b) [110] orientation. Two types of stress are applied in these SiNWs, (i) hydrostatic pressure and, (ii) uniaxial stress along the wire axis. This figure is taken from Ref. [57].

2. Specific heat (C_v)

Variation in the phonon dispersion under strain also changes the C_v of SiNWs. Compressive (tensile) strain decreases (increases) the C_v in both types of SiNWs (Fig. 7.15a,b)). This variation in C_v is similar to the bulk Si behavior as reported in Refs. [209, 230]. Under hydrostatic stress the C_v decreases by $\approx$ 2.7% at 2% compression and increases to $\approx$ 2.6% at 2% expansion compared to the unstrained C_v value for both the SiNW orientations. Under uniaxial deformation the variation is $\leq$ 1% for $\pm$2% strain for both wire orientations (Fig. 7.15a,b). *Hence, C_v variation is isotropic under strain in ultra-scaled SiNWs.*

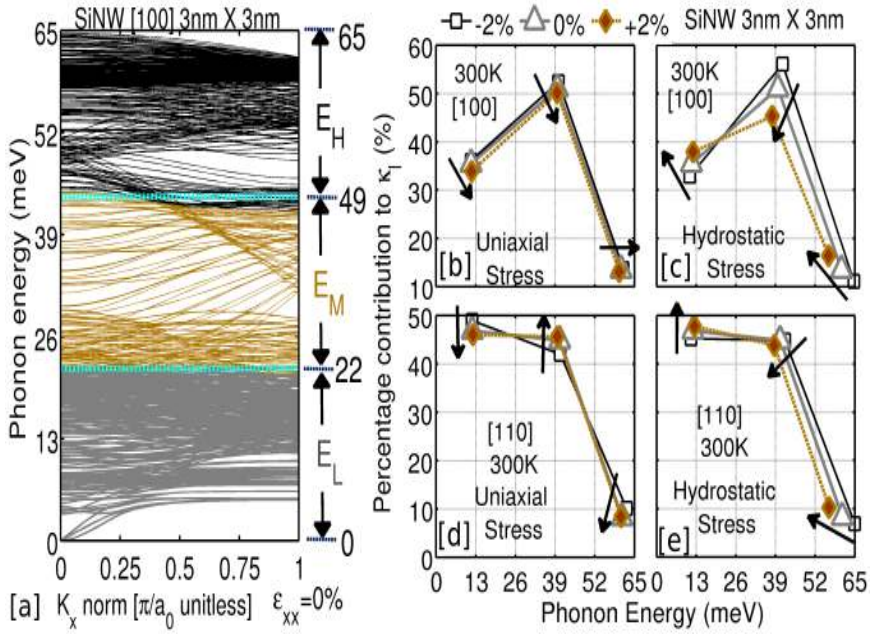


Fig. 7.16. (a) Phonon dispersion of 3nm $\times$ 3nm [100] SiNW with the three energy ranges considered for κ_l analysis. The percentage contribution to κ_l from different energy ranges, for [100] SiNW under (b) uniaxial stress, (c) hydrostatic stress and, for [110] SiNW under (d) uniaxial stress and (e) hydrostatic stress. Arrows show the variation in contribution from compression (Cm) to tension (Tn). This figure is taken from Ref. [57].

Reason for the variation in κ_l

To understand the variation in ballistic κ_l with strain, the energy dependent contributions are analyzed using Eq.(7.5). The entire phonon spectrum is grouped into three energy ranges, (i) E_L ('low' bands), (ii) E_M ('mid' bands) and, (iii) E_H ('high' bands) (see Fig. 7.16 a). These bands show variable contributions under strain which determine the overall effect on κ_l (Table 7.1).

Table 7.1
Value of band contribution to κ_l under strain (Fig. 7.16). Variation shown from compression (Cm) to tension (Tn) for uniaxial (U) and hydrostatic (H) strain for both SiNW orientations (Or).

Strain, [Or] E_i (meV) $\rightarrow$	$\overline{\kappa_l(L)}$ (0-22)	$\overline{\kappa_l(M)}$ (22-44)	$\overline{\kappa_l(H)}$ (44-65)	Dom. band	Cm to Tn
U, [100]	36%-34% $\downarrow$	52%-50% $\downarrow$	13%-13%	L,M	$\downarrow$
H, [100]	32%-37% $\uparrow$	56%-45% $\downarrow$	11%-16% $\uparrow$	M	$\downarrow$
U, [110]	49%-46% $\downarrow$	42%-46% $\uparrow$	10%-8% $\downarrow$	L,H	$\downarrow$
H, [110]	45%-48% $\uparrow$	45%-44% $\downarrow$	7%-10% $\uparrow$	L,H	$\uparrow$

Under uniaxial strain, in [100] SiNW contribution to κ_l is mainly from $E_L + E_M$, which decreases from ~88% under compression (Cm) to ~84% under tension (Tn) (Fig. 7.16b), whereas in [110] SiNW the contribution to κ_l is mainly from $E_L + E_H$, which reduces from ~59% (Cm) to ~54% (Tn) (Fig. 7.16d). Under hydrostatic strain, in [100] SiNW main contribution to κ_l is from E_M, which reduces from ~56% (Cm) to ~45% (Tn) (Fig. 7.16c), while in [110] SiNW main contribution to κ_l is from $E_L + E_H$, which increases from ~52% (Cm) to ~58% (Fig. 7.16e). These details are also summarized in Table 7.1. *Thus, low/mid energy contribution for [100] SiNW and low/high energy contribution for [110] SiNW explains the anisotropic nature of* κ_l.

Reason for C_v variation

Under the action of strain the contribution of the phonon bands in E_H range varies considerably as shown in Fig. 7.17. Under uniaxial stress, both [100] and [110] SiNWs show almost no variation in the E_L and E_M range, and minute variation in the E_H range(Fig. 7.17a,c). The contribution increases from Cm to Tn in the E_H range which governs the C_v trend under uniaxial strain (Fig. 7.15). Under hydrostatic stress, contribution from the E_H range increases from Cm to Tn, but in a much larger magnitude compared to uniaxial stress, for both the wire orientations (Fig. 7.17b,d). This explains the larger variation in C_v under hydrostatic stress (Fig. 7.15). *Thus, the higher energy bands decide the strain behavior of C_v under strain, for ultra-scaled SiNWs.*

7.3.4 Summary of the work

The ballistic thermal conductance behaves an-isotropically under strain, however, C_v shows an isotropic behavior. The observed trends in the thermal properties can be understood by the different types of contribution of phonon modes in different energy ranges. The behavior of C_v in SiNWs is similar to bulk Si however, κ_l variation is very different from bulk Si. Under the low stress condition hydrostatic strain can be beneficial in engineering C_v and uniaxial stress for engineering κ_l for cooling lasers. However, high external strain ($|\epsilon| > 2\%$) field may be needed to engineer κ_l to improve the efficiency of TE devices [152].

7.4 Thermal transport in ultra-short SiGe superlattice nanowires

SiGe superlattice nanowires have attracted the attention of the thermoelectric community for a long time due to the possibility of integrating these structures in the CMOS flow as well as higher tunability of the thermal conductivity [60]. In this section the thermal transport in ultra-short SiGe superlattice nanowires are studied

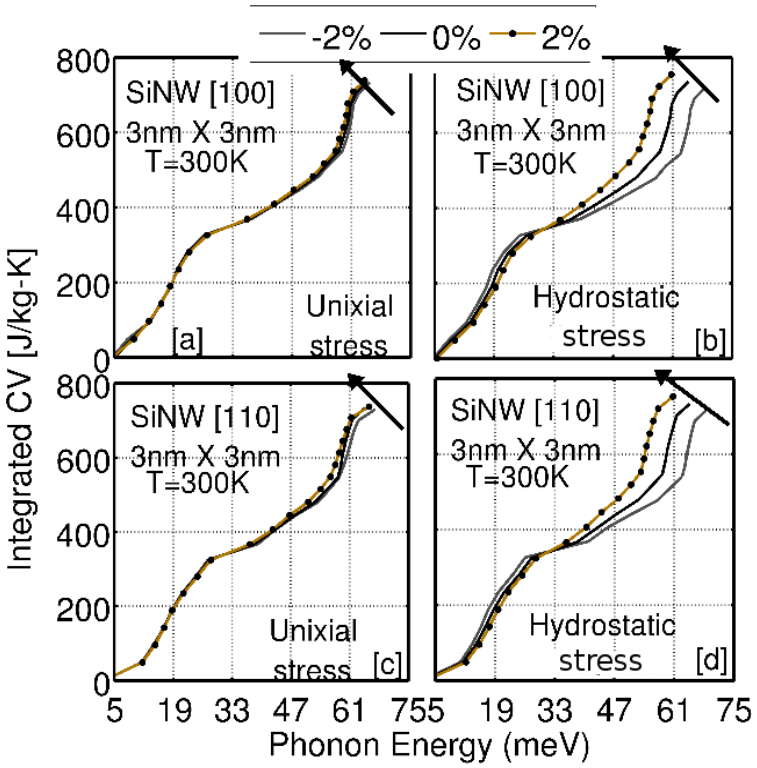


Fig. 7.17. Variation in CV with phonon energy bands under various conditions. 3nm × 3nm [100] SiNW with (a) uniaxial stress, (b) hydrostatic pressure. 3nm × 3nm [110] SiNW with (c) uniaxial stress, (d) hydrostatic pressure. The higher sub-bands show larger variation in CV contribution compared to the lower energy sub-bands. The figure is taken from Ref. [57].

to understand the ballistic phonon transport in these structures (radiative transport or Casimir limit [142,232,233]). Two main aspects are studied here, (i) understanding the effects of interface orientation and randomness on thermal boundary resistance (TBR) of a single Si/Ge interface, and (ii) the in-plane and cross-plane heat flow in SiGe superlattice nanowires.

At the nano-scale an atomic understanding of the thermal transport is necessary. Though Boltzmann Transport Equation and Molecular Dynamics (MD) are extensively used to study thermal transport but they have their own pitfalls (see Chapter

5). Here Phonon Green's function (PGF) method is used for studying the thermal transport (described in detail in Chapter 5).

7.4.1 Thermal boundary resistance of Si/Ge interfaces

Whenever two different types of materials are combined to form an interface and heat flows across that interface an additional resistance to the heat flow occurs which is called thermal boundary resistance (TBR) [234]. The TBR associated with the Si/Ge interface at the atomic level is studied in this section. The TBR of a solid-solid interface is traditionally described by Acoustic Mode Mismatch (AMM) model [234] if the two media have a large acoustic mismatch (mismatch in sound velocity) or by using the Diffuse Mode Mismatch (DMM) model [234] where all phonons scatter diffusively at the interface [234]. For temperatures in the intermediate and higher range heat transport is mainly diffusive where phonons scatter at the interface and lose their memory and the transmission is mainly weighted by the mismatch in the density of phonon modes. These classical models give TBR values in the low $10^{-9} m^2 K/W$ range. However, atomic interface disorder can increase these TBR values by an order of magnitude as observed in metal-oxide interfaces [235].

Nanowire details

Square superlattice nanowires with width (W) and height (H) = 2, 3, and 4nm with two wire orientations of [100] and [110] are studied. The SiGe channel is 3nm long (Lc) with 1.5nm Si length (L_{Si}) and 1.5nm long Ge region (L_{Ge}). As shown in Fig. 7.18, 5 different types of interfaces are studied. An ideal interface is taken where the atoms are assumed to be arranged at the zinc-blende lattice positions (Fig.7.18a). Then non-ideal Si/Ge interfaces are created by mixing, (i) 2 atomic layers or 1 monolayer (ML), (iii) 2 MLs, (iv) 3 MLs, and (iv) 4 MLs as shown in Fig. 7.18b-e. Thermal current in these structures are calculated using PGF method at three different terminal temperatures of 200K, 300K, and 400K. This allows to

understand the temperature dependence of the thermal boundary resistance (TBR). The lumped thermal resistance formulation is shown in Fig. 7.18f.

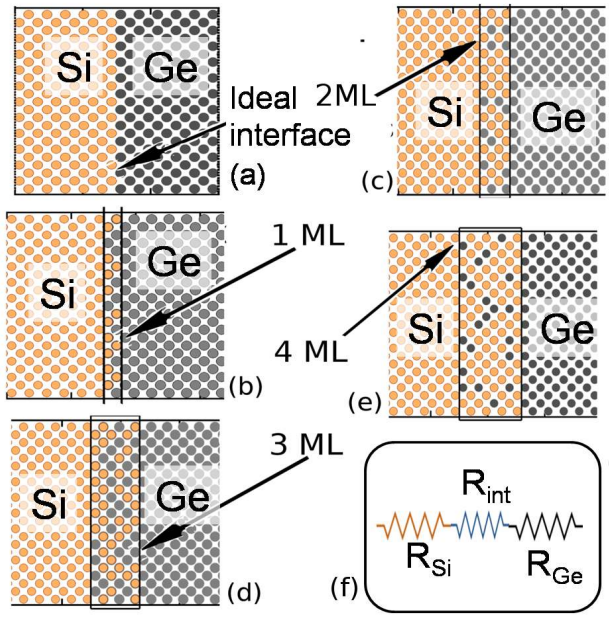


Fig. 7.18. The different types of SiGe interfaces which are used for calculating the thermal boundary resistance (TBR). (a) Ideal interface, (b) 1 monolayer of disorder, (c) 2 monolayers of disorder, (d) 3 monolayers of disorder, and (d) 4 monolayers of disorder.(f) The lumped thermal resistance formula used for calculating the thermal resistance for Si/Ge interface

TBR calculation method

For a typical Si/Ge interface (Fig. 7.18a) the total thermal resistance (R_{th}^{total}) can be written as,

$$R_{th}^{total}(T) = R_{th}^{Si}(T) + R_{th}^{Ge}(T) + R_{th}^{int}(T) \text{ ,where} \quad (7.7)$$

$$R_{th}(T) = \frac{1}{\kappa_l(T)}. \quad (7.8)$$

where R_{th}^{int} is interface thermal resistance at temperature 'T'.

The value of κ_l is calculated using Eq.(5.30) of Chapter 5. To obtain the value of $R_{th}^{Si/Ge}$ thermal transport in nanowire structure with Lc = 3nm is calculated. For calculating Si (Ge) thermal resistance both the contacts and channel are composed of Si (Ge). Once the $R_{th}^{Si/Ge}$ value is known at a given temperature, T, then interface thermal resistance can be obtained. The value of TBR is obtained from this interface resistance as,

$$TBR_{Si/Ge} = Area \times R_{th}^{int}. \tag{7.9}$$

Depending of the type of thermal transport across the interface $R_{th}^{Si/Ge}$ can be obtained in two regimes,

1. **Ballistic phonons:** The thermal resistance does not scale with the length of the Si or Ge region. This can happen when the phonon mean free path (mfp) is longer than the length of the segment. According to Chen et. al. [236] at 300K, the mfp of bulk Si and Ge can be as high as 41 and 28 nm respectively. In nanowires the mfp value can further decrease due to the additional boundary scattering. Thus, under this condition the R_{th}^{int} can be directly obtained from Eq.(7.7).

2. **Diffusive phonons:** In case the mfp is extremely short in the channel (<1nm) then instead of using the ballistic values of $R_{th}^{Si/Ge}$ the length dependent value of thermal resistance has to be used. Then Eq.(7.7) is modified as,

$$R_{th}^{total}(T) = \rho_{th}^{Si}(T) \cdot \frac{L_{Si} - L_{int}/2}{Area} + \rho_{th}^{Ge}(T) \cdot \frac{L_{Ge} - L_{int}/2}{Area} + R_{th}^{int}(T) \tag{7.10}$$

where, $\rho_{th}^{Si/Ge}$ is the lattice thermal resistivity calculated using the PFG method for a pure Si/Ge channel with similar material used for the leads.

The result for the diffusive and ballistic TBR calculations are shown in Fig. 7.19. An interesting observation is that ballistic phonons match the MD calculations [237] very well where as the diffusive results match the other Green's function calculation from Zhang et. al [152]. As the ballistic calculations agree with MD simulations, this formulation is used for the analysis of TBR is the next section.

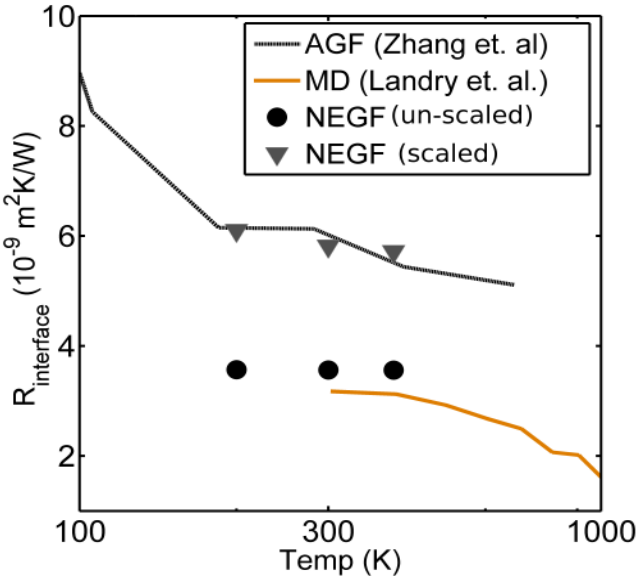


Fig. 7.19. Benchmarking of SiGe TBR with other theoretical calculations. Other theoretical calculations include atomistic Green's function results from Zhang et al. [152] and MD results from Landry et al. [237]. The unscaled values represent the ballistic phonon PGF results, whereas the scaled values are obtained by using Eq.(7.10).

Results and Discussion

Figure 7.20 shows the TBR variation with T in SiGe SL nanowires with [100] and [110] orientations. For the ideal interfaces the TBR shows a smaller value for [110] wires compared to [100] wires. The [100] TBR value is about $4 \times 10^{-9} m^2K/W$ and [110] TBR value is about $3 \times 10^{-9} m^2K/W$. For the temperature range of 200K to 500K TBR decreases a little. The temperature variation is similar to the MD calculations in Ref. [237]. The weak dependence of TBR on the temperature is attributed to the absence of anharmonic phonon scattering processes [237]. The [110] wires show smaller TBR since these wires have larger number of phonon modes compared to the [100] wires allowing more heat flow as shown in Fig. 7.21a. This is due to the anisotropic nature of the phonon dispersion in Si and Ge nanowires also outlined in Ref. [151].

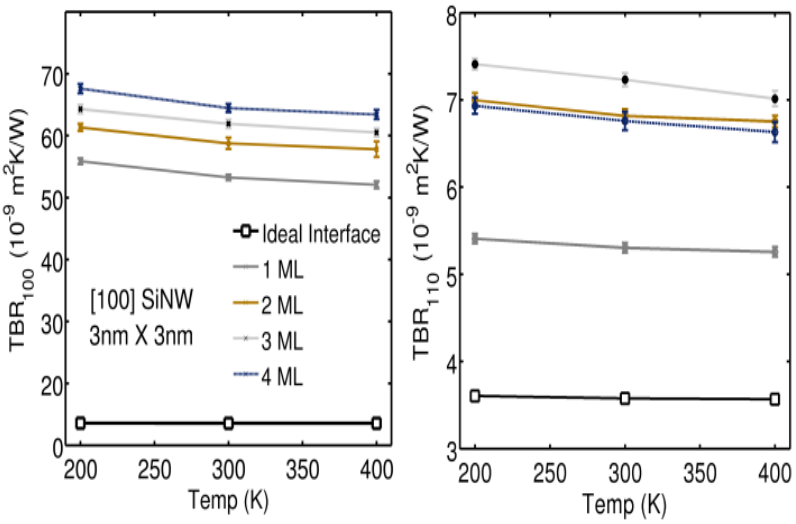


Fig. 7.20. Orientation and layer disorder dependence of TBR in SiGe interfaces.

The atoms at the interfaces of materials can easily diffuse into each other [238]. This kind of atomic diffusion affects the interface physical properties like TBR. The variation in TBR with atomic diffusion is studied in a systematic way. The layers on both Si and Ge side are mixed in steps of 1 monolayer (ML[1]), 2ML, 3ML and 4ML. The Si and Ge atoms are randomly distributed in these layers. To obtain a good statistical average 30 to 50 samples are created. The results for the TBR variation with T and ML mixing is shown in Fig. 7.20. The [100] oriented wires have much larger TBR compared to the [110] wires. The TBR increases as the number of ML mixing increases for [100] wires but falls for [110] wires ($TBR_{3ML} > TBR_{4ML}$). Also the decay of TBR with T is higher for distorted layers compared to the ideal interfaces showing higher phonon coherency loss due to atomic diffusion.

The increase in the [100] SL TBR with larger ML distortion is consistent with the continuous reduction in phonon modes as shown in Fig. 7.21b. The modes are limited ∼39meV which is the Ge phonon energy range. So all the higher energy phonon modes from Si are cut-off. Also the temperature range in the study suppresses phonon-phonon scattering [237] otherwise the higher energy phonons in Si could decay

[1] 1 ML contains two atomic layers.

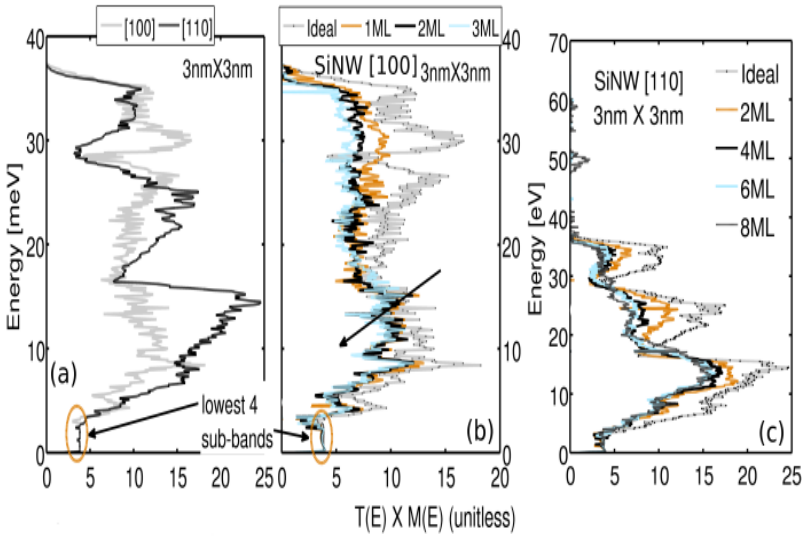


Fig. 7.21. Transmission across single Si/Ge interface with different orientations and layer mixing.

to contribute higher heat flow. The [110] SLs show increase in the TBR as ML mixing increases from 1 to 3 but then it reduces. This happens since the structures with 4 ML mixing also show some modes in the energy range outside the Ge limit of 39meV. This type of transmission leak comes from the atomic mixing on the [110] planes which is absent in [100] layers. This type of behavior could only be observed using an atomistic phonon model.

TBR of SiGe: Conclusions

The significance of the TBR and its variation with wire orientation, interface distortion and temperature are studied in this section. In the temperature range where phonon-phonon scattering is less, the TBR shows a weak T dependence. ML mixing increases the TBR by 2 orders of magnitude for [100] wires due to strong suppression of phonon transport however, [110] oriented interfaces show an increase of $\sim 3\times$ in TBR compared to the ideal case. Thus, atomic layer arrangement strongly affects the thermal transport across nano-scale interfaces.

7.4.2 Cross-plane and In-plane heat transport

SiGe structures are useful in tuning the thermal conductance of superlattice nanowires. Since SiGe can be grown in a variety of ways such as digital alloys, nanocomposities, etc, it is interesting to study the flow of heat in these structures to understand the nature of heat flow. Two types of structures are chosen for the study of heat flow,

1. **Cross-plane (CP) structure:** The Si/Ge interfaces are orthogonal to the heat flow direction as shown in Fig. 7.22a.

2. **In-plane (IP) structure :** The Si/Ge interfaces are parallel to the heat flow direction as shown in Fig. 7.22b.

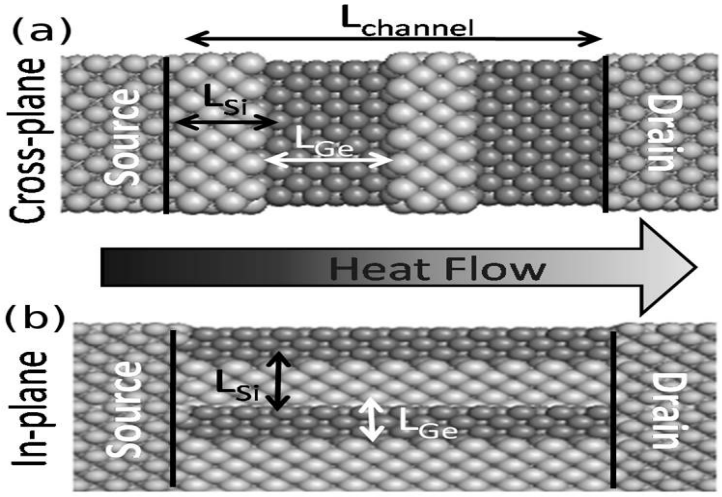


Fig. 7.22. Two types of SiGe structures used to study the ballistic thermal transport. (a) Cross-plane structure and (b) In-plane structure.

Nanowire and simulation details:

Square superlattice nanowires with W and H = 3nm with three wires orientations of [100], [110] and [111] are studied. The SiGe channel is 6nm long. For the CP

structure two supercells of 3nm each are repeated in the channel. Within a given supercell L_{Si} is varied from 0 to 3nm in steps of 0.5nm (Fig. 7.22a), whereas the rest of the length of the supercell is filled with Ge. The total length of the supercell is fixed at 3nm always. For the IP case L_{Si} is also varied from 0 to 3nm in steps of 0.5nm. Remaining region is filled with Ge as shown in Fig. 7.22b. Four different types of contact combinations (source/drain) are used, (i) Si/Si, (ii) Ge/Ge, (iii) Si/Ge, and (iv) Ge/Si. The thermal current in these structures are calculated using PGF method at a terminal temperature of 300K.

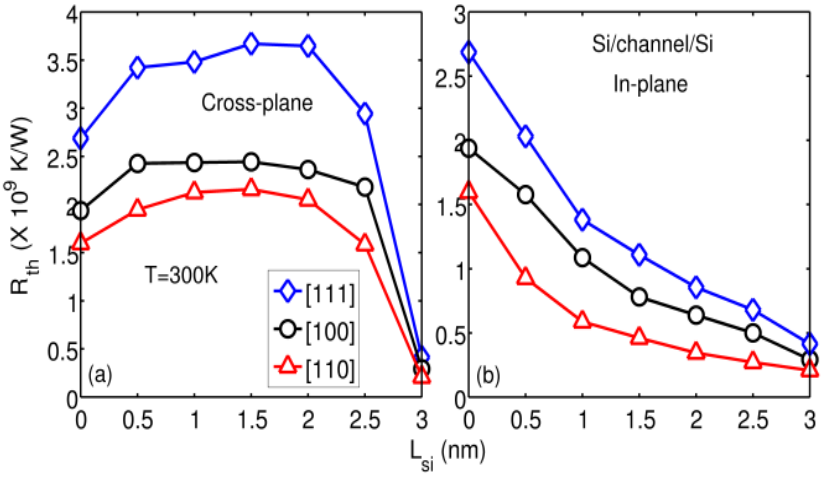


Fig. 7.23. Effect of channel orientation contact on the cross-plane and in-plane thermal transport in SiGe superlattice nanowires. Source and drain are of Si.

Results and Discussion

Two main effects are studied, (i) effect of the interface orientation, and (ii) effect of the type of contact on the heat flow in cross-plane and in-plane nanowires.

1. Orientation effect: Figure 7.23 shows the effect of orientation on the thermal resistance with L_{Si} in SiGe superlattices. The thermal resistance is highest for the [111] case followed by [100] and then [110] in both CP and IP cases. This is the reverse order of the thermal conductance reported for these three orientation in Ref. [151].

The CP case shows a non-monotonic variation in R_{th} whereas the IP case shows a monotonic variation with L_{Si}. This happens since the CP case represents a series combination of thermal resistances and TBR and the total heat flow is controlled by the TBR [235]. When the whole system has only Si then the TBR vanishes and hence total R_{th} of the system falls. For the IP case the heat flow is through a parallel combination of thermal resistance [235]. The heat flow is controlled by the low thermal resistance path which is in Si. The TBR plays a small role in the overall heat flow. As the L_{Si} value increases the heat flow becomes easier and hence the R_{th} value drops as shown in Fig. 7.23b.

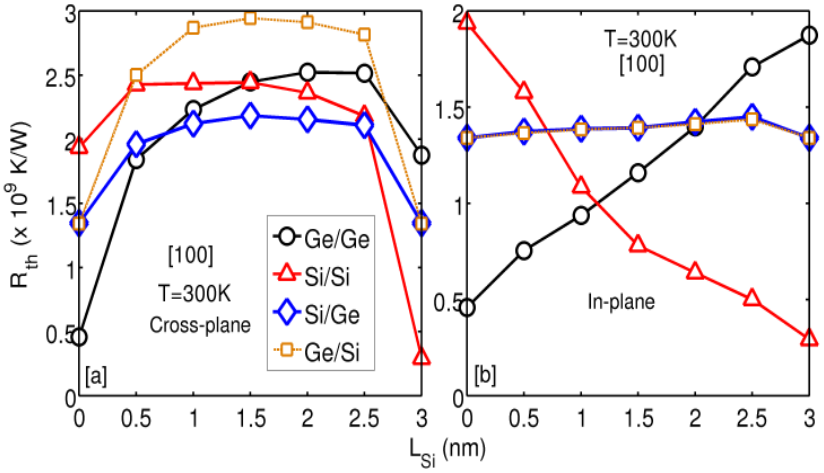


Fig. 7.24. Effect of contact on the cross-plane and in-plane thermal transport in SiGe superlattice nanowires. The wire orientation is [100]

2. Effect of the contacts: Figure 7.24 shows the role of contact on the total heat flow through nanowires. At the nano-scale the contacts have significant role in governing the overall thermal transport very similar to the mesoscopic electron transport [44]. The mismatch of contact and channel material plays a significant role in deciding the thermal resistance in both CP and IP structures. In the CP structures the R_{th} value shows a maxima due to the role of TBR. For the IP structure the TBR only comes from the contacts (no internal material interfaces) and hence there is a monotonic behavior in the thermal resistance.

7.4.3 Summary of the work

The role of SLs on the thermal transport at the nano-scale is shown. The concept of TBR and the importance of atomic distortion, orientation and temperature on TBR is provided here which is play a significant role in nano-scale thermal management. Also the role of CP and IP structures to tune and manage heat flow in SiGe SLs is provided. The importance of orientation and contacts is explained which are important design parameters for the heat flow control in nanostructures.

7.5 Summary and Outlook

At the nano-scale thermal properties can be tuned by various methods. As investigated in this chapter, porosity is a useful tool to modulate the thermal conductivity in nanowires making more options available for better thermoelectric devices as well as other applications. Role of strain in engineering the thermal properties is also investigated. Larger strain values (>2%) can be beneficial for SiNWs. Also it is shown that at the nano-scale the thermal boundary resistance of Si/Ge nanowire interface is strongly affected by the interface orientation as well as the interface disorder. The thermal transport in cross(in)-plane SiGe superlattice nanowires reveals a strong dependence on the type of contacts as well as the wire orientation. The simulation study here provides a good insight about the thermal transport and methods to tune the heat flow at the nano-meter level which will be useful in designing nano-scale devices.

8. THERMOELECTRIC PROPERTIES IN SEMICONDUCTORS: THEORY

8.1 Introduction and Motivation

The limited availability of the fossil fuels and the harmful effects of burning these fuels has kicked research in different areas for exploring cleaner, greener and sustainable renewable energy resources. In today's world, many options are being explored which includes solar energy, wind energy, thermoelectricity, tidal energy, and geothermal energy [239]. Renewable energy supplies ∼19% of global final energy consumption. Out of all the renewable energy sources, thermoelectricity, the interconversion of the heat into electricity and vice versa [240–244], is unique since it can be used as an energy generator deriving power out of waste heat as well as a quite efficient cooler/heater and temperature probe as shown in Fig. 8.1.

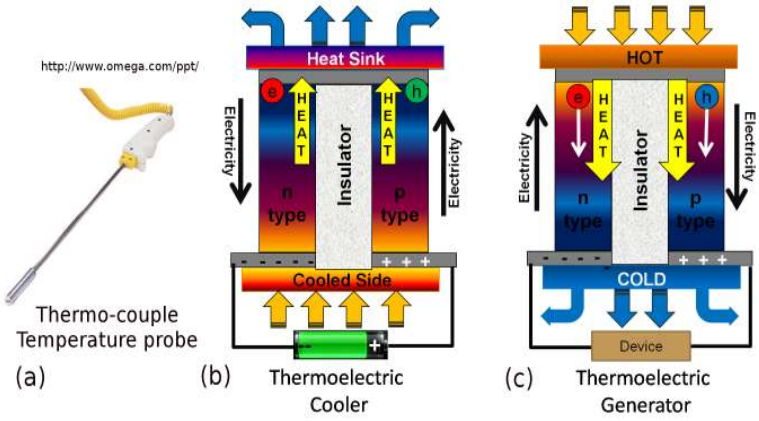


Fig. 8.1. Different types of thermocouples based on the thermoelectric phenomena. (a) Thermocouple based thermometer (*http://www.omega.com/ppt*), (b) Thermoelectric cooler, and (c) Thermoelectric generator.

This chapter focuses on understanding the thermoelectric (TE) phenomena in semiconductors. Since semiconductors do not have as many electrons as metals, the electricity and heat flow is controlled by electrons and phonons, respectively. This provides two separate knobs to control the electricity and heat in these materials. An atomistic level investigation of the electronic (Chapter 2) and thermal (Chapter 5) properties in semiconductor nanostructures allow the investigation of the thermoelectric effect in semiconductor nanostructures.

In this chapter the following topics are addressed. A brief description on the system level performance and the thermoelectric efficiency (ZT) of the materials is provided in Sec. 8.2. This is followed by a discussion on the types of materials used for thermoelectric devices in Sec. 8.3. A new algorithm counting the modes from material energy dispersion is presented in Sec. 8.4. The main results on the algorithm and discussion are outlined in Sec. 8.5. Summary and outlook are provided in Sec. 8.6.

8.2 Main concepts in thermoelectricity

For any engine working on the thermoelectric phenomena, like thermo-cooler (Fig. 8.1), converts the system heat into electricity or vice versa. In order to measure the performance of such systems coefficient is used called the 'Coefficient of Performance' (C_{OP}). The C_{OP} value in turn is associated with the thermoelectric figure of merit, ZT. This section provides the definition of C_{OP}, ZT and the connection between the two.

8.2.1 Coefficient of performance, C_{OP}

System Level Performance

Since the early days the thermoelectric modules were designed to replace the conventional refrigeration technology, their efficiency is measured by the term C_{OP}.

This is a common term used in refrigeration. For a typical TE generator C_{OP} is defined as [245],

$$C_{OP}^{GEN} = \frac{Energy\ provided\ to\ the\ load}{Heat\ energy\ absorbed\ at\ hot\ junction} \tag{8.1}$$

and the efficiency for thermoelectric coolers is defined as [245],

$$C_{OP}^{REF} = \frac{Cooling\ Effect}{Energy\ Input} \tag{8.2}$$

The optimal C_{OP} value for TE coolers (generators) only depends on a term called 'Z_{avg}' (for the pair of n and p materials used, see Fig. 8.1)defined as [245],

$$Z_{avg} = \frac{(S_n - S_p)^2}{[\sqrt{\kappa_n \rho_n} + \sqrt{\kappa_p \rho_p}]^2} \tag{8.3}$$

where, $\kappa_{n/p}$, $\rho_{n/p}$ and $S_{n/p}$ are the thermal conductivity, electrical resistivity and Seebeck coefficient, respectively for the n and p type materials. The optimal C_{OP} for refrigeration is then related to this Z_{avg} by (Eq.(2.9) in [245]),

$$C_{OP}^{opt,REF} = \frac{T_h}{T_c - T_h} \cdot \frac{\sqrt{1 + Z_{avg}T_m} - T_c/T_h}{\sqrt{1 + Z_{avg}T_m} + 1} \tag{8.4}$$

where, T_m is the mean temperature. Similarly the optimal C_{OP} for generators is defined as ((Eq.(2.18) in [245]),

$$COP_{OP}^{opt,GEN} = \frac{T_h - T_c}{T_h} \cdot \frac{\sqrt{1 + Z_{avg}T_m} - 1}{\sqrt{1 + Z_{avg}T_m} + T_c/T_h} \tag{8.5}$$

A good reference to connect the vendor data to the C_{OP} values for TE devices is provided in Ref. [246].

8.2.2 Measuring the 'goodness' of TE materials

In the last section the system level performance was connected to the material level term called 'ZT'. The first measurement of the solid state thermoelectric efficiency, Z, was proposed by Altenkirch in 1911 [243] which was later modified into

the dimensionless quantity of 'ZT' by Ioffe in 1949 [240]. Usually for the calculation of C_{OP} the Z of the n-p material pair is needed. However, the search of good TE materials is normally done for a single material. Hence, the definition of ZT for a single material, at a temperature 'T', is given by,

$$ZT = \frac{S^2 G}{\kappa_{total}} \cdot T \tag{8.6}$$

$$\kappa_{total} = \kappa_e + \kappa_l \tag{8.7}$$

where, $\kappa_{e/l}$ represent the electron(lattice) thermal conductivity. All these parameters themselves are a function of temperature (T). It has been shown [247] that TE coolers with ZT of 1 operate at only 10% of Carnot efficiency. At infinite ZT, 100% of Carnot efficiency would be achieved, but that limit need not be reached to allow many new technological uses. Some 30% of Carnot efficiency (comparable to home refrigeration) could be reached by a device with a ZT of only 4. Increasing ZT by a factor of 4 is still a formidable challenge but progress towards higher ZT (~ 2.4 reported in [215]) is going on.

8.2.3 Material composition of ZT

The material parameters which form the ZT as shown in Fig. 8.2. The material dependent quantities are explained briefly,

1. *Seebeck coefficient (S):* This measures how much potential difference develops across material junction when temperature gradient is maintained.

2. *Peltier coefficient(Π):* This measure how much temperature difference generates when a potential difference is maintained across a material. This is in a way opposite of Seebeck coefficient.

3. *Electrical Conductance (G):* This measures the ability of a material to transport electrons, which is a measure of charge current.

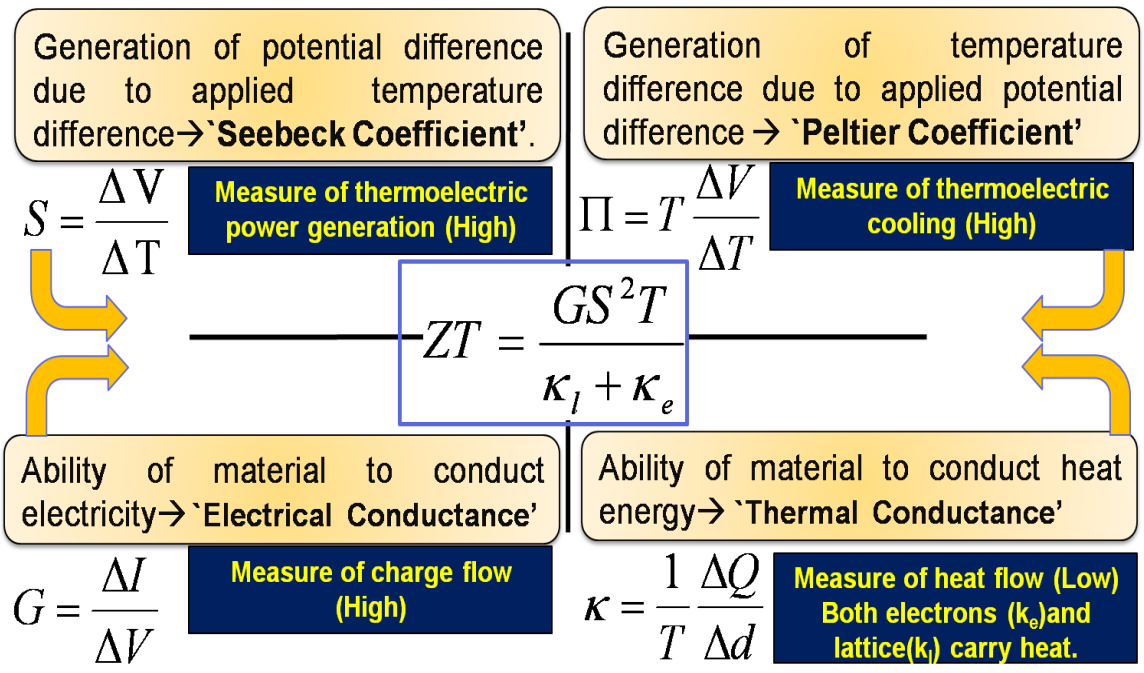


Fig. 8.2. The main concepts of thermoelectricity. All the terms are also explained in brief and how do they combine to make the thermoelectric figure of merit called 'ZT', a dimensionless quantity proposed by Altenkirch and Ioffe [240, 243]. The requirement for each parameter for a 'good' TE materials are given in the smaller dark-colored blocks.

4. *Thermal conductance ($\kappa_{e,l}$):* This measure how much heat flows through the system from high temperature to low temperature region. Both electronic (κ_e) and lattice (κ_l) parts are considered.

Combining all these functionalities together can show how good or bad the material is for thermoelectric purposes. A 'good' thermoelectric material, as a rule of thumb, should have *high S, high G and low* κ, since, good TE materials should be able to transport charge efficiently while maintaining a good thermal gradient at the same time.

8.3 Thermoelectric Materials

Once the ZT of a material is defined the million dollar question arises what materials to use for TE applications. Materials can be broadly classified as (i) insulators, (ii) metals and (iii) semiconductors. Insulators have poor electrical conductivity (low G) so they cannot act as TE materials. Metals on the other hand, have relatively low Seebeck coefficients. In addition, the thermal conductivity of a metal, which is dominated by electrons, is proportional to the electrical conductivity, as dictated by the Wiedemann-Franz [248] law. It is thus hard to realize high ZT in metals. The natural choice then are the semiconductors. In semiconductors, the thermal conductivity consists of contributions from the electrons (κ_e) and the phonons (κ_l), with the majority of heat being carried by the phonons (true for low doping and low temperature cases). They have better Seebeck values and moderate electrical conductivities which can be modulated by doping. This makes them very suitable for TE applications. The solid-state thermoelectric calculations are based on the linear Onsager thermodynamic relations [241] which depend on material specific properties such as Seebeck coefficient (S) and electrical conductance (G) as shown in Fig. 8.3.

8.3.1 Advances in TE materials

Over the last five decades TE research is focused on obtaining materials with ZT $\geq$ 1 which could lead to higher thermoelectric conversion rates at room temperature [6]. Initial thermoelectricity works focused on bulk semiconductors. However, around 1990s the pioneering work of Dresselhaus et. al. [7] and Mahan et.al [249] opened up ways to engineer electronic density of states (DOS) using dimensional scaling of semiconductor structures which took the ZT beyond 1 [250–252]. Also nanostructuring allows phonon tailoring to precisely control the lattice thermal conductivity (κ_l) of semiconductors [59, 60] which can help in enhancing the ZT further.

The development in the TE materials can be categorized into two different engineering approaches. These are,

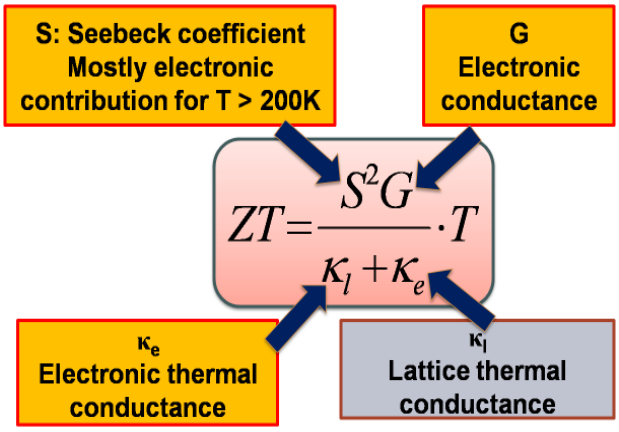


Fig. 8.3. The linear thermoelectric efficiency coefficient (ZT). The parameters in yellow boxes depend on electronic property of the solid and the gray box represent the lattice contribution to the thermoelectric efficiency. This chapter outlines the theoretical details and the methods to calculate these parameters in semiconductors for thermoelectric analysis.

- **Modification of electron DOS:** This method engineers the numerator of ZT ($=S^2$G), also called the Thermoelectric Power-Factor [30]. This involves the modification of the electronic bandstructure via dimensional scaling and alloying. Some of the prominent efforts in this direction are [7, 38, 249, 253].

- **Suppression of κ_l:** This idea is to block the phonons. The leading approach in this area is the 'Phonon Glass Electron Crystal' (PGEC) method [36, 37]. Some of the noticeable efforts in this area are [5, 36, 37, 215]. The traditional cooling materials belonging to this category are alloys of Bi_2Te_3 with Sb_2Te_3 (such as $Bi_{0.5}Sb_{1.5}Te_3$, p-type) and Bi_2Te_3 with Bi_2Se_3 (such as $Bi_2Te_{2.7}Se_{0.3}$, n-type), with a ZT ~ 1 at room temperature (300K) [30, 240].

It is now well known that the PGEC approach has serious limitations in improving ZT and improvements in the electronic properties are also required [254]. A variety of different materials are being used to obtain high ZT which can belong to either alloying or DOS engineering. Some of the ways that are currently being pursued to improve the ZT are new materials [5], new structures like nanowires [32,33], quantum

wells [255, 256], superlattices [215] and nanocomposites [257] and strain engineering [258]. Certain non-linear transport phenomena like tunneling and thermionic emission [259] has also been used to improve the ZT of TE systems.

Some of the latest material innovations in the field of thermoelectricity are shown in Fig. 8.4. These are,

- Nanocomposites, Ref. [30]
- Nanowires, Ref. [31–33].
- Superlattices, Ref. [34].
- Complex materials, Ref. [36, 37].
- Hollow-porous materials, Ref. [38].
- Metal nitride superlattice, Ref. [39].

8.4 Modeling Approach and Methodology

The TE devices and materials are shirking in size for improving the ZT [6,7]. This has resulted in mixing of materials which can no longer be represented by the bulk properties of the original material [29]. So, continuum material based models like effective mass, bulk Fourier law, etc are not very useful. The demand is more for the models which can take into account the variation of material, strain, potential at the atomic level. The time is right to apply the bottom-up approach to thermoelectricity, as shown in Fig. 8.5, which has been successfully applied to explain the electronic transport in mesoscopic transistors [44] .

Due to the endless possibilities available and the impossibility to manufacture every combination of materials and structures, computer modeling is becoming an important tool to explore the possibilities in thermoelectricity. In this chapter, the ideas around the bottom-up view of thermoelectricity as shown in Fig. 8.5, are developed to enable a better understanding of the materials and the underlying physics

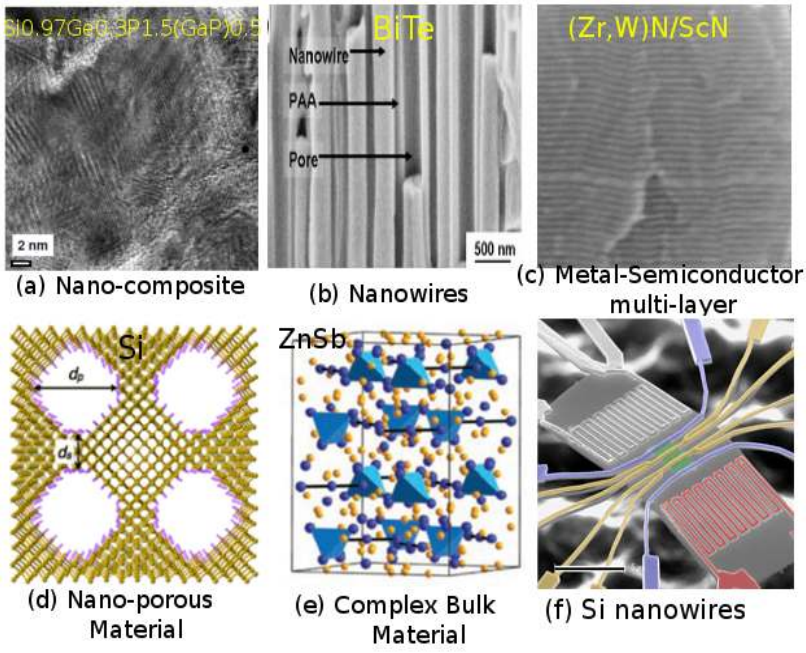


Fig. 8.4. Modern Thermoelectric Materials that are reported to have high ZT (≥ 1). (a) Nanocomposites [30], (b) Bi_2Te_3 nanowires [31], (c) Metal-semiconductor multilayer [39], (d) Nanoporous Si [38], (e) Complex bulk Material, $ZnSb$ [36] and (f) Silicon nanowires [32].

at the nano-scale. The three main ingredients for developing a nano-scale modeling approach for TE materials are:

- **Electronic Structure calculation:** In order to understand the transport properties like G, S and κ_e of electrons at the nanometer regime a good electronic structure calculation is needed. An atomistic semi-empirical Tight-binding model [40, 65] is used which has been a very established method for nano-scale transistor simulations as discussed in detail in Chapters 2,3 and 4.

- **Phonon calculation:** At the nanometer level, lattice behavior is very different from bulk [260]. In order to model the lattice thermal properties the MVFF method [50]is developed for the bulk and nano-scale semiconductors as provided in Chapter 5.

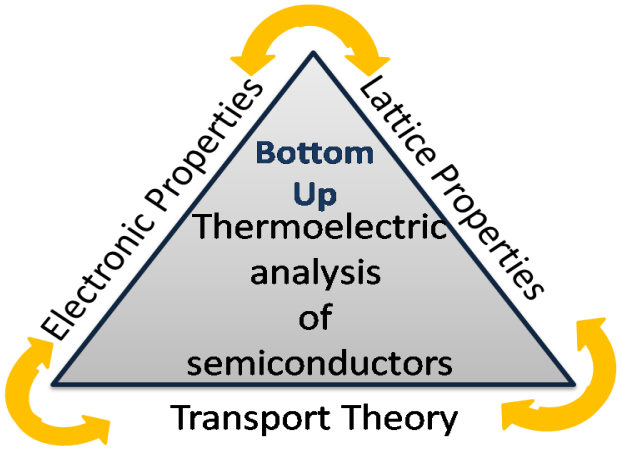


Fig. 8.5. Central theme of this chapter is shown in this 'triangle of thermoelectricity'. The main focus is on the (a) calculation of electronic structure in the nano-scale semiconductors and their alloys, (b) calculation of phonons in ultra-scaled semiconductors to obtain thermal properties and (c) calculation of transport properties to understand the thermoelectric properties of semiconductors.

- **Transport calculation:** Another important aspect is to calculate the electronic and phononic transport properties to calculate the ZT. For this purpose Landauer's approach [51] is very suitable for both electrons and phonons (see details in Chapter 2 and 5) .

8.4.1 Landauer Approach for calculating TE parameters

Many different theoretical approaches have been applied to obtain the thermoelectric parameters. Boltzmann Transport Equation (BTE) method has been applied extensively time within the relaxation time approach (RTA) [30, 261] for solving the problems in thermoelectricity. Other approaches include MD [164, 165] (can treat atomic level changes but has serious size constraint) and Green's function method [151]. For low temperature Landauer's approach is very useful in obtaining the linear response of the system to calculate the transport properties [51]. Recently

it has been also shown that Landauer's approach and BTE lead to similar conclusions in mesoscopic systems [262].

Using the electronic structure of the semiconductor, the electronic properties namely (i) the conductance (G), (ii) the Seebeck coefficient (S) and (iii) the electronic thermal conductivity (κ_e) for an 'N' dimensional system are calculated using the Landauer formalism [51] in the low temperature difference and zero current limit as shown, in Eq.(8.8-8.10).

$$G = \frac{2q^2}{h} \cdot \left(\Lambda_0 \right) \ [\Omega^{-1} m^{N-1}] \tag{8.8}$$

$$S = \frac{k_B}{-q} \cdot \left(\frac{\Lambda_1}{\Lambda_0} \right) \ [V/K] \tag{8.9}$$

$$\kappa_e = \frac{T_l 2k_B^2}{h} \cdot \left(\Lambda_2 - \frac{\Lambda_1^2}{\Lambda_0} \right) \ [W/m^{N-1}K] \tag{8.10}$$

where h is the Planck's constant, q is the electronic charge, k_B is the Boltzmann constant, T_l is the lattice temperature. This provides the three electronic parameters in the yellow boxes shown in Fig. 8.3. The dimensionless parameter Λ_m is defined in Eq.(8.11).

$$\Lambda_m = \int_{E_{min}}^{E_{max}=E_{fs}+10k_BT_l} \left(\frac{E - E_{fs}}{k_B T_l} \right)^m \cdot \mathcal{T}(E) \cdot \mathcal{M}(E) \cdot \left(\frac{-\partial f_{FD}}{\partial E} \right) \cdot dE \tag{8.11}$$

where, f_{FD} is the Fermi-Dirac distribution for the electrons, $\lambda(E)$ is the mean-free-path (MFP) of the electron, L is the length of the conductor, E_{fs} is the Fermi level and E is the energy of the electrons. This unitless parameter in Eq.(8.11) contains the information of the bandstructure in terms of number of modes at an energy E, M(E), which represents how many conducting channels (or k states) are available at energy E. For the numerical calculation of Λ_m it is important to correctly fix the upper and lower limit of energy integration depending on the position of the Fermi-level (E_{fs}). In the calculations E_{max} should be atleast $10k_BT_l$ higher than the E_{fs} for the integral to converge (details in Sec. 8.4.4).

The lattice thermal conductivity (κ_l) can be similarly calculated using Landauer's approach as [138, 153, 263],

$$\kappa_l(T) = \hbar P_1 \quad [W/m^{N-1}K] \tag{8.12}$$

$$P_j = \int_{\omega_{min}}^{\omega_{max}} \mathcal{T}(\omega) \cdot \mathcal{M}(\omega) \cdot \omega^j \cdot \frac{\partial}{\partial T}\left[(\exp(\frac{\hbar\omega}{k_B T}) - 1)^{-1}\right] \cdot d\omega \tag{8.13}$$

where P_j is the jth order phonon energy integration. The terms $\mathcal{M}(\omega)$ and $\mathcal{T}(\omega)$ are the density of modes and the transmission of the modes at phonon energy ω, respectively.

The transmission of a conducting channel at energy E, under the diffusive transport assumption, is approximately given by,

$$\mathcal{T}(E) \approx \frac{\langle\lambda(E)\rangle}{L} \tag{8.14}$$

where, $\langle\lambda(E)\rangle$ is the energy dependent MFP of the carrier and L is the length of the conductor. This enables the inclusion of simple scattering processes in the calculation of G, S and κ_l as suggested by Kim et al. [264]. Under the ballistic transport assumption all the energy channels conduct completely which is captured by setting $\mathcal{T}$(E)=1. However, in reality thermoelectric devices rarely operate in the ballistic regime. Different kinds of scattering processes can be captured in the calculations by setting $\mathcal{T}(\mathrm{E}) \leq 1$. More details on the calculation of the $\mathcal{T}$(E) under scattering is provided in Sec. 8.4.6.

8.4.2 A new mode counting algorithm

As outlined in the previous section, at the core of the Landauer's approach is the calculation of modes ($\mathcal{M}$(E)) [262–264]. The value $\mathcal{M}$(E) represents the number of conducting channels available for the carriers, like electrons or phonons, at a given energy. Most of the previous work using Landauer's approach relied heavily on very fine energy dispersion calculations and then calculating the $\mathcal{M}$(E) (by band-counting)

Table 8.1
Dimensionality of structure and dependence on 'k' vectors

Structure (dimension)	Periodic dim. (P)	Confined dim. (C)	$K_\perp$	$K_\parallel$	K
Dots (0D)	0	3	0	0	$\|\mathrm{K}\| = 0$
Wires (1D)	1	2	0	1	$[K_\parallel]$
Films (2D)	2	1	1	1	$[K_\perp, K_\parallel]$
Bulk (3D)	3	0	2	1	$[K_\perp^1, K_\perp^2, K_\parallel]$

from the dispersion. These methods are computationally very slow and inefficient since the energy grid for the modes and the dispersion needs to be the same or commensurate. Even BTE calculations require very fine k-grid in a reduced BZ. The reduction in the BZ size is often compensated by the increase in the fineness of the k-grid, thus leaving the computation time very similar or even increasing it.

In this section an efficient and robust method to obtain the modes from a given complex energy dispersion (electronic or phonon),E(k), is provided. The present method has the following advantages over the previous band-counting methods [262–264],

- The energy dispersion can be quite sparse. The sparsity limit on the energy grid is discussed later in this chapter.
- The energy grid for the $\mathcal{M}$(E) and dispersion does not have to be one-to-one.
- Since dispersion grid can be sparse, the dispersion compute time is reduced.
- The sparsity of the $\mathcal{M}$(E) energy grid also allows faster calculation of the TE parameters (G, S, κ_e, and κ_l), but at the cost of some accuracy loss.

8.4.3 Mode calculation steps

The step by step procedure for the calculation of $\mathcal{M}$(E) (applicable to both electrons and phonons) is given below,

- Obtain the energy dispersion of an N-D system, where $N = 0$, 1, 2 or 3, periodic material. The momentum vector $'K'$ can be decomposed into two components, (i) along the transport direction denoted by $K_{\parallel}$ and, (ii) in the direction perpendicular to the transport direction denoted by $K_{\perp}$ depending on the dimensionality of the structure (see Table 8.1).

- For each combination of $K_{\perp}$, a 1D $E(K_{\parallel})$ is obtained which is used for mode counting. The energy grid for the $\mathcal{M}$(E) (EGD) is created based on the 1D $E(K_{\parallel})$ for all the $K_{\perp}$. This energy grid does not have to be one-to-one with the energy values from the $E(K)$ data. The details of choosing the energy limits for the electrons and phonons are outlined in Sec. 8.4.4 and Sec. 8.4.5, respectively. The energy grid should be carefully chosen so as to provide a reasonable compromise between the computation time and accuracy of the results.

- For a 1D $E(K_{\parallel})$, the group velocity (v_{grp}) is calculated to find out the regions of monotonic variation in the energy with $K_{\parallel}$. Only positive $K_{\parallel}$ are considered since the $E(K_{\parallel})$ relations are symmetric. The +ve half group velocity is calculated as,

$$v_{grp} = \frac{1}{\hbar}\frac{\partial E(K)}{\partial K_{\parallel}} \tag{8.15}$$

  The monotonic velocity regions for an example $E(K)$ are shown in Fig. 8.6.

- These monotonic energy regions are then used for counting modes. The EGD points are calculated by the interpolation of the $E(K_{\parallel})$ data points. The details for calculating the modes on the EGD is shown in Fig. 8.7. As a by-product of the calculation one also obtains the carrier velocity which can be used for the calculations of MFP.

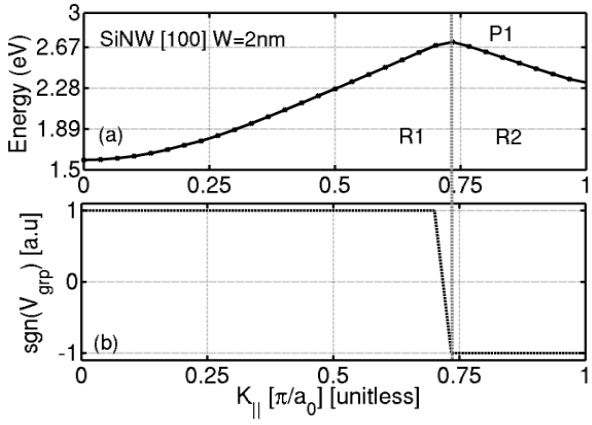


Fig. 8.6. Velocity at each point in the positive half of first CB sub-band for a 2nm × 2nm [100] SiNW. The important thing to note in the given band are the points where sign of the group velocity changes as shown in the bottom plot (b). These point is indicated as P1 in (a) and the corresponding region of interest is marked as R1, and R2 (b). Each point provides monotonic velocity range (increasing or decreasing) and calculations for $\mathcal{M}$(E) are performed separately for these ranges within a sub-band.

- The modes from each of the 1D $E(K_{\|})$ are then added over all the $K_{\perp}$ and divided by the unit-cell area (A_{uc}) to obtain the total $\mathcal{M}$(E).

The present method has the advantage that the original $E(K_{\|})$ can be sparse compared to the energy grid on which the $\mathcal{M}$(E) is calculated since the monotonic regions of $E(K_{\|})$ allow to interpolate the dispersion data to be used for $\mathcal{M}$(E) and velocity calculations. The strength of the algorithm to obtain the $\mathcal{M}$(E) for different K-grid densities is shown in Fig. 8.8. Since the algorithm can work on sparse dispersion data, the time to obtain the total modes is also reduced. However, this method is also limited by the fact that the dispersion should not be too sparse such that the original features of the dispersion are lost. In that case interpolation will give erroneous results. Also this method assumes that all the K vectors for a given energy dispersion are all orthogonal. The sensitivity of the final TE results on the K-grid sparsity and the compute time for $\mathcal{M}$(E) are discussed in Sec. 8.5.1 and Sec 8.5.2, respectively.

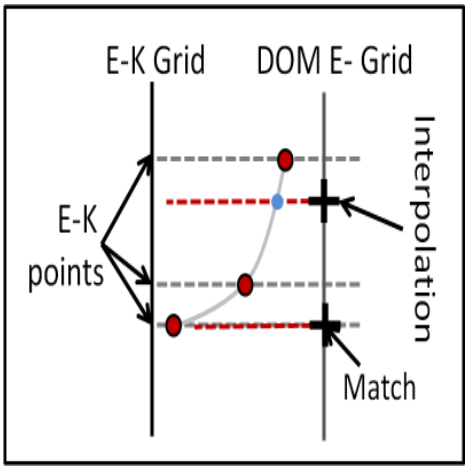


Fig. 8.7. The $E(k)$ points on the provided energy dispersion shown by dots. The energy grid for $\mathcal{M}$(E) (EGD) points are shown using crosses. These energy points are of two types, (i) the point matches an energy data point on the $E(k)$ grid, and (ii) the one which requires interpolation of the provided $E(k)$ relationship. The interpolation (either linear or quadratic) is done in the appropriate monotonic energy region like R_1 or R_2, as shown in Fig. 8.6. In this way the energy grid is created for $\mathcal{M}$(E) calculation.

Apart from the general steps adopted for the calculation of the $\mathcal{M}$(E) for both electronic and phonon dispersion, some special care in selecting the energy ranges, involved in Eq.(8.11) and (8.13), must be taken. The details about the implementation of these equations are given.

8.4.4 Electron transport kernel

In real materials, the electronic dispersion has many energy bands. However, the simulations are performed within a finite energy range depending on the position of the Fermi-level (E_F). To obtain correct results the energy cut-offs (E_{min}, E_{max} in Eq.(8.11)) are chosen such that the integral values for the transport parameters (Eq.(8.8-8.11)) do not show any variation. The bounds for the energy grid (Eq.(8.11)) of the $\mathcal{M}$(E) is obtained as follows,

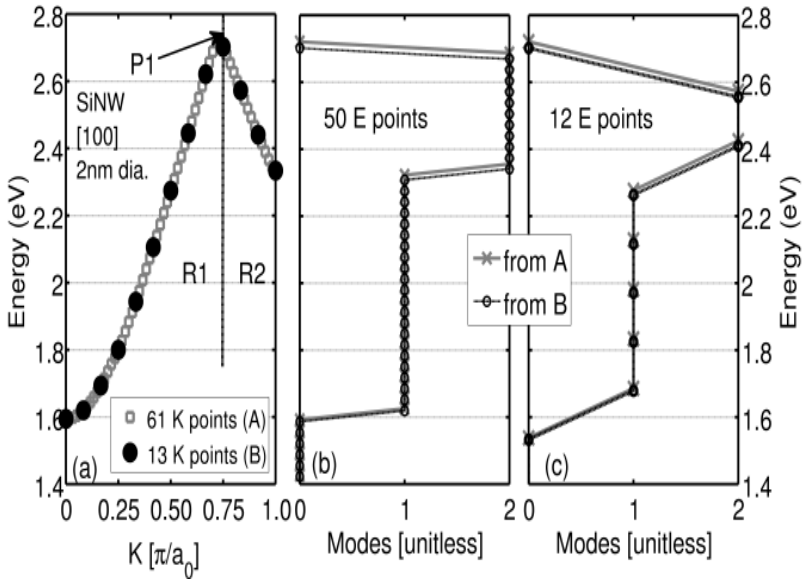


Fig. 8.8. (a) $E(k)$ relation with different number of k points. Case A with 61 K points and case B with 13 K points. Also the two monotonic $E(k)$ regions are shown (R1 and R2) along with the turn around point P1. $\mathcal{M}$(E) calculated for the two $E(k)$ grids using (b) 50 energy points and (c) 12 energy points. The $\mathcal{M}$(E) matches 100% for all the 4 cases showing the robustness of the $\mathcal{M}$(E) calculation method. As long as the sparse $E(k)$ captures the important turn around points (like P1) correctly the $\mathcal{M}$(E) calculation algorithm obtains the correct number of modes.

$$E_{max} = Ec \quad or \quad min[max[E(K_{\parallel})\forall K_{\perp}]] \tag{8.16}$$

$$E_{min} = Ev \quad or \quad max[min[E(K_{\parallel})\forall K_{\perp}]], \tag{8.17}$$

where $min(max)$ represent the minimum (maximum) value in a given numerical array. The terms Ec and Ev define the conduction band minima (CBM) and the valence band maxima (VBM), respectively (Fig. 8.9). Also calculations show that in order to obtain correct results, the E_F value can vary between the following limit,

$$E_{min} + 10k_BT \leq E_F \leq E_{max} - 10k_BT \tag{8.18}$$

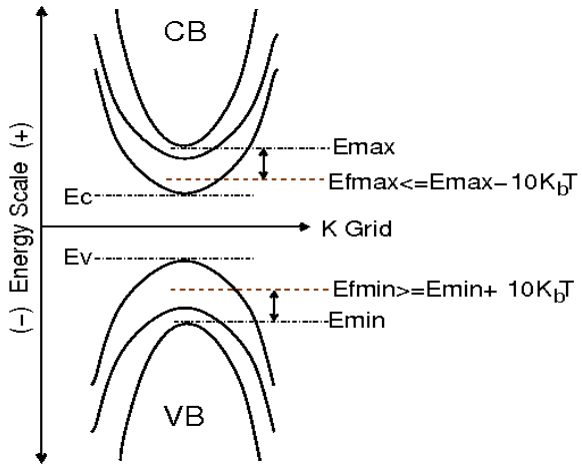


Fig. 8.9. Schematic showing the range of energy limit and the range of Fermi-level used for the calculation of the integral in Eq.(8.11) for electrons.

where k_B and T are the Boltzmann's constant and the temperature. The range of $10k_BT$ is a good choice for the integrals involved in the TE parameter calculations since the integrals become invariant to the choice of energy grid as shown in Fig. 8.10.

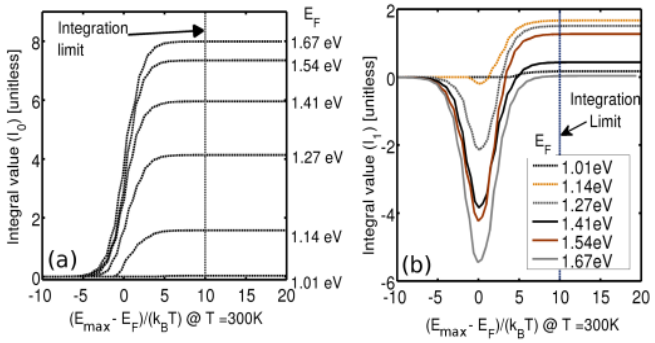


Fig. 8.10. Variation in the values of (a) I_0 and (b) I_1 (Eq.(8.11)) for different values of the Fermi-level (E_F). When the E_F is atleast $10k_B$T below the E_{max} then the integral values show less than 1% variation. Similar result is also obtained for the integral Λ_2.

8.4.5 Lattice transport kernel

The lattice kernel calculations do not depend on any kind of Fermi-level. Unlike the electron bands, the phonon bands are always within a fixed energy range with a varying number of sub-bands for different dimensional structures [196,212]. Also there is no negative phonon energy dispersion in stable semi-conductor structures [156], hence the energy grid of the $\mathcal{M}$(E) always contains positive values. The energy limit for the lattice kernel is chosen as follows,

$$\omega_{min} = 0 \quad or \quad \text{User defined} \tag{8.19}$$

$$\omega_{max} = \Omega_{max} \quad or \quad \text{User defined,} \tag{8.20}$$

where Ω_{max} is the maximum energy limit of the phonon dispersion.

8.4.6 Transmission calculation

For ballistic transport of electrons or phonons $\mathcal{T}$(E) for all the modes is 1. However, in reality carriers undergo a lot of scattering which depends on the dimensionality of the system, doping and temperature. This reduces the transmission of the modes below 1. For a conductor of length L, $\mathcal{T}(E)$ is given by [262, 263],

$$\mathcal{T}(E) = \frac{<< \lambda(E) >>}{L + << \lambda(E) >>} \tag{8.21}$$

where $<< \lambda(E) >>$ is the MFP obtained by the summing over all allowed k states at energy E. When $L >>$ MFP (diffusive limit) then Eq.(8.21) can be approximated as,

$$\mathcal{T}(E) \approx \frac{<< \lambda(E) >>}{L} \tag{8.22}$$

So all the scattering mechanisms present in a system is lumped in one single number, the 'mean free path'. The energy dependence of the MFP can be broadly categorized in two parts, (i) constant MFP (no energy dependence) and, (ii) energy dependent MFP. For some common scattering mechanisms such as ionized impurity and

acoustic phonon, $\lambda(E)$ can be expressed in a power law form as $\lambda(E) = \lambda_0(E/(k_BT))^r$, where E is the kinetic energy of the carrier, λ_0 is a constant and 'r' is a characteristic exponent describing a specific scattering process [262].

In most of the BTE calculations the scattering time (τ_{scat}) is used instead of MFP. Again for τ_{scat} the energy dependence are of two types, (i) energy independent, and (ii) energy dependent. The constant τ_{scat} case is physically hard to justify [262] while it is known that particles scatter to/from different energy states with different time constants. The connection of the scattering time to MFP is given as [262],

$$<< \lambda(E) >>= 2 \cdot \frac{\sum_K v_{\parallel}^2(K,E) \cdot \tau_{scat}(K,E)}{\sum_K |v_{\parallel}(K,E)|} \tag{8.23}$$

Here the summation is over all the K states at a given energy E. If the scattering time is assumed isotropic in K then the MFP is given as,

$$<< \lambda(E) >>= 2 \cdot \Big[\frac{\sum_K v_{\parallel}^2(K,E)}{\sum_K |v_{\parallel}(K,E)|}\Big] \cdot \tau_{scat}(E) \tag{8.24}$$

In the present algorithm, the MFP can also be calculated efficiently since the velocities are already obtained as a by-product of the $\mathcal{M}$(E) calculation. In the case of constant scattering time, the energy dependence of the MFP comes purely from the electronic bandstructure.

8.5 Results and Discussion

In this section the results on the dependence of calculated TE parameters on the sparsity of the K-grid using the algorithm are provided. The timing analysis is provided to get an idea about the total speed up with K-grid reduction and what part of the calculation consumes the maximum compute time. Also the comparison of the $\mathcal{M}$(E) and TE parameters, calculated from the algorithm, with analytical expressions and real materials are provided.

Table 8.2
Parameters used for the generation of parabolic bands

Structure (Dim)	$m^*_{\parallel}$ $\times m_0$	$m^*_{\perp 1}$ $\times m_0$	$m^*_{\perp 2}$ $\times m_0$	E_c eV	E_v eV	a_0 nm
Wires (1D)	1	–	–	0.2	-0.2	1
Films (2D)	1	1	–	0.2	-0.2	1
Bulk (3D)	1	1	1	0.2	-0.2	1

8.5.1 Sensitivity analysis: How robust is the algorithm ?

To understand the strengths and limitations of the algorithm, K-grid sensitivity tests are performed using parabolic $E(k)$ dispersions for 3D, 2D and 1D cases. The parameters used for the generation of the parabolic bands are shown in Table 8.2.

To start the sensitivity calculations, first a base K-mesh is chosen. A K-grid with 100 points in each direction (-π/a_0 to π/a_0) is found to be sufficient to provide stable results. A finer K-mesh does not change the final results by more than 0.5% for any of the calculated TE values. Three different types of studies were performed to determine the sensitivity of the algorithm to reduction in $K_{\parallel}$ and $K_{\perp}$,

- Case A: Reduction in $K_{\parallel}$ down to $\sim$ 60%-80%, keep $K_{\perp}$ fixed at 100 grid points.
- Case B: Reduction in $K_{\perp}$ down to $\sim$ 60%-80%, keep $K_{\parallel}$ fixed at 100 grid points.
- Case C: Reduction in both $K_{\parallel}$ and $K_{\perp}$ down to $\sim$ 60%-80%.

The percentage error in the maximum power factor (PF_{max}) is related to the error in S and G by the following,

$$\frac{\Delta PF_{max}}{PF_{max}} = 2 \cdot \frac{\Delta S}{S} + \frac{\Delta G}{G}, \tag{8.25}$$

where ΔS/ΔG are the variations in Seebeck coefficient and electronic conductivity. The final fluctuation in the PF_{max} depends on the sign of ΔS/ΔG. However, all the

fluctuation plots are shown for the absolute value of the errors. Whenever the final error in PF_{max} is smaller than the corresponding error in S or G indicates a sign change in either of the quantities.

For the sake of brevity only the 2D results are shown. Other dimensions (3D and 1D) show similar results and the outcomes are similar. For the 1D system only case C is applicable (as there is no $K_\perp$ present in the 1D case).

Sensitivity Analysis: Case A

The reduction in $K_\parallel$ down to 60% results in less than 1% variation in S and $\sim 6\%$ variation in G (Fig. 8.11 a). The corresponding fluctuation in PF is around 5% (Fig. 8.11 b). The Fermi-level at which the maximum PF is extracted however remains unchanged. So the fluctuation in the TE values arises just from the fluctuation in the $\mathcal{M}$(E). Thus, the present $\mathcal{M}$(E) calculation method is quite robust to reductions in $K_\parallel$ given the $K_\perp$ has good mesh density.

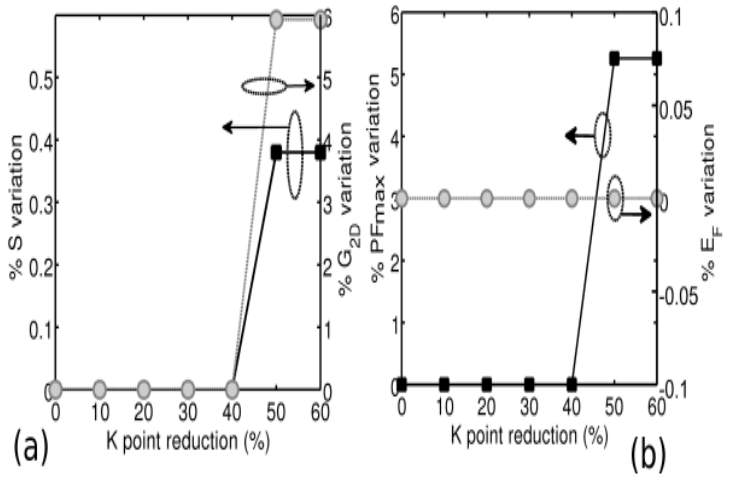


Fig. 8.11. Impact of $K_\parallel$ point reduction on (a) S (left) and G (right) and (b) PF (left) and E_F (right) in a 2D structure. All the values are extracted at the maximum PF point. The $K_\perp$ has 100 grid points. Even for 60% reduction in $K_\parallel$ points none of the TE values show more than 6% variation.

Sensitivity Analysis: Case B

The reduction in $K_\perp$ down to 60% results in less than 2% variation in S and $\sim$ 12% variation in G (Fig. 8.12 a). The maximum fluctuation in PF is around 10% (Fig. 8.12 b). The Fermi-level at which the maximum PF is extracted shows a maximum variation of $\sim$2.5%. Thus, the fluctuation in the TE values arises from the fluctuation in, (i) the $\mathcal{M}$(E) and, (ii) the E_F. The present $\mathcal{M}$(E) algorithm is quite sensitive to variations in $K_\perp$.

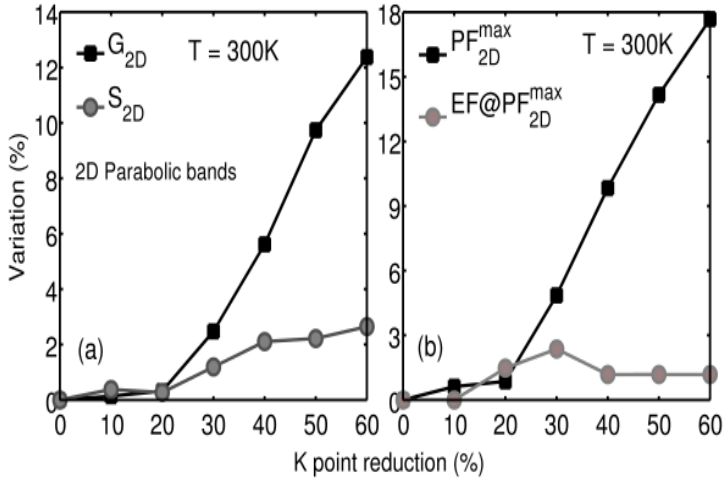


Fig. 8.12. Impact of $K_\perp$ point reduction on (a) S (left) and G (right) and (b) PF (left) and E_F (right) in a 2D structure. All the values are extracted at the maximum PF point. The $K_\parallel$ has 100 grid points. For 60% reduction in K-points G shows a maximum variation of 12% and PF_{max} has variation of around 10%.

Sensitivity Analysis: Case C

The reduction in all the K points down to 60% results in less than 5% variation in S and $\sim$ 13% variation in G (Fig. 8.13 a). The maximum fluctuation in PF is around 10% (Fig. 8.13 b). The Fermi-level at which the maximum PF is extracted shows a maximum variation of $\sim$2.5%. Thus, the fluctuation in the TE values arises from the fluctuation in, (i) the $\mathcal{M}$(E) and, (ii) the E_F. This case has almost similar

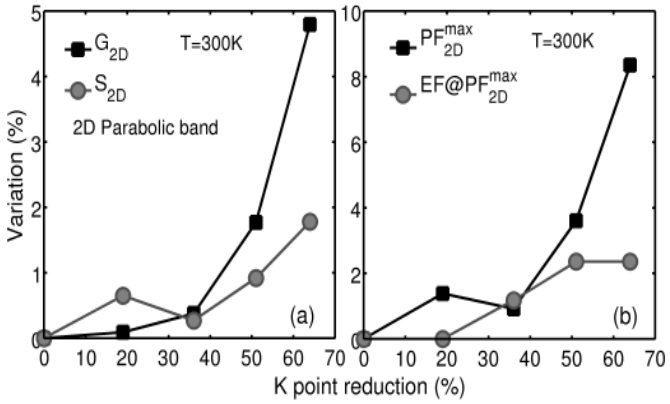


Fig. 8.13. Impact of reduction in all the K-points, on (a) S (left) and G (right) and (b) PF (left) and EF (right) in a 2D structure. All the values are extracted at the maximum PF point. G shows a larger fluctuation ($\geq$10%) compared to S fluctuation ($\leq$4%) which also reflects in the PF_{max} fluctuation.

k-grid sensitivity as case B, again showing that the present mode counting algorithm is sensitive to the variations in $K_{\perp}$.

8.5.2 Timing analysis

The present algorithm can calculate the TE parameters within reasonable error limits as shown in the previous section. Another obvious question that arises is how much computational speed-up can be achieved. The time to calculate the $\mathcal{M}$(E) for the three cases presented in the previous section is analyzed for 3D, 2D and 1D structures.

As the K density along all directions is reduced, the speed up for each dimension is different. For the 3D system, the time required goes up with total number of K-points (NK) with a power of 1.46 ($NK^{1.46}$). For the 2D case the power law is $NK^{0.48}$, and for 1D case the time taken is almost constant (in the given NK range). The algorithm takes roughly 900 seconds for 1 million K-points (100×100×100) for 3D case on nanoHUB.org workspace [265]. For the 2D case the time taken for ten

thousand K-points (100×100) is nearly 2 seconds and for 1D case the time taken is roughly 0.1 second for 100 K-points. All these results are shown in Fig. 8.14.

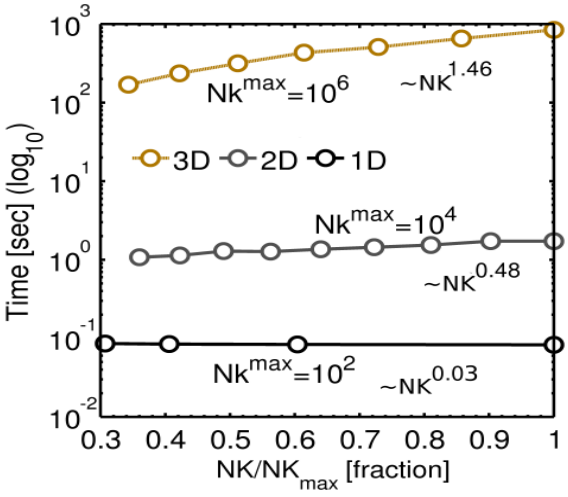


Fig. 8.14. $\mathcal{M}$(E) compute time for 1D, 2D and 3D parabolic bands. The number of K points are reduced along all the K-directions equally. The 3D case takes the maximum time due to higher number of K-points, followed by the 2D and the 1D case.

For the 2D and 3D cases, the algorithm requires different compute times with reductions in K-points along both the transport and the transverse direction. The compute time for the $\mathcal{M}$(E) (t_{DOM}) is roughly independent of the K-point reduction in transport direction for both the 2D and 3D cases as shown in Fig. 8.15. However, for a 60% reduction in $K_\perp$, the 2D case shows a t_{DOM} speed up factor of ∼2× (Fig. 8.15a). While for the 3D case, a speed up of ∼ 6× is observed (Fig. 8.15 b). A reduction in all K-points along all directions shows a similar speed up as the $K_\perp$ case (Fig. 8.15). Thus, the present algorithm shows a good speed up with $K_\perp$ point reduction.

8.5.3 Discussion: Algorithm aspects

The TE sensitivity analysis and t_{DOM} speed up reveal that the mode counting algorithm is more sensitive to the $K_\perp$ points compared to the $K_\parallel$ points. A reasonable

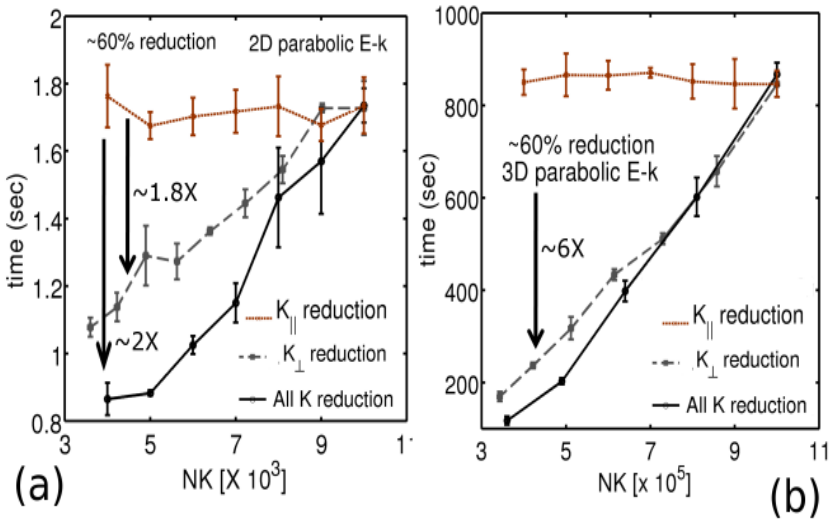


Fig. 8.15. $\mathcal{M}$(E) compute time (t_{DOM}) for the three types of K-point reduction for the (a) 2D structure and (b) 3D structure. For both the cases the compute time is almost independent of $K_{\|}$ reduction (brown line). reduces with $K_{\perp}$ point reduction. For each point 5 compute times are averaged.

reduction in $K_{\perp}$ must be chosen in order to optimize the compute time and to obtain reasonably stable TE parameter values. A summary of all the analysis is provided in Table 8.3. This table also provides the limits for reduction in K points in the $E(k)$ data-set to obtain TE parameters within a 10% error margin. In most of the cases a 50% reduction in K-points is easily achievable without a big penalty ($< 5\%$) on the calculated TE values.

The sensitivity analysis presented here is for parabolic bands, however, the general features of the algorithm remain quite similar even for the dispersions of real materials which are more complex than parabolic bands. Similar conclusions are obtained for phonon dispersions. Another way to speed up the calculations in this algorithm is to perform parallel computations. For $\mathcal{M}$(E) calculations the $K_{\perp}$ and $K_{\|}$ computations are independent of each other and hence the calculation for each $K_{\perp}$ can run on different processors thus considerably speeding up the compute time. In the present case, all the results are from serial calculations on a single processor.

8.5.4 Calculation of the TE parameters

The final verification of the algorithm is done by calculating the TE parameters for (i) the parabolic bands in 3D, 2D and 1D cases, and (ii) bulk Bi_2Te_3.

Parabolic Bands

The parameters used for the bands are shown in Table 8.2. For all dimensions the number of energy points in the $\mathcal{M}$(E) (EGD) is kept constant at 500. The analytical results for the modes and TE parameters are obtained from Ref. [262] and [264]. The number of modes for all the three dimensions compare very well ($\leq$ 4% error) with the analytical results as shown in Fig. 8.16. Using the modes, the TE values are calculated. Only the 2D case is shown in Fig. 8.17. The agreement with the analytical calculations is very good with $\leq$ 1% error in the numerical values. The 3D and 1D cases also show very good agreement with the analytical calculations. Thus, the algorithm provides accurate results for the electronic TE parameters.

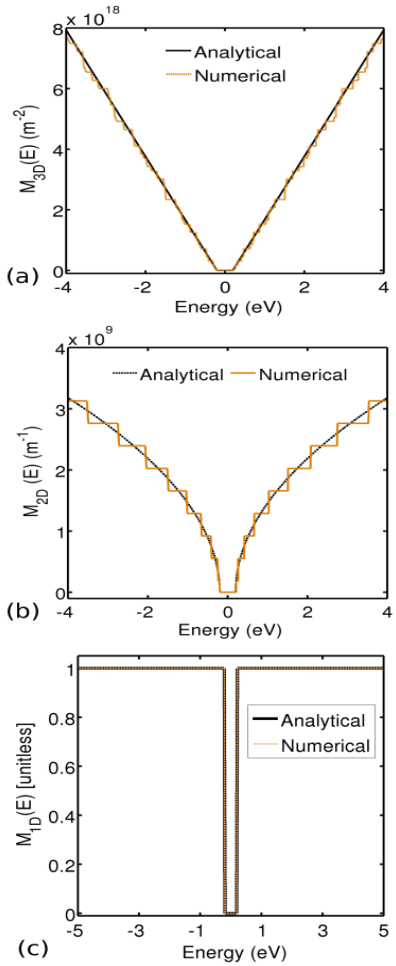


Fig. 8.16. Comparison of the numerical modes calculation using the algorithm with analytical modes calculation using parabolic bands with $m^* = m_0$ (from Ref [264]) for (a) 3D, (b) 2D and (c) 1D structure. The steps in the 2D case appear due to the sparse energy grid chosen.

Table 8.3
Summary of sensitivity and timing analysis for the mode counting algorithm with different K-grid sparsity.

Dimension	K-grid direction	Max. K reduction (%)	Max. error (%) S	G	PF	E_F	Good $E(k)$ sparsity ($\leq$)	$\mathcal{M}$(E) speed up (60% K red.)
3D	$K_{\parallel}$	80	-4.41	3.02	-5.65	4.14	70%	1.02×
3D	$K_{\perp}$	64	-5.3	-4.45	-11.49	1.02	50%	8.4×
3D	All-K	66	-5.3	15.2	5.9	5.2	50%	3.6×
2D	$K_{\parallel}$	60	-0.4	6	5	0	60%	1.1×
2D	$K_{\perp}$	60	-0.32	-9.30	-9.95	1.18	<50%	1.8×
2D	All-K	58	4.2	-13.3	-4.4	1.18	50%	1.5×
1D	All-K	80	4	13.2	20	3.8	70%	1.05×

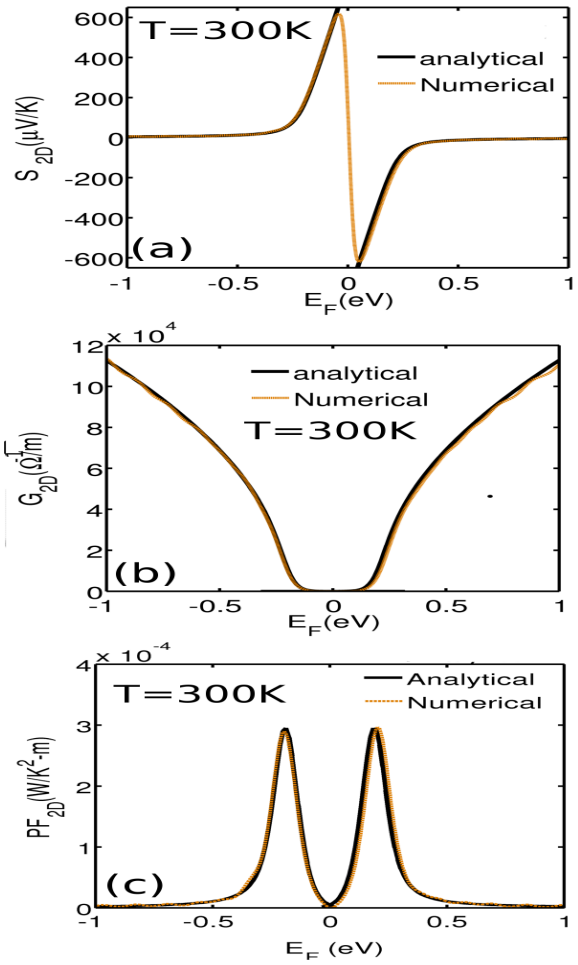


Fig. 8.17. Comparison of the numerical calculation with analytical expression for effective mass from Ref [264] for a 2D system for (a) Conductance (b) Seebeck Coefficient and (c) Thermoelectric Power Factor at 300K. The numerical results compare within 1% to the analytical values. The parameters used for the parabolic bands are provided in Table 8.2.

Real Bands: Bulk Bi_2Te_3

As a next step of verification, the algorithm is tested for the calculation of TE parameters for Bi_2Te_3. The same Tight-binding electronic dispersion is used for the calculation of the $\mathcal{M}$(E) as used in Ref. [262]. The agreement with the published $\mathcal{M}$(E) results is very good (within 1% error) (Fig. 8.18 a). Using the $\mathcal{M}$(E), the S

and G are also calculated which are used to obtain the PF. The calculated PF again shows a very good agreement with the published theoretical result [262] as well as with the experimental data [266] (Fig. 8.18 b). The lattice thermal conductivity of bulk Bi_2Te_3 is calculated using Eq.(8.12) and the phonon scattering processes outlined in Ref. [263]. The phonon dispersion is obtained using GULP [267]. The agreement of the calculated phonon modes with the published theoretical result [263] is very good as shown in Fig. 8.19a. Also the lattice thermal conductivity calculated in the present work shows a very good agreement with the experimental data [268]. Thus, the present algorithm provides accurate for the TE values, even for real materials.

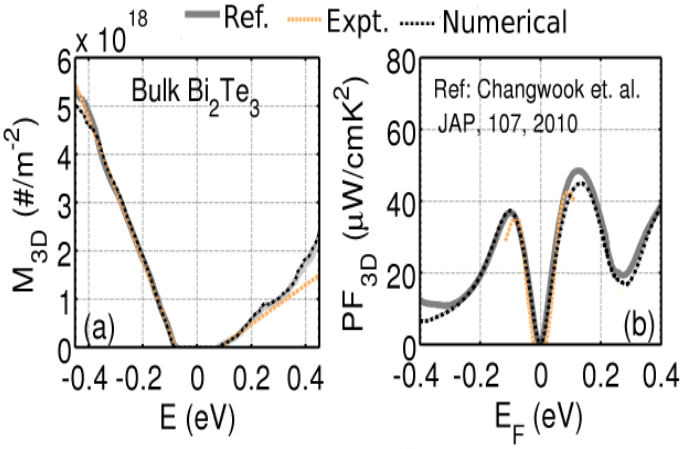


Fig. 8.18. Comparison of (a) $\mathcal{M}$(E) calculation and (b) Power factor at 300K for Bi_2Te_3, using the algorithm, with the theoretical calculations reported in Ref. [262] and experimental results from [266]. The electronic energy dispersion for bulk Bi_2Te_3 is obtained using the $sp^3d^5s^*$ tight-binding model [269]. The PF matching for Bi_2Te_3 is obtained assuming a constant mean-free-path of 18, 4 nm for conduction and valence bands respectively as reported in Ref. [262].

8.6 Summary and Outlook

In this chapter the reasons to pursue atomistic modeling of the thermoelectric properties in semiconductors are provided due to the shrinking dimensions of the TE

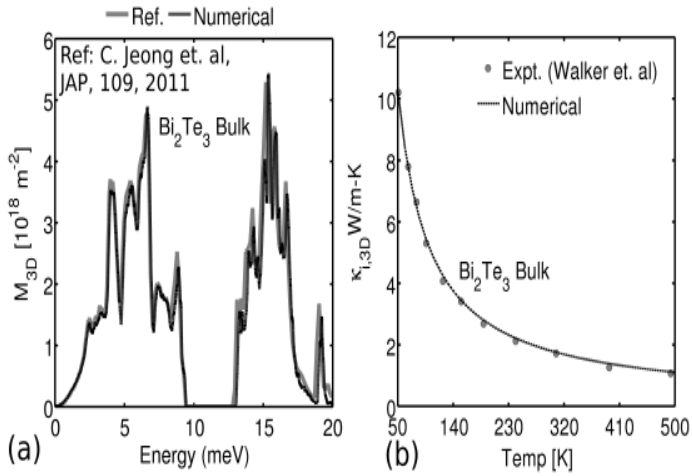


Fig. 8.19. (a) Comparison of the bulk Bi_2Te_3 phonon modes calculated using the algorithm and theoretical value reported in Ref. [263]. The bulk phonon dispersion is obtained using GULP [267]. (b) Comparison of the simulated and experimental [268] thermal conductivity for Bulk Bi_2Te_3 from 50 to 500K. The phonon scattering mechanisms considered here are outlined in detail in Ref. [263].

devices [30, 164, 165]. An efficient algorithm to calculate the electron and phonon modes in any dimension is presented. The algorithm provides an efficient implementation of the TE parameters calculation based on Landauer's approach and is likely to be extremely useful in readily and accurately evaluating existing as well as new thermoelectric materials. The algorithm is found to be sensitive to the transverse K point density in the $E(k)$ relation both in terms of the final TE parameter calculations as well as the compute time. A proper optimization of the K-point reduction is provided to allow for fast and accurate TE parameter calculations. The results from the algorithm are also bench-marked with analytical and real material TE parameter values. This algorithm will be useful for developing computer programs to evaluate the TE performance of new and artificial materials in the future.

9. BALLISTIC THERMOELECTRIC PROPERTIES IN SEMICONDUCTOR NANOWIRES

9.1 Introduction and Motivation

Nanowires have been shown as potential candidates for thermoelectric (TE) applications [32, 33] due to their ability to modulate the electronic DOS as well as suppressing the thermal conductivity by increased boundary scattering [270]. Figure 9.1 shows the ability to engineer the materials properties by dimensional scaling. It is essential to understand the effect of size scaling and different materials on nanowire thermoelectric properties. Such investigation may lead to smarter ideas for designing better TE modules [219, 271].

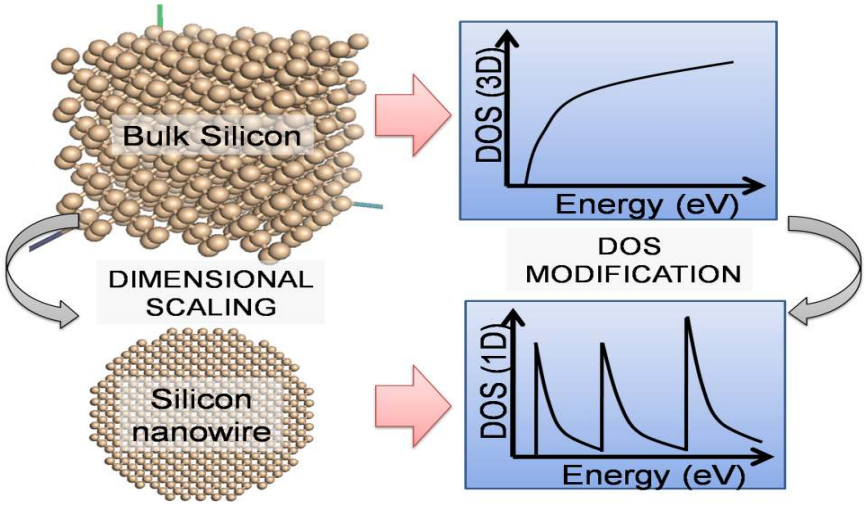


Fig. 9.1. With dimensional scaling the density of states of electrons gets modified due to geometrical confinement which can be useful for engineering electrical and thermal properties to make more efficient thermoelectric devices. This idea was proposed by Dresselhaus [7] and Mahan and Sofo [249].

This chapter is mainly focused on the application of the thermoelectric theory, developed in Chapter 8, to semiconductor nanowires. The simulation work by Kim et al. [264] provides gives a good overview of the dimensional dependence of the TE parameters using parabolic bands. The work in this chapter focuses on the application of full bandstructure, calculated using TB [40, 41] (see Chapter 2), to obtain the electronic transport parameters of nanowires and to understand the effects of cross-section size, orientation, strain, and nanowire material on these TE parameters.

The present chapter is organized as follows. First a study of the ballistic electronic thermoelectric parameter dependence on the size and orientation of nanowires is performed in Sec. 9.2. This is followed by the use of strain as a way to improve the PF in Sec. 9.3. Summary and outlook is provided in Sec. 9.4.

9.2 Ballistic electronic TE parameters in nanowires

In this section the influence of nanowire cross-section size, orientation and direction of confinement on the PF in Silicon (indirect) and GaAs (direct) [272] nanowires is studied. The main objective is to understand the variation of the thermoelectric parameters in different types of materials.

9.2.1 Comparison of GaAs and Si nanowires

This part provides a comparison of the electronic TE parameters for GaAs and Si nanowires.

Device details and Procedure

This part studies Si and GaAs nanowires with rectangular cross-section with width (W) and height (H) ranging from 2nm to 14nm with increments of 2nm in size. The surface atoms of these free standing nanowires are assumed to be hydrogen terminated [123] with no surface reconstruction [273]. The channel orientation of

these nanowires is [100]. Energy dispersion of the conduction bands for the nanowires are calculated using the TB model outlined in Chapter 2 and in Refs. [40, 45, 65, 66]. The energy dispersion for the CB for Si and GaAs are shown in Fig. 9.2. Once the electronic structure is obtained the thermoelectric parameters are calculated using Landauer's approach [51] as described in Sec. 8.4.

Results and Discussions

Only half of the k space is shown in the Fig. 9.2 since the +k and -k states are symmetric in energy for the NWs. Also the CBM has been shifted to 0eV to allow better comparison of the number of sub-bands and their spacing in energy. The E(k) for the smallest, 2nm × 2nm, Si and GaAs NW are shown in Fig. 9.2(a) and (c), respectively with 20 sub-bands each. The E(k) of the largest, 14nm × 14nm, Si and GaAs NWs are shown in Fig. 9.2(b) and (d), respectively with 140 sub-bands. The exact same number of sub-bands are also used for the numerical calculation of the thermoelectric parameters.

E(k) dependence on cross-section size: Electronic structure is a strong function of nanowire confinement dimension (W,H) as shown in Fig. 9.2. With increasing cross-section size the energy sub-bands start to bunch together since the effect of transverse confinement reduces. This results in two very important changes in the CB dispersion with dimension, (1) the energy separation between the sub-bands reduces which rapidly reduces the energy spread of the sub-bands and (2) the degeneracy of the valleys start to approach the bulk value and the number of bands in a given energy interval increase [274]. These two factors have a strong influence on the value of S and G of these wires. The interplay of these two factors reduce the value of S as the cross-section size increases. The value of G increases with increase in cross-section size since the number of conducting channels increase [274]. However, the number of electron channels (or modes) per unit area of the wire increases with decreasing wire cross-section area. This happens since the total number of modes become constant

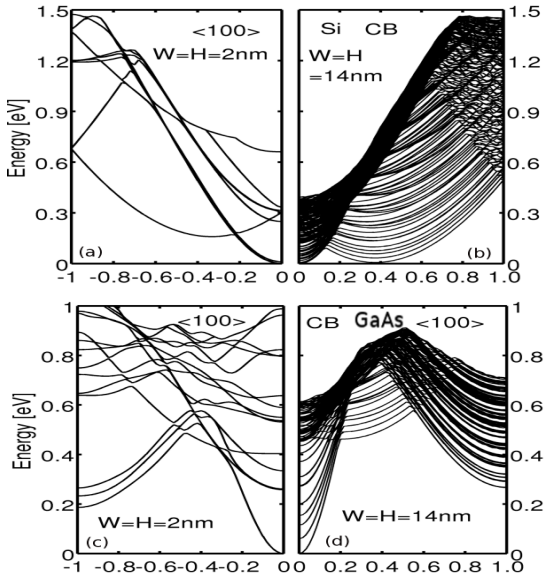


Fig. 9.2. Energy dispersion of conduction band for nanowires with rectangular cross-section of size (a) 2nm x 2nm and (b) 14nm x 14nm for Silicon and (c) 2nm x2nm and (d) 14nm x 14nm for GaAs. For smaller cross-section wires (2nm × 2nm) 20 sub-bands are shown and for larger wires (14nmx14nm) 140 sub-bands are shown. The same number of sub-bands are used in the calculation of TE parameters.

for extremely small wires (close to 1), hence the modes per area keep increasing with decreasing area [264, 274]. So a careful designing of the wire dimensions is required to extract the optimal PF in these nanowires taking into account these trade-offs.

Influence of wire dimension on the thermoelectric parameters: The results for the various thermoelectric parameters like S, G and PF are shown in Fig. 9.3. The G value is much larger in Si compared to GaAs for a fixed W and H due to higher valley degeneracy compared in Si. The value of G keeps increasing with cross-section size due to the reasons explained above. The S value in Si and GaAs nanowires are comparable which reflects that S depends primarily on the position of the Fermi Level (E_f) w.r.t CBM. The S values degrades very rapidly once E_f enters the CB. The value of S increases as wire dimension increases for both the materials since the number of bands near the Fermi-level are increase due to weaker geometrical confinement which reduces the sub-band energy separation [274]. The value of PF is higher in SiNW

compared to GaAs NW due to higher value of G. The value of S^2G increases with wire dimensions for both the materials.

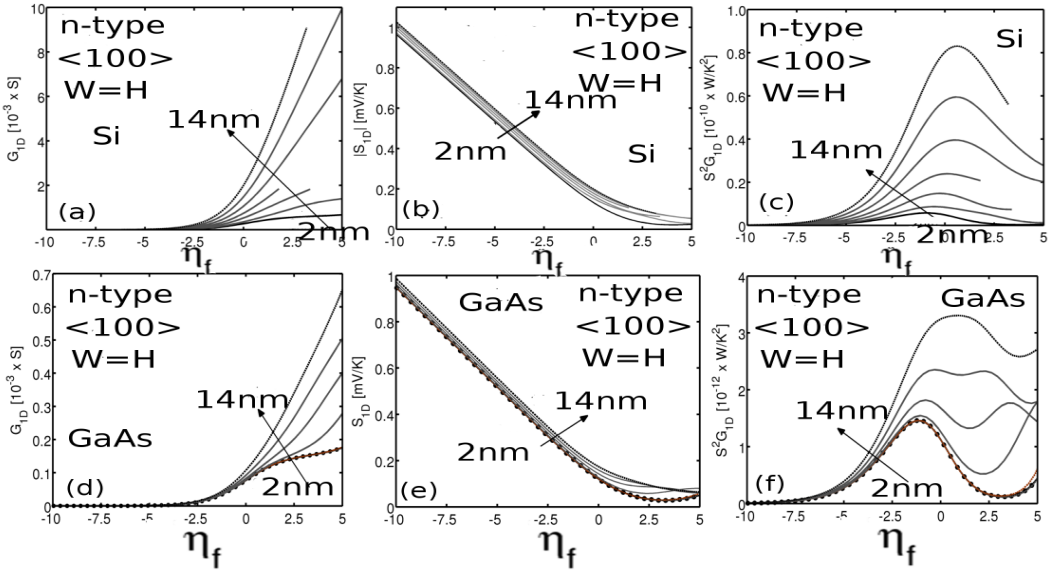


Fig. 9.3. Variation in G, S and PF with respect to $\eta_f = (E_f - E_c)/k_B T_l$ in 1D nanowires for different wire widths (W). (a) Variation in G, (b) variation in —S— and (c) variation in PF for different size Silicon nanowires. (d) Variation in G, (e) variation in —S— and (f) variation in PF for different size GaAs nanowires. S values in Si and GaAs are comparable where as the G is much higher in Si due to higher valley degeneracy which results in higher PF in Si compared to GaAs.

Distribution of thermoelectric metrics at PF_{max}: The value of PF_{max}, G and S at PF_{max} are shown in Fig. 9.4b and c. The value of S stays more or less constant for both the materials with cross-section variation . However, G shows a big change for wires with W/H $\leq$ 6nm for both Si and GaAs due to the reasons explained above and outlined in Refs. [66, 264]. This also results in an increase in the value of PF_{max} for the NWs as shown in Fig. 9.4a. Again the PF_{max} value is smaller for GaAs compared to Si.

Summary of the work

The Landauer's model is applied for the thermoelectric calculations in nanowires of different semiconductor materials. It is found that GaAs and Si show very similar Seebeck coefficient for electrons. However, the conductance value is higher for Si due to its higher valley degeneracy near the Fermi-Level. In both the material wires it is found that any significant improvement in the PF_{max} is obtained for wires with W/H $\leq$ 6nm.

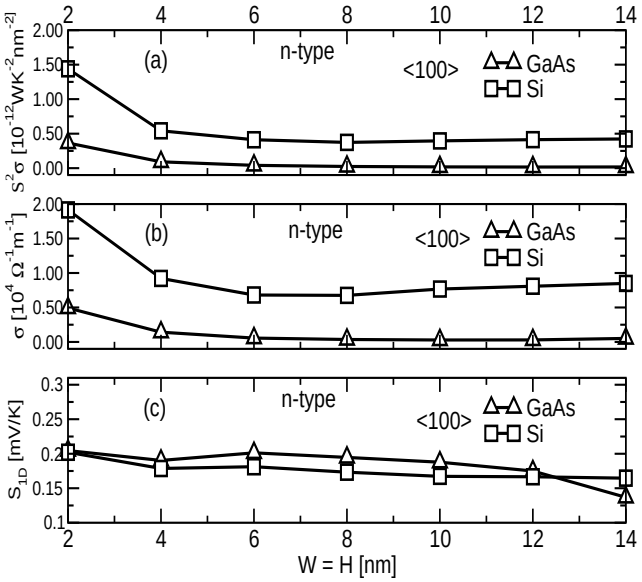


Fig. 9.4. (a) Value of PF_{max} for various Si and GaAs nanowires with W = H. W and H are varying from 2nm to 14nm in steps of 2nm. (b) Variation of G_{1D} at PF_{max} in Si and GaAs with W(H). The value saturates for larger wires. (c) Variation of $|S_{1D}|$ at PF_{max} in Si and GaAs. GaAs shows slightly higher $|S_{1D}|$.

9.2.2 Atomistic effects on the ballistic PF of Si nanowires

Improvement in ZT can be achieved by improving the thermoelectric power-factor (S^2G), the numerator of ZT. In this section the PF is studied using a combination of semi-empirical Tight-Binding method and Landauer approach. The effect of cross-

sectional confinement and wire orientation on the power-factor (PF) are studied. Details of this work are in Ref. [275].

Device details and Procedure

SiNW with cross-section size from 2nm × 2nm till 14nm × 14nm are simulated with sub-bands varying from 30 to 500 respectively. Large number of sub-bands are needed for the correct calculation of S and G. The projected unitcells for the three orientations (a) [100], (b) [110], and (c) [111] are shown in Fig. 9.5. In the E(k) calculation all the wire surfaces are hydrogen passivated. The X-axis denotes the transport direction and Y-Z denote the wire confinement directions as shown in Fig. 9.5.

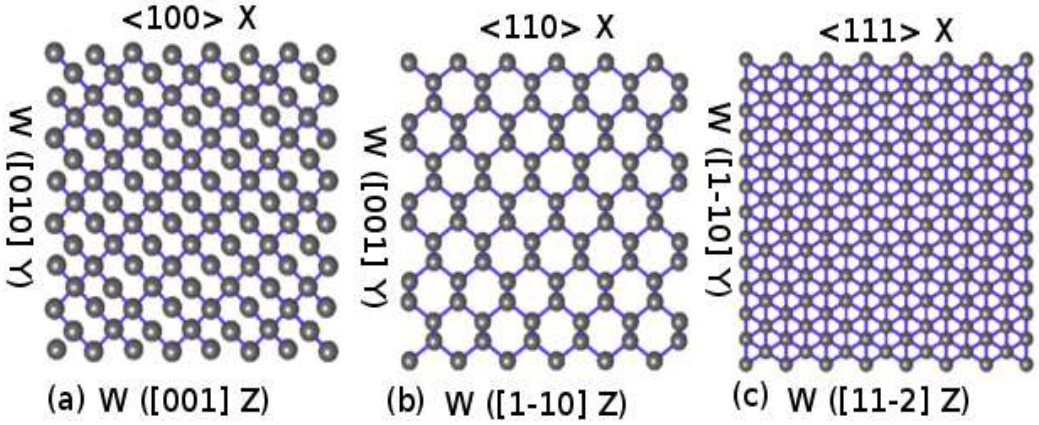


Fig. 9.5. Projected unitcells of SiNWs with different channel orientations (a) [100], (b) [110] and (c) [111] with W = 3nm, H = 3nm.

Results and Discussion

Effect of height and width confinement on E(k) and S: The unitcells show a very different atomic arrangements for different orientations as shown in Fig. 9.5. Atoms are arranged symmetrically along W-H for [100] oriented wires. In [111] and [110] oriented wires Y-Z directions are not symmetric. This geometrical asymmetry changes

the confinement in the unitcell at the atomic level, which affects the the energy bands. This in turn affect the thermoelectric properties. The E(k) for three different orientations show that (i) ⟨100⟩ oriented wires are symmetric for both Y-Z direction confinement as shown in Fig. 9.6, (b) ⟨111/110⟩ wires have different effect of confinement along W and H direction as shown in Fig. 9.7 and 9.8. This implies that width and height confinement are not equivalent at the atomic level which affect the electron modes ($\mathcal{M}(E)$) and hence the TE parameter values.

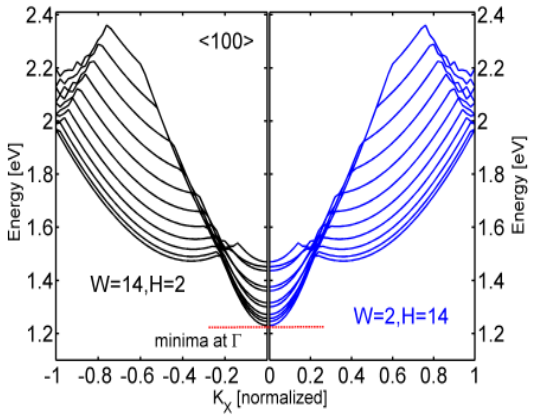


Fig. 9.6. Effect of W and H confinement on the E(k) of [100] SiNW. The width and height confinements are similar which result in exactly same E(k). The atomic structure is shown in Fig. 9.5(a).

The difference in the geometrical confinement changes the valleys which are occupied first. This changes the DOS of the system and S and G in turn. The effects of confinement and asymmetry in the Seebeck coefficient (S) are captured in Fig. 9.9. The [100] SiNWs show symmetric S for both W and H confinement as shown in Fig. 9.9a. Wires below 5nm × 5nm show higher S. For [110] SiNWs the asymmetry is more pronounced as shown in Fig. 9.9b. It is more beneficial to confine the [110] wires along the height (Y) than width. The [111] wires also show asymmetry in S with confinement as shown in Fig. 9.9c. S has higher value for W confinement than H confinement in [111] SiNWs. Thus, directional confinement of nanowires is an important design parameter to make high S value TE devices at the nano-scale.

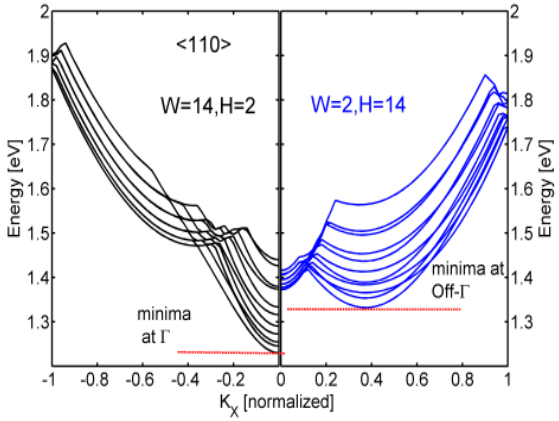


Fig. 9.7. Effect of W and H confinement on the E(k) of [110] SiNW. The width and height confinements are different as seen from the atomic arrangements (Fig. 9.5b) which affect the E(k).

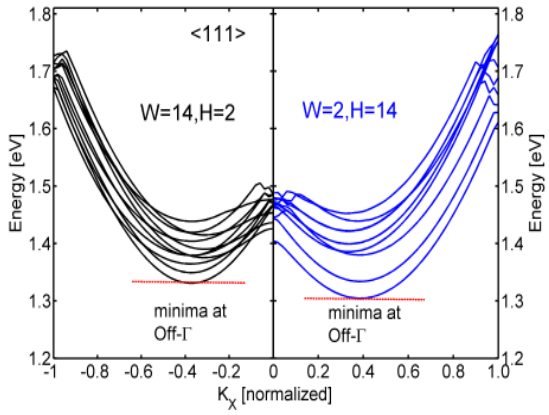


Fig. 9.8. Effect of W and H confinement on the E(k) of [111] SiNW. The width and height confinements are different as seen from the atomic arrangements (Fig 9.5c) which affect the E(k).

Directional dependence of PF_{max} in SiNW: The maximum PF shows a significant improvement only for wires with cross-section dimensions below 6nm × 6nm for all the orientations as shown in Fig. 9.10a. The [111] oriented SiNWs show the best PF since they have more number of degenerate valleys near the Fermi Level (∼6 compared to 4 and 2 in [100] and [110], respectively [66]). The S value at PF_{max} is

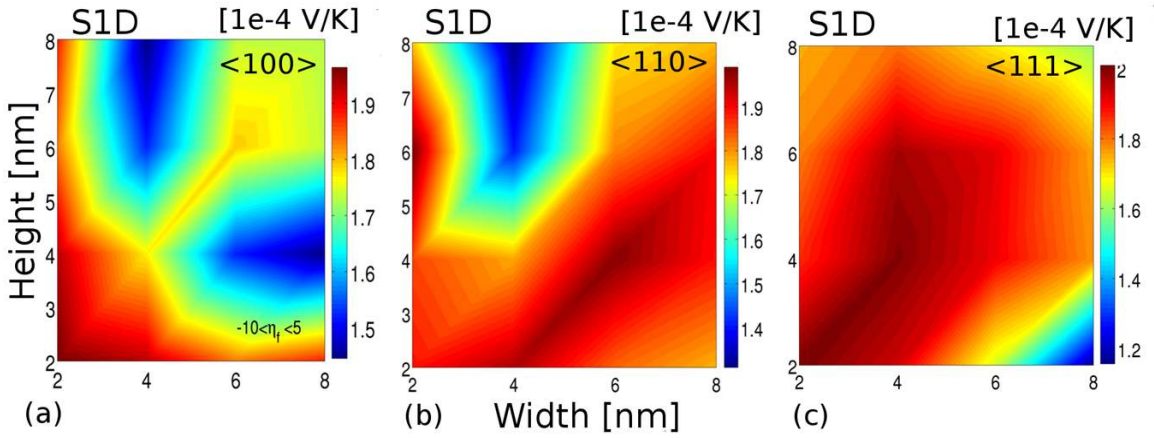


Fig. 9.9. Orientation dependence of Seebeck Coefficient in SiNW at PF_{max}

almost the same for all the wires as shown in Fig. 9.10b. However, the G/area value increases below 6nm as shown in Fig. 9.10c, with [111] SiNWs as the best performer.

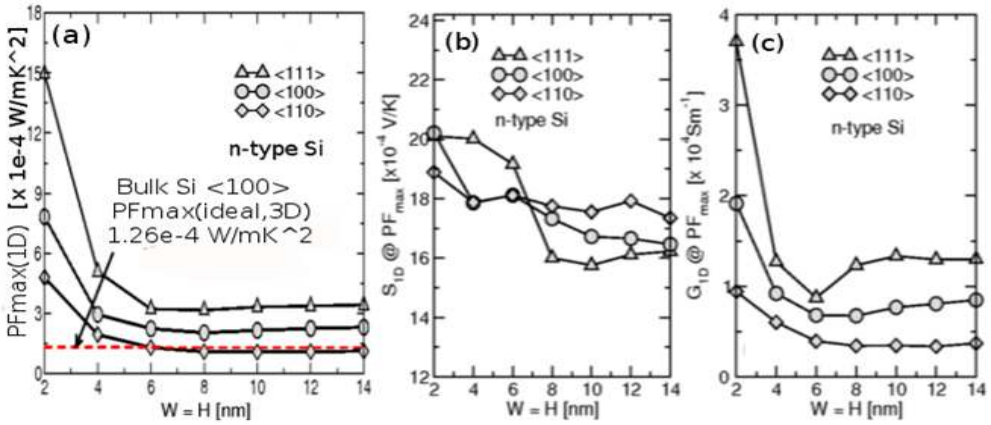


Fig. 9.10. Dimensional dependence of PF_{max} in SiNW

Summary of the work

SiNWs below 6nm × 6nm can serve as good candidates for high PF material with ⟨111⟩ as the best candidate. At the atomic level the width and height confinement

is very different and this will play a crucial role in designing better thermoelectric structures. Confinement direction plays a vital role in obtaining high S value in SiNWs.

9.3 Impact of Uniaxial strain on ballistic PF in NWs

It has been shown previously that strain can improve the ZT in thermoelectric materials [258]. In this section uniaxial strain is used to check whether it improves the TE PF. Si and Ge circular nanowires are strained in both the compressive and tensile regime and the change in the PF, G and S are observed as shown in Fig. 9.11. Both Si and Ge NW (diameter = 4nm) show improvement in the PF with uniaxial compressive strain. The reason for this improvement is explained in Sec. 9.3. One important observation is that GeNW do not show saturation ($\sim 2.25\times$ improvement over the unstrained value) in PF improvement unlike SiNW (only $\sim 1.14\times$ improvement over the unstrained value) where the PF starts degrading for higher compressive strain (Fig. 9.11).

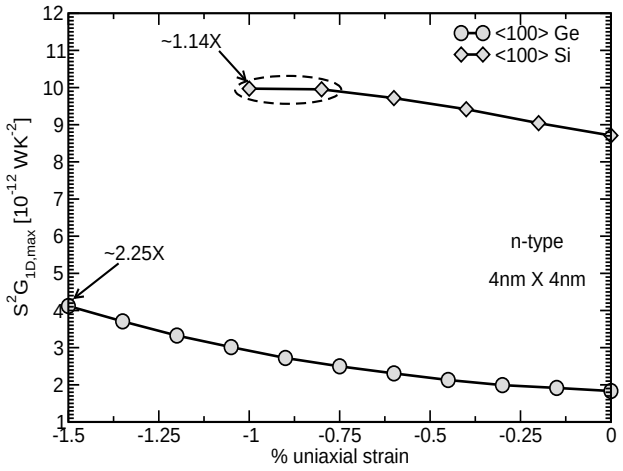


Fig. 9.11. Ballistic PF in n-type Si and Ge NW with diameter = 4nm and [100] orientation. Both the materials show an improvement in the PF with compressive strain since there are more bands close to the Fermi-level which improves the PF.

Another important study is to observe the dependence of both n and p-type ballistic PF in SiNW with the diameter variation as shown in Fig. 9.12. It is observed that the n-type PF improves for both the wire cross-section sizes with uniaxial compressive strain since the number of bands increase around the Fermi-level. The improvement in 4nm diameter wire is more compared to the 6nm diameter wire. Another important point to observe is that p-type PF degrades for any kind of strain. The reason is that the number of bands near the Fermi-level are more in the unstrained case compared to the strained case.

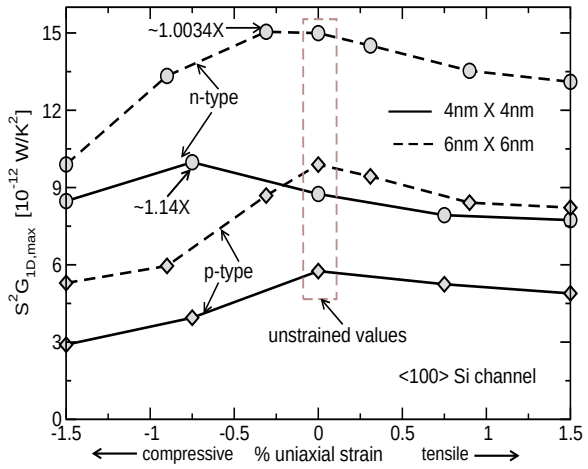


Fig. 9.12. n-type and p-type ballistic PF in [100] SiNW at diameter = 4 and 6nm. n-type PF improves with compressive uniaxial strain for both the wires, however, p-type PF degrades with both uniaxial compressive and tensile strain.

Why improvement in PF with strain ?

The improvement in the TE PF due to strain comes from the fact that the Seebeck coefficient improves compared to the unstrained case. This is explained by taking a simple 2 parabolic band calculation. The Ek for the two cases (1) unstrained and (2) strained are shown in Fig. 9.13. The individual Seebeck coefficient and conductance for each band 'i' is denoted by S_i and G_i.

In the case of more than one bands the effective S and G can be calculated as,

$$G_{eff} = \sum_{i \in n} G_i \tag{9.1}$$

$$S_{eff} = \frac{\sum_{i \in n} G_i \cdot S_i}{\sum_{i \in n} G_i} \tag{9.2}$$

where, n is the total number of sub-bands used for the calculation. The effective PF can be defined as,

$$\begin{aligned} PF_{eff} &= S_{eff}^2 G_{eff} \\ &= \left[\frac{G_i \cdot S_i}{\sum G_i}\right]^2 \cdot \sum G_i \qquad (9.3) \\ &= \frac{\left[G_i \cdot S_i\right]^2}{\sum G_i} \qquad (9.4) \end{aligned}$$

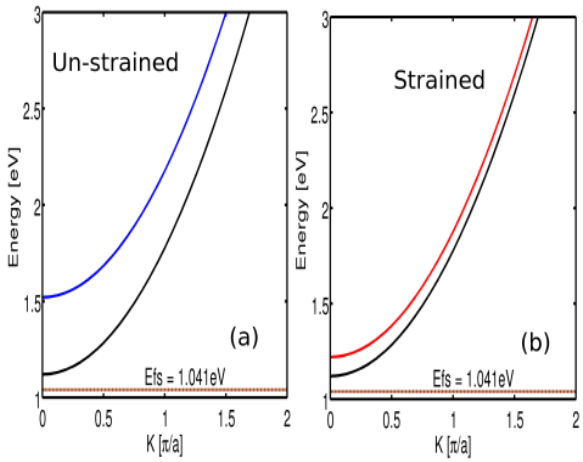


Fig. 9.13. Parabolic bands that are (a) unstrained, far separated from each other, and (b) strained (tensile), closer to each other. These bands are used to understand the reason for improvement from strain when the bands move closer to the Fermi Level.

Now applying this to the specific example of the two-band case the following is obtained,

$$G_{12} = G_1 + G_2 \tag{9.5}$$

$$S_{12} = \frac{G_1 \cdot S_1 + G_2 \cdot S_2}{G_2 + G_2} \tag{9.6}$$

Around the Fermi-Level where the maximum value of PF is attained the G_{12} can be approximated as,

$$\begin{aligned} G_{12} &= G_1 + G_2 \\ &\approx G_1 \quad since\ G_1 \gg G_2 \end{aligned} \tag{9.7}$$

Also the S_{12} value can be approximated as,

$$\begin{aligned} S_{12} &= \frac{G_1 \cdot S_1 + G_2 \cdot S_2}{G_1 + G_2} \\ &\approx S_1 + S_2 \cdot \frac{G_2}{G_1} \quad \text{due to Eq.(9.7)} \end{aligned} \tag{9.8}$$

Hence, we can see that the conductance remains unaffected whereas, the Seebeck value increases. The increase in the S value depends on two things, (a) the actual value of S_2 and (b) the ratio of G_2 and G_1. The following quantities for the un-strained and strained cases are shown in Fig.9.14 and 9.15, respectively.

The G value under strain and without strain remains more or less fixed (for the Fermi-level where PF is maximized). However, the effective S value under strain shows a significant jump ($\sim$ 4.4%) from the unstrained case. This increase in S translates into the increase in PF as shown in Fig. 9.16.

Summary of the work

Strain can be an effective way of improving the ZT in semiconductors which modifies the electronic structure (Fig. 9.17). The results reported here are qualitative in nature since only the ballistic values have been investigated. The inclusion of scattering can change the results which is studied in Chapter 10.

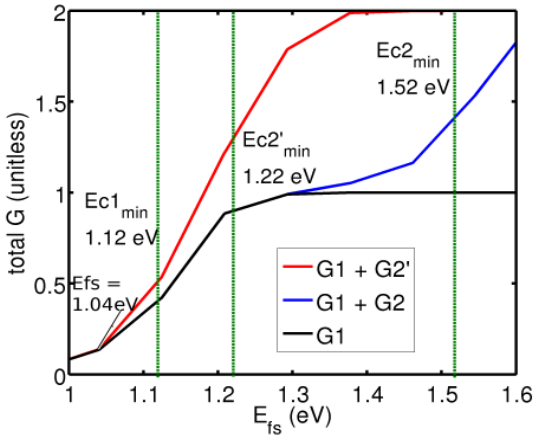


Fig. 9.14. Conductance (G) value for 1 band (black) and 2 band unstrained (blue) and strained (red) case. G increases when the number of channels increase. However, in the case of two band the strained and unstrained values of G are very close. The E_{fs} value where PF maximizes is at 1.041eV. At this point the G_{12}(unstrained) $\approx$ G_{12} (strained) $\approx$ 0.1357. So the G value remains unchanged from the 1 band case at this Fermi-level value.

9.4 Summary and Outlook

The atomistic model for the calculation of the electronic part of ZT has been applied to study the TE properties in a variety of semiconductor nanowires like Si, Ge and GaAs. It is found that the geometrical confinement, orientation, material and cross-section size play a significant role in the determination of the thermoelectric parameters. At the ultra-scale limit the meaning of width and height confinement can be very different which can lead to better design ideas for thermoelectric materials. A significant improvement in the ballistic PF and ZT is observed for [111] oriented wires, wires with dimension below 6nm and under the action of compressive uniaxial strain.

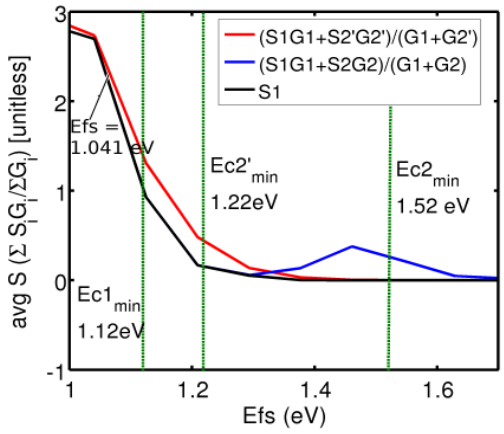


Fig. 9.15. Seebeck Coefficient (S) value for 1 band (black) and 2 band unstrained (blue) and strained (red) case. S increases when the number of channels increase near the Fermi-level. The S value increases from 4.27 (1 band case) to 4.28 (for two band unstrained case). The S value for the strained case increases from 4.27 (1 band) to 4.46 (2 band strained) ($\sim$ 4.4% inc.). Hence, S value shows a good jump under strain.

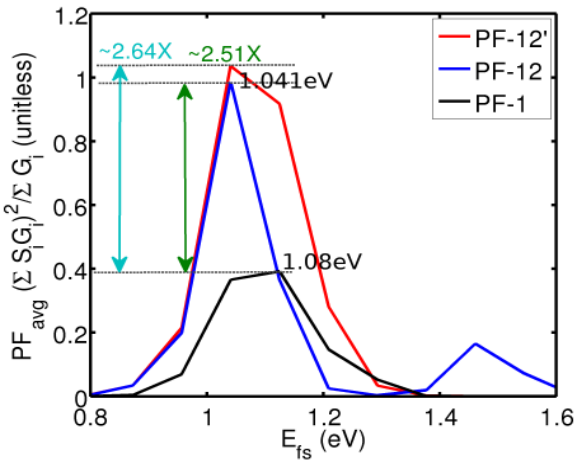


Fig. 9.16. Effective PF for 1 band (black) and 2 band unstrained (blue) and strained (red) case. The power-factor increases by $\sim 2.64\times$ for the strained case which is around $\sim 1.05\times$ more than the unstrained case.

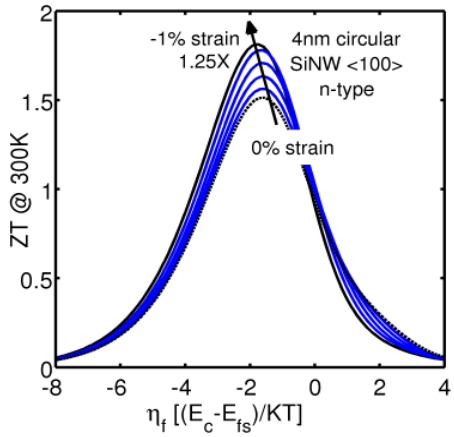


Fig. 9.17. ZT improvement for 4nm SiNW for n-type carries with uniaxial strain. Compressive uniaxial strain improves the ZT by $\sim$ 16% at T = 300K. Lattice thermal conductivity (κ_l) of 2 W/m-K is used which has been measured for Si nanowires [276].

10. DIFFUSIVE THERMOELECTRIC PROPERTIES IN SEMICONDUCTOR NANOWIRES

10.1 Introduction and Motivation

In the last two decades TE efficiency of semiconductors has considerably improved (ZT moved from 1 to above 2 [251]). The main reason for such an enhancement in ZT is due to the use of nanowires [32, 33], thin-films [250, 255], quantum dots [19], superlattices [252], nano-alloys and nano-composities [251, 277, 278]. A typical application of SiGe material in different type of TE structures is shown in Fig. 10.1. The emphasis is on achieving higher electronic PF (see Chapter 8 for details) as well as suppressing the lattice thermal conductivity. This chapter provides reliable modeling and simulation to study the thermoelectric performance of semiconductor nanowires.

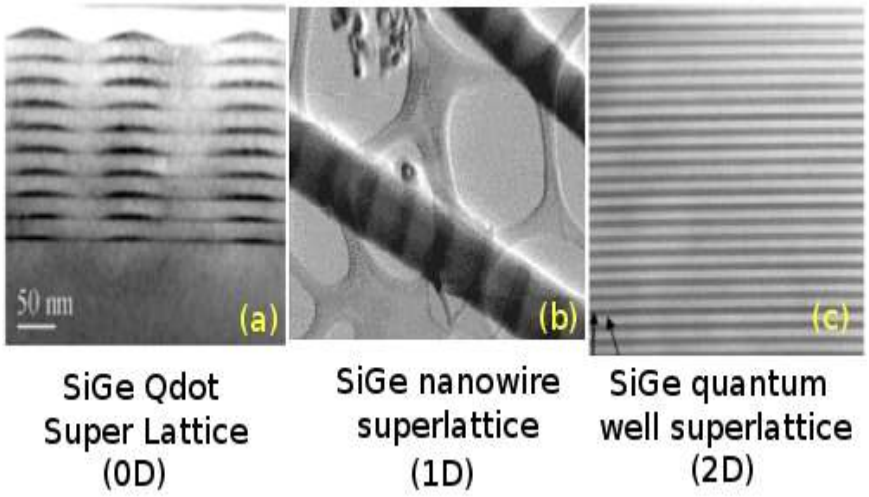


Fig. 10.1. Structural modification: SiGe superlattice (SL) in different dimensionalities (a) quantum dot SL with 0D structure [19], (b) nanowire SL a 1D structure [35] and (c) quantum-well structure (2D) [34]. They all report suppression of lattice thermal conductivity which can greatly enhance ZT.

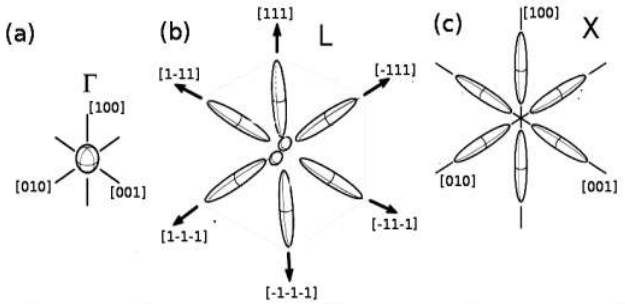
This chapter is mainly focused on the application of diffusive thermoelectric theory to explore the ways to improve the PF as well as ZT in semiconductor nanowires. The application of strain and wire orientation to optimize the ZT in GaAs nanowires is investigated. The porous Si nanowires are explored for ZT improvement motivated by the work on porous bulk Si [38, 220]. Finally all the understanding assimilated from modeling, simulations and benchmarking is used for creating a thermoelectric analysis tool, called the LANTEST.

The present chapter is organized as follows. A comprehensive analysis of thermoelectric performance of n-type GaAs nanowires is provided in Sec. 10.2. Thermoelectric performance analysis of porous SiNWs using simulations is carried out in Sec. 10.3. Section 10.4 briefly discusses the LANTEST tool. Summary and outlook are provided in Sec. 10.5.

10.2 TE properties of n-type GaAs nanowires: Role of strain and orientation

The thermoelectric PF and ZT of GaAs nanowires (NWs) can be improved by (i) choosing a proper wire growth and channel orientation and, (ii) by applying uniaxial tensile stress. In this work the impact of these two factors on PF and ZT are studied. Tensile stress, channel direction and cross-section size allows bandstructure engineering to tune the electronic conductance (G) and the Seebeck coefficient (S).

Inherent low thermal conductivity and high electron mobility can make GaAs a promising thermoelectric material [270,279]. However, GaAs suffers from DOS bottleneck which results in low electron density [280] and hence low electronic conductivity (G). It has been shown experimentally that nanowires (NWs) can improve the ZT many times over bulk material [32] due to two main reasons, (i) strong reduction κ_l [279, 281], and (ii) electronic DOS engineering allowing to increase the thermoelectric PF [32, 262]. The definitions of PF and ZT of a material are provided in Chapter 8.



Valley	Γ	L	X
ΔEc (eV)	0	0.28	0.47
m^*_l/m_0	0.067	1.9	1.3
m^*_t/m_0	0.067	0.075	0.22

Fig. 10.2. Three important conduction valleys in bulk GaAs, (a) Γ valley, (b) *L* valley and, (c) *X* Valley. The important masses and the energy difference (ΔE) of the valleys from Γ valley are also shown.

GaAs has 3 important conduction band valley minima, namely the Γ valley, the L valley and the X valley (Fig. 10.2). In relaxed bulk GaAs these valleys are well separated in energy (Fig. 10.2) and the electronic conduction dominantly takes place in the Γ valley which has a very small transport mass ($m^*_{tr} \sim 0.067m_0$, where m_0 is the free electron mass) but also has low DOS resulting in the 'DOS bottleneck' [280]. However, recent experimental work shows that uniaxial tensile stress can reduce this DOS bottleneck in GaAs by increasing the L valley contribution in the electronic transport [282]. Another recent proposal suggests the use of nanostructures grown on (111) surfaces to enhance DOS by confining one of the L valleys [100]. Guided by these experimental and theoretical work, a theoretical study is conducted to understand the impact of (a) channel and growth direction (X/Y), (b) uniaxial strain, and (c) cross-section size on the thermoelectric power factor and the ZT of n-type GaAs NWs.

Fabrication Details: The advancement in the process technology now allows the fabrication of high quality pure GaAs nanowires as well as core-shell nanowires. Some of the important fabrication processes are, (i) vapor-liquid-solid (VLS) technique for both n and p-type wires [23, 283] (ii) molecular beam epitaxy (MBE) [284, 285], and

(iii) solid phase nanowire growth [286]. Thus, better quality GaAs nanowires can be used for manufacturing thermoelectric modules.

10.2.1 Theory and Approach

The calculation of the electronic TE parameters (G, S and κ_e) is done using the Landauers approach as described in Chapter 8. Scattering is included in the transport using a constant relaxation time (τ_0). The constant τ assumption works well when the scattering mechanisms are assumed to be dominated by the acoustic and the zone center optical phonons (which are proportional to the electronic DOS) [219,287]. The value of τ_0 is chosen such that the electron mobility (μ_e) for a 6nm $\times$ 6nm square relaxed GaAs-NW comes out to be around 1200 $cm^2/V.s$ at an inversion charge density (Ns) of $1 \times 10^{12} cm^{-2}$ (Fig. 10.3). The bulk GaAs μ_e reported in the literature, at this Ns value, varies between 7100 to 2000 [284]. However, a lower mobility value is chosen to account for the additional defects that can be present in the nanowires like surface roughness (SR), impurities, etc [287]. The value of $\tau_0 = 1$ femto second (fs) is used in all the calculations.

The correct calculation of the DOM in ultra-scaled GaAs NWs relies on an accurate electronic bandstructure model. In the present study an atomistic 10 band $sp^3d^5s^*$ TB model [40, 65] is used. To properly model the band curvature (related to the effective mass) and the band off-sets for the X and L valleys in GaAs, a new set of $sp^3d^5s^*$ TB parameters have been been obtained which is provided in Appendix F.

10.2.2 NW details

Atomistic square GaAs NWs with intrinsic channel are studied with specific channel (X) and growth (Y) directions for a given width (W) and height (H=W) as shown in Fig. 10.4. Six different combinations of [X]/(Y) are considered for these NWs as outlined in Table 10.1 with W ranging from 2 to 6 nm. Uniaxial tensile strain (ϵ_{xx})

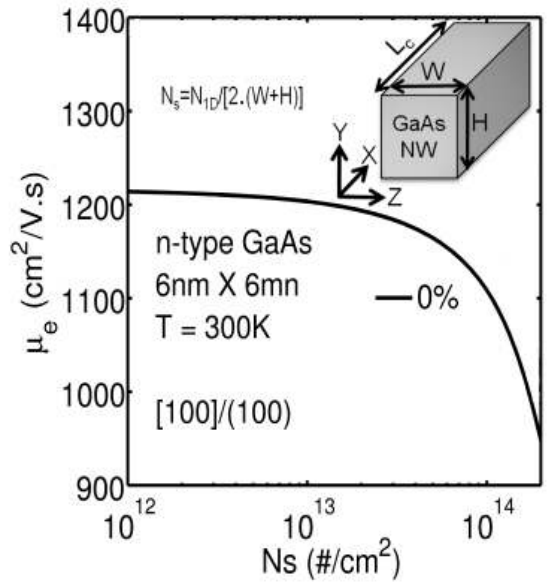


Fig. 10.3. Electron mobility calibration for GaAs nanowire of 6nm × 6nm cross-section size at T=300K.

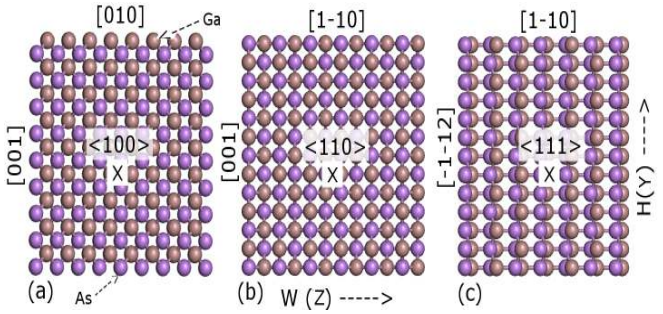


Fig. 10.4. Three projected unit cells (out of six considered in the work) of GaAs NWs with W = 3nm (Table 10.1). Y is the growth direction whereas X is the transport direction. (a) dev. I [100]/(100), (b) dev. III, [110]/(110), and, (c) dev. IV [111]/(110). The side wall orientations are also shown.

values used are 0, 0.5, 1, 2, 3 and 5% along the X direction. All the device terminal characteristics are calculated at T = 300K.

Table 10.1
Details of the channel orientation (X) and the growth direction (Y) for GaAs NWs used in this study.

NW label	I	II	III	IV	V	VI
Channel [X]	[100]	[1-10]	[1-10]	[1-11]	[001]	[011]
Growth (Y)	(100)	(111)	(110)	(110)	(110)	(100)

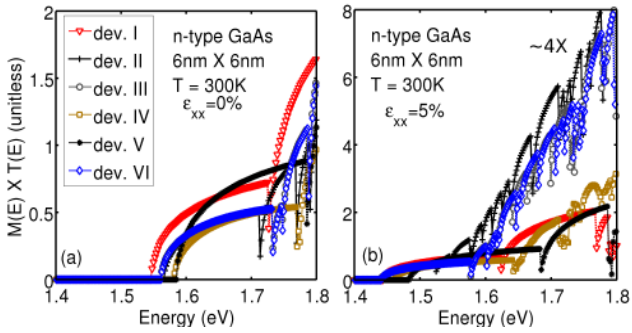


Fig. 10.5. Number of modes in all the 6 types of nanowires with cross-section size 6nm × 6nm under (a) relaxed condition, and (b) uniaxial strain. The number of modes in dev. II, III and VI increases by ∼4× under strain.

10.2.3 Results and Discussion

Uniaxial strain modifies the electronic density of states (DOS) which can affect both the electronic transport properties as well as the electronic scattering rates. The enhancement in the thermoelectric PF and ZT is optimized by the interplay of proximity of the Γ-L valley and scattering of the electrons in these valleys. The three engineering knobs which are controlled to optimize the thermoelectric performance in n-type GaAs nanowires are (i) uniaxial strain(STR), (ii) cross-section size (CS) and, (iii) wire orientation (OR).

The effect of the three factors (STR, CS and Or) on the transport properties is captured by the modes whereas the scattering effect for each mode is captured by the transmission ($\mathcal{T}$) (Eq.(8.21) and (8.24), Chapter 8). The effective modes ($\mathcal{M} \times \mathcal{T}$) for all the devices with 6nm × 6nm cross-section are shown for the relaxed and 5% uniaxial tensile strain case in Fig. 10.5 a and b, respectively. For the unstrained case all the devices show similar effective DOM (Fig. 10.5 a). For the strained case the effective DOM starts at a lower energy since the conduction bands (CB) shift downwards in energy under tensile strain(Fig. 10.5b). Devices II, III and VI show a ∼4× increase in the effective modes which eventually improves the thermoelectric PF in these nanowires (Fig. 10.5b).

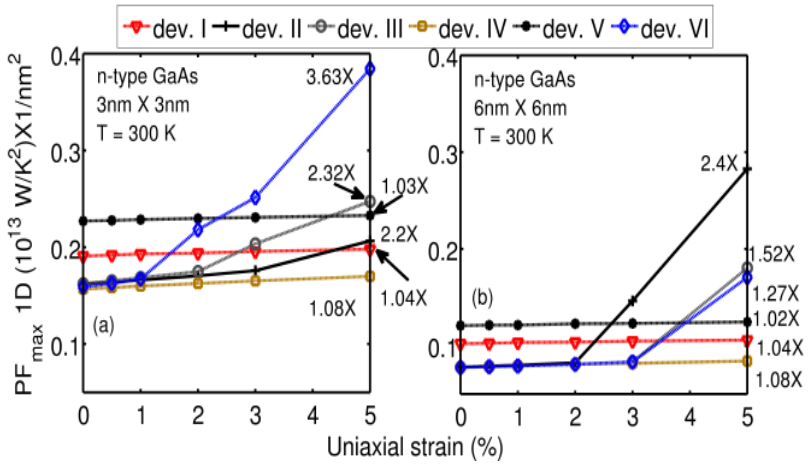


Fig. 10.6. Thermoelectric PF variation with uniaxial strain in (a) 3nm × 3nm and (b) 6nm × 6nm cross-section size GaAs-NWs for all the 6 device types (Table 10.1).

Uniaxial tensile stress improves the maximum thermoelectric PF in both 3nm and 6nm cross-section size wires as shown in Fig. 10.6. For 3nm wires the maximum improvement is obtained in device VI under 5% strain (∼3.6×) as compared to the unstrained device (Fig. 10.6a). Devices II and III also show ∼2.2× increase in the PF (Fig. 10.6a). These three devices also show an improvement of ∼2.5-1.5× for 6nm wires (Fig. 10.6b). The enhancement in the PF for these three devices is obtained by the increased contribution of the L valley to the conductance (G) under uniaxial tensile stress along with the Γ valley [282]. Smaller wires show larger improvement in PF due to reduced scattering effect on G as the valleys (Γ-L) are further apart in energy compared to the 6nm wires.

The impact of the wire cross-section size on the PF is shown in Fig. 10.7. As the wire cross-section size reduces the G per unit area increases since the number of conducting channels become constant for small diameter wires. This results in an increase in the PF per unit area for smaller wires. Under the unstrained case device I (where the Γ valley dominates the electronic transport) shows the maximum PF (Fig.10.7a). However, application of the uniaxial stress can increase the influence of the L valley on G which improves the overall PF (Fig. 10.7b). Device II, III and

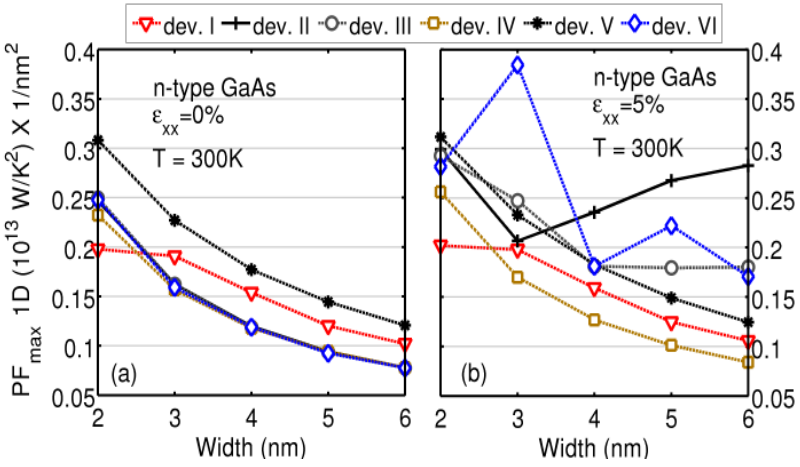


Fig. 10.7. Variation in the peak PF for n-type GaAs-NWs with cross-section size for all the devices types for (a) unstrained case and (b) strained case with 5% uniaxial strain.

VI show improvement in the PF even though the scattering also increases since the CB valleys move closer under strain. Thus, with the proper choice of orientation and wire cross-section size the PF of the n-type GaAs-NWs can be improved even in the presence of electron scattering.

The increase in the peak PF can be understood from the behavior of the individual components of the PF (S and G) under different strain, cross-section size and orientation. The S and G value for device VI are shown in Fig. 10.8 since in these wires the PF improves for all the cross-section sizes (2nm to 6nm). For 3nm × 3nm both S and G improve with uniaxial tensile strain (Fig. 10.8a, b). However, S and G improvements originate from different physical processes. The CB valleys (both Γ and L) come closer to the Fermi level (E_F) under tensile strain which increases the value of S. The value of G improves since the CB valleys are optimally separated in energy to provide more conducting channels for electrons and also suppresses the inter-valley scattering (Fig. 10.8 a and b). However, the larger wires (6nm cross-section size) show insignificant improvement in S and G with strain (Fig. 10.8 c and d). Thus, uniaxial tensile strain improves the peak PF more in smaller wires compared to the larger wires.

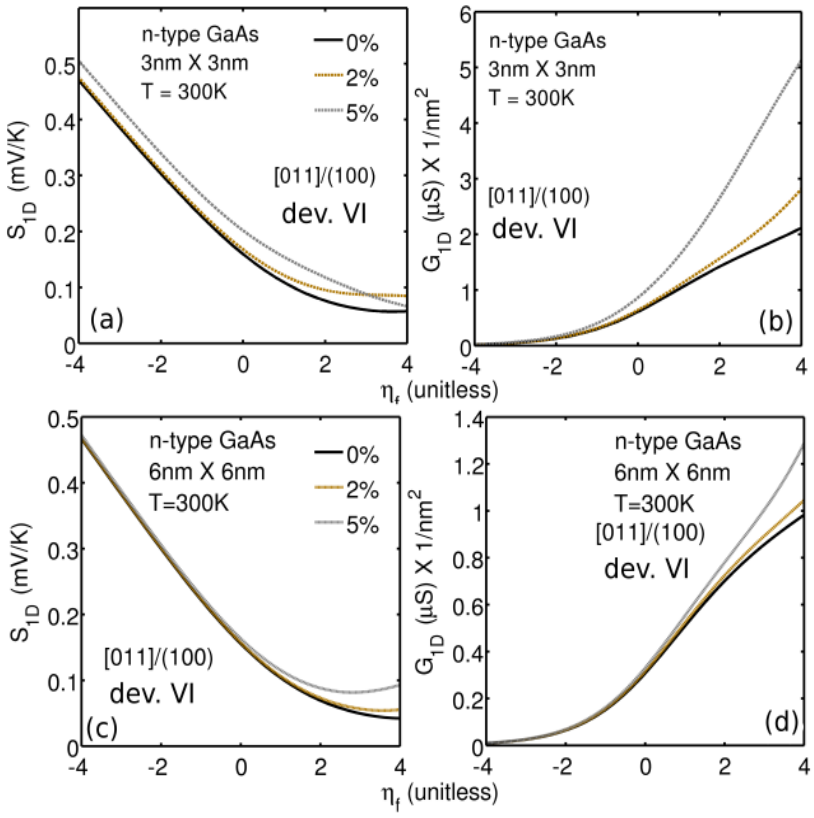


Fig. 10.8. Variation in S and G with strain for various the reduced Fermi-level positions $\eta_f = (\frac{(E_C - E_F)}{k_B T})$. Variation in (a) S, and (b) G for 3nm × 3nm NWs for 3 different uniaxial strain values (0, 2 and 5%). Similar variation in (c) S, and (d) G for 6nm × 6nm NWs for the three strain levels.

The enhancement in the PF also helps in improving the ZT. The ZT is calculated at T=300K using the electronic properties obtained using Landauers approach [51] and a κ_l value of 1W/m-K as reported for GaAs NWs in Refs. [270,279]. It is important to note that ZT depends on the total thermal conductivity which is contributed by the lattice (κ_l) and the electrons (κ_e). The peak PF and the peak ZT value are obtained at different values of the reduced Fermi-level (η_f) (Fig. 10.9). The PF is maximum when the product of S and G is the highest. The peak ZT value is obtained when the ratio of the PF and total thermal conductivity ($\kappa_l + \kappa_e$) is the highest.

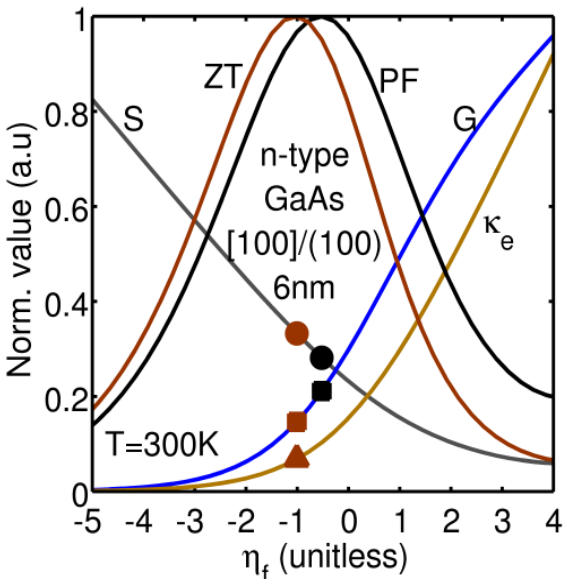


Fig. 10.9. Variation of the various transport parameters with η_f for device I with a 6nm × 6nm cross-section size. The peak ZT and the peak PF are obtained at slightly different values of the Fermi-level.

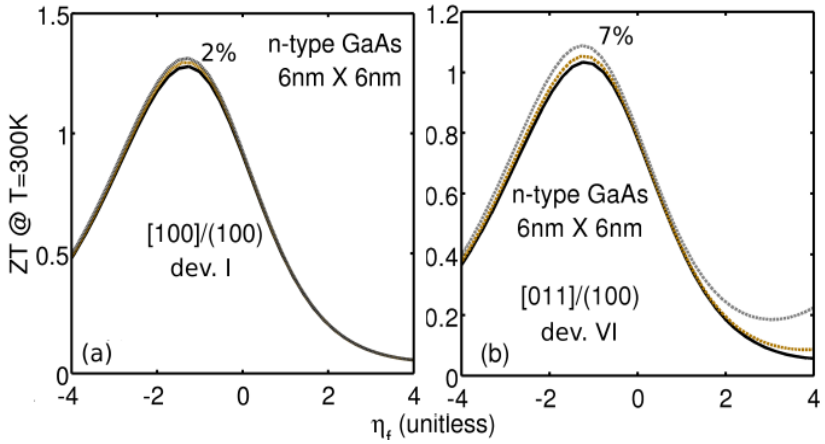


Fig. 10.10. ZT variation for 6nm × 6nm GaAs NW with strain for (a) device I, and (b) device VI. A reasonably good ZT of ∼1 at T=300K is obtained for both the devices. The enhancement with strain is around 4% and 7% in device I and VI, respectively.

The variation in the ZT with strain for device I and VI with a cross-section size of 6nm × 6nm is shown in Fig. 10.10. Under identical strain condition($\epsilon_{xx} = 5\%$) device

I and device VI show very small ZT enhancement (5-7%) (Fig. 10.10). The reason for these small enhancement in these two devices are different. In device I, the Γ valley dominates the electronic transport which results in smaller G (DOS bottleneck) and hence smaller ZT. Whereas, for device VI though the Γ and L valleys come close to each other under strain, the inter-valley scattering suppresses G which results in a small increase in the ZT. Thus, larger wires do not show significant improvement in the peak ZT value with uniaxial tensile strain.

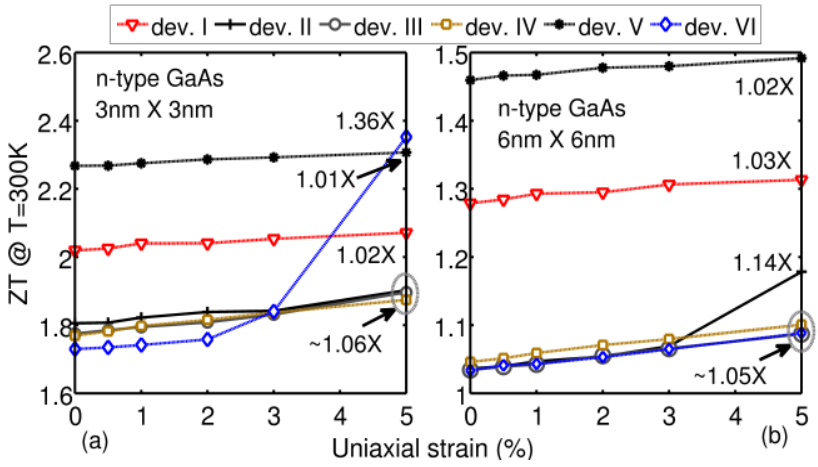


Fig. 10.11. Variation in the peak ZT at 300K for all the devices with uniaxial strain with cross-section size of (a) 3nm × 3nm, and (b) 6nm × 6nm. A reasonable good ZT of ∼1 is obtained for all the 6nm wires which increases up to 2 for 3nm wires. Device II and VI show good enhancement in the peak ZT with strain.

Figure 10.11 shows the peak ZT variation with strain for different devices. Smaller nanowires show higher ZT value (around 2-2.5) compared to the larger nanowires (around 1.5-1.1) due to larger PF. Device VI shows ∼36% enhancement in the peak ZT for smaller wires for 5% strain (Fig. 110.11a). This improvement in device VI becomes possible due to the suppression of the inter-valley scattering in the smaller wires governed by the optimal energy separation of the Γ-L valleys because of the geometrical confinement. For 6nm NWs, device II shows ∼14% improvement in the

peak ZT value for 5% uniaxial tensile strain. Thus, smaller wires show larger gain in ZT under strain due to the reduced inter-valley scattering of the electrons.

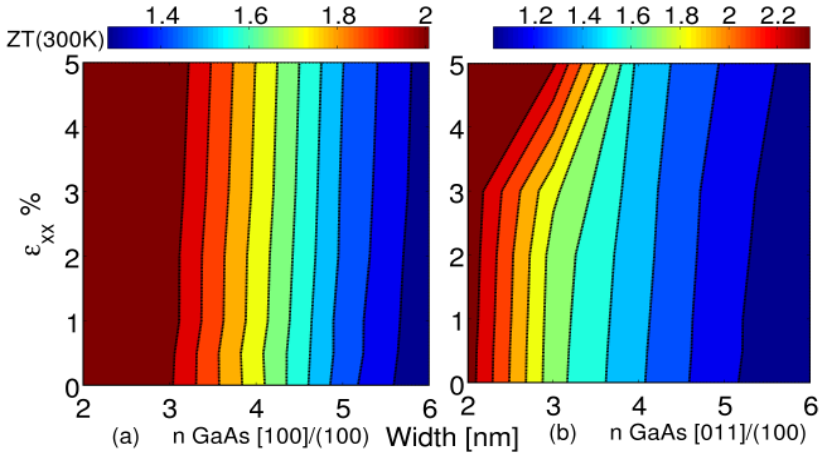


Fig. 10.12. A 2-D contour plot for the variation in the peak ZT for (a) device I, and (b) device VI for different cross-section sizes and strain levels. The smaller wires show better enhancement in the peak ZT as strain is applied which is due to the optimal proximity of the valleys to enhance S and G yet keeping the scattering rates low.

The complete effect of strain and cross-section size on the peak ZT is provided in Fig. 10.12 for device I and VI. The ZT value varies from ∼1 for 6nm size wires to ∼2.5 for 2nm size wires. Under uniaxial tensile strain the enhancement in ZT is higher for device VI compared to device I due to the increased contribution of the L valley to the conductance. Improvement in the ZT with uniaxial tensile strain is larger for smaller wires due to reduced electron scattering. The absolute ZT values may further reduce due to surface roughness scattering of electrons which has not been included in the present study. However, the order and the trend of the ZT is expected to remain the same. The complete effect of the orientation, cross-section size and the strain for optimal value of PF and ZT are summarized in Fig 10.13.

DESIGN SPACE FOR OPTIMAL THERMOELECTRIC PERFORMANCE OF N-TYPE GAAS NWS.

OR	PF		ZT	
	STR	CS	STR	CS
Dev.I	Weak improvement ∼	Small size better	Weak improvement ∼	Small size better
Dev.II	Strong improvement ↑	Small size better	Strong improvement ↑	Small size better
Dev.III	Strong improvement ↑	Small size better	Weak improvement ∼	Small size better
Dev.IV	Weak improvement ∼	Small size better	Weak improvement ∼	Small size better
Dev.V	Weak improvement ∼	Small size better	Weak improvement ∼	Small size better
Dev.VI	Strong improvement ↑	Small size better	Strong improvement ↑	Small size better

Fig. 10.13. Design space for optimizing the PF and ZT of GaAs nanowires using different strain and wire orientation.

10.2.4 Summary of the work

The possibility of n-type GaAs NWs to serve as the next generation thermoelectric material has been shown. A proper choice of growth and channel orientation along with uniaxial stress and cross-section size provides a good way to enhance both the PF and the ZT of GaAs NWs. A 5% uniaxial tensile stress can improve the PF and ZT by ∼3× and ∼1.14×, respectively in 6nm NWs which further increases with W scaling. The GaAs-NWs grown on (110) or (111) surfaces with [110] transport orientation provide a improvement in the ZT and PF compared to the other wafer and wire orientations. Wire cross-section sizes below 6nm are more conducive to ZT and PF enhancement under strain due to suppressed electron scattering resulting from the interplay of the geometrical confinement and the uniaxial strain.

10.3 Tuning TE properties using porosity in SiNWs

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This section explores the effect of pores on the thermoelectric efficiency of SiNWs. In Chapter 7, Sec. 7.2, the effect of pores on the lattice thermal conductivity of SiNWs was analyzed. Here this work is extended to electronic calculations too. Combining both the results the PF and ZT of [100] SiNWs is investigated. This work is inspired by numerous experimental works on suppression of thermal conductivity using pores [59, 216, 220] and the theoretical investigation done on bulk Silicon to optimize the ZT as provided in Ref. [38].

10.3.1 Procedure for calculation

First the electronic bandstructure is calculated using an atomistic 10 band $sp^3d^5s^*$ Tight-binding model with spin-orbit coupling [40]. The phonon dispersion in the nanowires is calculated using the MVFF model [212] (Chapter 5). All the surface atoms are assumed to be passivated by hydrogen for electronic calculation. This allows for the assumption of almost free surface atoms for phonon calculation due to the large mass difference between Si and Hydrogen ($Si_{mass} : H_{mass} = 28{:}1$). From the electronic and phononic dispersions the thermoelectric parameters are calculated using Landauer approach [51] as explained in Chapter 8. Scattering is also included in these calculations (see Chapter 8 for detail) which are bench-marked using experimental data. All the calculations are performed at 300K.

10.3.2 SiNW details

The SiNWs used for this study are of size 4nm × 4nm with [100] wire orientation as shown in Fig. 10.14. The porous SiNWs have 4 pores with hole radius (R_h) of 0.4nm. The separation between the pores (D_{sep}) is changed from 0 to 1nm in steps of 0.2nm. The total number of atoms removed is roughly 14%. This is done to ensure

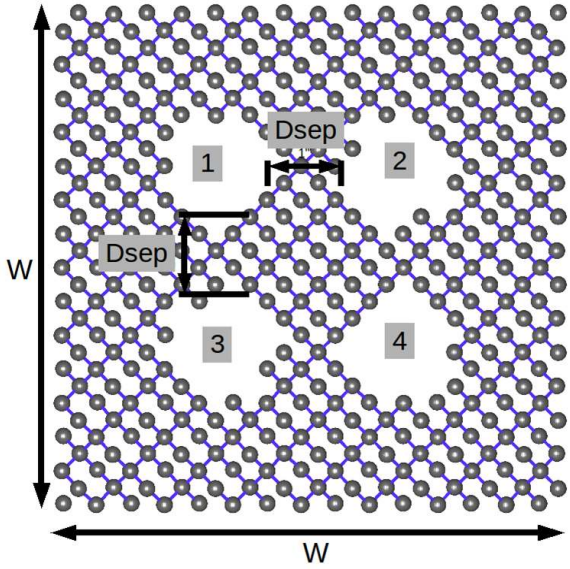

Fig. 10.14. Projected unitcell of [100] SiNW of size 4nm × 4nm with 4 pores each of radius (R_h) 0.4nm and separated by 1nm (D_{sep}).

structural stability of the nanowires which is further corroborated by the non-negative phonon dispersion obtained for all the wires [156]. The wire is assumed to be very lightly doped (near to intrinsic level).

10.3.3 Inclusion of scattering

Electron mobility: Before the analysis of the thermoelectric parameters it is important to benchmark the scattering mechanisms included in the study. Scattering of electrons in SiNWs is included using a constant scattering time, τ_{scat}. This scattering rate is calibrated such that the electron mobility (μ_e) in a 4nm × 4nm [100] filled SiNW comes out to be ∼200 $cm^2/V.s$ at a surface inversion electron density (Ns) of $10^{12}cm^{-2}$ (Fig. 10.15). This value is of the same order and smaller than the experimental results obtained for 48nm [288] and 44nm [224] wide SiNWs. A lower electronic mobility makes sense since electrons are expected to scatter more due to surface roughness in narrow wires [98]. The value of τ_{scat} used is 12 femto seconds (Fig. 10.15). This τ_{scat} is used for all the calculations.

Table 10.2
Values of the phonon scattering parameters.

Structure	B (s/K)	a (K)	D $(s^{-}3)$	F (unitless)	l (m)
Bulk Si	2.8×10^{-19}	140	1.32×10^{-45}	0.4	7.16×10^{-3}
SiNW	1.95×10^{-19}	140	1.19×10^{-45}	1.8	8×10^{-9}

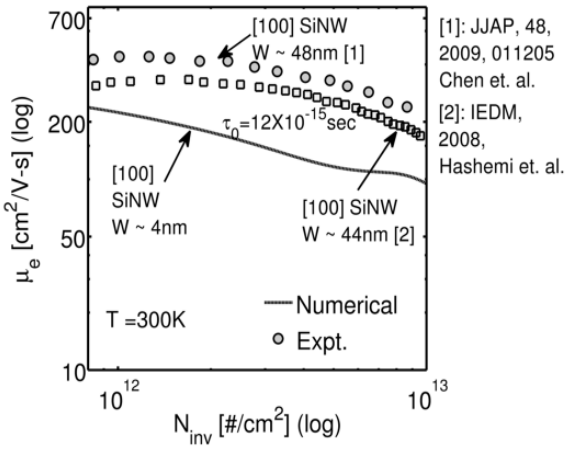

Fig. 10.15. Benchmarking experimental electron mobility (μ_e) vs inversion charge density for SiNWs using full-band electronic dispersion calculated using $sp^3d^5s^*$ TB model. Experimental data for SiNW μ_e is obtained for two different diameter nanowires, (i) for 48nm wide nanowire from Ref. [288], and (ii) for 44nm wide nanowire from Ref. [224]. The simulation is done for 4nm $\times$ 4nm square SiNW which is used for the present study. All the calculations are done at 300K. A scattering time constant (τ_0) of 12 femto-seconds is used for simulations.

Lattice thermal conductivity: In order to benchmark the scattering processes for phonons the lattice thermal conductivity is bench-marked with bulk Si and SiNW of diameter 17.5nm as shown in Fig. 10.16. The types of phonon scattering included in this study are, (i) normal and umpklapp scattering ($\tau_u^{-1} = B\omega^2 e^{-aT}$), (ii) impurity scattering ($\tau_I^{-1} = D\omega^4$), and (iii) boundary scattering($\tau_b^{-1} = V(\omega)/[F \cdot l]$) [263]. Here T is temperature and $V(\omega)$ is the phonon average group velocity at phonon frequency ω. Table 10.2 shows the values used for matching the Bulk Si and SiNW thermal conductivity.

10.3.4 Results and Discussion

The electronic structure (CB) and phonon dispersion for filled and porous SiNWs are shown in Fig. 10.17. The porous wire has holes separated by 1nm. The presence of

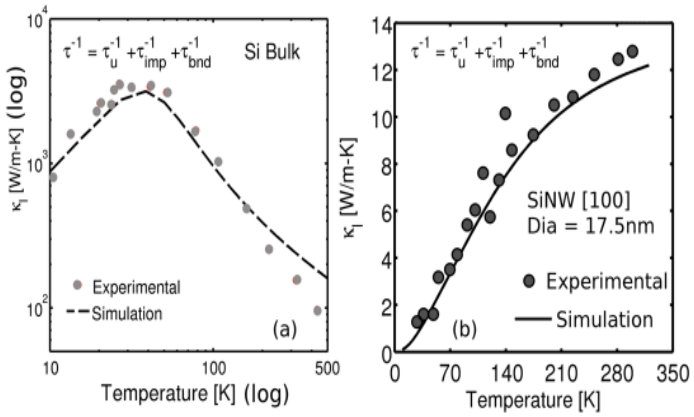

Fig. 10.16. Benchmarking experimental phonon thermal conductivity vs. temperature for (a) Bulk Si, and (b) [100] SiNW of diameter 15nm using full phonon dispersion calculated using the MVFF model and including three types of phonon scattering, (i) umpklapp and normal scattering, (ii) impurity scattering, and (iii) boundary scattering. Experimental data for bulk Si is obtained from Ref. [289] and for Silicon nanowire is obtained from Ref. [290].

pores in the wire increase the geometrical confinement which shift the CBM higher for the hollow wire by 0.2eV as shown in Fig. 10.17b. The presence of pores also results in valley splitting, a phenomena observed in highly confined nanostructures [66]. The phonon dispersion for the porous nanowire shows more bands. The reason for this is already explained in Sec. 7.2.2 in Chapter 7. Next the thermoelectric transport parameters are investigated.

First the effect of porosity on the 1D electronic conductance and Seebeck Coefficient (S) are shown w.r.t Fermi-level in Fig. 10.18. The value of conductance and S degrade due to the presence of pores in the SiNWs. However, an important point to notice it that as the value of D_{sep} increases and as the pores move apart the value of conductance and S improve as shown in Fig. 10.18. Such an improvement in the electronic property w.r.t D_{sep} comes since electrons see lesser interference from pores when they are farther apart compared to the situation when all the pores are closer (small D_{sep}).

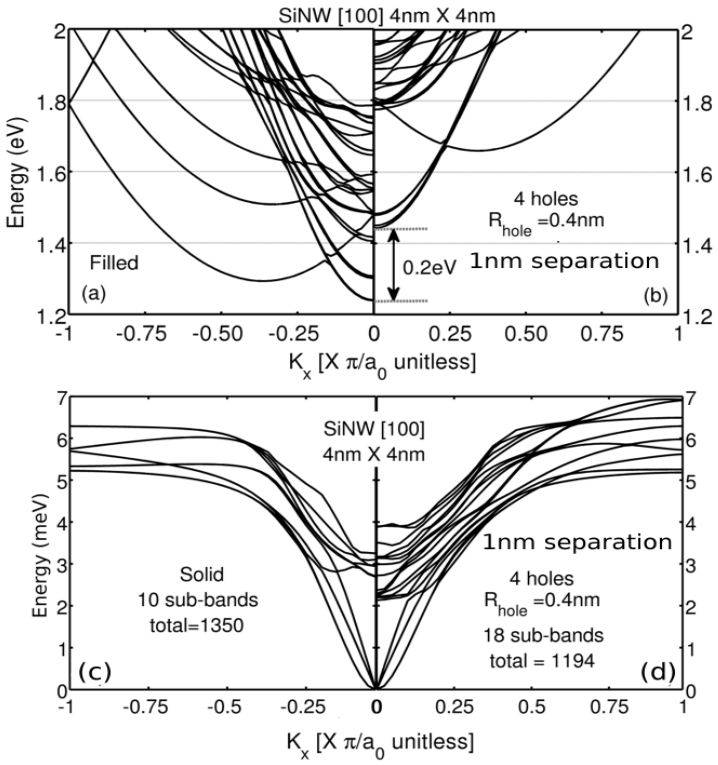

Fig. 10.17. Electronic dispersion of conduction band for (a) filled, and (b) hollow (4 pores, $R_h = 0.4$nm, $D_{sep} = 1$nm) SiNWs. Phononic dispersion for same SiNW with (c) filled, and (d) hollow nanowire. Electronic dispersion is calculated using $sp^3d^5s^*$ TB model, whereas phonon dispersion is calculated using the MVFF model.

A better idea about the variation in the electronic parameters and the lattice parameters is provided in Fig. 10.19. The values of electronic conductance, S and κ_l at the ZT_{max} values are shown w.r.t D_{sep}. Both conductance and S show a non-monotonic behavior with D_{sep} due to the reason mentioned above. At $D_{sep} = 1$nm, the electronic conductance drops by ∼40% and S drops by ∼12% at 300K as shown in Fig. 10.19 a and b. However, κ_l decreases monotonically with D_{sep} and shows a maximum drop of $\sim 50\%$ at $D_{sep} = 1$nm (Fig. 10.19 c). A monotonic fall in κ_l and improvement in the electronic parameters with increasing D_{sep} plays an important role in improving the final ZT.

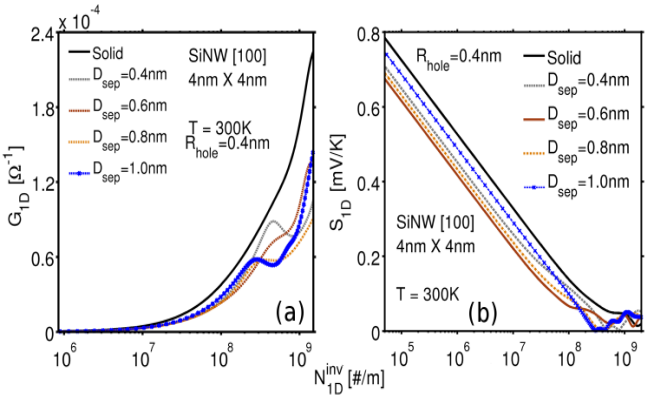

Fig. 10.18. Variation of the (a) electronic conductance, and (b) Seebeck coefficient with pore separation (d_{sep}) for 4 pores case compared to the solid SiNW with [100] orientation and cross-section size of 4nm $\times$ 4nm.

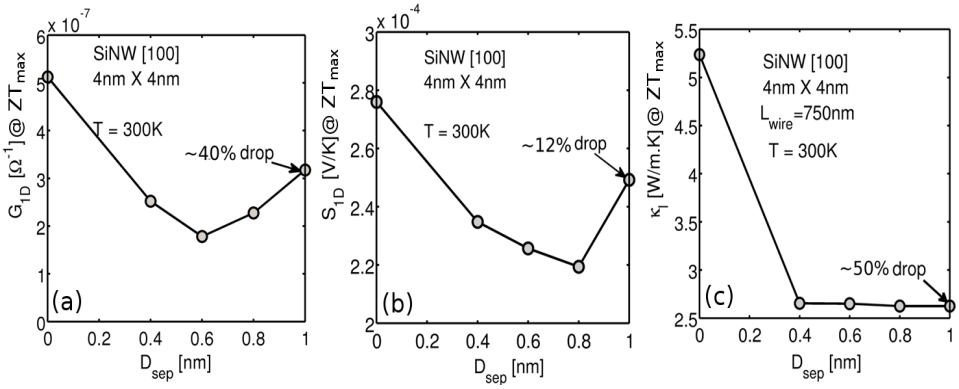

Fig. 10.19. Variation of the 1D (a) electronic conductance, (b) Seebeck coefficient, and (c) thermal conductivity value with pore separation (d_{sep}) at ZT_{max} in a [100] oriented 4nm $\times$ 4nm SiNW with 4 pores.

The effect of pore separation on PF and ZT are shown in Fig. 10.20. The overall electronic contribution falls due to the presence of pores which results in a loss of PF by $\sim$ 50% as shown in Fig. 10.20a. However, a large reduction in lattice thermal conductivity and a small reduction in electron thermal conductivity enhances the overall ZT by $\sim$ 13% as shown in Fig. 10.20b. Thus, the presence of pores in SiNWs with optimal separation can enhance ZT at the cost of electronic PF loss.

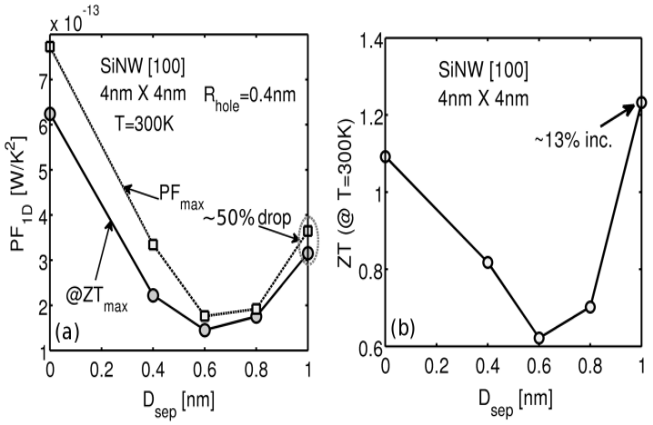

Fig. 10.20. Variation of the 1D (a) PF, and (b) ZT with pore separation (d_{sep}) in a [100] oriented 4nm × 4nm SiNW with 4 pores. PF reduces by ∼ 50% but overall ZT improves by ∼ 13% due to a large reduction in the lattice thermal conductivity.

10.3.5 Summary of the work

It is possible to enhance the thermoelectric properties in SiNWs using porosity. The loss of electronic PF (∼50%) is accommodated by the larger suppression in lattice thermal conductivity (∼50%) along with a small reduction in electron thermal conductivity (∼ 13%). The final result is the ZT enhancement of SiNWs at room temperature by about 13%. This type of realistic simulation procedure is useful for guiding advanced experimental methods in the future for designing better Si thermoelectrics.

10.4 Thermoelectric simulation tool: LANTEST

This section provides a brief discussion on the tool for thermoelectric analysis on materials in 1, 2 and 3 dimension. This tool is based on the mode counting method outlined in Chapter 8.

Figure 10.21 shown the front panel of the tool which will start functioning on nanoHUB.org. The main features of this tool are:

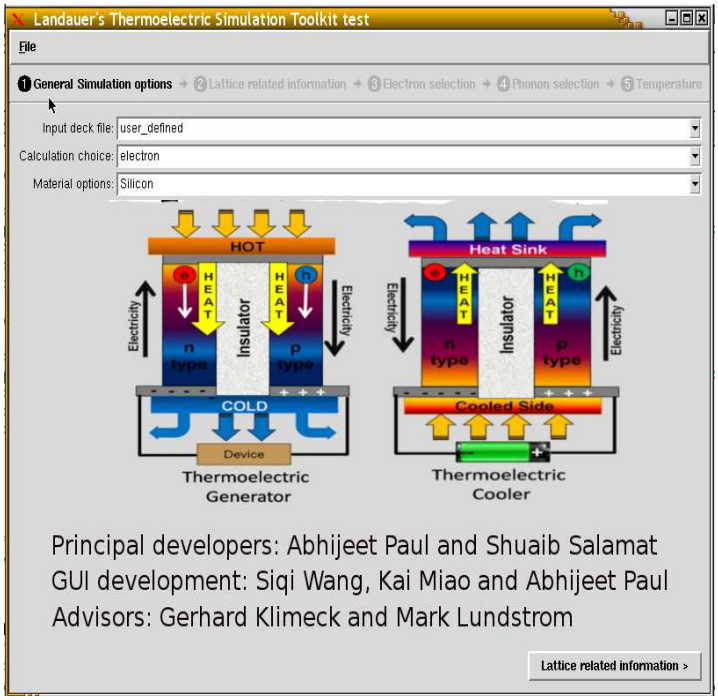

Fig. 10.21. LANTEST Simulation toolkit on nanoHUB.org providing others a way to calculate the thermoelectric parameters.

- Carrier types: This tool can handle both electron and phonons for the calculation of thermoelectric parameters. The same mode counting routine is applied to electrons and phonons.

- Dimensionality: This tool can handle 3D bulk, 2D thin layer and 1D wire structures. This enables analysis of the thermoelectric properties in confined and periodic structures.

- Scattering: The tool can handle scattering for both electrons and phonons. The scattering includes different process such as acoustic phonon, ionized impurity scattering for electrons. For phonons scattering mechanisms like impurity, normal and umpklapp, etc are available.

- Analytical calculations: This tool also allows analytical calculations of thermoelectric properties. The electron properties can be calculated using 3D, 2D

and 1D effective mass parabolic bandstructure. The phonon properties can be evaluated using the linear acoustic phonon dispersion (using V_{snd}) and constant optical phonon dispersion.

- Flexible: This tool can be used easily from an input-deck allowing to different types of calculations. The front-end of the tool creates the input-deck depending on the inputs from the user.

- Temperature and doping: The tool can calculate the Fermi-level in structures based on charged neutrality for different doping and temperature conditions like freeze-out, intrinsic and extrinsic zones. Also features like band-gap narrowing is taken into account for the correct calculation of transport parameters.

- Dispersion Input: The tool can take electronic and phonon dispersion from different types of simulators like quantum espresso, GULP, etc.

- Visualization: The tool provides a variety of plots and results for the user. An example plots are shown in Fig. 10.22

This tool is intended for other researchers to allow them understand and inspect different material systems for future thermoelectric applications.

10.5 Summary and Outlook

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This chapter provides some useful insight into ways of engineering thermoelectric properties of nanowires using simulations. The simulations carried out in this chapter are realistic in the sense not just the effect of bandstructure is considered but also the scattering effects are taken into account. Even in the presence of scattering it is possible to tune and enhance the ZT in n-type GaAs nanowire by a proper choice of strain, orientation and wire cross-section size. For SiNWs porosity can be used to enhance ZT by the drastic suppression of lattice thermal conductivity. But this

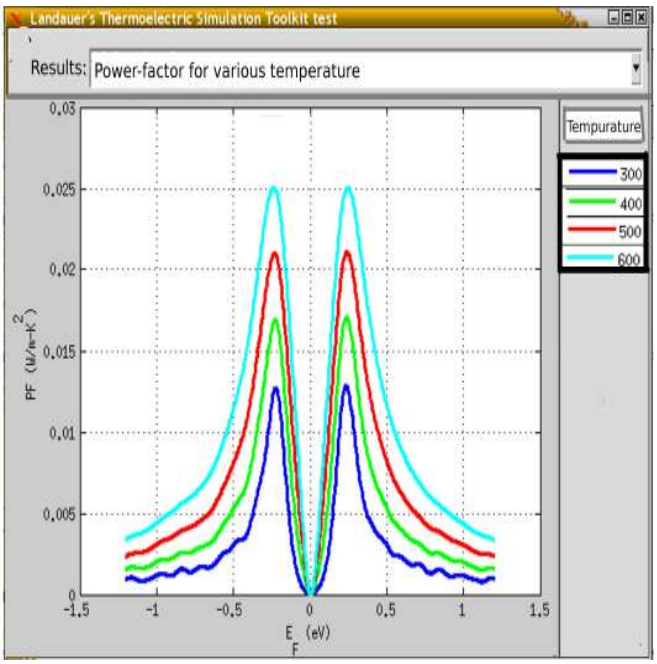

Fig. 10.22. Power-factor plot for parabolic band simulation on LANTEST tool on nanoHUB.org

comes at a cost of reduced PF compared to filled SiNWs. Finally a free tool called 'LANTEST' is shown which will be available on nanoHUB.org for other researchers to examine different materials for thermoelectric applications.

11. SUMMARY AND FUTURE WORK

The present thesis utilizes computational and numerical modeling based on solid-state physics to explore the electron and lattice behavior at the nano-scale. The summary for the three focus areas are provided below.

11.1 Electronic Transport

Chapter 2 to 4 were mainly inspired by Moore's law [1,2]. Atomistic bandstructure calculations are combined with transport theory to explore the electronic transport in nanostructures. Some of the key findings of this work are:

1. The simple ToB model works reliably for transistors where S/D tunneling is small and the channel length $\geq 5\times$ the body width.

2. SiGe/Si core/shell p-FETs outperform Si for very thin Si shell with high-κ gate dielectric. The n-FETs outperform Si for optimally thick Si shell. Higher Ge content in the core improves performance for both n- and p-FETs.

3. The performance of GaAs UTB p-FETs improves for decreasing body thickness, high-κ gate dielectric and compressive biaxial strain. [110] oriented UTB on (110) surface gives the best performance.

4. Bulk SiGe p-MOSFETs show improvement in performance and reliability as Ge% in the SiGe layer increases due to higher compressive biaxial strain which reduces effective transport electron mass (better performance) and increases the gate tunneling mass as well as the hole-oxide barrier height (better reliability).

5. PbSe nanowires have non-parabolic dispersion. [110] oriented PbSe nanowires show highest ballistic electronic conductance for both n- and p-type transport.

Some of the key accomplishments are:

1. Developed new electronic structure calculation using TB for SiGe alloy and Lead chalcogenides like PbSe. The model is extended to nanowires.

2. Explained the experimental CV results for n-type Si NWFETs using self-consistent TB simulations.

3. Developed two new interface trap extraction methods in ultra-scaled Si n-FinFETs. These methods do not require any special structure, thus, paving the way for trap metrology in the ultimate MOSFETs.

4. Developed highly parallel C++ code called OMEN-BSLAB for electronic structure and self-consistent calculation. This tool also powers the Bandstructure Lab V2.0 on nanoHUB.org.

11.2 Thermal Transport

The work in Chapters 5, 6, and 7 address the nano-scale thermal transport. The key findings in this segment are:

1. Triangular SiNWs depict the highest C_v and the lowest κ_l making them suitable for thermoelectric applications. [110] SiNWs have the highest κ_l making them suitable for MOSFETs.

2. Compressive (tensile) uniaxial stress increases (decreases) κ_l of [100] and [110] SiNWs thus, allowing strain engineering of heat flow at the nano-scale

3. Higher pore density with optimal placement reduces κ_l better than closely placed pores in Si and GeNWs.

4. Thermal boundary resistance shows very weak interface orientation dependence for ideal interfaces. However, for disordered interfaces, [100] interface shows an increase of 2 orders in TBR whereas [110] shows an increase of $\sim 2\times$ only. Thus, [110] interfaces block heat lesser compared to [100] interfaces.

The key accomplishments in this segment are:

1. Developed code for the calculation of phonons and heat transport analysis in zinc-blende semiconductors (bulk and nanowires) using the MVFF model.

2. Bench-marked the simulated acoustic and optical phonon shifts in SiNWs calculated using MVFF model against the experimental Raman Spectroscopy data.

3. Correlated the phonon shifts and thermal properties of SiNWs to their shape, size and orientation enabling nano-scale metrology and compact thermal modeling.

4. Explained the nature of CP and IP heat flow in ultra-short SiGe superlattices. CP heat flow is TBR dominated whereas IP heat flow is controlled by the layer with highest thermal conductivity. The effect of contacts and superlattice orientation are also explained.

11.3 Thermoelectric Phenomena

Chapters 8, 9, 10 are focused on the thermoelectric theory and use of semiconductor nanostructrures for TE applications. The key findings in this segment are:

1. n-type GaAs NWs with [110] channel on (110) or (111) substrate show enhancement in PF($\sim$3$\times$) and ZT ($\sim$ 1.7$\times$) with increasing uniaxial tensile strain and decreasing cross-section size due to L-valley contribution.

2. Well separated pores in SiNWs enhance the ZT due to the strong suppression of κ_l at the loss of electronic PF.

The main accomplishments in this segment are:

1. Developed a new mode counting algorithm for the robust calculation of transport parameters within Landauer's approach.

2. Developed a simulator for TE analysis of semiconductor. This code powers the LANTEST tool to be released on nanoHUB.org

11.4 Contributions on nanoHUB.org

Another important aspect of this PhD is the contribution of many tools and resources on nanoHUB.org (*www.nanohub.org*). This web-portal provides a new way of spreading the new developments in the field of nanotechnology and sharing knowledge with fellow researchers. The key accomplishments are:

1. During the entire PhD work contributed six educational tools on semiconductor theory.

2. Contributed two research grade tools, (a) Bandstructure Lab for electronic structure solution in zinc-blende semiconductors, and (b) LANTEST, a tool for the thermoelectric analysis of the semiconductor materials with different dimensionality.

3. The contributed resources and tools have served more than 7000 users world wide till date.

A detailed report on the nanoHUB contributions is provided in Appendix G.

11.5 Future Work

This thesis makes a small contribution to the huge big global effort for understanding the physics of nano-scale which has the potential of redefining the development trends of mankind. This field of nanotechnology has brought with it both opportunities and challenges which will require more human effort to utilize and overcome them in the times to come. Even though transistor scaling has slowed down, Moore's law as hit a flat, the learning from the semiconductor industry has played important role in empowering other areas such as energy harvesting [184], energy storage [291], nano-medicine [292–294] and computer modeling [28]. Some of the opportunities and challenges which still needs to be addressed are provided next. Some of the points are relevant from this thesis point of view and some from the more general nanotechnological point of view.

11.5.1 Opportunities and Challenges

The key opportunities are broken into three general areas which are described below:

- **Theoretical:** These are the opportunities from a theory perspective. Areas like nano-scale device modeling, computation and prediction provides vast areas for more work. Some of the interesting areas are :

    1. Quantum Transport: The application of quantum transport like NEGF has a broader base and can be applied to many other areas. Some noticeable efforts are application to lasers [295], electroluminiscence [296] and spin [297].
    2. Material Properties: Good methods for determining the material properties of both synthetic as well as natural materials. Many DAT and Molecular Dynamics calculations are available but are limited by computational requirements and system size that can be solved. Here methods like empirical Tight-binding will play a vital role.
    3. Thermodynamics: A proper integration of thermodynamics into models like Tight-binding and MVFF can be very beneficial. This will allow for better estimation of many physical quantities with temperature, pressure and volume variation which at present are limited to DFT type calculations.
    4. More and more than Moore: The scaling in semiconductor industry has long been guided by Moore's law [1,2] but now system diversification by including sensors, actuators, etc is becoming attractive to serve the consumer market. Also non-silicon devices provide new opportunities of looking into new physics and transport mechanisms like topological insulators and 2D systems like Graphene, Boron-Nitride.

- **Technological**: These are the experimental breakthroughs needed to push the present technology ahead to reach the new frontiers of science. Some of the interesting areas are:

    1. Lithography: The limitation of double immersion lithography kicked in research in Extreme Ultra-violet (EUV) lithography. EUV holds key to the ultimate scaling of the transistors as well as other devices like memories, etc [298]. This area provides a lot of new opportunities.
    2. Spin devices: The fabrication of realistic spin devices which can work at par with CMOS technology also brings in a lot of new opportunities in terms of device, circuit and system design.
    3. Energy harvesting: The search for renewable energy resources is getting faster and broader. In this direction nanotechnology again plays a vital role in improving solar-cells, thermoelectric modules and fuel cells.
    4. Energy storage: There is greater need for better energy storage devices. Since the lithium on earth is limited, the use of other materials is very important. In recent times breakthrough using SiNWs have been achieved [291, 299]. Search for other material systems provides a lot of exciting opportunities.
    5. Nano-medicine: The applications of nanotechnology has also proved immensely useful in designing new drugs for cancer, AIDS, etc. A lot of growth is present in this area [292–294].

- **Environmental:** These are the technologies which can improve the health of our globe. There is an increases consciousness to have greener technologies. Some exciting areas are:

    1. Alternative energy: Areas of photo-voltaics, solar cells and thermoelectricity provide a lot of opportunities.

2. Emission control: The reduction of green-house gas emission is a top priority. Hybrid automobiles and better sensors designs provide nice opportunities.

While a lot of opportunities have been outlined, these come with challenges too. Some of the prominent challenges in the field of nanotechnology are:

- What will replace Si ?: Though a lot of other material options are tried like III-V, Carbon nanotubes, Graphene, etc, but Silicon still holds the top spot in terms of performance and integration when it comes to a billion transistors on micro-processors. However, certain niche applications might see the use of other materials too.

- Need for better device simulators: There is a demand for better device simulators which can capture the quantum mechanical effects in a more elaborate way going beyond the commercial drift-diffusion simulators with quantum corrections.

- Improving thermoelectric efficiency: Even though a lot of advances have been made, but the thermoelectric efficiency of 2 to 3 at room temperature still eludes and more work needs to be done. Non-linear thermal transport might hold the key.

- Device and circuit interaction: There is an increased need for device and circuit interaction at the nano-scale. Better device designs do not ensure good circuit designs until and unless these two areas go hand in hand. With larger process variations and stringent lithography requirements it is necessary to have better feedback from process to circuit and vice-versa.

The above list is not exhaustive by any means. A bird's eye-view of the opportunities and challenges in the world of nanotechnology provides some good direction about the application of the ideas developed in this thesis. While working on a PhD

we mostly concentrate on one or two areas and go deep into it, but at the same time it is important to realize the bigger picture to find out areas where the methods and skills developed during the PhD can be applied. Some of the interesting areas where the work in this thesis could be extended are:

- Non-silicon devices: The ideas of transport and bandstructure can be used to investigate non-silicon materials and variety of structures which will be very useful in answering many questions after 2013 on Moore's scaling graph.

- Electron-phonon interaction: An elaborate electron-phonon interaction scheme can be made possible with better computers and newer libraries allowing for better parallel and distributed computations. Also cloud computing will play a significant role in making these computation heavy softwares available to other researchers and industry.

- Full-band Scattering calculation: The used of wave-function from the Tight-binding calculation for nano-structures can be used for evaluating the scattering integrals within relaxation time approximation (RTA). This can provide better estimate of electron mobility at the nano-scale. Similar scattering mechanisms can be implemented for phonons using the Dynamical matrix obtained by the MVFF model and Fermi-Golden-Rule.

- Thermodynamics: Inclusion of thermodynamics to phonon calculations adds another facet to the calculations done in this thesis. Many of the physical properties of the nano-structures will behave very differently under the application of external pressure and heat.

- Non-linear thermoelectrics: The investigation of tunneling and emission based thermoelectric devices could be done using the NEGF method which can open up new areas in nano-scale heat and energy transport.

The work cataloged in this thesis addresses some of the interesting theoretical developments and their application to the nano-scale semiconductors. The work is

expected to be useful for others who would pursue research in the area of solid state physics and nanoelectronics. The application aspect has been given a lot of emphasis since the conversion of theoretical understanding to practical applications is the central thrust of engineering.

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APPENDICES

A. DETAILS OF BULK ZINC-BLENDE COPLANAR INTERACTION

The coplanar interactions are important to obtain the flat nature of the acoustic phonon branches in Si and Ge. There are 24 such interactions in a zinc-blende crystal. The normalized locations of all the atoms involved in the coplanar interactions are shown in table A.1. The corresponding groups used for bulk phonon dispersion calculations are given in table A.2.

Table A.1
Normalized atomic coordinates ($[\overline{x}, \overline{y}, \overline{z}] = [x, y, z]/a_0$) used for coplanar interaction calculation.

No.	$\overline{x}$	$\overline{y}$	$\overline{z}$	No.	$\overline{x}$	$\overline{y}$	$\overline{z}$
1*	0	0	0	14	0	0.50	-0.50
2*	0.25	0.25	0.25	15	-0.50	-0.50	0
3	0.25	-0.25	-0.25	16	-0.50	0	0.50
4	-0.25	0.25	-0.25	17	0	-0.50	0.50
5	-0.25	-0.25	0.25	18	0.25	0.75	0.75
6	0	0.50	0.50	19	-0.25	0.75	0.25
7	0.50	0	0.50	20	-0.25	0.25	0.75
8	0.50	0.50	0	21	0.75	0.25	0.75
9	0	-0.50	-0.50	22	0.75	-0.25	0.25
10	0.50	-0.50	0	23	0.25	-0.25	0.75
11	0.50	0	-0.50	24	0.75	0.75	0.25
12	-0.50	0	-0.50	25	0.75	0.25	-0.25
13	-0.50	0.50	0	26	0.25	0.75	-0.25

*Belong to the main bulk unitcell used for DM calculation.

Table A.2
Atoms forming the coplanar interaction groups. 4 atoms in each group.

No.	Members				No.	Members			
1	2	1	3	9	13	1	2	6	18
2	2	1	4	12	14	1	2	7	21
3	2	1	5	15	15	1	2	8	24
4	3	1	2	6	16	6	2	1	3
5	3	1	4	13	17	6	2	7	22
6	3	1	5	16	18	6	2	8	25
7	4	1	2	7	19	7	2	1	4
8	4	1	3	10	20	7	2	6	19
9	4	1	5	17	21	7	2	8	26
10	5	1	2	8	22	8	2	1	5
11	5	1	3	11	23	8	2	6	20
12	5	1	4	14	24	8	2	7	23

*Atom numbers are same as shown in table A.1.

B. DERIVATION OF DYNAMICAL MATRIX FROM EQUATION OF MOTION

A crystal in equilibrium has zero total force. However, in the presence of perturbations like lattice vibrations, etc. a small restoring force works on the system. The total force (F_{total}) under small perturbation is given by the Taylor series expansion as,

$$\begin{aligned} F_{total} &= -\sum_{i\in N} \frac{\partial U}{\partial \Delta R_i} (= 0\, at\, eqb.) \\ &\quad -\frac{1}{2}\sum_{i,j\in N} \frac{\partial^2 U}{\partial \Delta R_i \partial \Delta R_j} \cdot \Delta R_j + \dots \end{aligned} \tag{B.1.1}$$

where, N represents all the atoms present in the system and U is the potential energy of the system. In Eq.(B.1.1) first term in RHS is zero under equilibrium. The next non-zero term is the second term in Eq.(B.1.1). Under harmonic approximation, only the second term is considered and the higher order (anharmonic) terms are neglected. Now combining Eq.(5.1) and Eq.(B.1.1) one can obtain the following,

$$F_{total} = \sum_{i\in N} m_i \frac{\partial^2}{\partial t^2} \Delta R_i$$

$$= -\frac{1}{2}\sum_{i,j\in N} \frac{\partial^2 U}{\partial \Delta R_i \partial \Delta R_j} \cdot \Delta R_j \tag{B.1.2}$$

$$= DR \tag{B.1.3}$$

where, D is called the 'Dynamical matrix' and R is a column vector of displacement for each atom given as,

$$D = \begin{bmatrix} D(11) & D(12) & \cdots & D(1N) \\ D(21) & D(22) & \cdots & D(2N) \\ \vdots & \vdots & \ddots & \vdots \\ D(N1) & D(N2) & \cdots & D(NN) \end{bmatrix} \tag{B.1.4}$$

$$R^T = \begin{bmatrix} \Delta R_1 & \Delta R_2 & \cdots & \Delta R_N \end{bmatrix} \tag{B.1.5}$$

Definition of $D(ij)$ is given in Eq.(5.9).

C. TREATMENT OF SURFACE ATOMS

The damped displacement of the surface atom 'j' can be represented the matrix Ξ^j given as,

$$\Xi^j = \begin{bmatrix} \epsilon_x^j & 0 & 0 \\ 0 & \epsilon_y^j & 0 \\ 0 & 0 & \epsilon_z^j \end{bmatrix} \tag{C.1.1}$$

Taking into account the individual components the displacement vector for the atom 'j' we obtain,

$$\tilde{r}_n^j = \epsilon_n^j r_n^j \quad n \in [x, y, z] \tag{C.1.2}$$

This modifies Eq.(5.9) as,

$$\tilde{D}_{mn}^{ij} = \epsilon_n^j D_{mn}^{ij} \tag{C.1.3}$$

Combining Eq.(C.1.1) and (C.1.3) the dynamical matrix component between atom 'i' and 'j' can be represented as,

$$\tilde{D}(ij) = \begin{bmatrix} \epsilon_x^i D_{xx}^{ij} \epsilon_x^j & \epsilon_x^i D_{xy}^{ij} \epsilon_y^j & \epsilon_x^i D_{xz}^{ij} \epsilon_z^j \\ \epsilon_y^i D_{yx}^{ij} \epsilon_x^j & \epsilon_y^i D_{yy}^{ij} \epsilon_y^j & \epsilon_y^i D_{yz}^{ij} \epsilon_z^j \\ \epsilon_z^i D_{zx}^{ij} \epsilon_x^j & \epsilon_z^i D_{zy}^{ij} \epsilon_y^j & \epsilon_z^i D_{zz}^{ij} \epsilon_z^j \end{bmatrix} \tag{C.1.4}$$

which can be written in a compressed form as,

$$\tilde{D}(ij) = \Xi^i D(ij) \Xi^j \tag{C.1.5}$$

The value of $\epsilon_{x,y,z} \in [0, 1]$, where completely free surface atoms have value 1 and completely tied atoms have value 0.

D. INCLUSION OF MASS IN DYNAMICAL MATRIX

In Eq. (5.13) the mass of the atoms in on the RHS. It is convenient to include the mass in DM itself. This modifies the the LHS of the equation. The modified DM component between atom 'i' and 'j' thus, becomes,

$$\tilde{D}(ij) = \begin{bmatrix} \frac{1}{\sqrt{m_i}} D^{ij}_{xx} \frac{1}{\sqrt{m_j}} & \frac{1}{\sqrt{m_i}} D^{ij}_{xy} \frac{1}{\sqrt{m_j}} & \frac{1}{\sqrt{m_i}} D^{ij}_{xz} \frac{1}{\sqrt{m_j}} \\ \frac{1}{\sqrt{m_i}} D^{ij}_{yx} \frac{1}{\sqrt{m_j}} & \frac{1}{\sqrt{m_i}} D^{ij}_{yy} \frac{1}{\sqrt{m_j}} & \frac{1}{\sqrt{m_i}} D^{ij}_{yz} \frac{1}{\sqrt{m_j}} \\ \frac{1}{\sqrt{m_i}} D^{ij}_{zx} \frac{1}{\sqrt{m_j}} & \frac{1}{\sqrt{m_i}} D^{ij}_{zy} \frac{1}{\sqrt{m_j}} & \frac{1}{\sqrt{m_i}} D^{ij}_{zz} \frac{1}{\sqrt{m_j}} \end{bmatrix} \tag{D.1.1}$$

here m_i and m_j are the masses of atom 'i' and 'j' respectively. Eq.D.1.1 can be written in a compressed manner as,

$$\bar{D}(ij) = M_i^{-1} D(ij) M_j^{-1}, \tag{D.1.2}$$

where M_i is given as,

$$M_i = \begin{bmatrix} \sqrt{m_i} & 0 & 0 \\ 0 & \sqrt{m_i} & 0 \\ 0 & 0 & \sqrt{m_i} \end{bmatrix} \tag{D.1.3}$$

E. FITTED ANALYTICAL EXPRESSIONS FOR DM PROPERTIES

- *Atoms in a [100] SiNW unitcell*: The N_A data obtained for the square wires till 6nm $\times$ 6nm can be fitted to a quadratic polynomial given as,

$$N_A(W) = 27.57W^2 + 4.59W \tag{E.1.1}$$

  Using Eq.(E.1.1) for a 16nm $\times$ 16nm SiNW gives around 7128 atoms.

- *Non-zero elements in a [100] SiNW DM*: The data for non-zero elements in the DM for SiNW with W till 6nm can be fitted to a quadratic polynomial given by,

$$NZ(W) = 3156W^2 - 495.5W \tag{E.1.2}$$

  Using Eq.(E.1.2) for a 16nm $\times$ 16nm SiNW yields around 800117 non-zero elements in the DM.

- *Percentage fill factor for a [100] SiNW DM*: The data for percentage fill-factor of the DM for SiNW with W till 6nm can be fitted to an exponential expression given by,

$$\%fill - factor(W) = 94.61e^{(-0.9907W)} + 5.389e^{(-0.1591W)} \tag{E.1.3}$$

  Using Eq.(E.1.3) a 16nm $\times$ 16nm SiNW DM is estimated to be filled only 0.42%. Using the numbers obtained from Eq.(E.1.1) and Eq.(E.1.2) for a 16nm SiNW gives a fill factor of $\sim$ 0.175%. This shows that the DM matrix is very sparsely filled for larger wires.

- *Mean assembly time for [100] SiNW DM*: The data for mean $time_{asm}$ of the DM for SiNW with W till 6nm can be fitted to a quadratic polynomial given by,

$$NZ(W) = 0.9079W^2 - 0.3789W \; secs \tag{E.1.4}$$

F. NEW TIGHT-BINDING PARAMETERS FOR BULK GAAS CONDUCTION BAND

These are $sp^3d^5s^*$ Tight-binding parameter with spin orbit coupling optimized for all the important conduction band (CB) valleys (Γ, X and L).

The value of the parameters are provided in Table F.1.

The strain parameters are same as the values taken from Table III of Ref. [76].

The reliability of the new parameters for the CB are provided in Fig. F.1 using fitting by genetic algorithm [68].

Table F.1
New Tight-binding parameters for bulk GaAs optimized for the CB valleys.

Parameter name	Anion(new value)	Cation (new value)
Es	-5.50042	-0.201505
Ep	4.15107	6.54437
Es^*	19.71059	17.693667
Ed	13.03169	11.551671
λ	0.17234	0.015148
$Vss\sigma$	-1.847935	-1.847935
$Vs^*s^*\sigma$	-4.329177	-4.329177
$Vss^*\sigma$	-1.457501	-2.342977
$Vsp\sigma$	2.581621	3.636062
$Vs^*p\sigma$	1.947961	0.358026
$Vsd\sigma$	-3.074239	-2.381203
$Vs^*d\sigma$	-0.470978	0.096126
$Vpp\sigma$	4.391532	4.391532
$Vpp\pi$	-2.071916	-2.071916
$Vpd\sigma$	-2.237740	-1.041446
$Vpd\pi$	2.360061	2.104964
$Vdd\sigma$	-1.437424	-1.437424
$Vdd\pi$	2.015471	2.015471
$Vdd\delta$	-1.801308	-1.801308

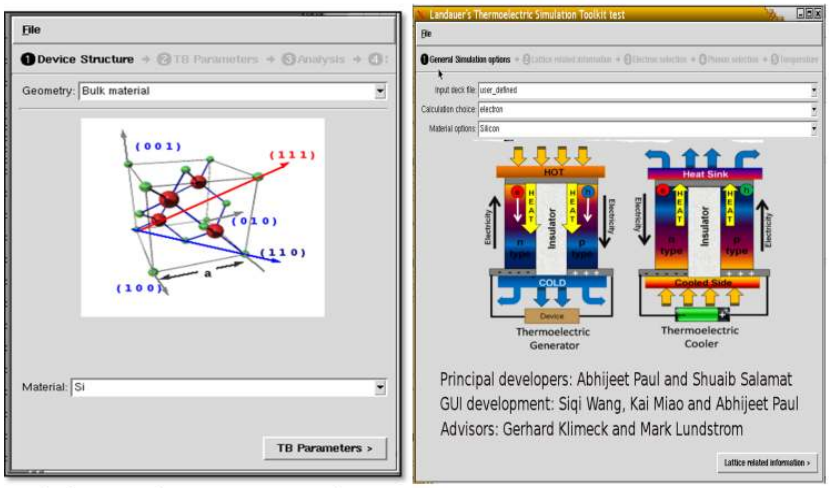
Value	Target	Percentage	description
1.4250922	1.4240000	7.6701072e-02	Eg_gamma
Gamma Valley			
1.4200150	1.4240000	2.7984597e-01	Ec_gamma
0.0680807	0.0670000	1.6129394e+00	mstar_c_001
X-valley			
1.9658849	1.9000000	3.4676260e+00	EC
1.3063896	1.3000000	4.9150802e-01	m*long
0.2119485	0.2300000	7.8484750e+00	m*trans
L-valley			
1.7085047	1.7080000	2.9551497e-02	EC
1.8947132	1.9000000	2.7825241e-01	m*long
0.0754385	0.0754000	5.1076876e-02	m*trans
Spin orbit coupling			
0.3475784	0.3400000	2.2289464e+00	Delta_so
Valence band edge			
-0.0050772	0.0000000	5.0772299e-01	Vhh
Light Hole			
-0.0779693	-0.0871000	1.0483057e+01	mstar_lh_001
-0.0677305	-0.0804000	1.5758120e+01	mstar_lh_011
-0.0653757	-0.0786000	1.6824832e+01	mstar_lh_111
Heavy Hole			
-0.2861754	-0.4030000	2.8988742e+01	mstar_hh_001
-0.6434737	-0.6600000	2.5039918e+00	mstar_hh_011
-0.9761467	-0.8130000	2.0067250e+01	mstar_hh_111
Split-off hole			
-0.1460649	-0.1500000	2.6234025e+00	mstar_so_001

Fig. F.1. Fitness of the new Tight-binding parameters for bulk GaAs optimized for the CB valleys. The green encircled portion shows the good fitting for conduction band. However, the fitting for the valence band is not that good.

G. DEVELOPMENT OF TOOLS AND RESOURCES ON NANOHUB.ORG

This appendix provides some detailed information on the contributions made on nanoHUB.org (*www.nanohub.org*) between 2006 and 2011. The contributions on nanoHUB.org can be broadly classified into two categories:

- **Tools:** These are online software which can be used by other nanoHUB users to perform some calculations. Some of the tools that have been developed are shown in Fig. G.1 and G.2.
- **Resources:** This category includes the online presentations, homework problems and articles. A detailed contribution list is shown in Fig. G.3 a.



(a) Bandstructure Lab

(b) Thermoelectric Simulation Toolkit

Fig. G.1. Research grade tools on nanoHUB.org (a) Bandstructure Lab, (b) Thermoelectric Simulation toolkit

G.1 Description of resources

Types of tools: The tools contributed on nanoHUB.org are of two types. These are (i) Research grade tool such as Bandstructure Lab (*https://nanohub.org/resources/1308*), see Fig. G.1, and (ii) educational purpose tool which are used by students to understand the basic concepts of semiconductor and device physics like the Periodic Potential Lab (*https://nanohub.org/resources/3847*), see Fig. G.2. A detailed list of the contributed tools can be found at *https://nanohub.org/members/15437/contributions*.

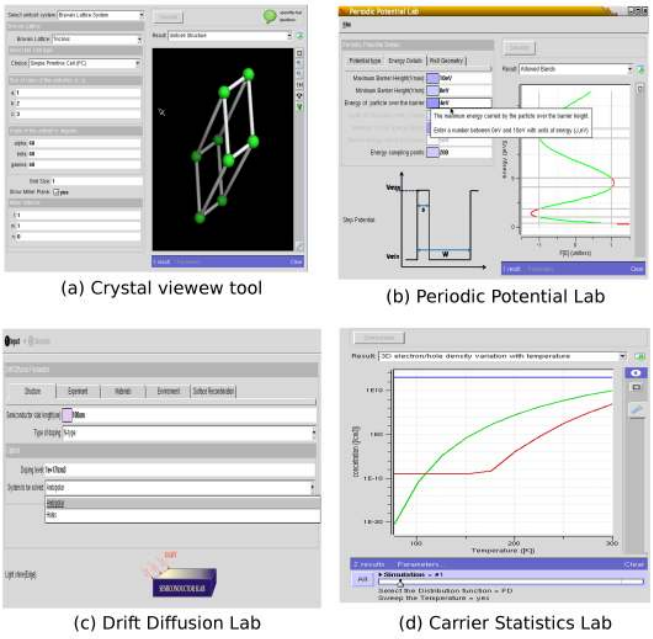


Fig. G.2. Educational tools on nanoHUB.org (a) Bandstructure Lab, (b) Thermoelectric Simulation toolkit

Types of Resources: There are different types of resources which have been contributed to nanoHUB which include presentations, animations, user guides, etc. A detailed information is provided in Fig. G.3a.

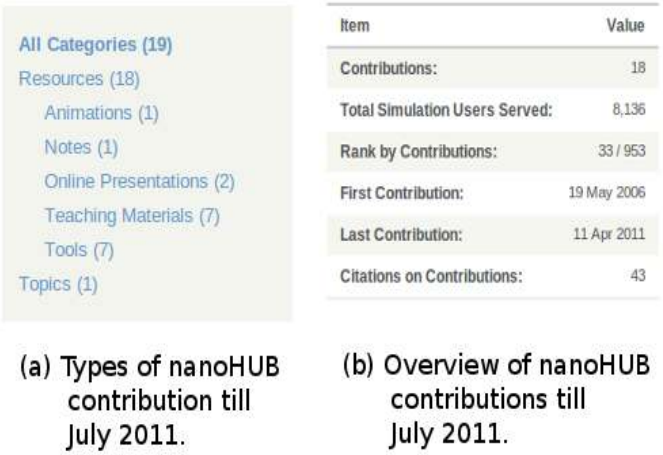


Fig. G.3. (a) The types of resources contributed to nanoHUB.org. (b) Some statistics on about the overall contribution on nanoHUB.org

G.2 Usage statistics of resources

From nanoHUB.org a detailed resource utilization idea can be obtained. Many information can be extracted such as, (i) number of users served, (ii) citations for the tools, (iii) ranking as a developer and many other items as shown in Fig. G.3b. A break-up of the usage of the tools is shown in Fig. G.4. Till July 2011, a total of 8136 users have used the tool with a total of 133,241 simulations being run.

Also a detailed resource utilization data is available for the resources deployed on nanoHUB. Figure G.5 shows the usage statistics for the contributed resources on nanoHUB.org. Around 3500 users have utilized the resources with largest utilization of Carrier Statistics lab (Fig. G.5).

The website nanoHUB.org also provides valuable information on the time based utilization of the contributed resources. Figure G.6 shows the utilization of all the resources from Fall 2006 till July 2011. More than 7500 users have used the contributed resources. This has led to around 43 citations in the literature (Fig. G.3b). An interesting pattern which shows up in the time based utilization is that, the usage of the tools go up during the Fall and Spring semesters which is mainly due to the use of the educational tools. The research tools are used all around the year.

Tool usage on nanoHUB.org till July 2011.

#	Tool Name	Users served in last 12 months	Simulation Runs in last 12 months	Total users served	Total Simulation Runs	Citations	Published On
1	OMEN Nanowire	239	2,162	564	4,699	7	15 Dec 2008
2	BJT Lab	614	3,218	1,145	6,516	1	20 Mar 2008
3	Drift-Diffusion Lab	544	5,087	1,245	12,533	-	04 Feb 2008
4	Periodic Potential Lab	310	3,098	923	10,085	1	28 Jan 2008
5	Carrier Statistics Lab	615	7,075	1,253	14,125	-	22 Jan 2008
6	Crystal Viewer Tool	1,046	8,158	2,571	20,503	1	11 Jan 2008
7	Band Structure Lab	1,163	17,429	4,176	64,780	36	19 May 2006
	total	3,131	46,227	8,136	133,241		

source: https://nanohub.org/members/15437/usage

Fig. G.4. A detailed usage statistics of the contributed tools on nanoHUB.org till July 2011. url:*https://nanohub.org/members/15437/usage*.

Resource Usage on nanoHUB.org till July 2011.

#	Resource Title	Users served in last 12 months	Total users served	Citations	Published On
1	Periodic Potential Lab Worked Examples Teaching Materials	12	12	-	11 Apr 2011
2	Thermoelectric effects in semiconductor nanostructures: Role of electron and lattice properties Online Presentations	413	413	-	06 Oct 2010
3	InAs: Evolution of iso-energy surfaces for heavy, light, and split-off holes due to uniaxial strain. Animations	4	8	-	25 May 2010
4	NCN Student Meet Presentations Notes	47	74	-	11 Feb 2010
5	Comparison of PCPBT Lab and Periodic Potential Lab Online Presentations	37	70	-	10 Aug 2009
6	Band Structure Lab: First-Time User Guide Teaching Materials	0	0	-	15 Jun 2009
7	Periodic Potential Lab: First-Time User Guide Teaching Materials	8	8	-	07 Jun 2009
8	Crystal Viewer Tool: First-Time User Guide Teaching Materials	366	821	-	01 Jun 2009
9	Carrier Statistics Lab: First-Time User Guide Teaching Materials	894	1,460	-	09 Mar 2009
10	Homework Exercise on Bravais Lattices, Crystal Structures, Miller Indices Teaching Materials	152	465	-	30 Mar 2008
11	Homework Exercise on Fermi-Dirac and Maxwell-Boltzmann Distributions Teaching Materials	278	762	-	24 Jan 2008

source: https://nanohub.org/members/15437/usage

Fig. G.5. A detailed usage statistics of the contributed resources on nanoHUB.org till July 2011. url:*https://nanohub.org/members/15437/usage*.

A very good way of increasing scientific collaboration is the use of web and nanoHUB.org provides a very useful and strong way to increasing the presence in the world of technology. The contributions on nanoHUB.org has provided a world-wide visibility to the work on nanotechnology. This even surpasses the work in published journals which only caters to a niche audience.

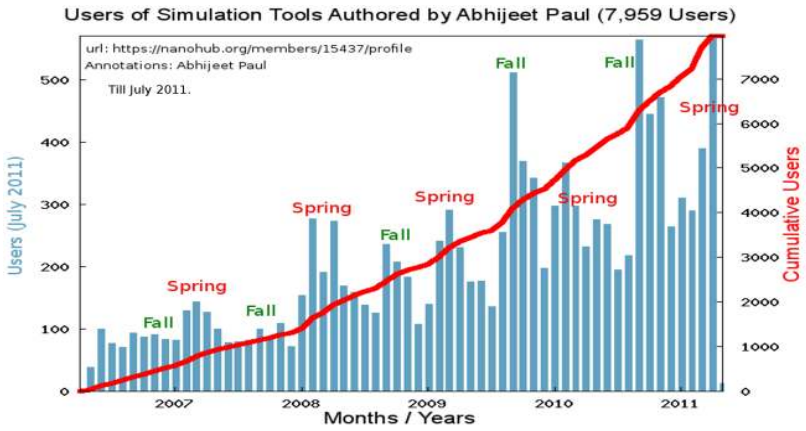


Fig. G.6. A detailed usage statistics graph of the contributions made by Abhijeet Paul on nanoHUB.org from Fall 2006 till July 2011. url:*https://nanohub.org/members/15437/usage*.

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PUBLICATION LIST

The chapter-wise publication list includes relevant journals and conference proceedings which form this thesis. Some of manuscripts are under review or under preparation at the time of thesis preparation. This list is as follows:

Chapter 2:

1. "On the validity of the top of the barrier quantum transport model for ballistic nanowire MOSFETs", **Abhijeet Paul**, Saumitra Mehrotra, Mathieu Luisier, and Gerhard Klimeck, *13th International Workshop on Computational Electronics (IWCE)*, May 2009, Tsinghua University, Beijing, China.

Chapter 3:

1. "Performance Prediction of Ultra-scaled SiGe/Si Core/Shell Electron and Hole Nanowire MOSFETs", **Abhijeet Paul**, Saumitra Mehrotra, Mathieu Luisier, Gerhard Klimeck, *IEEE Elec. Dev. Lett.*, Vol. 31 pp. 278-280, 2010, doi:10.1109/LED.2010.2040577.
2. "Atomistic study of electronic structure of PbSe nanowires", **Abhijeet Paul** and G. Klimeck, *Appl. Phys. Lett.* 98, 212105, (2011).
3. "Atomistic approach to alloy scattering in $Si_{1-x}Ge_x$", S. Mehrotra, **Abhijeet Paul** and G. Klimeck, *Appl. Phys. Letts.* 98, 173503, (2011).
4. "Performance enhancement of GaAs UTB pFETs by strain, orientation and body thickness engineering", **Abhijeet Paul**, Saumitra Mehrotra, Gerhard Klimeck, Mark Rodwell, presented in *68th IEEE Device Research Conference*, Santa Barbara, USA, 2011.

Chapter 4:

1. "Characterization and Modeling of Subfemtofarad Nanowire Capacitance Using the CBCM Technique", Hui Zhao, Raseong Kim, **Abhijeet Paul**, Mathieu Luisier, Gerhard Klimeck, Fa-Jun Ma, Subhash C. Rustagi, Ganesh S. Samudra, Navab Singh, Guo-Qiang Lo, Dim-Lee Kwong, *IEEE Elec. Dev. Lett.*, Vol. 30, pp. 526-528, 2009, doi:10.1109/LED.2009.2015588

2. "Thermionic Emission as a tool to study transport in undoped nFinFETs", Giuseppe C. Tettamanzi, **Abhijeet Paul**, Gabriel P. Lansbergen, Jan Verduijn, Sunhee Lee, Nadine Collaert, Serge Biesemans, Gerhard Klimeck, Sven Rogge, *IEEE Elec. Dev. Lett.*, Vol. 518 pp. 2521-2523, 2009; doi:10.1109/LED.2009.2036134.

3. "Intrinsic Reliability improvement in Biaxially Strained SiGe p-MOSFETs", Shweta Deora, **Abhijeet Paul**, Bijesh R, Jeff Huang, Gerhard Klimeck, Gennadi Bersuker, Paul Kirsch, Raj Jammy, *IEEE Elec. Dev. Lett.*, Vol. 32, pp. 255-257, 2011, doi:10.1109/LED.2010.2099101.

4. "Interface Trap Density Metrology of state-of-the-art undoped Si n-FinFETs", Giuseppe Carlo Tettamanzi, **Abhijeet Paul**, Sunhee Lee, Saumitra R. Mehrotra, Nadine Collaert, Serge Biesemans, Gerhard Klimeck, Sven Rogge, *IEEE Elec. Dev. Lett.* Vol. 32, 2011, doi:10.1109/LED.2011.2106150.

5. "Interface trap density metrology from sub-threshold transport in highly scaled undoped channel Si n-FinFETs", **Abhijeet Paul**, Giuseppe Carlo Tettamanzi, Sunhee Lee, Saumitra R. Mehrotra, Nadine Collaert, Serge Biesemanns, Sven Rogge, and Gerhard Klimeck, accepted in *Journal of Applied Physics*, 2011.

Chapter 5:

1. "Modified valence force field approach for phonon dispersion: from zinc-blende bulk to nanowires, methodology and computational details", **Abhijeet Paul**, Mathieu Luisier and Gerhard Klimeck, *Journal of Computational Electronics*, Vol. 9, Oct. 2010.

2. "Atomistic modeling of the phonon dispersion in free-standing ⟨100⟩ Si nanowires", **Abhijeet Paul**, M. Luisier and G. Klimeck, *14th Int. Workshop on Comp. Electronics (IWCE)*, Pisa, Italy, 2010, doi:10.1109/IWCE.2010.5677959.

Chapter 6:

1. "Influence of cross-section geometry and wire orientation on the phonon shifts in ultra-scaled Si nanowires", **Abhijeet Paul**, Mathieu Luisier, and Gerhard Klimeck, under review in *Journal of Applied Physics*, 2011.
2. "Shape and orientation effects on the ballistic phonon thermal properties of ultra-scaled Si nanowires", **Abhijeet Paul**, Mathieu Luisier, and Gerhard Klimeck, submitted to *Journal of Applied Physics*, 2011.
3. "Definition of bulk for electronic, structural and thermal properties of Silicon nanowires", **Abhijeet Paul**, Mathieu Luisier, and Gerhard Klimeck, *under preparation*, 2011.

Chapter 7:

1. "Tuning lattice thermal conductance by porosity control in ultra-scaled Si and Ge nanowires", **Abhijeet Paul** and Gerhard Klimeck, *Appl. Phys. Letts.*, 98, 083106, 2011.
2. "Tuning lattice thermal conductance in ultra-scaled hollow Si Nanowires: Role of porosity size, density and distribution", **Abhijeet Paul**, K. Miao, M. Luisier and G. Klimeck, *MRS Spring Meeting*, San Fransisco, April, 2011.
3. "Strain effects on the thermal properties of ultra-scaled Si nanowires", **Abhijeet Paul**, and Gerhard Klimeck, accepted for publication in *Applied Physics Letter*, 2011.
4. "Cross-plane and In-plane thermal transport in ultra-short SiGe superlattice nanowires", **Abhijeet Paul**, Kai Miao, Mathieu Luisier, and Gerhard Klimeck, *under preparation*, 2011.

5. "Analysis of thermal boundary resistance of nanowire Si/Ge interfaces using Green's function method", Kai Miao, **Abhijeet Paul**, Mathieu Luisier, and Gerhard Klimeck, *under preparation*, 2011.

Chapter 8:

1. "An efficient algorithm to calculate intrinsic thermoelectric parameters based on Landauer approach", **Abhijeet Paul**, Shuaib Salamat, Changwook Jeong, Gerhard Klimeck and Mark Lundstrom, to be submitted to *Journal of Computational Electronics*, 2011.

Chapter 9:

1. "Atomistic modeling of the thermoelectric power factor in ultra-scaled silicon nanowires", **Abhijeet Paul** and Gerhard Klimeck, *2010 IEEE Silicon Nanoelectronics Workshop*, Honolulu, HI, June 13-14, doi:10.1109/SNW.2010.5562583, 2010.

Chapter 10:

1. "Enhancement of thermoelectric efficiency by uniaxial tensile stress in n-type GaAs nanowires", **Abhijeet Paul**, Kai Miao, Ganesh Hegde, Saumitra Mehrotra, Mathieu Luisier and Gerhard Klimeck, presented in *IEEE NANO conf.*, Portland, Or, USA, August, 2011.
2. "Tuning thermoelectric efficiency of Silicon nanowires using porosity control", **Abhijeet Paul** and Gerhard Klimeck, *under preparation*, 2011.

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Abhijeet Paul received his BS and MS in Electrical and VLSI Micro-electronics, respectively, both from IIT Bombay, India, in 2006. He joined the PhD program in the school of Electrical and Computer Engineering at Purdue University, West Lafayette, USA, under the guidance of Prof. Gerhard Klimeck, in Fall 2006. At Purdue he was the member of the Network for Computational Nanotechnology (NCN) center and the NCN student committee. His research at Purdue was focussed on multi-scale computational modeling of the electrical and thermal properties in semiconductor nanostructures. He was involved in the development of physics based computational models and device simulation tools, using high performance computing, for the next generation semiconductor devices. He has contributed 8 tools and 12 resources on the cyber nanotechnology portal called nanoHUB.org including the most used tool called Band Structure Lab. His contributed resources have supported >7000 users till Oct. 2011 on nanoHUB.org. He was awarded the Bilsland Dissertation Fellowship for the year 2011-12, at Purdue University. He has (co)-authored 17 peer-reviewed journal papers and 25 conference papers/posters. He is a student member of the IEEE and the American Physical Society (APS). After the PhD he will join GLOBALFOUNDRIES, a semiconductor foundry, at Albany Nanotech in NewYork as a Device Research Engineer working on 14nm Si CMOS technology.