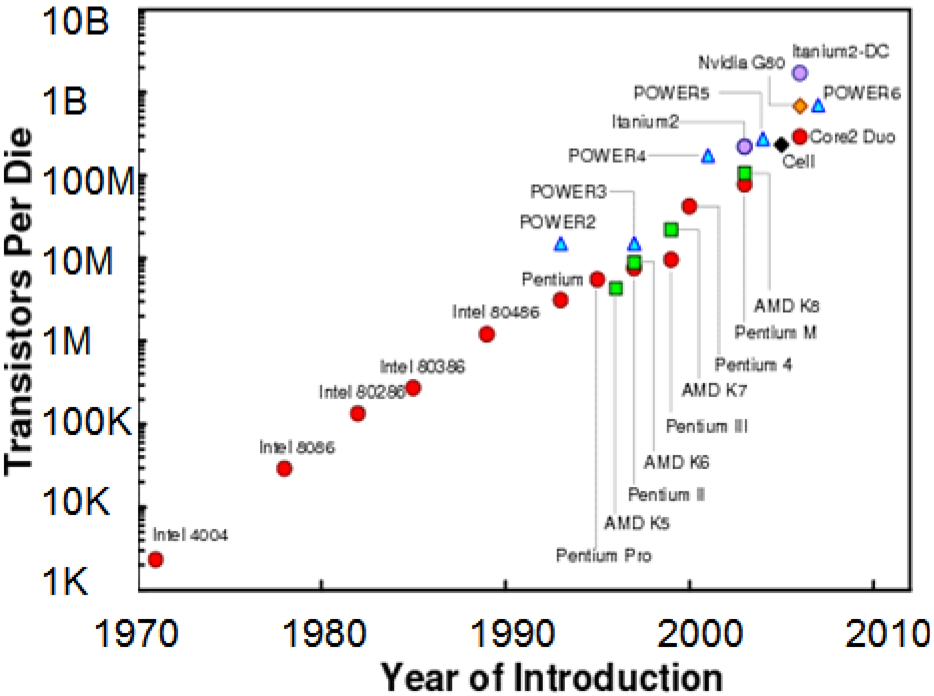
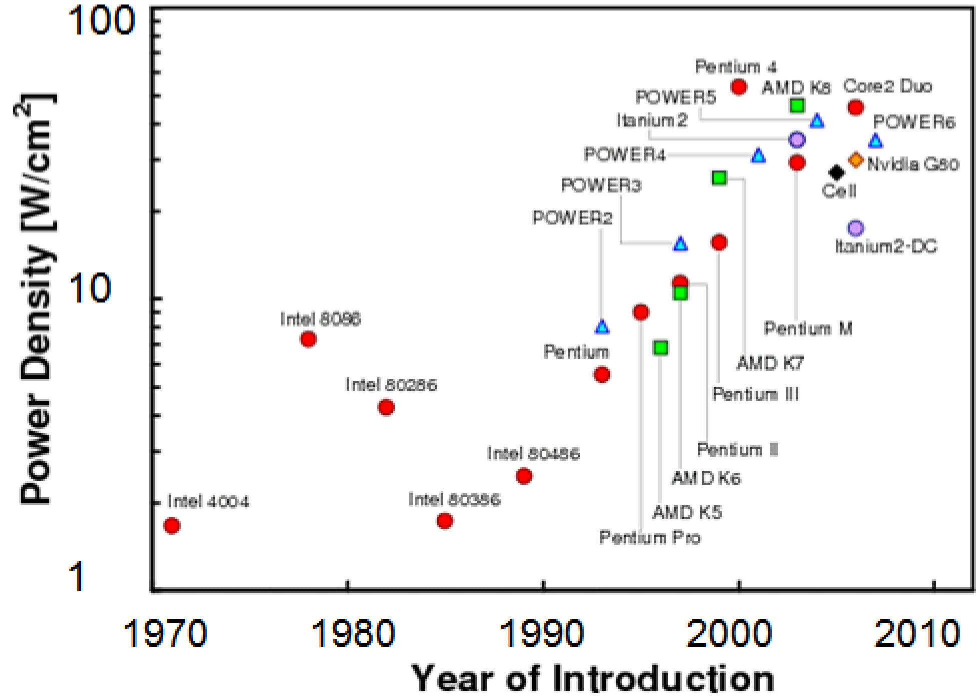
Design and Simulation of Two-dimensional Superlattice Steep Transistors

Pengyu Long,
Network for Computational Nanotechnology, Purdue University,
West Lafayette, IN 47907, USA
long106@purdue.edu

Motivation



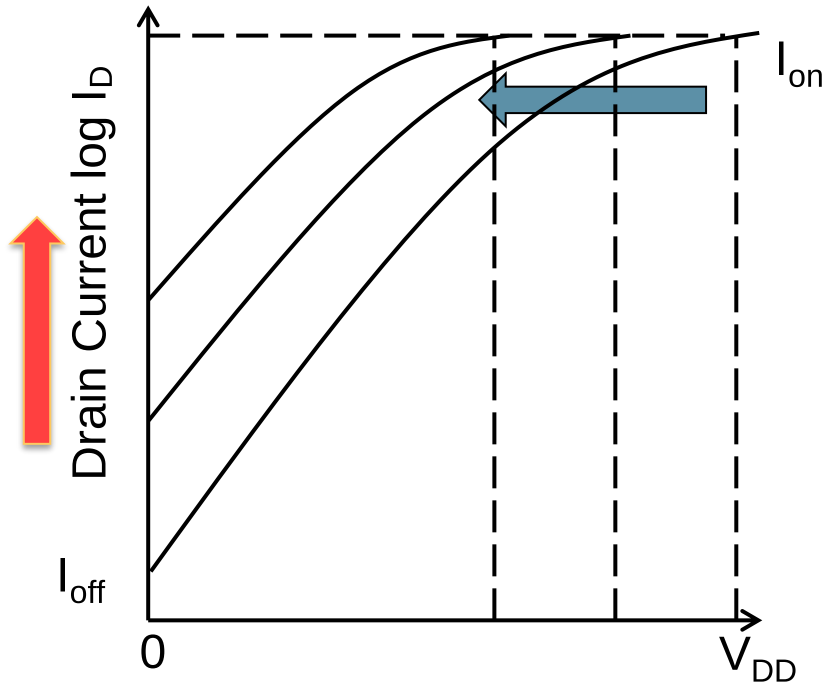


transistor density increase → power density increase

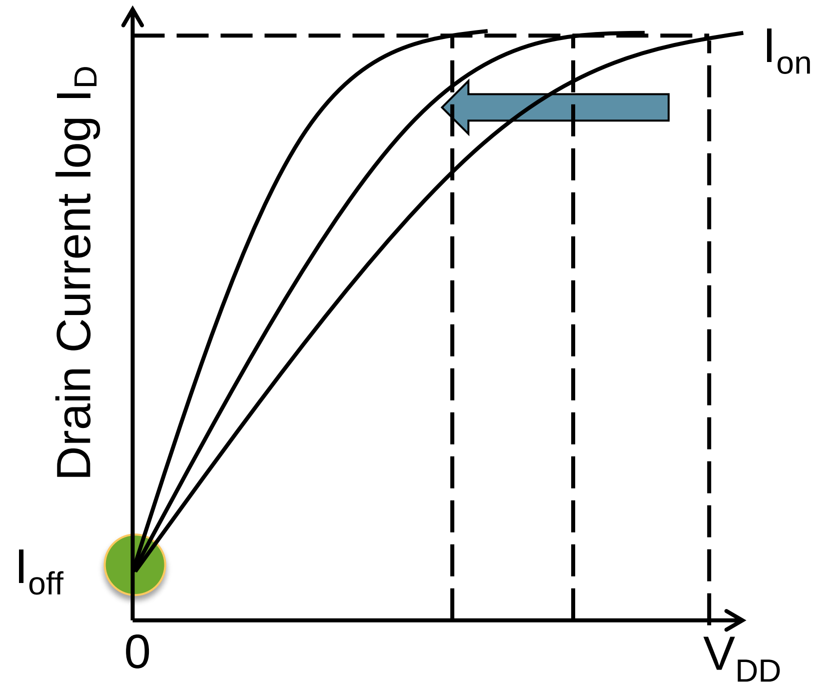
Isci C. Workload adaptive power management with live phase monitoring and prediction[D]. Princeton University, 2007.

Motivation: reduce power density

- Constant Subthreshold Swing:
  - » Reducing the supply voltage(V_{DD}) → reduced power, but increase in I_{off}



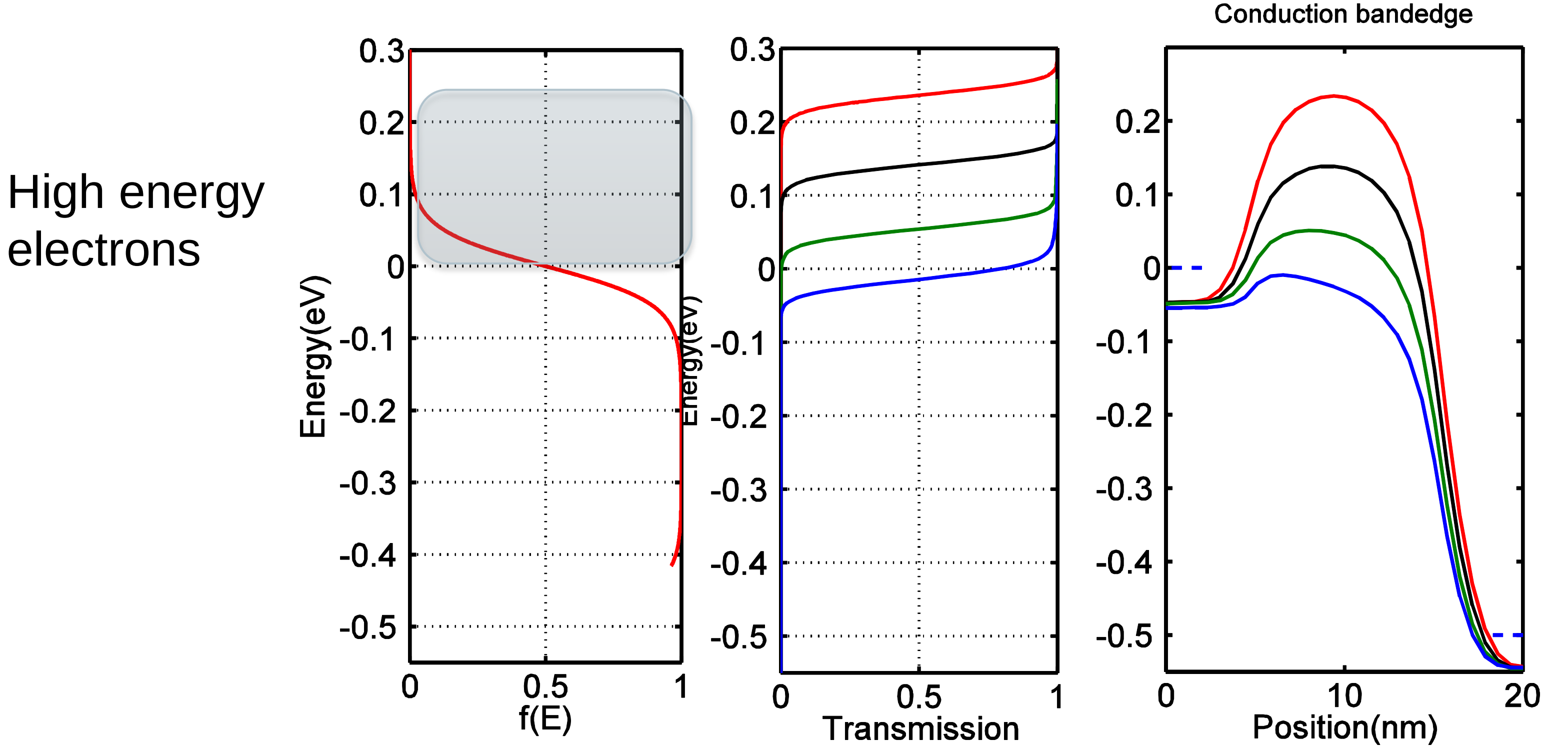
- Steeper Subthreshold Swing:
  - » Reducing V_{DD} → reduced power, I_{off} doesn't increase!



Low power design → require steep Subthreshold Swing

How to reduce the Subthreshold Swing

- Problem: The 60mV/dec limit: comes from high energy electrons in f(E)

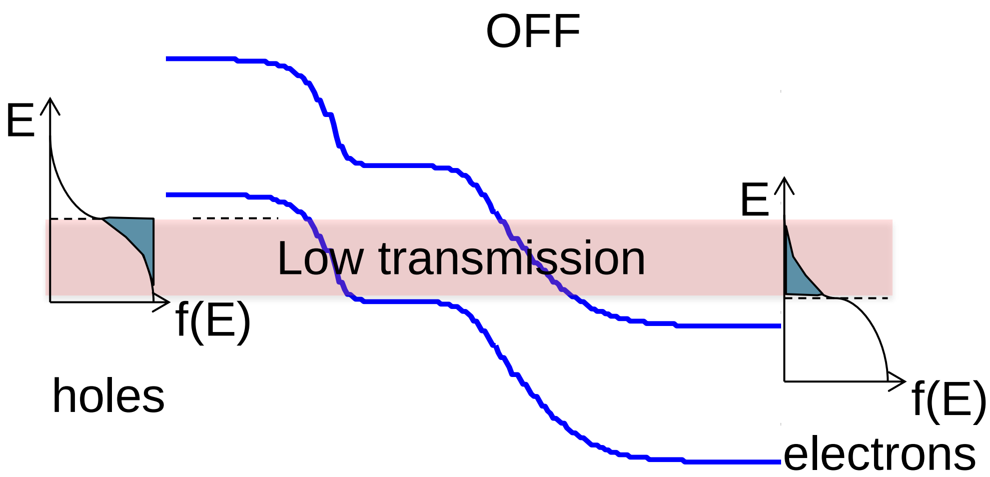


High energy electrons have high transmission to get into channel.

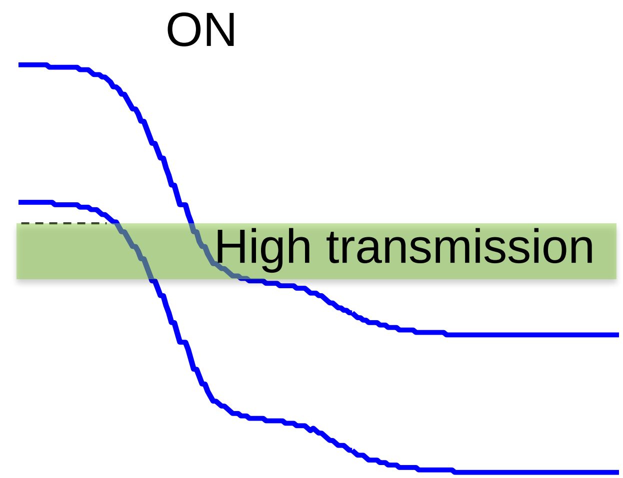
Solution: add an energy filter to suppress high energy electrons

How to reduce the Subthreshold Swing

- Existing energy filter design: Tunneling FET (TFET)



Off: bandgap blocking high energy carriers



On: band-to-band tunneling

Energy filter → High energy carriers are suppressed → steep Subthreshold Swing

Problem: At on-state, the tunneling transmission is small → limited I_{on}

Energy filter with high I_{on}

Band-to-band tunneling:

- high energy electrons are blocked → Steep subthreshold swing
- Limited tunneling probability→ Limited I_{on}

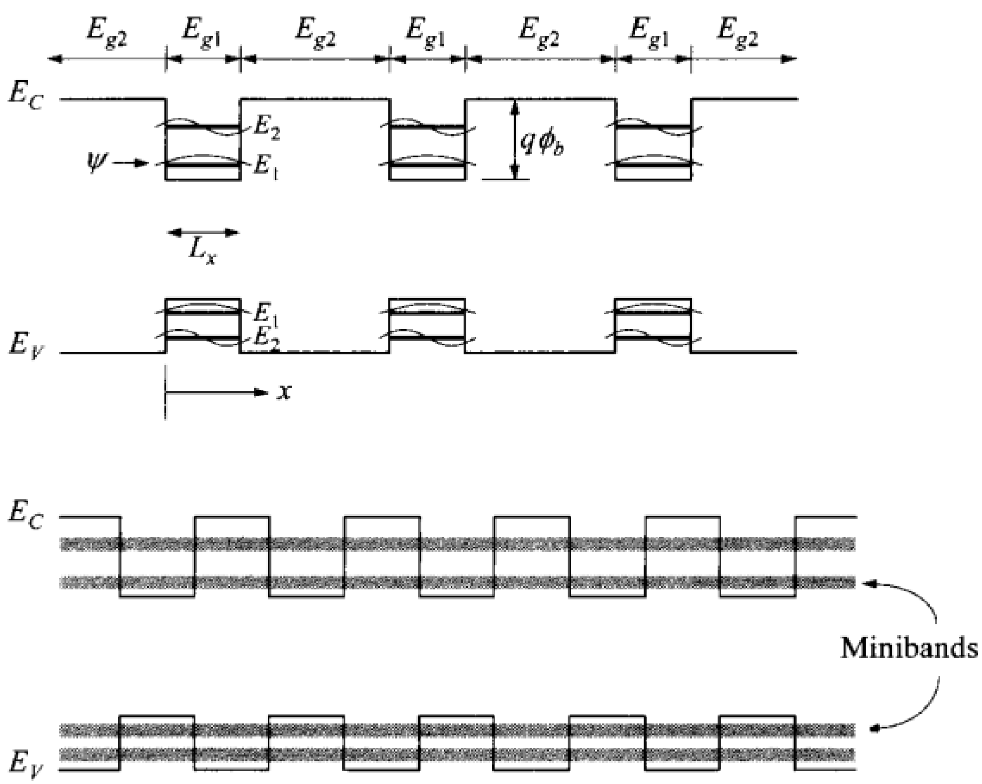
Any energy filters that has both **steep subthreshold swing** and **high I_{on}**?

	Suppress high energy carries	High transmission at on-state
Band-to-band tunneling	Yes	limited
Resonant tunneling	Yes	Yes

New solution: superlattice energy filter

Superlattice:

- Minigap: intrinsic energy filter→ steep Subthreshold swing.
- Wide and smooth miniband → high I_{on}



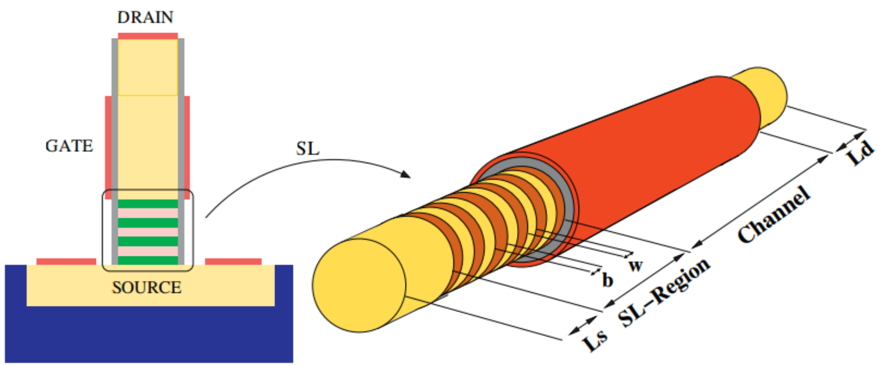
- Separated quantum wells
  - wavefunction are separated → discrete confined states

Thinner barriers

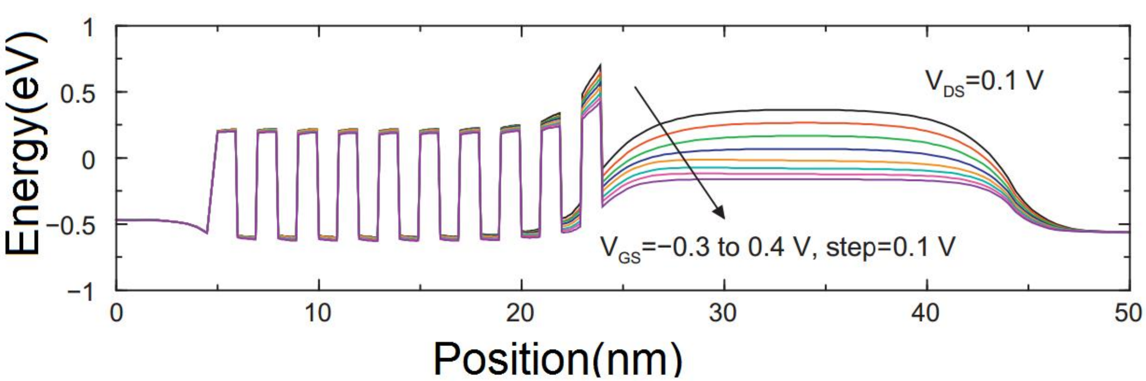
- Superlattice
  - wavefunction are overlapped →smooth minibands

Sze S M, Ng K K. Physics of semiconductor devices[M]. John Wiley & Sons, 2006.

Nanowire superlattice MOSFET



Proposed in literature



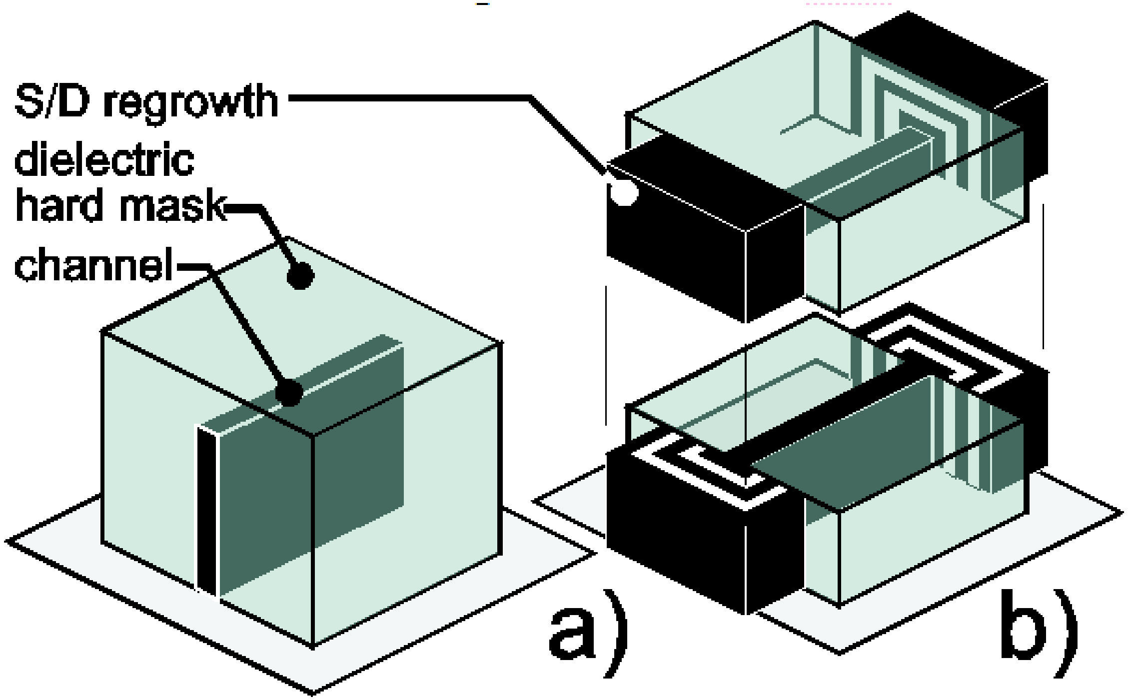
The superlattice has to be in the source

- If placed in channel: distorted by Vgs
- If placed in the drain: distorted by Vds

Vertical nanowires might be hard to fabricate and achieve high I_{on} per die.

- Maiorano P, Gnani E, Grassi R, et al.. Solid-State Electronics, 2014, 98: 45-49.
- Gnani E, Reggiani S, Gnudi A, et al. ICSICT, 2010, 1: 2.

- In this work, the concept is applied to 2D geometry.



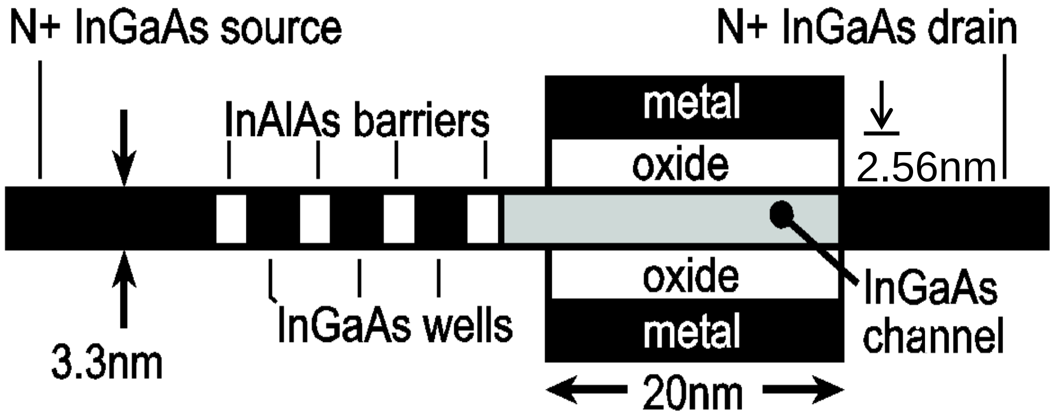
Step 1:
first form an InGaAs fin

Step 2:
growth of InGaAs and InAlAs

more easily fabricated and achieve higher I_{on} per die than vertical nanowires

2D superlattice MOSFET

- Double Gate MOSFET with 4-barrier superlattice in the source.
- The transverse direction is periodic(infinitely long).



$e = 20$

Transverse direction (perpendicular to screen)

Superlattices considered:

- InGaAs/InAlAs
- InAs/InAlAs

Can achieve higher I_{on} per die than vertical nanowires

Method and design Targets

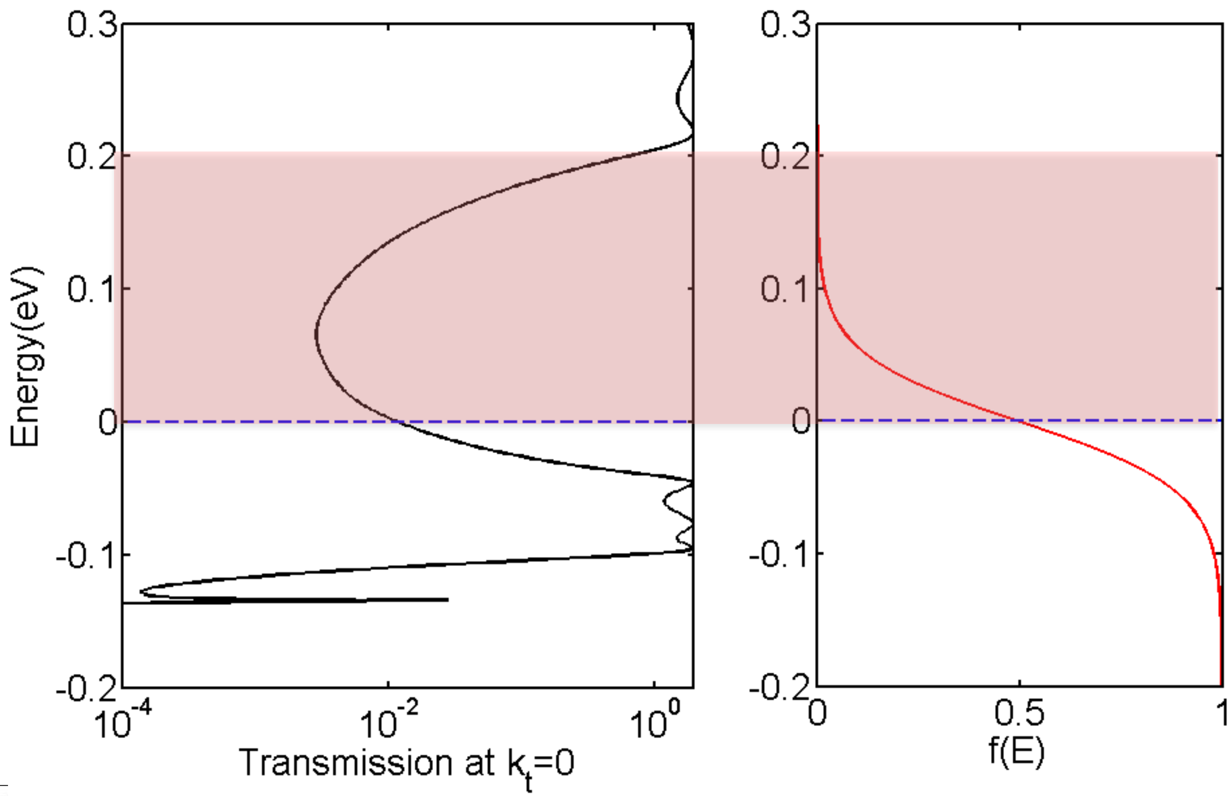
- Method:
  - Ballistic transport : quantum transmitting boundary method(QTBM)
  - sp3d5s* tight binding basis to represent band structure
  - Open-boundary Schrödinger equation & Poisson equation solved self-consistently.

- Optimization design for superlattice MOSFETs
- Target:
  - steep Subthreshold Swing
  - High I_{on}
- Strategy:
  - Geometry optimization
  - Material

Steep Subthreshold Swing

Design Target 1: steep Subthreshold Swing → source E_f should be aligned with max of 1st miniband

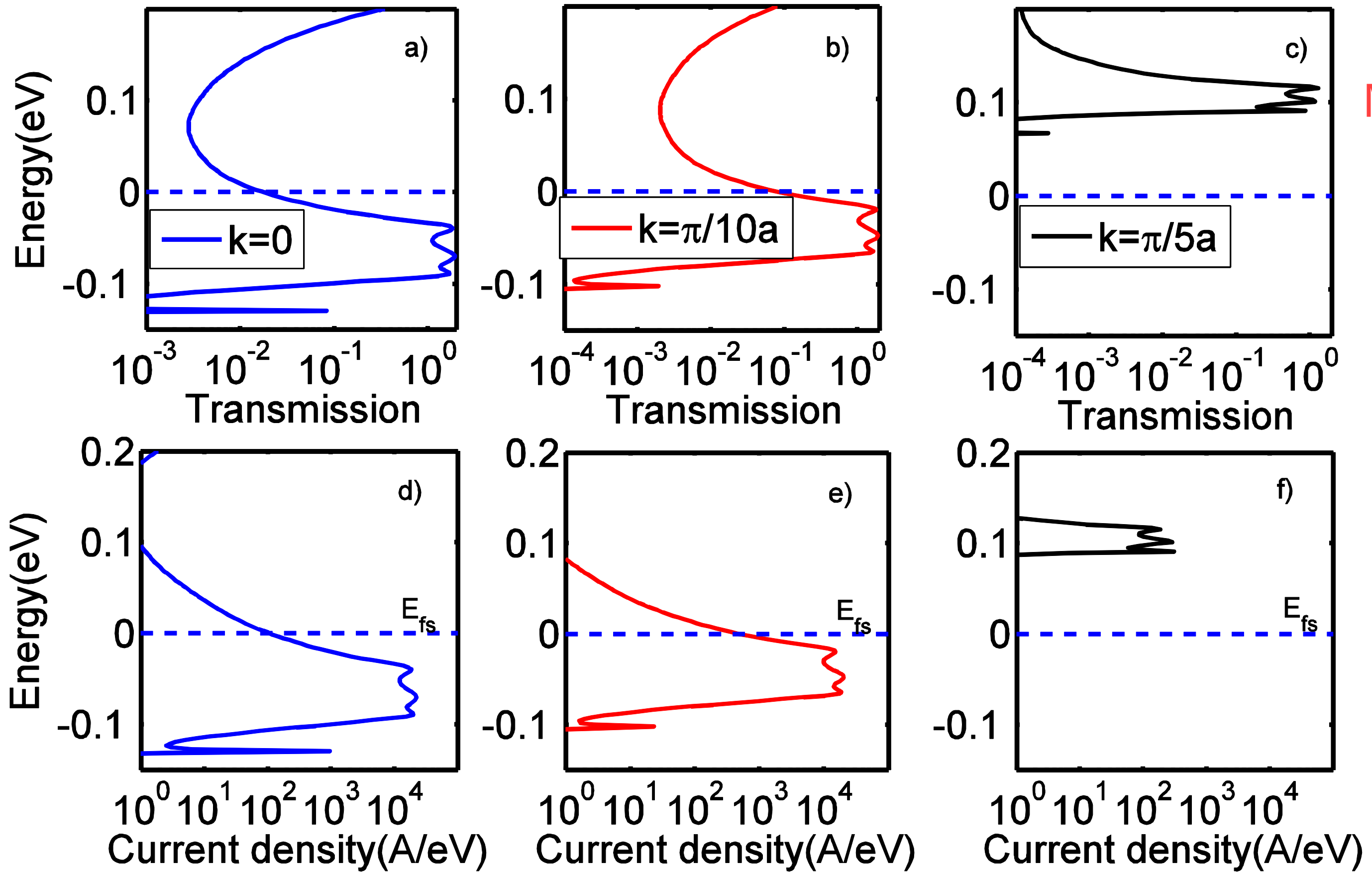
$$I_D \propto (2q/h)\cdot(W/\pi)\int_{-\pi/a}^{\pi/a}\int_{-\infty}^{+\infty} T(E,k_t)\, f(E)\, dE\, dk_t$$



High Energy electrons: Low transmission

Transverse k dependence

- However, the max of 1st miniband varies with k_t



Misaligned!

π/a is the boundary of 1st Brillion Zone

The max of 1st miniband is misaligned with E_f at high k_t.

→ Does steep S.S. hold?

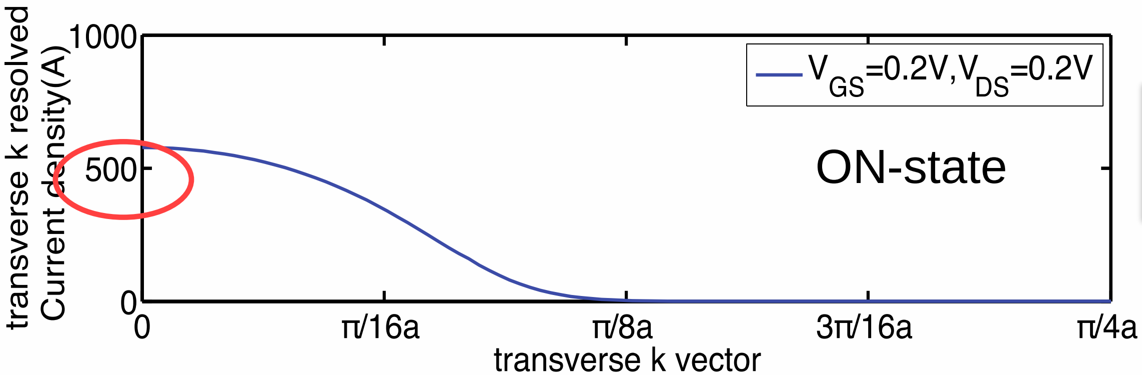
Steep SS still hold, because **small k_t carries most current.**

Transverse k resolved current density

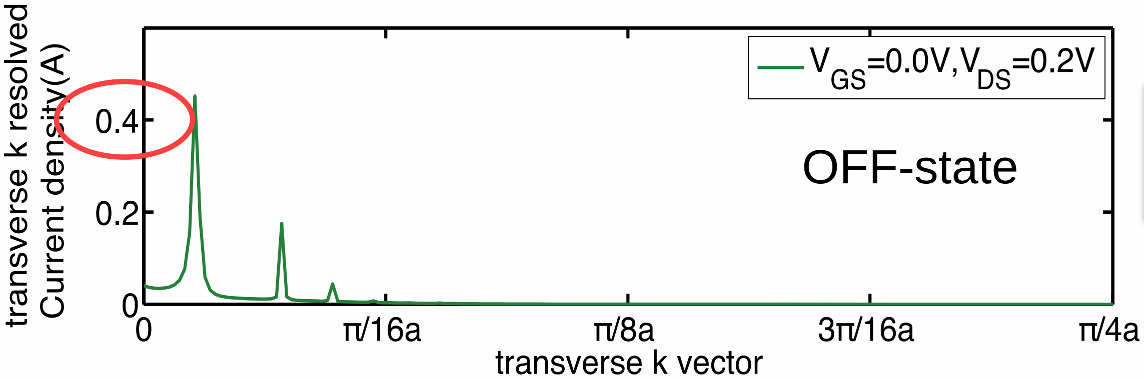
- At high k, the 1st miniband is far away from the source E_f.

→ Less electrons are conducting.

→ They carry much less current than k=0.



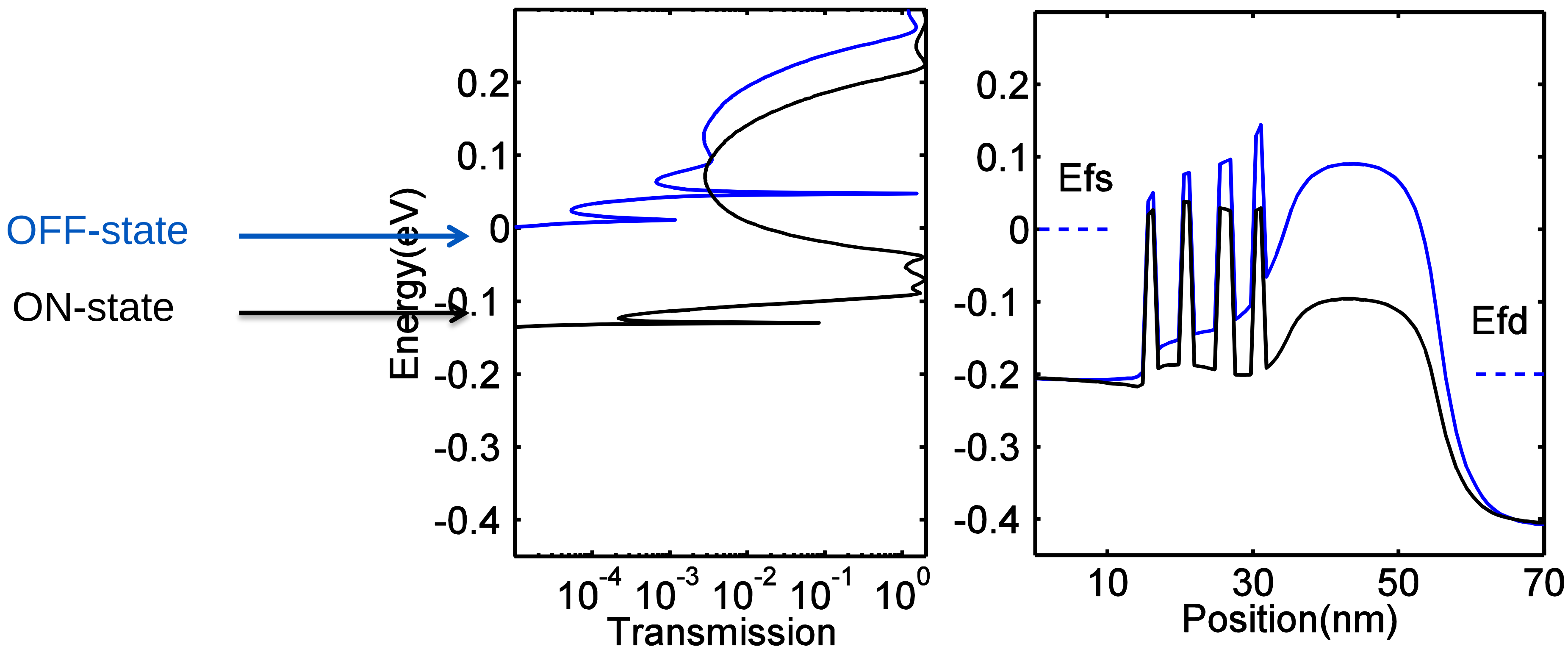
current is carried by smooth **1st miniband**.



current is carried by sharp **resonant peaks**

Current is always carried by small k_t.

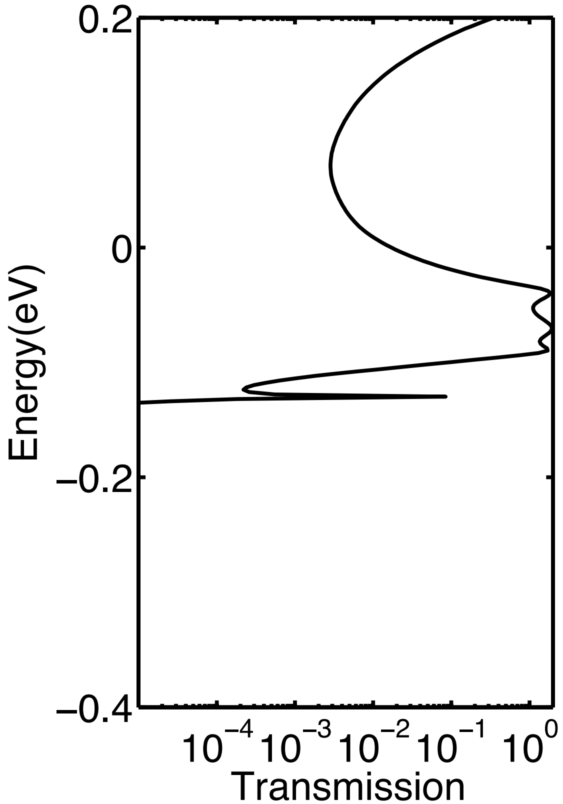
Transmission and Ec at k_t=0



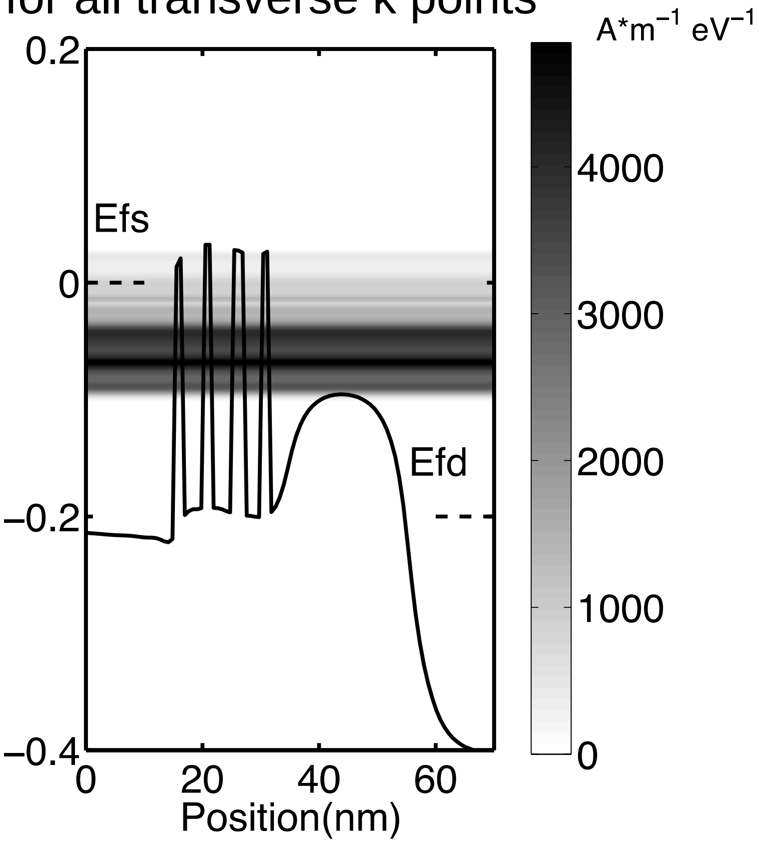
- OFF-state: current carried by narrow resonance peaks.
- ON-state: current carried by 1st miniband.

Energy resolved current density

Transmission probability at k_t=0



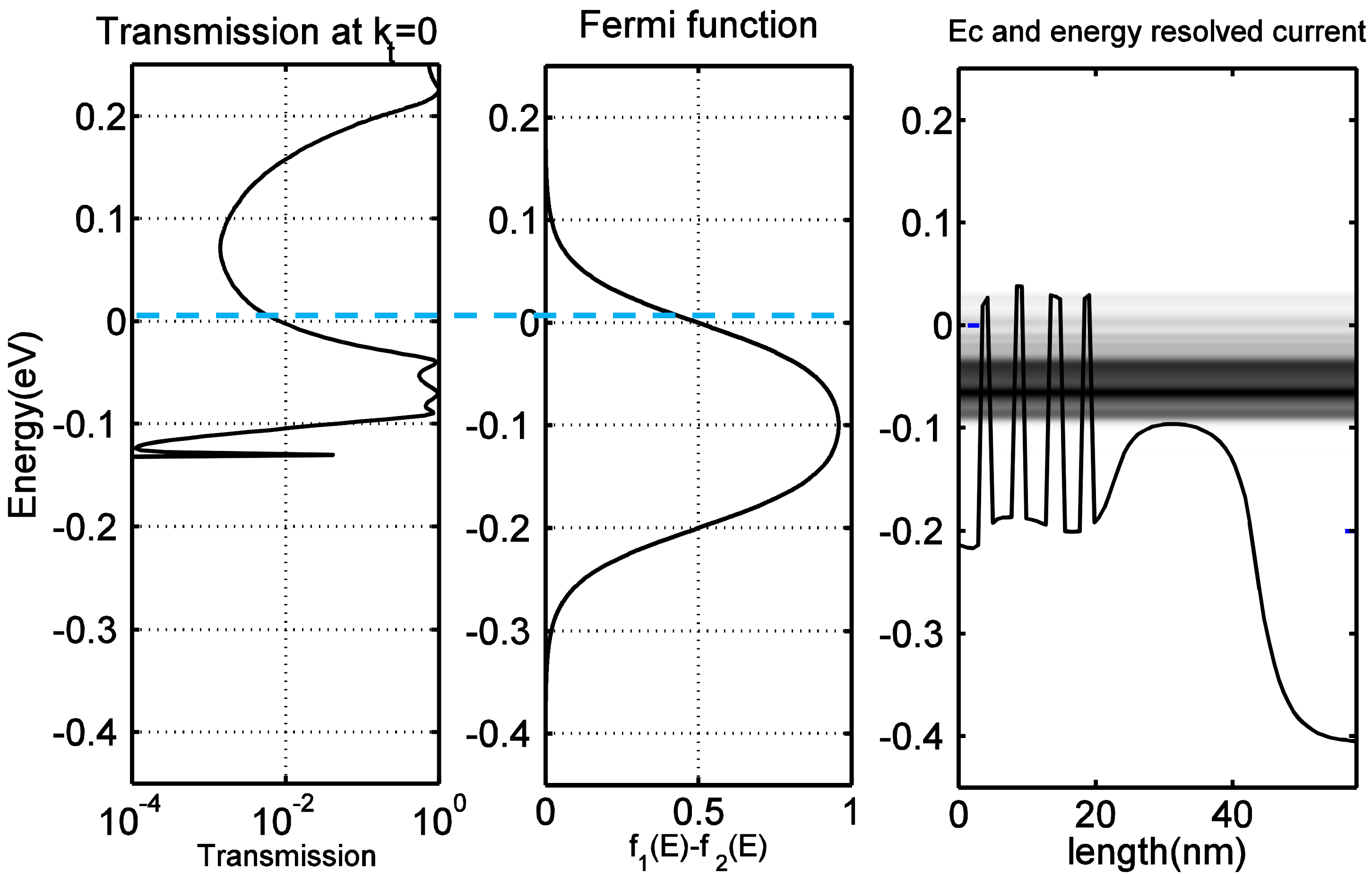
Energy resolved current density for all transverse k points



Current density is strongly confined to the 1st miniband of k_t=0.
Current contribution from higher k_t are small

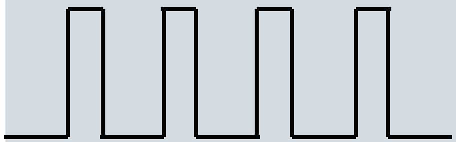
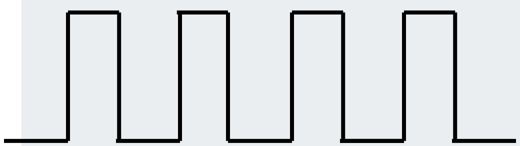
Design target 1: steep Subthreshold Swing

- **Conclusion**:
  - » source Ef should be aligned with upper edge of 1st miniband **for small k_t**.
  - » High k_t carriers little current



Maximum I_{on}

- **Design Target 2:** maximum I_{on} → minimize fluctuations in 1st miniband → adjust barrier thickness

	miniband	minigap
Thin barriers 	small fluctuations(big I_{on})	bigger transmission (big I_{off})
Thick barriers 	big fluctuations(big I_{on})	small transmission (low I_{off})

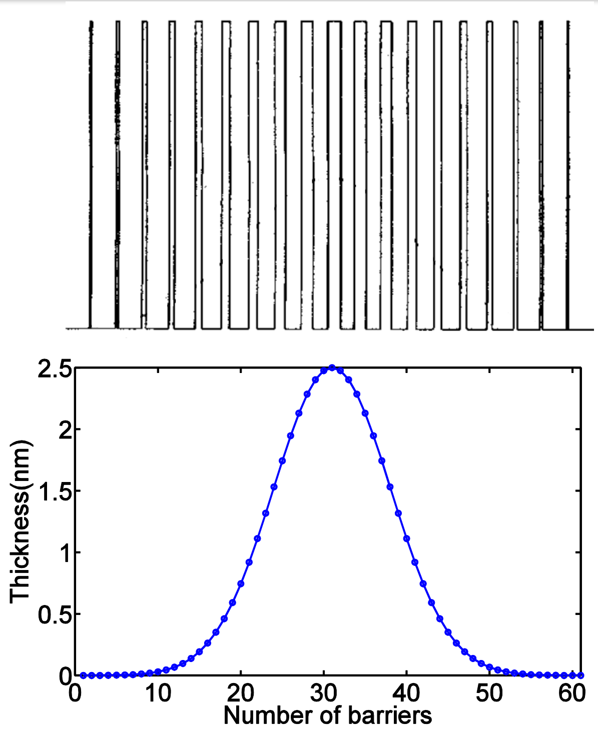
How to balance between off-state and on-state performance?

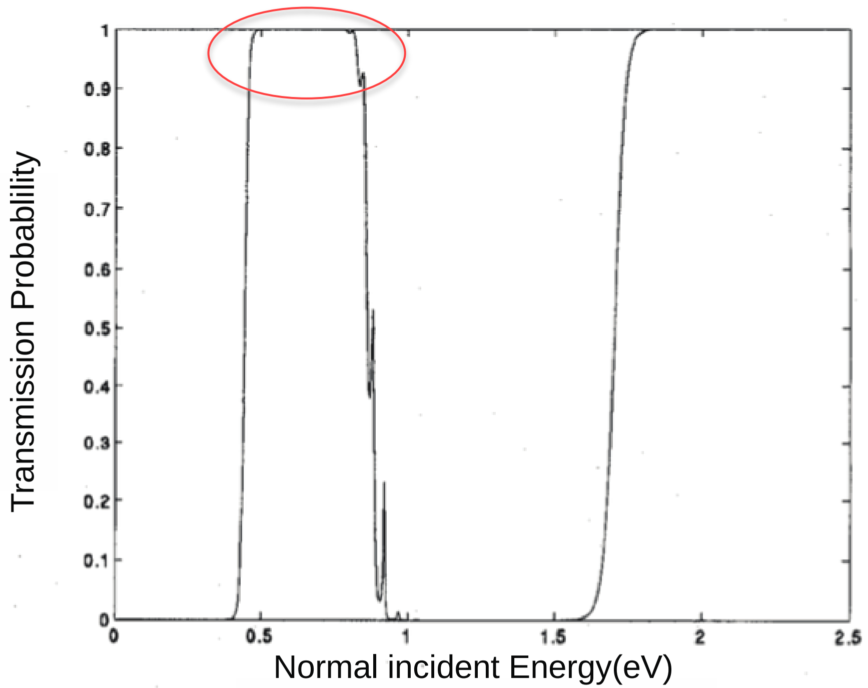
Maximum I_{on}: design guideline

Similar to designing a band-pass wave filter:

fluctuation comes from mismatch between contact and heterojunction

minimize fluctuation → decrease the mismatch





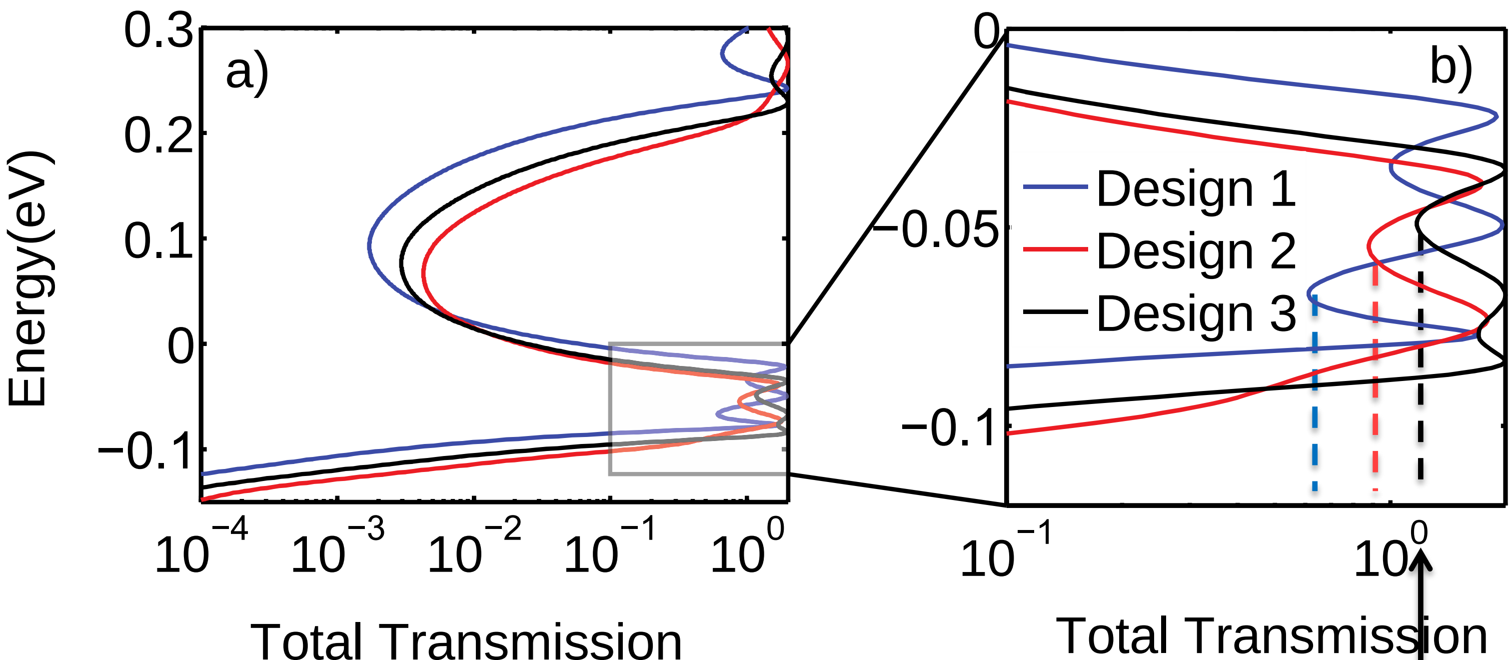
Conclusion:

Barrier thickness close to Gaussian distribution → flat miniband →maximum I_{on}

Tung H H, Lee C P.. Quantum Electronics, IEEE Journal of, 1996, 32(12): 2122-2127.

Maximum I_{on}: graded barriers

- However, too many barriers add to the total length of the device.
- A 4-barrier superlattice is optimized following the “graded barrier” guideline.



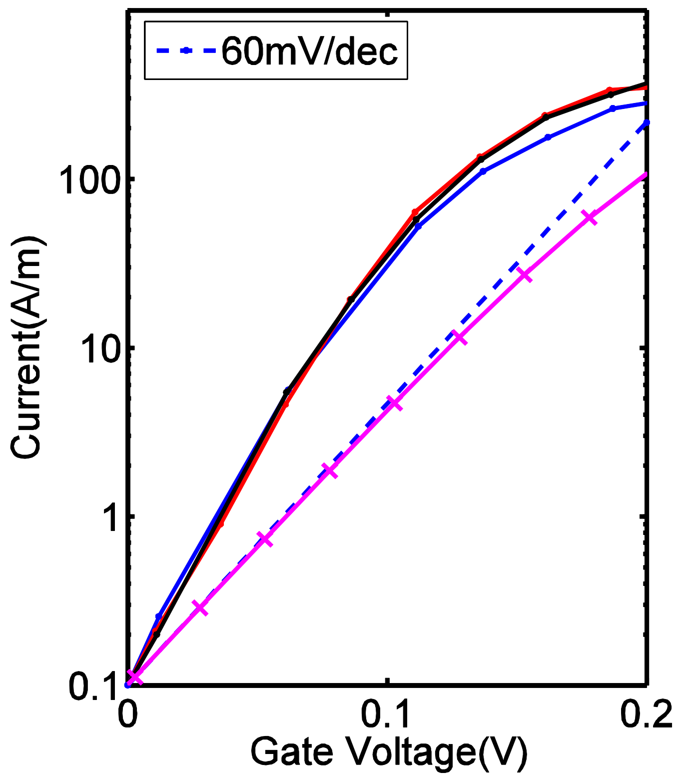
- All have 12 monolayer* (ml) length wells,
  - Design 1: 5ml barriers,
  - Design 2: 3ml, 6ml, 6ml and 3ml barriers,
  - Design 3: 4ml, 6ml, 6ml and 4ml barriers.

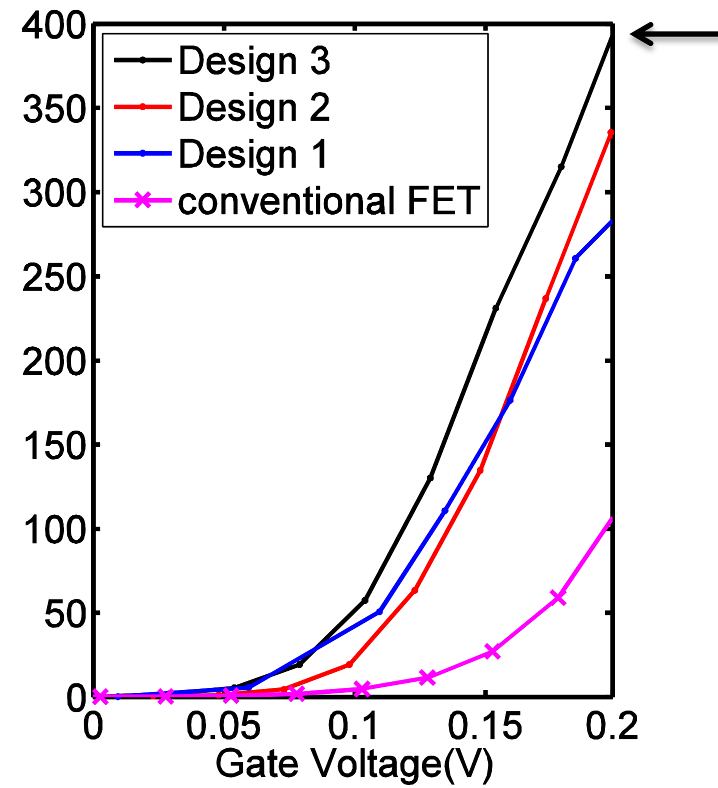
Design 3 has the flattest passband → the biggest on-current

*One monolayer is made up of one layer of cations and one layer of anions.

Transfer characteristics

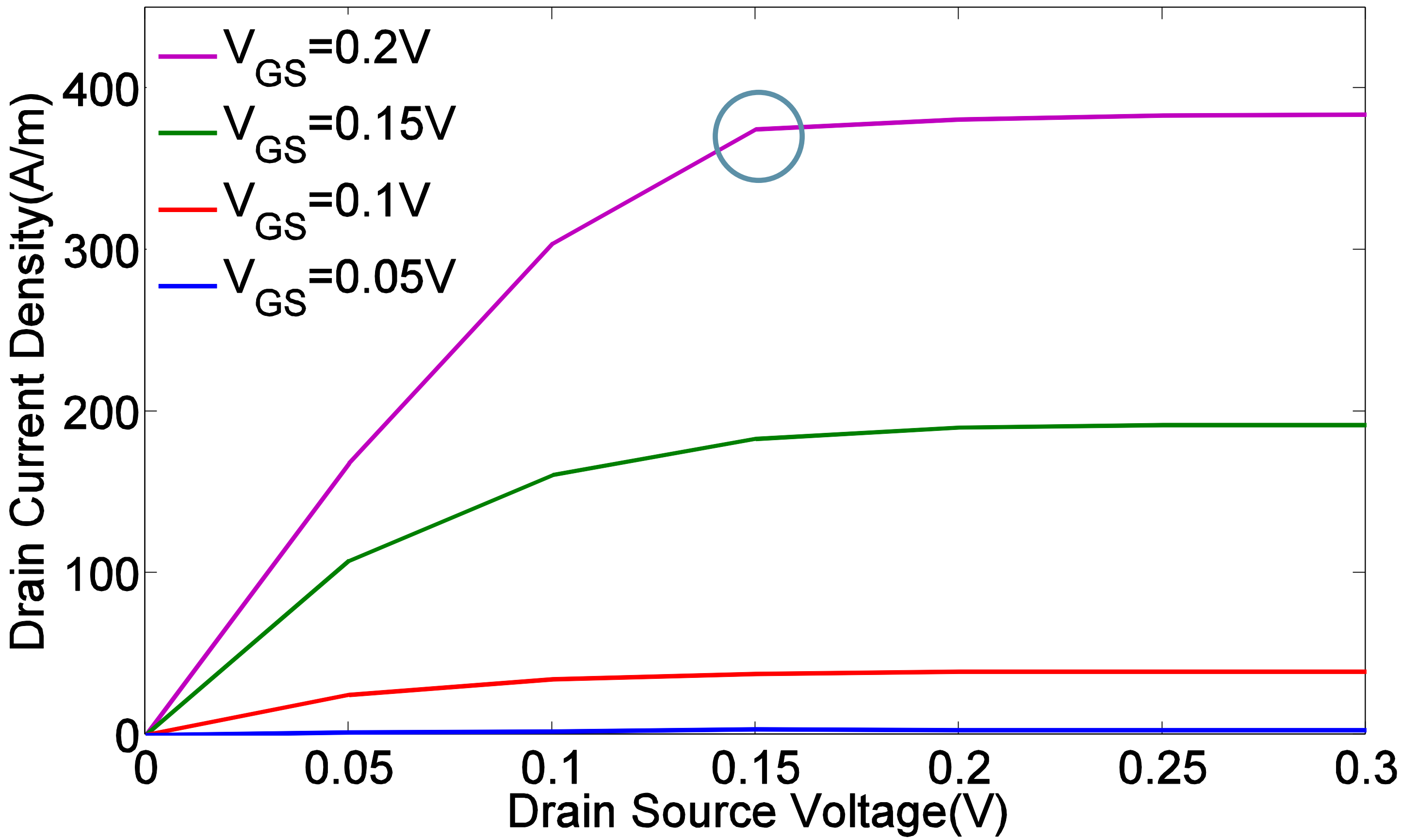
	S.S.(mV/dec)
Design3	37.5
Design2	33.8
Design1	29.4





- Design 3 has the flattest passband → biggest I_{on}
- Superlattice MOSFET has better S.S. and higher I_{on} than conventional MOSFETs

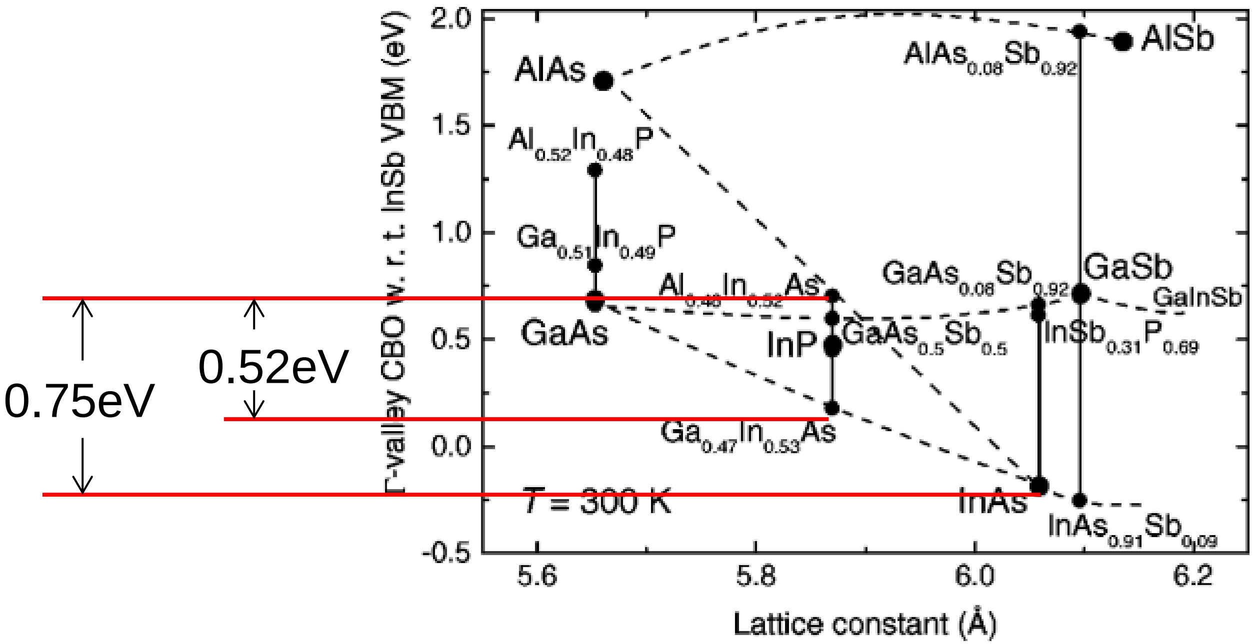
Output characteristics



Result: The current saturates at ~ 0.2V for V_{gs}=0.2V .
Reason: 1st miniband is no wider than 0.2eV

Conclusion: This device should work under low V_{DD}

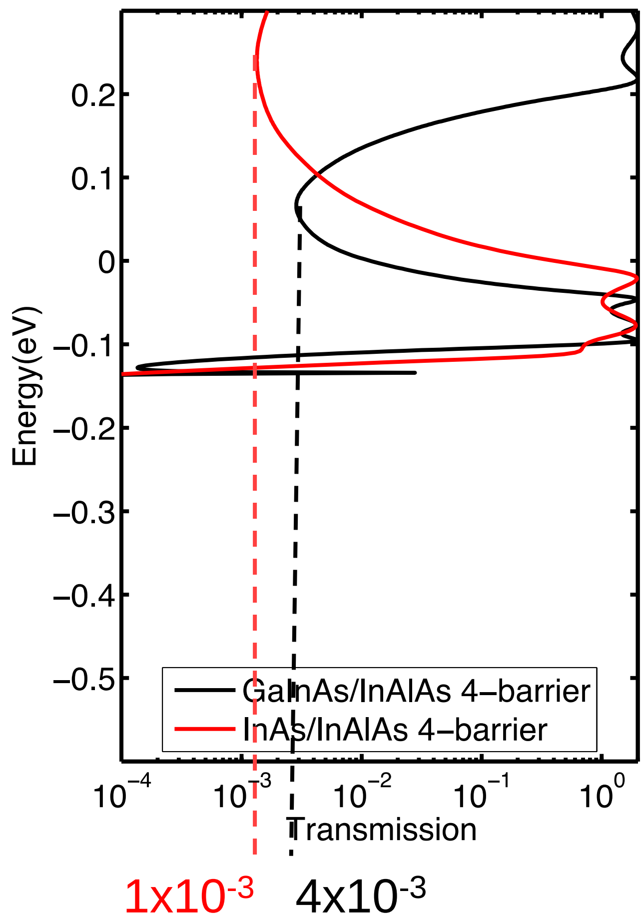
Material Optimization

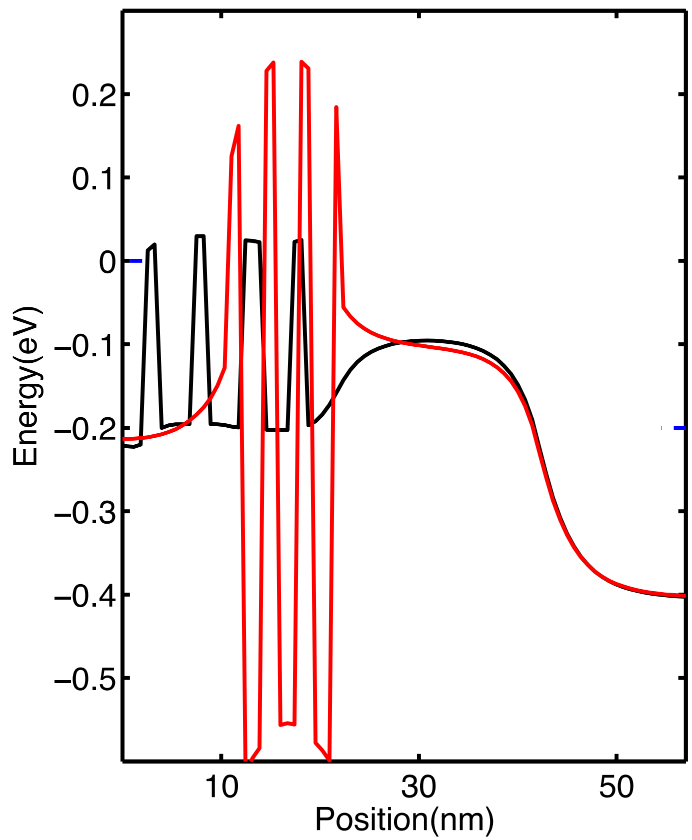


- Motivation: InAs/InAlAs superlattice has a bigger band offset than InGaAs/InAlAs.
  → lower transmission in the minigap
  → lower I_{off}

Vurgaftman I, Meyer J R, Ram-Mohan L R.. *Journal of applied physics*, 2001, 89(11): 5815-5875.

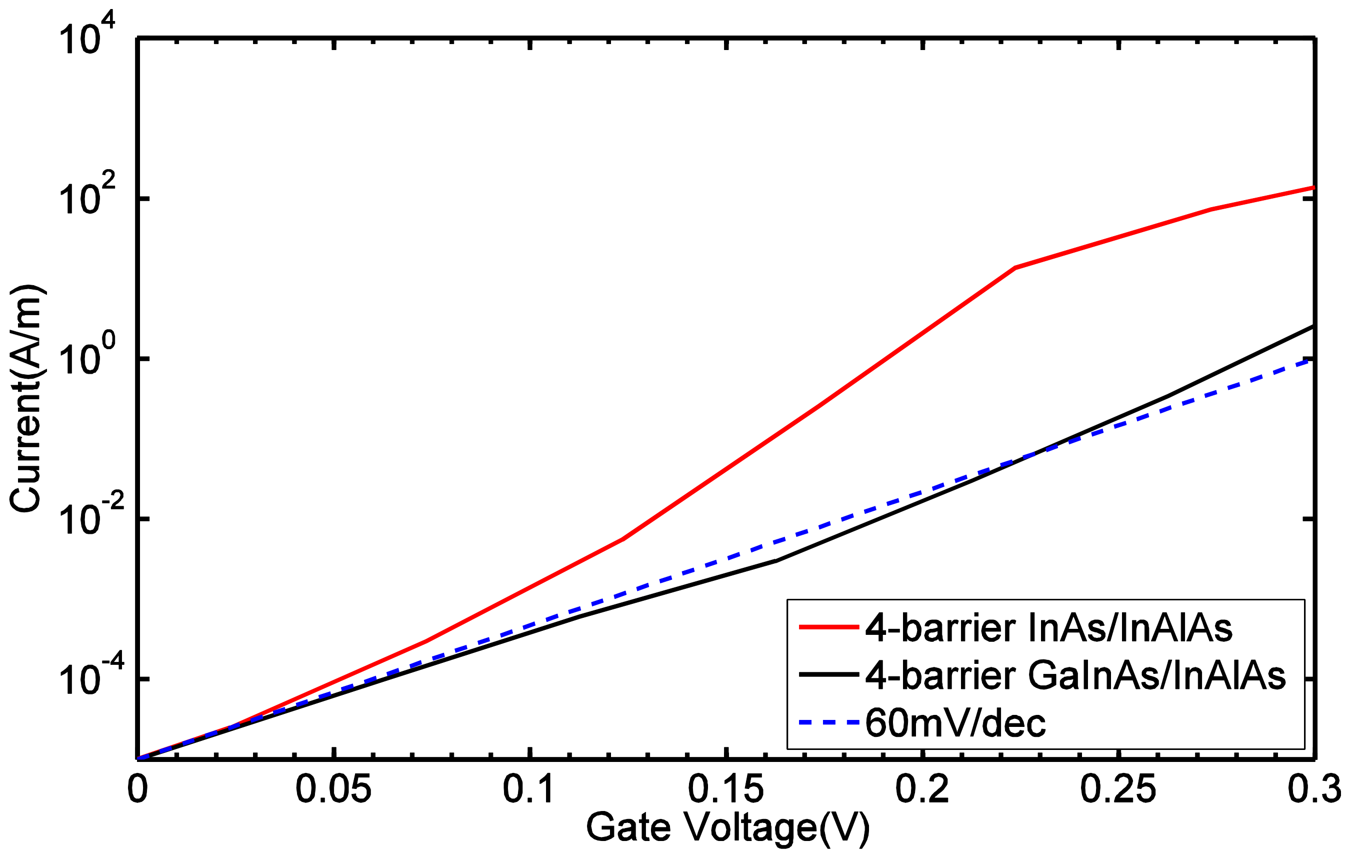
Effect of Conduction band offset





- Transmission in the minigap reaches ~$1x10^{-3}$
- 1st Miniband is wider, carries more current

Effect of Conduction band offset on Id-Vg



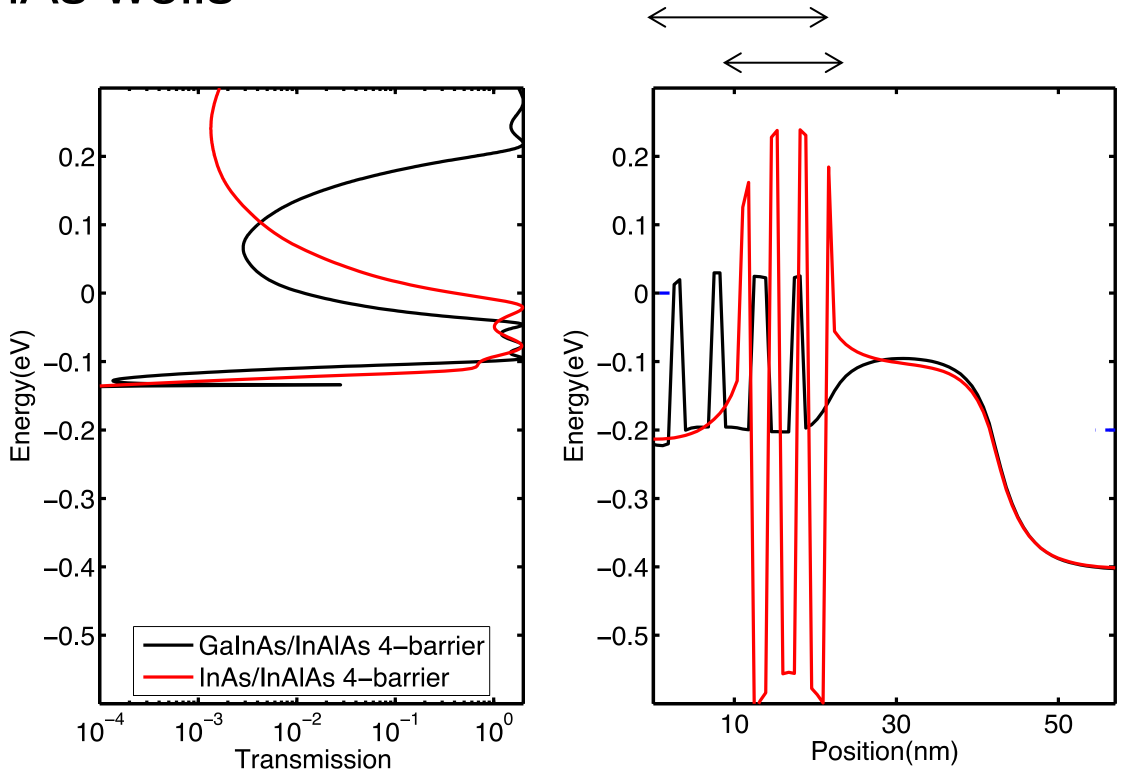
1×10^{-5}A/m Low power VLSI I_{off} standard is used.

InAs/InAlAs shows both sharper S.S. and higher ON/OFF ratio

InAs/InAlAs: more superlattice periods

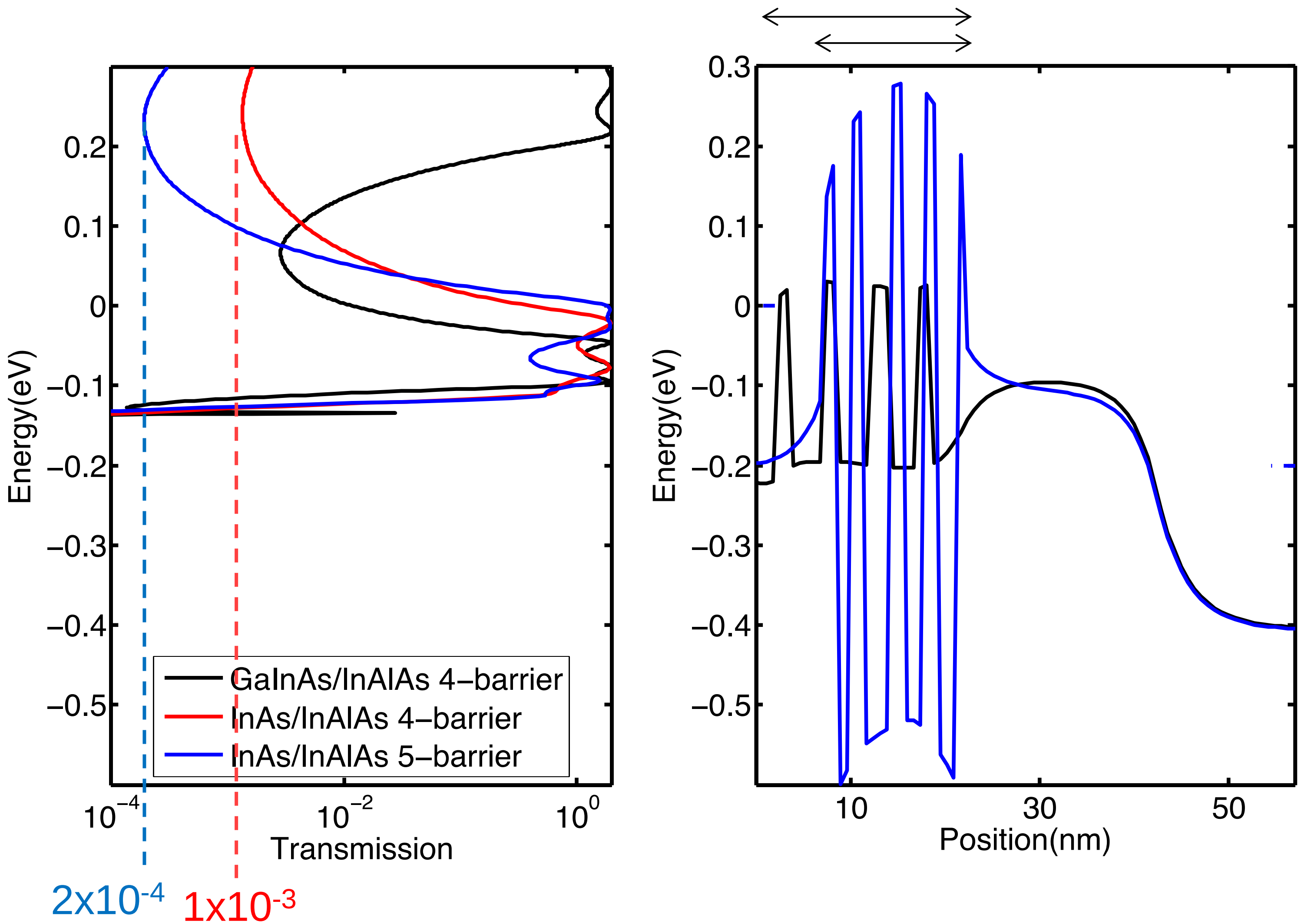
- InAs has a lower E_c than InGaAs .
- To still align max of 1st miniband with source E_f

→ thinner InAs wells



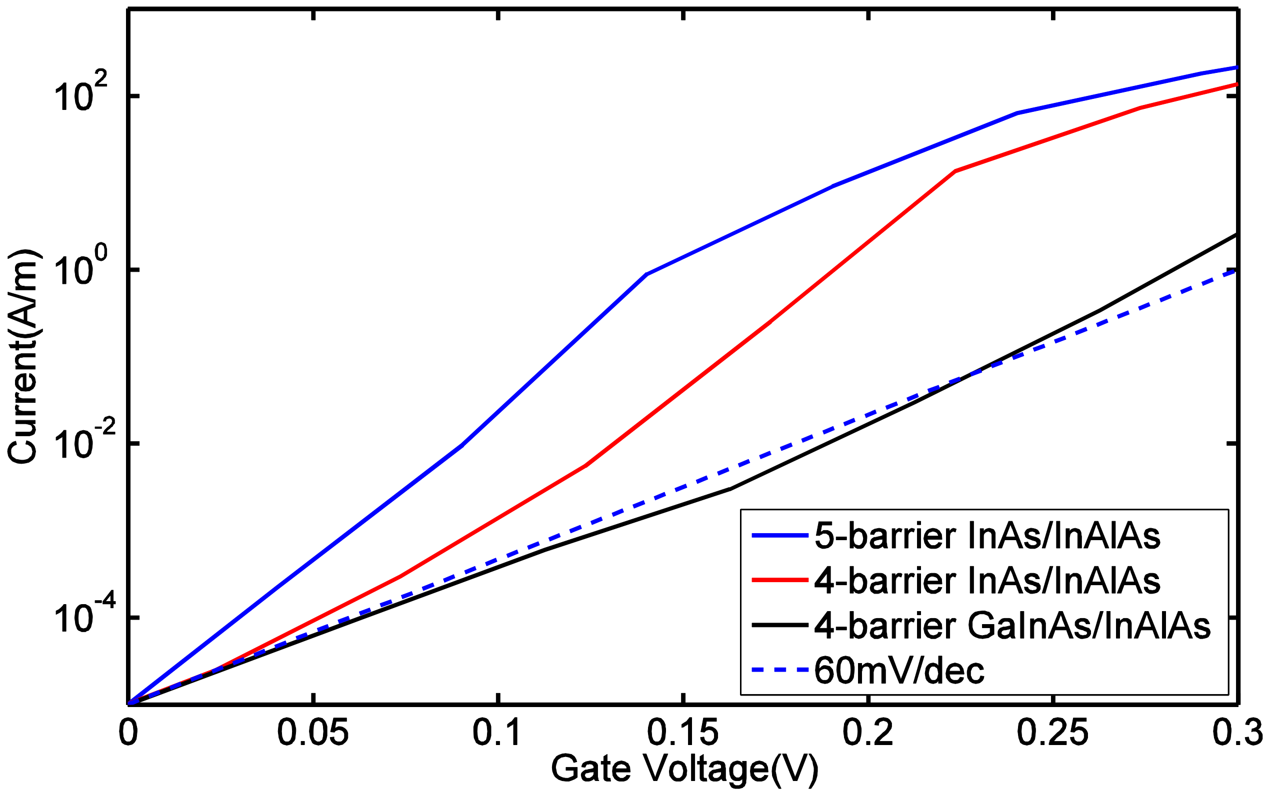
Conclusion: For InAs, we can fit more superlattice periods to fit into the same length.

Effect of number of periods



Transmission in the minigap reaches ~1×10^{-3} in 5 barrier design
The length of InAs/InAlAs superlattice is no longer than InGaAs/InAlAs

Effect of number of periods on Id-Vg



- Using 10^{-5}A/m as I_{off}, the 5-barrier design has the steepest S.S. and biggest I_{on}/I_{off} ratio

Conclusion: InAs/InAlAs superlattice may be more suitable for low power applications than InGaAs/InAlAs superlattice MOSFET.

Effect of biaxial strain

- InAs and InAlAs have different lattice constant.
- If the structure is relaxed, there might be strain in both InAs and InAlAs.

  → E_c and 1st miniband might shift.

- Conclusion: The optimum design might be different from discussed above.

- Currently we don't have strain tight binding parameters for InAlAs.

- Future work: relaxes the structure and then calculates transport.

Summary

- power density increase:
  - » Reducing V_{DD} can solve this problem, but causes increase in I_{off}
- Steep S.S. devices
  - » adding an energy filter can reduce S.S. to steeper than 60mV/dec
  - » TFET has sharp S.S., but limited I_{on}
- Superlattice MOSFET
  - » Nanowire superlattice MOSFETs have both sharp S.S. and big I_{on}, but hard to get high I_{on} per die.
  - » We propose 2D superlattice MOSFET
- Design and simulation
  - » Most of the current carried by small wave vector k_t
  - » Wells and barriers are adjusted for max I_{on}
- Material Optimization
  - » Bigger band offset, InAs/InAlAs gives smaller I_{off}
  - » 5-barrier design gives sharper S.S. and higher I_{on}/I_{off} ratio.

Acknowledgement

Committee members:

Prof. Klimeck, Prof. Rodwell, Prof. Ye

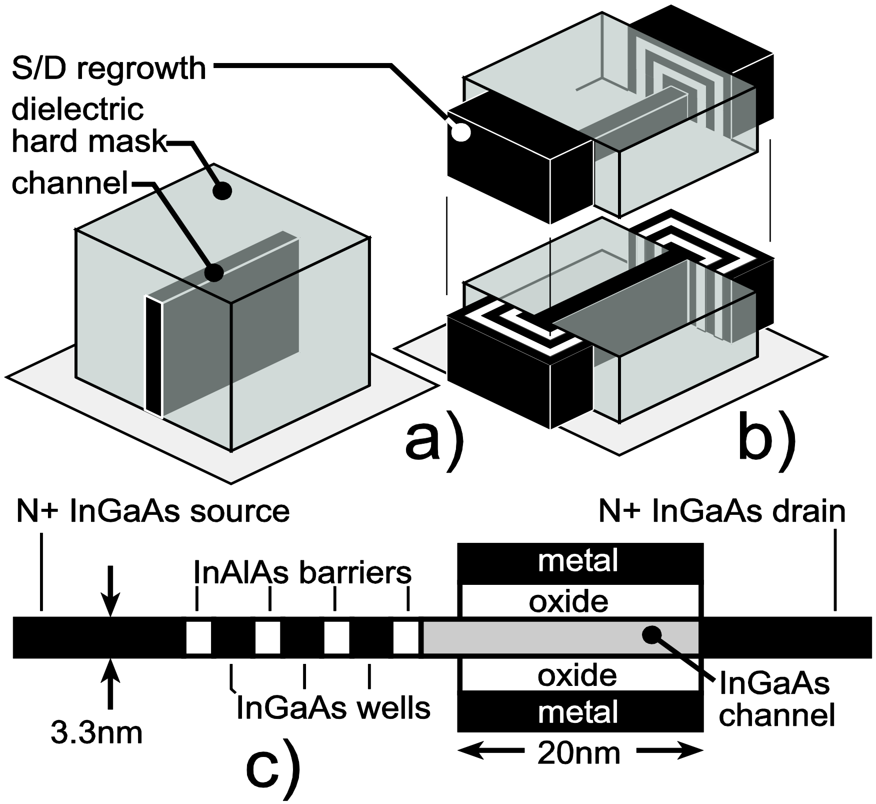
Faculty members and group members:

Prof. Povolotskyi, Prof. Kubis

Bozidar Novakovic, Jun Huang, Zhengping Jiang, Yaohua Tan, Yu He, Xufeng Wang and all other NCN friends for help and thoughtful discussions

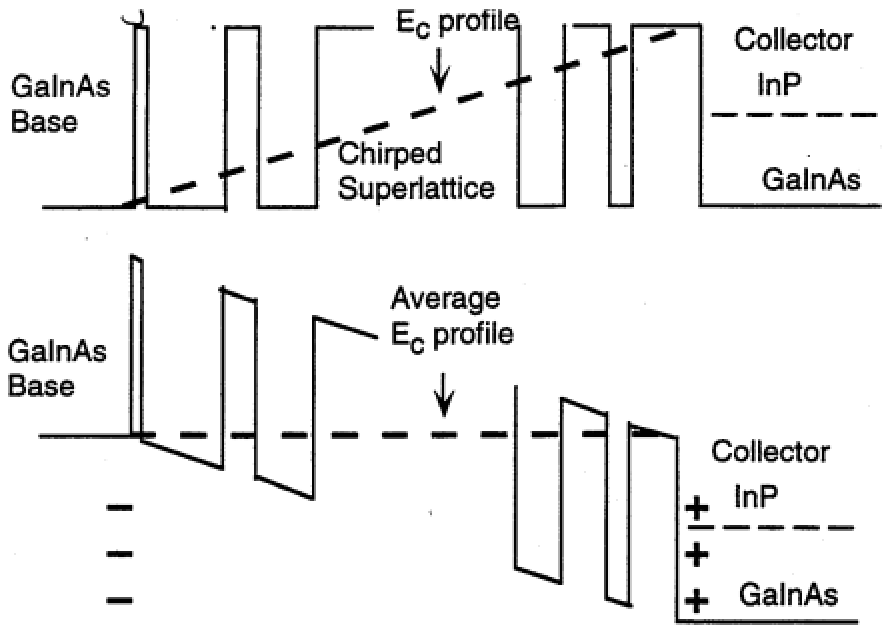
Backup slides

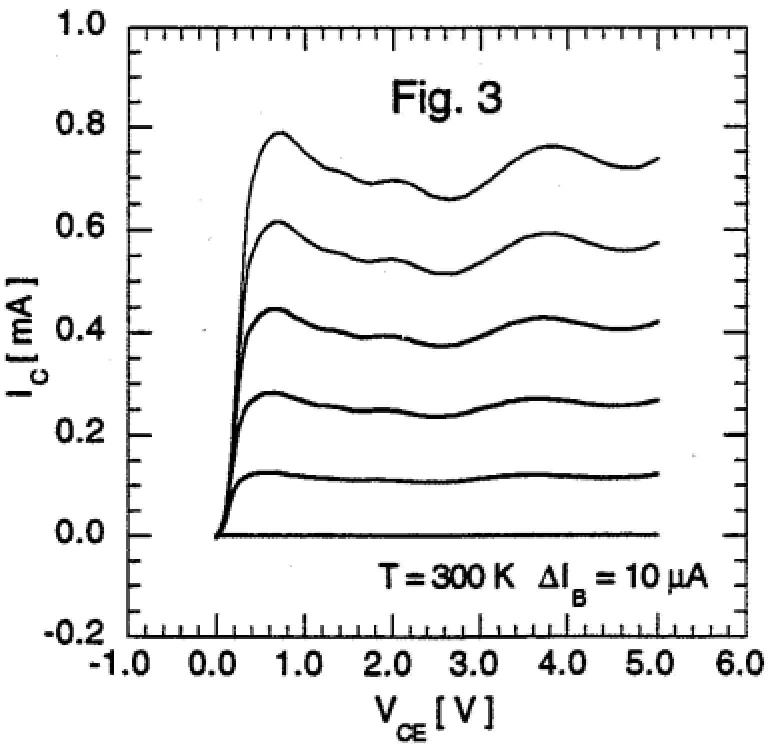
Radical transport vs planar transport



- Radial transport might result in different confinement.
- To maintain the desired transmission, wells and barrier thickness need to be adjusted.

Superlattice in both source & drain

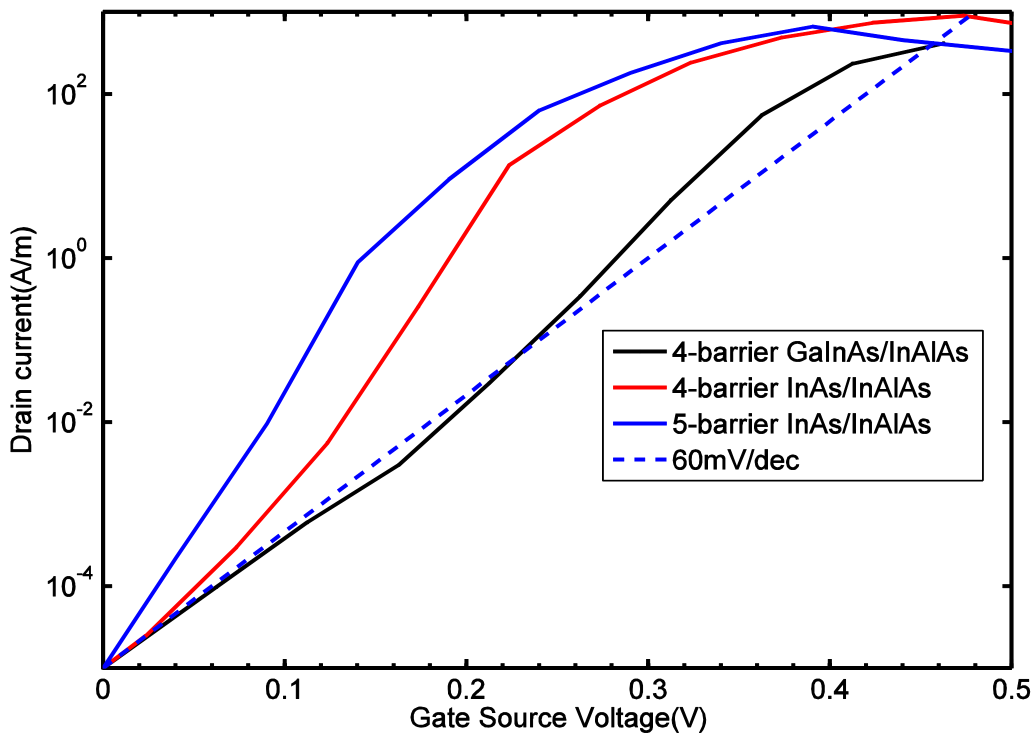




- Output characteristics might be distorted.
- This can be eliminated by growing the source and drain separately.

Nguyen C, Sun H C, Liu T. Chirped superlattice hot electron transistor[C]//Device Research Conference, 1995. Digest. 1995 53rd Annual. IEEE, 1995: 82-83.

Exact design for InAs/InAlAs superlattice



- 4-barrier design:3ml, 5.5ml, 5.5ml and 3ml thick InAlAs barriers, and 6.5ml, 7.5ml 6.5ml thick InAs wells.
- 5-barrier design: 3ml, 5.5ml, 5.5ml, 5.5ml, 5.5ml, 3ml InAlAs barriers, and 6ml, 8ml, 8ml, 6ml InAs wells,