Phonon-limited mobility and injection velocity in n- and p-doped ultrascaled nanowire field-effect transistors with different crystal orientations

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Abstract

In this paper, ultrascaled n- and p-channel Si nanowire field-effect transistors (NW FETs) with [100], [110], and [111] as channel orientations are simulated in the presence of electron-phonon scattering using a sp^3d^5s* tight-binding approach and confined phonon dispersions. The low field mobility, the injection velocity, and the ballisticity of these devices are extracted and compared to n-type InAs and p-type Ge NW FETs. It is found that a [110] Si channel represents the best compromise between high n- and p-type performances in the considered NW FETs.

Introduction

Nanowire (NW) field-effect transistors (FETs) have established themselves as a credible alternative to planar bulk MOSFETs [1-3] at the end of the semiconductor road map. The excellent electrostatic control of ultrascaled Si nanowires FETs allows for a significant reduction of short channel effects, even in devices with a gate length much shorter than 20nm. NW diameters below 5nm are required to obtain the best performances [2].

To support the experimental development of ultrascaled NW FETs, modeling tools that can properly capture the physics of these devices are extremely important. At the nanometer scale, quantum mechanical effects such as energy quantization and tunneling cannot be ignored and must be taken into account by the chosen simulation approach. It is therefore necessary to go beyond classical (drift-diffusion) and semi-classical (Monte-Carlo) models that have been very popular to design bulk MOSFETs.

So far, there have been many quantum mechanical studies of NW FETs, but most of them consider only ballistic transport in the effective mass approximation [4], k·p [5], or tight-binding [6] model. Some successful attempts to include interface roughness [7] and electron-phonon scattering [8] have been demonstrated, but they have almost always been limited to n-type devices with [100] transport and interactions with bulk phonons.

Here, a quantum transport solver based on the tight-binding model and confined phonons is used to investigate the performances of Si NW FETs with a diameter of 3nm. Two important device metrics, the low-field mobility [9] and the injection velocity at the virtual source [10] are computed and analyzed in the presence of electron-phonon scattering in n- and p-doped NW FETs with [100], [110], and [111] transport. Furthermore, the injection velocity of the Si devices is compared to that of a n-type [100] InAs and p-type [110] Ge NW FETs.

The key findings are that electron-phonon scattering severely limits the hole (electron) mobility of Si NW FETs with [100] ([111]) as transport direction and is less significant in [111] p-type and [110] n-type devices. Similarly, the injection velocity reaches its highest values in [111] p-doped and [110] n-doped Si transistors and its lowest values in the [100] p-doped and [111] n-doped NW FETs. A [110] channel appears to be the best choice to build Si NW FETs, but it cannot challenge [100] InAs and [110] Ge in terms of electron and hole injection velocity, respectively.

Approach

The structure of the considered circular gate-all-around NW FETs as well as their cross section, dimensions, doping concentrations, and supply voltages are given in Fig. 1. The simulation approach is described in Ref. [11] for [100] Si NW and is applied here to different crystal orientations and materials. Each atom is described in the sp^3d^5s* tight-binding model, the 3-D Schrödinger and Poisson equations are solved self-consistently on a finite element grid, the phonon modes are confined and computed using a modified Keating model [12]. The lowest subbands of the phonon spectrum of [100], [110], and [111] Si NWs can be seen in Fig. 2. The phonon mode polarization is taken into account in this approach and all the phonon energies are treated at the same level without any distinction between acoustic and optical branches.

Results

Low-field mobility: The method to compute the effective μ_{eff} and phonon-limited μ_{ph} low-field mobility in Si NW FETs is illustrated in Fig. 3. It is based on the dR/dL method [13]. Transistors with a gate length L_g=15, 22.5, and 30nm are simulated at a very low drain-to-source voltage ΔV=1e-5 V and different gate-to-source voltages V_{gs} including electron-phonon scattering. The channel resistance $R(L)$=$\Delta V/I_d(L)$ is extracted from the computed drain current $I_d(L)$. Three gate lengths are considered to make sure that $R(L)$ increases linearly as function of the scattering length L. Note that the

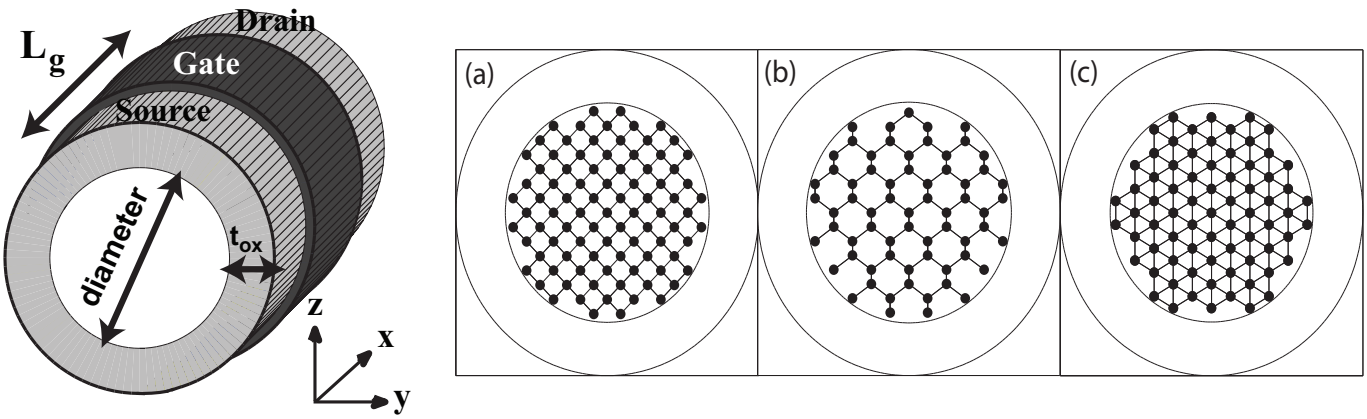

Fig. 1. Schematic view of the Si gate-all-around circular nanowire (NW) field-effect transistors (FETs) considered in this work. The diameter d is equal to 3nm, the source and drain extensions both measure 10nm, the gate length L_g is set to 15nm to calculate injection velocities and varies from 15nm to 30nm to determine the low-field mobility using the dR/dL method [13]. The equivalent oxide thickness (EOT) of all the transistors is 1nm. The transport direction x is aligned with the (a) [100], (b) [110], and (c) [111] crystal axis. The doping of the source and drain extensions amounts to N_D=1e20 cm^{-3} donors for the n-doped devices and N_A=1e20 cm^{-3} acceptors for the p-doped devices. The supply voltage V_{DD} is chosen to be 0.6 V. Note that the OFF-current of the different transistors is not aligned, but they all have the same dimensions and material parameters.

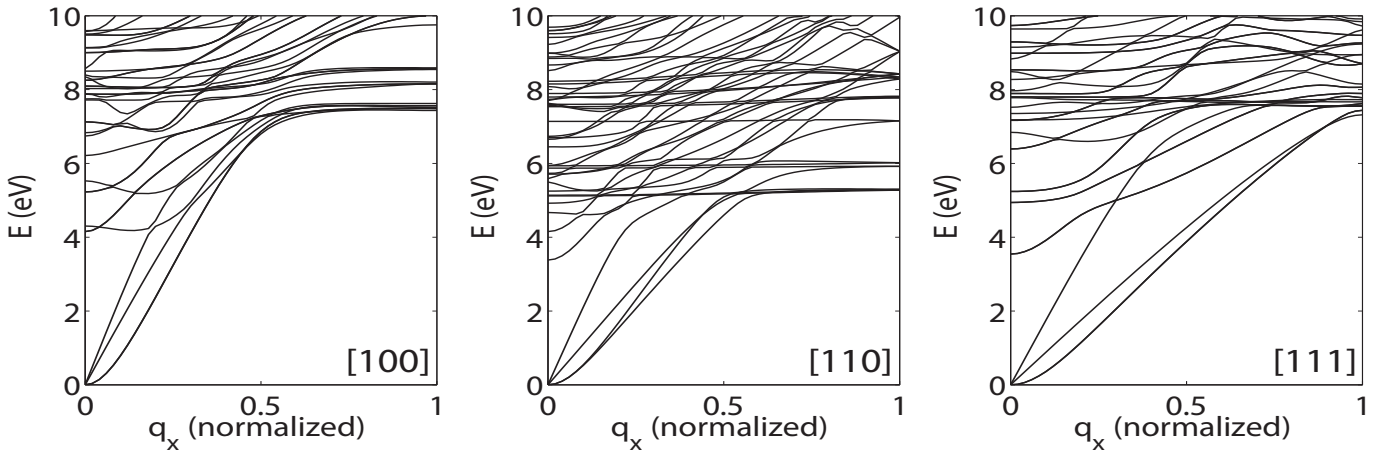

Fig. 2. Confined phonon dispersion of circular Si nanowires with d=3nm and transport along the [100] (left), [110] (center), and [111] (right) crystal axis as function of the wave vector q_x. The phonon bandstructure extends from 0 to 60meV, but only the 10 lowest meV are shown here. The phonon bandstructure calculation is based on a modified empirical Keating model including bond stretching, bond bending, angle-angle, and bond-bond interactions [12].

scattering length L is generally longer than the gate length L_g due to scattering in the source and drain extensions. To calculate L, it is assumed that the total resistance $R(L)$ is given by

$$R(L) \quad = \quad R_0 + R_{ph}(L), \tag{1}$$

where R_0 is the so-called ballistic resistance and is independent of length and $R_{ph}(L)$ is the electron-phonon scattering induced resistance which linearly increases as function of L. Finally, L is determined by making sure that R_0 and the 3 computed $R_{ph}(L)$ all lie on the same line.

The channel resistances $R(L)$ at V_{gs}=0.6 V of p- and n-doped Si nanowires with transport along [100], [110], and [111] are reported in Fig. 4. The derivative ρ_{1D}=$dR(L)/dL$ and the inversion charge P_{inv}/N_{inv} in the middle of the channel are used to compute the phonon limited mobility μ_{ph}

$$\mu_{ph} \quad = \quad \left(\frac{dR(L)}{dL}\right)^{-1} \cdot \frac{1}{q \cdot P_{inv}(N_{inv})}, \tag{2}$$

while the ballistic resistance R_0 and the scattering length L are used to compute the ballistic mobility μ_{bal}

$$\mu_{bal} \quad = \quad \frac{L}{q \cdot R_0 \cdot P_{inv}(N_{inv})}. \tag{3}$$

The effective μ_{eff} mobility is obtained from Matthiessen rule $1/\mu_{eff}$=$1/\mu_{bal}$+$1/\mu_{ph}$. Both μ_{ph} and μ_{eff} are shown in Fig. 5. Since each simulation is computationally very intensive and three simulations per device and gate voltage are required, only two mobilities per transistor have been calculated.

Injection velocity: Figure 6 illustrates how the injection velocity v_{inj} is extracted at the virtual source (top-of-the-barrier) of the NW FETs. After a self-consistent Schrödinger-Poisson

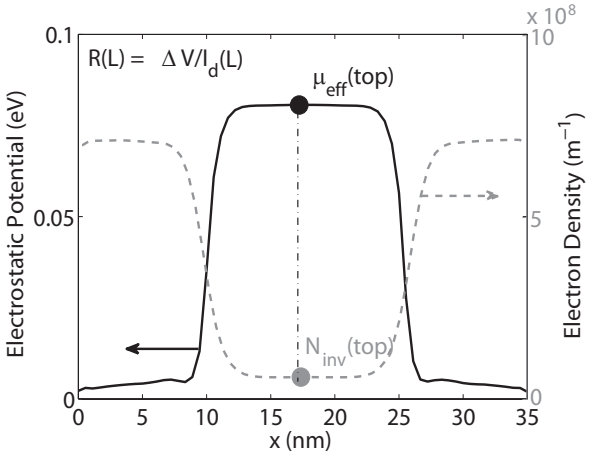

Fig. 3. Illustration of the method to extract the effective low-field mobility μ_{eff} at the top of the barrier in nanowire FETs. The device currents I_d are computed at a very small drain-to-source voltage ΔV=1e-5 V for different channel length L_g (self-consistent calculation). The resulting length-dependent resistance $R(L)$ is calculated as $R(L)$=$\Delta V/I_d(L)$. The corresponding inversion charge at the top of the barrier N_{inv} (P_{inv} for p-type devices) is also extracted.

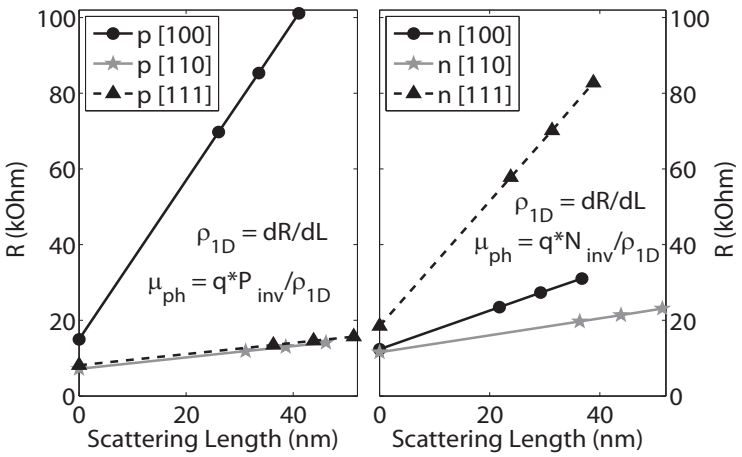

Fig. 4. Length-dependent channel resistance $R(L)$=R_0+$R_{ph}(L)$ of p- (left) and n-doped Si nanowire FETs with transport along [100] (black line with circles), [110] (gray line with stars), and [111] (dashed line with triangles) at V_{gs}=V_{DD}. The ballistic resistance R_0 does not depend on the device length, but the component induced by electron-phonon scattering $R_{ph}(L)$ increases linearly as function of the scattering length L. The phonon limited mobility μ_{ph} is calculated from ρ_{1D}=dR/dL and N_{inv} for electrons and P_{inv} for holes.

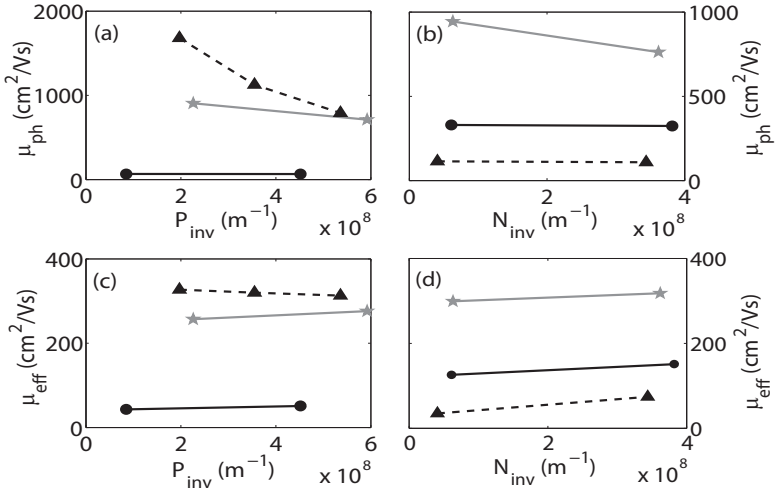

Fig. 5. Phonon-limited μ_{ph} (top) and effective mobility μ_{eff} (bottom) in p- (left) and n-doped (right) Si nanowire FETs with x=[100] (black line with circles), [110] (gray line with stars), and [111] (dashed line with triangles) as function of the inversion charge P_{inv}/N_{inv}. All the devices are simulated at V_{gs}=$\pm$0.4 and $\pm$0.6 V (and -0.5 V for the p-type [111] device). The voltages are then converted to inversion charges in each subplot. The relation $1/\mu_{eff}$=$1/\mu_{bal}$+$1/\mu_{ph}$ is used.

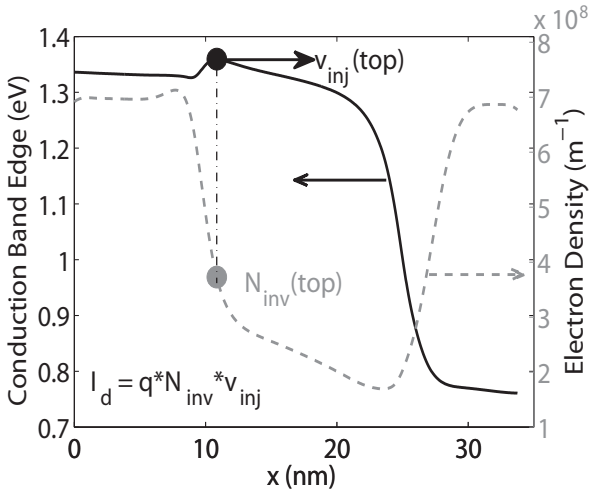

Fig. 6. Illustration of the method to extract the injection velocity v_{inj} at the top of the barrier (virtual source) in nanowire FETs with d=3nm and L_g=15nm. The device current I_d is calculated at V_{ds}=V_{DD} and different V_{gs}. For each gate voltage, the inversion charge P_{inv}/N_{inv} at the virtual source is extracted and the injection velocity is calculated as v_{inj}=$I_d/(q*N_{inv})$ or v_{inj}=$I_d/(q*P_{inv})$.

simulation with electron-phonon scattering, the position of the top-of-the-barrier is determined, the inversion charge at this point N_{inv}/P_{inv} and the drain current I_d are extracted, and the injection velocity v_{inj} is calculated as

$$v_{inj} = \frac{I_d}{q \cdot N_{inv}(P_{inv})}. \quad (4)$$

The results are shown in Fig. 7 (holes) and 8 (electrons). They are compared to the injection velocity of a p-doped [110] Ge and n-doped [100] InAs NW FET. As expected, Ge outperforms any p-channel Si device and InAs is much better than any n-type Si transistor. However, this study does not take into account interface roughness or surface reconfiguration that might be stronger in Ge and InAs when a high-κ layer is formed on their surface. Finally, the Si, Ge, and InAs ballistic factors are shown in Fig. 9 as well as the spectral current of the [110] Si n-FET in Fig. 10.

Results Analysis: A correlation between the low-field mobility and the injection velocity can be clearly observed in the results presented here. In effect, the devices with the highest effective mobility μ_{eff} also exhibit the highest injection velocity v_{inj} and vice versa. As compared to the experimental data reported in Ref. [2], the calculated effective mobility of the [110] n- and p-doped Si NW FETs are slightly

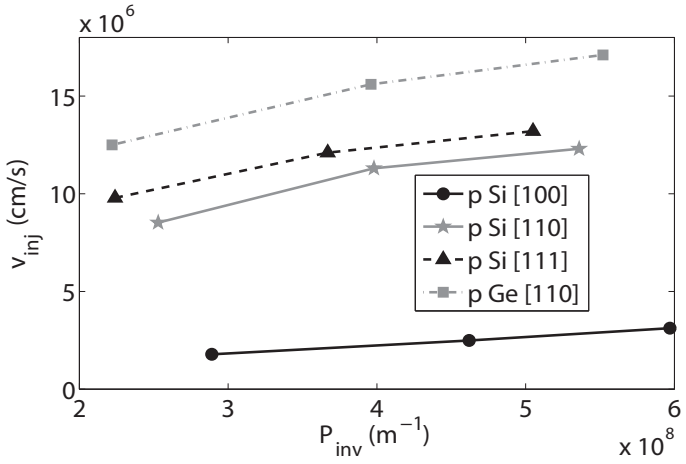

Fig. 7. Hole injection velocity v_{inj} at the virtual source of p-type nanowire FETs (d=3nm, L_g=15nm) in the presence of electron-phonon scattering. Si devices with x=[100] (black line with circles), [110] (gray line with stars), and [111] (dashed line with triangles) are shown as well as a Ge nanowire FET with x=[110] (dashed-dotted line with squares). The injection velocity are calculated at V_{gs}=-0.4, -0.5, and -0.6 V, converted to inversion charges P_{inv}.

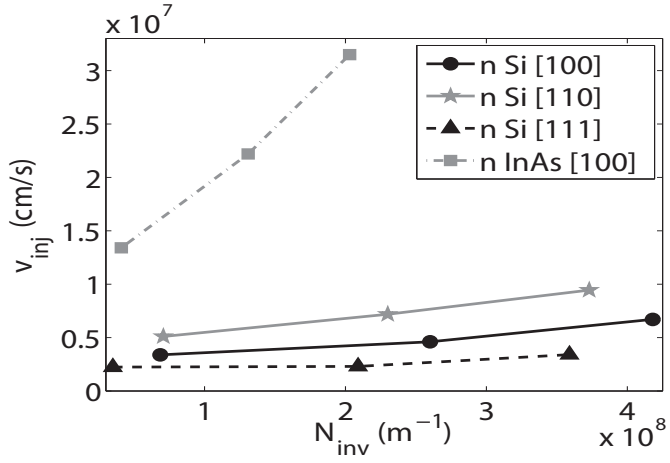

Fig. 8. Electron injection velocity at the virtual source of n-type NW FETs (d=3nm, L_g=15nm) in the presence of electron-phonon scattering. Apart from Si devices with x=[100] (black line with circles), [110] (gray line with stars), and [111] (dashed line with triangles), an InAs device with x=[100] (dashed-dotted line with squares) is also shown for comparison. The gate voltages (0.4, 0.5, and 0.6 V) are converted to inversion charges N_{inv}.

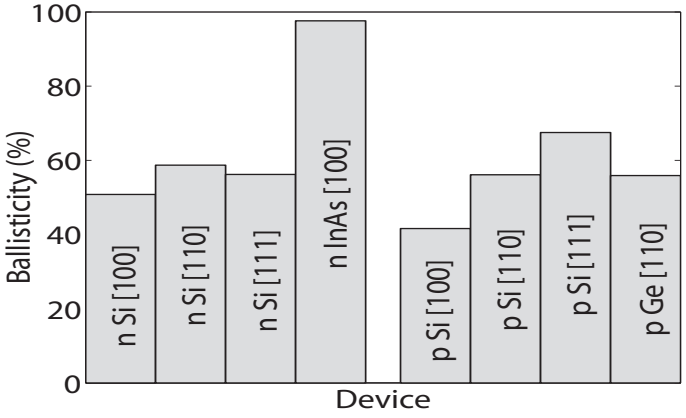

Fig. 9. Ballisticity of the 8 devices simulated in Fig. 7 and 8. The ballisticity is computed as the ratio between the injection velocity $v_{inj,scatt}$ in the presence of electron-phonon scattering and the ballistic injection velocity $v_{inj,bal}$.

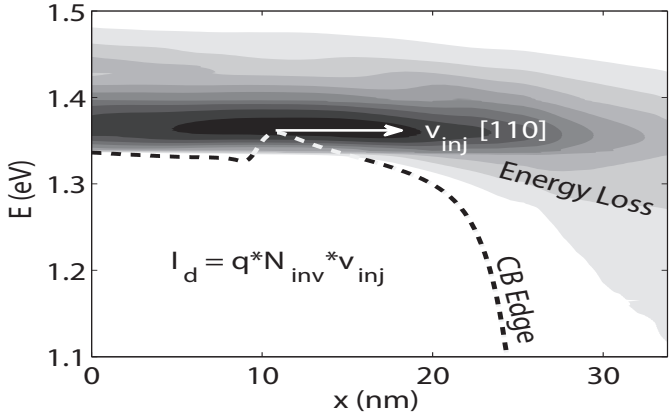

Fig. 10. Energy- and position-resolved current in the n-type Si nanowire FET with x=[110] at V_{gs}=V_{ds}=V_{DD}. Due to electron-phonon scattering, electron looses energy between the source and the drain contact.

higher, but only electron-phonon scattering is considered in these simulations and ideal device structures are assumed.

Conclusion

The low field mobility and injection velocity of n- and p-doped Si NW FETs have been computed in the presence of electron-phonon scattering. As next steps, larger devices will be investigated, interface roughness will be added, and the results will be compared to experimental data.

Acknowledgement

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