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Full-band and atomistic simulation of n- and p-doped double-gate MOSFETs for the 22nm technology node

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Introduction Double-gate metal-oxide-semiconductor field-effect transistors (DG MOSFETs) are promising candidates to replace the conventional planar bulk MOSFETs starting at the 22 nm technology node in 2012. Since the fabrication of novel devices is always a difficult and expensive process physics-based simulation tools can support their development. For example the surface orientation and the transport direction of DG MOSFETs profoundly affect their current characteristics. This issue is addressed in this paper for the three most important configurations experimented in the industry, (a) surface orientation along the (100) crystal axis and transport along the <100> axis, (b) surface along the (110) axis with <110> oriented channel, and finally (c) surface along the (111) axis and transport in the <112> direction. Realistic n- and p-doped Si MOSFETS are treated using an atomistic and full band simulator.

Method To simulate DG MOSFETS as shown in Fig. 1 a two-dimensional full-band Schrödinger-Poisson is sufficient. In effect the third dimension (in plane z-axis) is assumed periodic so that the density-of-states and the transmission through the structure depend on two spectral variables, the injection energy E into the device and the wave vector k_z that models the third dimension. The nearest-neighbor $sp^3d^5s^*$ tight-binding method is used as bandstructure model[1] since it allows a correct description of the electron and hole characteristics. Thus, the anisotropy of the Si bandstructure as illustrated in Fig. 2 is fully taken into account in the transport model. Spin-orbit coupling is neglected since it is weak in Si devices[2]. To calculate the electronic properties of the DG MOSFETs we use an approach equivalent to the Non-equilibrium Green's Function formalism, but more efficient in the case of ballistic transport[3]. The 2D Poisson equation is solved on a finite-element grid by assuming point charges on each atom constituting the transistor structure.

Results We consider n- and p-doped DG MOSFETs designed along the ITRS specifications for the 22 nm technology node[4], i. e. gate length L_g=22 nm, equivalent oxide thickness EOT=1.3 nm (SiO_2 layers), power supply voltage V_{dd}=$\pm$ 1 V. The work function of the metal gate contacts (ϕ_M=4.6 eV) is chosen so that the threshold voltage of the n- (p-) doped transistors lies around 440 (-470) meV. The body thickness of the transistors is set to t_{Si}=4.9 nm so that eventual surface effects and process variations have a limited influence on the simulation results.

The current characteristics $I_d - V_{gs}$ at $V_{ds} = \pm V_{dd}$ of the different DG MOSFETs presented in Fig. 1 are shown in Fig. 3 and some important quantities like ON-current, threshold voltage, and subthreshold swing are summarized in Fig. 4. The ITRS requires a OFF-current of 1e-5 μ A/μ m and a ON-current of 673 μ A/μ m for DG transistors at the 22 nm technology node. The three device structures fulfill these criteria with a considerable margin. However, it is worth noting that in reality the intrinsic ON-current is deteriorate by the source and drain access resistance and the OFF-current is increased by gate leakage mechanisms. These effects are not taken into account in this study.

According to bulk experimental data[5] the (100)/<100> configuration offers the highest (lowest) electron (hole) mobility, followed by (111)/<112>, and finally (110)/<110>. Keeping the dimensions and the threshold voltage constant, the device with the highest mobility exhibits the highest ON-current. Hence the experimental trends are confirmed by our simulation results for the ON-current, as shown in Fig. 3 and 4.

Conclusion In this paper we demonstrated a full-band and atomistic simulator dedicated to DG MOSFETs with arbitrary surface orientation and transport direction. Compared to previous full-band simulations of similar structures[6] we add a more comprehensive bandstructure model ideal for electrons and holes, we are able to simulate devices with realistic dimensions, and we can reproduce experimental trends.

References

[1] T. B. Boykin, G. Klimeck, and F. Oyafuso, Phys. Rev. B **69**, 115201 (2004).
[2] M. Luisier and A. Schenk, to appear in the J. of Comp. and Theor. Nanoscience, March 2008.
[3] M. Luisier, G. Klimeck, A. Schenk and W. Fichtner, Phys. Rev. B **74**, 205323 (2006).
[4] http://www.itrs.net/Links/2006Update/FinalToPost/04_PIDS2006Update.pdf
[5] B. Mereu, C. Rossel, E. P. Gusev, and M. Yang, J. of Appl. Phys. **100**, 014504 (2006).
[6] H. Minari and N. Mori, to appear in the J. of Comp. Elec. (2008), available at http://www.springerlink.com/content/j50664u6ptw10704/.

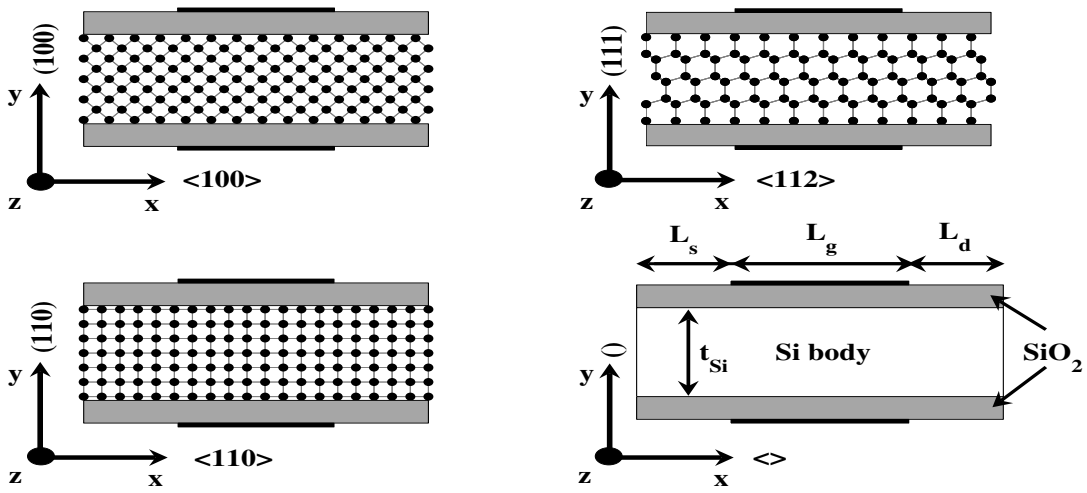

Fig. 1. Schematic view of double-gate field-effect transistors with different surface orientations y labeled () and transport directions x labeled <>. In all the structures the SiO_2 oxide layers (gray) have a thickness t_{ox}=1.3 nm, the Si body t_{Si}=4.9 nm, the gate length L_g measures 22 nm, the source L_s and drain L_d extensions 10 nm. The source and drain are doped with N_D=10^{20} cm^{-3} (N_A=10^{20} cm^{-3}) in n- (p-) MOSFETs.

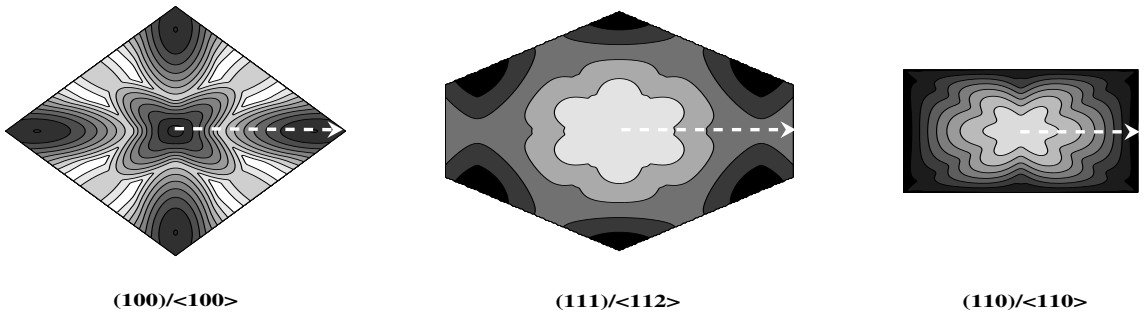

Fig. 2. Contour plot of the bandstructure of the semi-infinite source and drain extensions in the first Brillouin Zone for the (100) surface orientation (left, lowest conduction subband), the (111) surface (middle, highest valence subband), and the (110) surface (right, highest valence subband). White arrows depict the transport directions labeled <>.

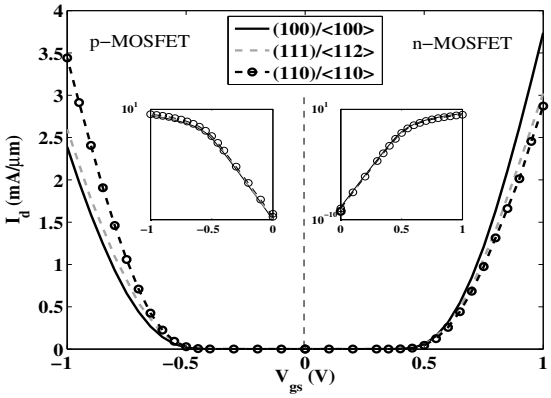

Fig. 3. Linear and logarithmic (insets) transfer characteristics I_d−V_{gs} of p- (left) and n- (right) doped double-gate FETs at $V_{ds} = \pm V_{DD}$. The currents of the three transistor configurations schematized in Fig. 1 are shown. All simulations are done at room temperature.

		(100) <100>	(111) <112>	(110) <110>
n	I_{ON} ($mA/\mu m$)	3.74	3.02	2.87
	I_{OFF} ($\mu A/\mu m$)	1.8e-6	8.5e-7	1.3e-6
	V_{th} (mV)	450	440	440
	S (mV/dec.)	63	64	63
p	I_{ON} ($mA/\mu m$)	2.4	2.6	3.44
	I_{OFF} ($\mu A/\mu m$)	3.6e-7	4e-7	6.8e-7
	-V_{th} (mV)	480	460	470
	S (mV/dec.)	66	62	63

Fig. 4. ON-current I_{ON} (I_{ON}=I_d at V_{ds}=V_{gs}=$\pm V_{DD}$, V_{DD}=1.0 V), OFF-current I_{OFF} (I_{OFF}=I_d at V_{ds}=$\pm V_{DD}$, V_{gs}=0 V), threshold voltage V_{th}, and sub-threshold swing S of the three n- (upper part of the table) and p-doped (lower part) FETs simulated in this work.