

Surface and Orientation dependence on performance of Trigated Silicon Nanowire pMOSFETs

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Abstract— Impact of surface and transport, orientation on hole transport in p-type silicon nanowire MOSFET has been studied using atomistic 10-band sp³s*-SO tight-binding valence band model along with semi classical ballistic top-of-the-barrier approach for tri-gated devices. (100) and (110) surface orientations for <100> and <110> transport orientations were studied. Study of channel current and charge show that, due to heavy hole mass anisotropy, different confinement surfaces impact device performance differently.

Keywords—component; nanowire, p-mosfet, top-of-the-barrier, tight-binding.

I. INTRODUCTION

As channel length (L_c) of Si MOSFETs continues to shrink to smaller dimensions new techniques for transport enhancement are being explored. Traditionally, pMOSFET devices have suffered from lower mobility, hence are considered to be a bottleneck in improving the overall CMOS performance. Hybrid orientation technology (HOT) has been proposed recently for the enhancement of CMOS performance by exploiting (110) surface for hole transport [1]. Neophytos et al. proposed that <110> oriented pMOS channel outperforms <100> in hole transport [2]. The effect of surface vis-à-vis transport direction is the prime motive in this study. Effect of surface and transport directions have been studied in ultra thin body structures [3], however, this is the first study in our knowledge for silicon nanowire (SiNW) pMOSFETs.

II. METHODOLOGY

In this study we have considered a 5 nm × 5 nm cross-section SiNW trigated pMOS device (Fig. 1) for four different surface and transport directions, i.e., A: (100)/<100>, B: (110)/<100>, C: (110)/<110>, D: (100)/<110>. Valence band electronic structure has been calculated using a 10 band sp³s*-SO (including spin orbit coupling) tight binding (TB) model [4] coupled self-consistently to a 2D Poisson equation solver. Upon convergence, transport properties are calculated using the semi-classical ballistic top-of-the-barrier (ToB) approach [5]. It has been shown that ToB can faithfully replicate results of a full 3D quantum simulation for $L_c \geq 4$ times the SiNW width [6]. Hence, our results are valid for $L_c \geq 20$ nm. The source and drain regions are p-type doped at $1e20/cm^3$ with intrinsic channel. $V_{DS} = -0.6V$ is applied for all I_{DS} - V_{GS} sweeps. Threshold voltage (V_t) was matched for all the simulations. Effective oxide thickness (EOT) was taken to be 0.5 nm. Surface atoms were H passivated.

III. RESULTS & DISCUSSION

In nanowires, due to confinement valence bandstructure becomes highly warped and non-parabolic. Due to heavier confinement mass heavy holes (HH) have smaller sub-band energy, whereas, light holes (LH) have lighter confinement mass resulting in higher sub-band energy. Hence it should be safe to say that lower sub-bands have more HH characteristics. HH quantization mass (m^*) along <110> ($m^* = 3.78$) is much higher than <100> ($m^* = 0.277$) (m^* obtained using Bandstructure Lab V2.0 on nanoHUB.org [7]). This is reflected in the preferential charge movement towards (110) surface (Fig. 2 & 3). Table I lists the m_{dos} for the four devices extracted from HH bandstructure.

In the tri-gated devices under study each have different number of (110) surfaces under the gate. (110)/<100> exhibits maximum gate capacitance and 1D inversion charge density since all three (110) surfaces are under gate control (Fig. 4 & 5). Fig. 6 shows the 1D E-k diagrams for the four devices. Both <110> oriented devices have same E-k due to exactly same crystal symmetry. Extracted transport effective masses (m_{trans}) are listed in Table I. <110> orientation has lighter m_{trans} , the effect of which is reflected in higher injection velocity ($V_{inj} \sim 1/\sqrt{m_{trans}}$) for <110> (Fig. 7).

From ballistic theory, the channel current (I_{bal}) is [5],

$$I_{bal} = q \times N_{inv} \times V_{inj} \quad (1)$$

where, q is charge of an electron, N_{inv} is the inversion electron density and V_{inj} is the injection velocity. I_{DS} - V_{GS} curves in Fig. 8 show that <110> devices are much superior to <100> devices. Normalized plot in Fig. 9 shows that although B has maximum N_{inv} (5% higher), V_{inj} for <110> (C&D) are about 70-80% higher. V_{inj} is the dominant term in (1) which determines the relative performance among the devices. We find that D exhibits best performance owing to two (110) surfaces under gate and <110> transport direction.

At high EOT values we observe that devices with same transport direction approach same I_{on} (Fig.10). Surface effects in holes can better be exploited by reducing EOT, which gives an added incentive to use high-k dielectrics [8]. However, it can be inferred from Fig. 10 transport orientation effect still dominates over surface effect.

IV. CONCLUSIONS

Surface and transport orientations play important role in hole device performance. Transport direction is much more dominant effect than surface. Lighter transport mass for <110>

results in better performance over $\langle 100 \rangle$. Surface effects can be better exploited by using thinner EOT.

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TABLE I. EFFECTIVE MASSES FOR HOLES IN DIFFERENT PMOS DEVICES

pMOS type	Effective mass	
	$m^*(\text{transport}) [m_0]$	$m^*(\text{dos}) [m_0]$
(100)/ $\langle 110 \rangle$	0.15	1.03
(110)/ $\langle 110 \rangle$	0.15	1.03
(110)/ $\langle 100 \rangle$	0.30	3.78
(100)/ $\langle 110 \rangle$	0.34	0.27

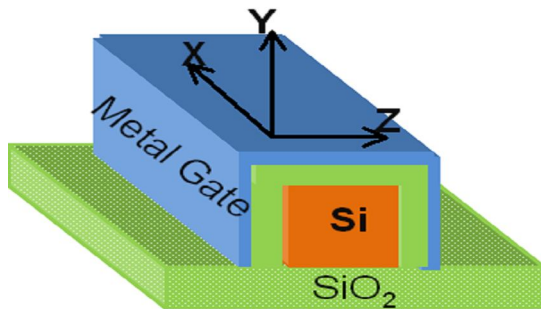


Fig.1. Device schematic of a trigated Silicon Nanowire (SiNW) MOSFET. X is the transport direction. Y and Z represent the two confined directions of the wire. Silicon nanowire has wrapped all around oxide.

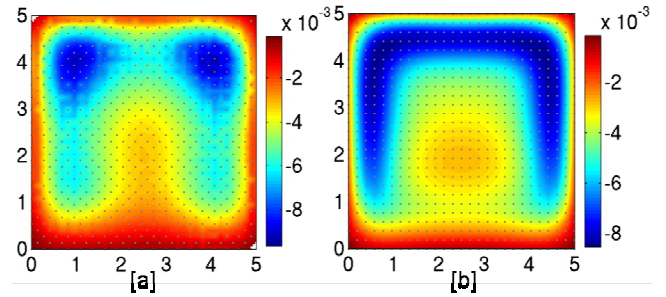


Fig. 2. Spatial distribution of holes in the cross-section of SiNW under $V_{GS} = -0.9V$ and $V_{DS} = -0.6V$ for [a] (100)/ $\langle 100 \rangle$ [b] (110)/ $\langle 100 \rangle$. Hole density is in #/nm (1D) obtained at each atomic location.

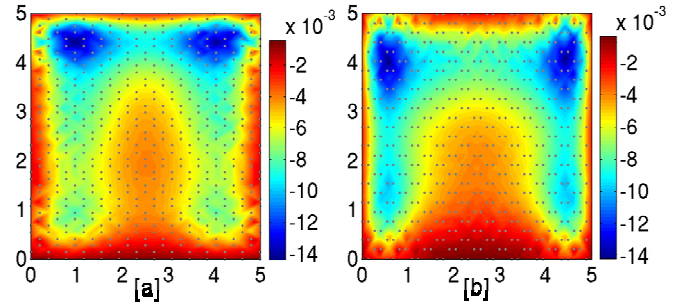


Fig. 3. Spatial distribution of holes in the cross-section of SiNW under $V_{GS} = -0.9V$ and $V_{DS} = -0.6V$ for [a] (110)/ $\langle 110 \rangle$ [b] (100)/ $\langle 110 \rangle$. Hole density is in #/nm (1D) obtained at each atomic location.

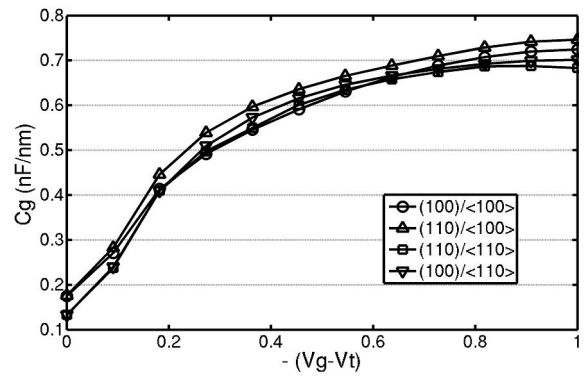


Fig. 4. Gate capacitance (C_g) for the 4 devices under study. (110)/ $\langle 100 \rangle$ device shows maximum C_g since all the four surfaces are (110).

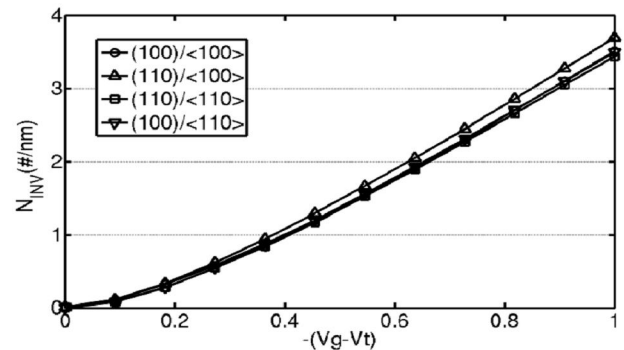


Fig. 5. 1D inversion density of holes in the four devices under study. (110)/ $\langle 100 \rangle$ device has maximum charge density since it has maximum (110) surfaces.

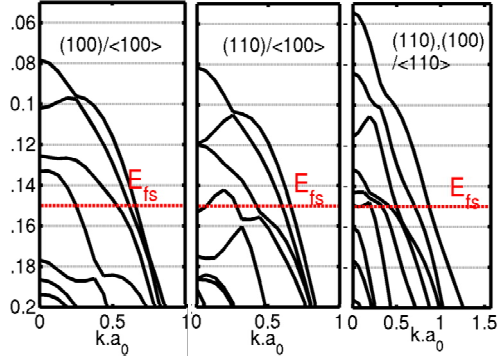


Fig. 6. 1D valence band dispersion curves for the four devices under study. (110)/<110> and (100)/<110> have same EK since they have same crystal symmetry. E_{fs} represents the position of the source fermi level.

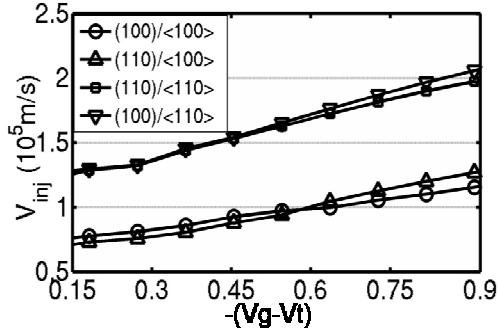


Fig. 7. Injection velocity for 4 devices under study. Devices with <110> transport orientation have lighter transport mass and hence have higher injection velocity compared to <100>.

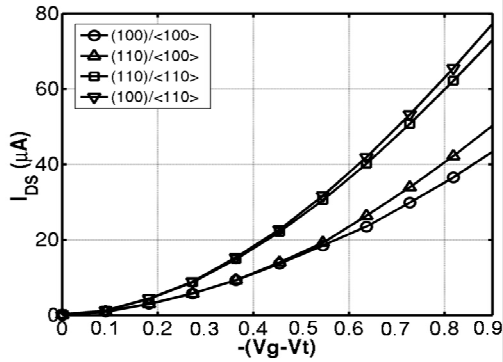


Fig. 8. I_{DS} - V_{GS} for 4 devices under study. Devices with <110> transport orientation have higher channel current compared to <100>.

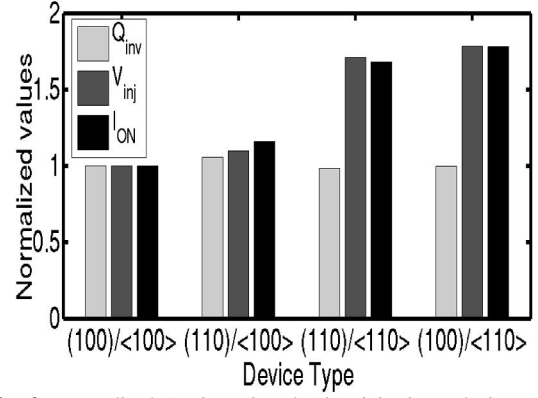


Fig. 9. Normalized 1D inversion density, injection velocity and I_{on} for the four devices with respect to (100)/<100>.

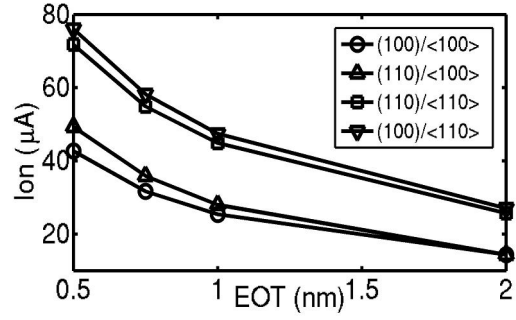


Fig. 10. Variation of I_{on} in the four devices with varying EOT. Thinner EOT makes I_{on} higher for devices with more (110) surfaces. I_{on} for <110> devices is always higher than <100> devices at same EOT.