Investigation of $\text{In}_x\text{Ga}_{1-x}\text{As}$ Ultra-Thin-Body Tunneling FETs using a Full-Band and Atomistic Approach

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***Abstract*—Using a 2-D, full-band, atomistic, quantum mechanical simulator based on the $sp^3d^5s^*$ tight-binding method with spin-orbit coupling, we investigate the performances of single- and double-gate relaxed $\text{In}_x\text{Ga}_{1-x}\text{As}$ $p-i-n$ ultra-thin-body (UTB) tunneling field-effect transistors (TFETs) with 20nm to 50nm gate lengths. The ON-current, OFF-current leakage, and subthreshold slope (SS) properties are analyzed as function of the In concentration in 5nm thick structures. We find (i) that devices with a high In concentration allow more ON-current, but suffer from higher OFF-currents and lower SS, (ii) that double-gate devices perform better than single-gate ones, and (iii) that a longer gate length reduces the source-to-drain tunneling leakage and the OFF-current of the UTB TFETs.**

I. INTRODUCTION

Tunneling field-effect transistors (TFETs) are expected to help reduce the power consumption of integrated circuits due to their potential low OFF-currents and subthreshold swing (SS) below 60 mV/dec at room temperature [1]. In effect the voltage swing required to switch TFETs from their OFF to their ON state is not limited by thermionic emission as in conventional MOSFETs, but depends on the band-to-band tunneling probability of valence band electrons, so that SS can go below 60 mV/dec.

Recent experimental works have shown that TFETs with a SS lower than 60 mV/dec can be realized using either carbone nanotube or silicon-on-insulator structures [2], [3]. A SS of 40 mV/dec and 52.8 mV/dec were reported, respectively. However, both devices exhibit low ON-currents so that alternative channel materials, such as graphene nanoribbons [4], Si/SiGe heterostructures [5], or III-V compound semiconductors [6], are investigated to increase the ON-current.

The small electron and hole effective masses of InAs or GaAs could enable large band-to-band tunneling in properly designed $p-i-n$ transistor structures. Computer aided design can help reduce the fabrication costs of such devices. For that purpose we use a quantum mechanical simulation tool that goes beyond the Wentzel-Kramers-Brillouin (WKB) approximation[7] that is essentially one-dimensional and ignores quantization and confinement effects. Hence, we present a 2-D, atomistic, full-band study of single- (SG) and double-gate (DG) $p-i-n$ ultra-thin-body TFETs based on relaxed $\text{In}_x\text{Ga}_{1-x}\text{As}$ with an indium concentration x ranging from 0 to 1. We demonstrate under which conditions these devices could offer large ON-currents and steep SS.

II. METHOD

We have developed an atomistic, full-band quantum transport simulator based on the nearest neighbor $sp^3d^5s^*$ tight-binding method with spin-orbit coupling and self-consistent solutions of 2-D Schrödinger and Poisson equations. In the case of ballistic transport we use a Wave Function (WF) approach which is numerically identical to the Non-equilibrium Green's Function (NEGF) formalism, but computationally much more efficient [8]. It consists in solving sparse linear systems of equations "Ax=b" instead of matrix inversion problems as in NEGF.

Each atom composing the active region of the simulation domain is represented by a matrix of size t_B=20. The total Hamiltonian matrix is then block tri-diagonal with sparse blocks whose size depends on the number of atoms in each atomic layer. The insulator layers that separate the III-V channel from the gate contacts do not participate to the transport calculation, are modeled as fictitious materials with an infinite band gap, and are solely characterized by their relative dielectric constant ϵ_R in the Poisson equation.

Carrier and current densities are obtained by injecting electrons and holes into the device structures from the source and drain contacts at different energies and wave vectors. The calculation of the electrostatic potential is self-consistently coupled to that of the charge density. Electrons that tunnel from the valence band of the p-doped side of the device into the conduction band of the n-doped side contribute to both the current and charge densities. The solution of Schrödinger and Poisson equations are massively parallelized to reduce the simulation time [9].

Our tool models quantization effects as well as the valence and conduction bands of various semiconductor materials simultaneously. The band gap and effective masses of InAs and GaAs are correctly reproduced only if spin-orbit coupling is included in the calculation. The neglection of this effect leads to an increase of the band gap and of the electron effective mass so that the band-to-band tunneling probability is underestimated.

Furthermore, the tight-binding model automatically accounts for the imaginary band dispersion that exists in the energy band gap. Band-to-band tunneling processes are therefore accurately modeled for direct gap materials even in the

Parameter	GaAs	InAs	B_{InAs_GaAs}
E_{sa}	-5.5004	-5.5004	0.0
E_{pa}	4.1511	4.1511	0.0
E_{sc}	-0.2412	-0.5819	-0.2040
E_{pc}	6.7078	6.9716	0.2621
E_{s*a}	19.7106	19.7106	0.0
E_{s*c}	22.6635	19.9414	-1.4772
E_{da}	13.0317	13.0317	0.0
E_{dc}	12.7485	13.3071	0.3427
$ss\sigma$	-1.6451	-1.6944	-0.0262
$s^*s^*\sigma$	-3.6772	-4.2104	-0.2850
$s_a^*s_c\sigma$	-2.2078	-2.4267	-0.0545
$s_as_c^*\sigma$	-1.3149	-1.1599	-0.1022
$s_ap_c\sigma$	2.6649	2.5982	-0.0667
$s_cp_a\sigma$	2.9603	2.8094	-0.1488
$s_a^*p_c\sigma$	1.9765	2.0677	0.0911
$s_c^*p_a\sigma$	1.0275	0.9373	-0.0902
$s_ad_c\sigma$	-2.5836	-2.2684	0.3152
$s_cd_a\sigma$	-2.3206	-2.2931	-0.0131
$s_a^*d_c\sigma$	-0.6282	-0.8994	-0.2711
$s_c^*d_a\sigma$	-0.1332	-0.4890	0.3556
$pp\sigma$	4.1508	4.3106	-0.1355
$pp\pi$	-1.4274	-1.2890	0.1185
$p_ad_c\sigma$	-1.8743	-1.7314	0.1210
$p_cd_a\sigma$	-1.8896	-1.9784	0.0876
$p_ad_c\pi$	2.5293	2.1889	-0.0979
$p_cd_a\pi$	2.5491	2.4560	-0.0931
$dd\sigma$	-1.2700	-1.5846	0.0327
$dd\pi$	2.5054	2.7179	0.2117
$dd\delta$	-0.8517	-0.5051	0.3464
λ_a	0.1723	0.1723	0.0
λ_c	0.0218	0.1312	0.0

TABLE I
TIGHT-BINDING DIAGONAL, SPIN-ORBIT, AND TWO-CENTER INTEGRAL PARAMETERS FOR GAAS AND INAS (BOTH TAKEN FROM REF. [10]). THE FOURTH COLUMN CONTAINS THE REQUIRED BOWING PARAMETERS B_{InAs_GaAs} TO OBTAIN INGAAS. ALL PARAMETERS ARE IN EV.

absence of scattering.

III. PARAMETRIZATION

Tight-binding parameters for InAs and Gas can be found in the literature [10], but there is no specific parameters for relaxed In$_x$Ga$_{1-x}$As. As a first approximation, the InAs and GaAs parameters can be linearly interpolated to obtain InGaAs. The band gap and effective masses are not correctly reproduced in this case as pointed out in Ref. [11] and shown in Fig. 1 and 2. A better description of In$_x$Ga$_{1-x}$As is possible by introducing bowing parameters B_{InAs_GaAs} for each on-site and two-center integral tight-binding parameters

$$P_{In_xGa_{1-x}As} = x \cdot P_{InAs} + (1-x) \cdot P_{GaAs} + x \cdot (1-x) \cdot B_{InAs_GaAs}. \quad (1)$$

The values of the different B_{InAs_GaAs} are listed in Table I and are optimized to ensure the correct reproduction of the widely accepted band gaps and effective masses of the ternary alloys [12] as illustrated in Fig. 1 and 2. Hence, no atomic disorder is taken into account in this work.

In fitting the B_{InAs_GaAs} we impose the condition that the parameters $P_{In_xGa_{1-x}As}$ are larger than the minimum of P_{InAs} and P_{GaAs} and smaller than the maximum of P_{InAs} and P_{GaAs} for all the values of x [13].

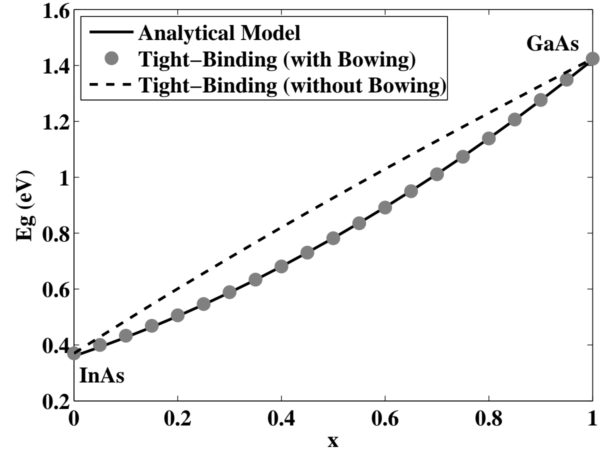

Fig. 1. Band gap of In$_x$Ga$_{1-x}$As at room temperature as function of the In concentration x. The solid line is the analytical model from Ref. [12], the dots the results from tight-binding with the bowing parameters in Fig. I, while the bowing parameters are ignored to obtain the dashed line (only linear interpolation of the InAs and GaAs parameters).

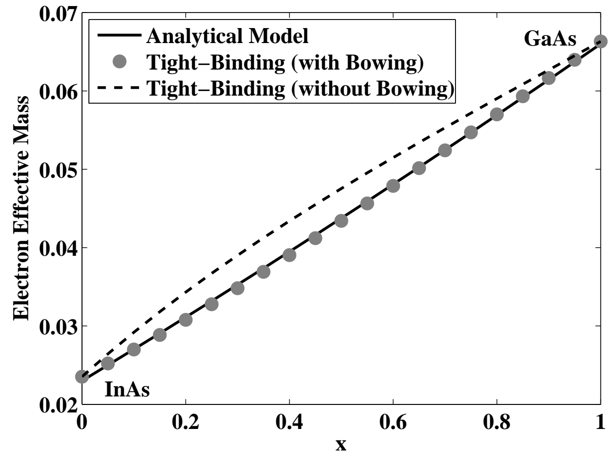

Fig. 2. Electron effective mass of In$_x$Ga$_{1-x}$As at room temperature as function of the In concentration x. The same plotting convention as in Fig. 1 are used.

IV. RESULTS

We consider single- and double-gate In$_x$Ga$_{1-x}$As $p-i-n$ ultra-thin-body (UTB) TFETs structures as depicted in Fig. 3. The source and drain regions measure 20nm and are highly doped with a concentration N_A=5e19 cm^{-3} and N_D=5e19 cm^{-3}, respectively. The body thickness t_{body} is set to 5nm, the insulator layer separating the gate from the channel to t_{ox}=1nm with a relative dielectric constant ϵ_R=12.7. The transport direction of the channel is aligned with the <100> crystal axis, the surface orientation is along (100).

We start with a gate length of L_g=20nm to attempt to fulfill the future ITRS requirement. The number of atoms taken into

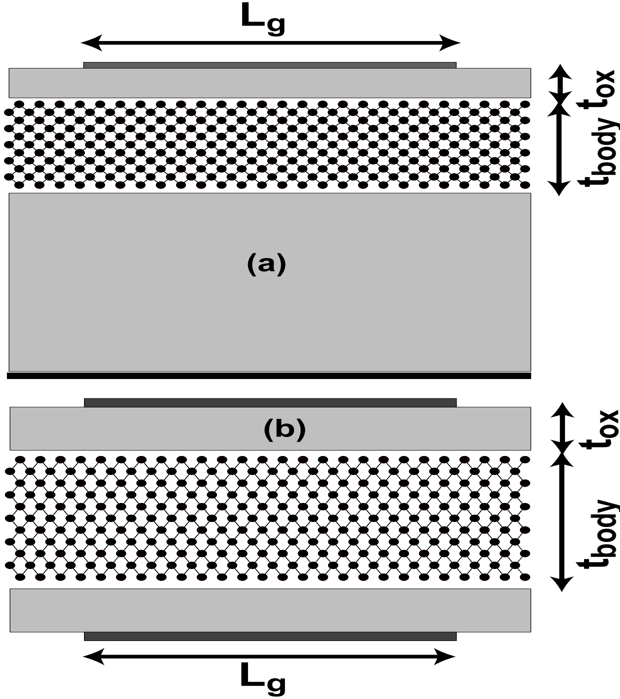

Fig. 3. TFET structures. (a) Single-Gate and (b) Double-Gate $p-i-n$ UTBs with t_{body}=5nm, t_{ox}=1nm, and 20nm long p-doped (N_A=5e19 cm^{-3}) source and n-doped (N_D=5e19 cm^{-3}) drain extensions.

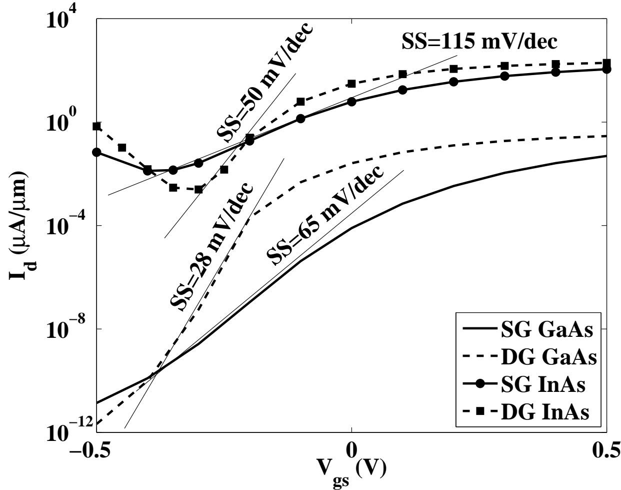

Fig. 4. Transfer characteristics $I_d - V_{gs}$ at V_{ds}=0.2 V of GaAs and InAs single- and double-gate TFETs with a gate length L_g=20nm. The subthreshold swing SS of the four TFETs is reported.

account in the Schrödinger equation ranges from 6732 for the InAs structure to 7632 for the GaAs TFET resulting in Hamiltonian matrices of size 134640 and 152640, respectively.

Single-gate structures are easier to manufacture than double-gate ones. However, due to a poorer electrostatic control [6], they exhibit larger SS, more than 60 mV/dec, and lower ON-currents than DG devices as can be seen from Fig. 4 to Fig. 7,

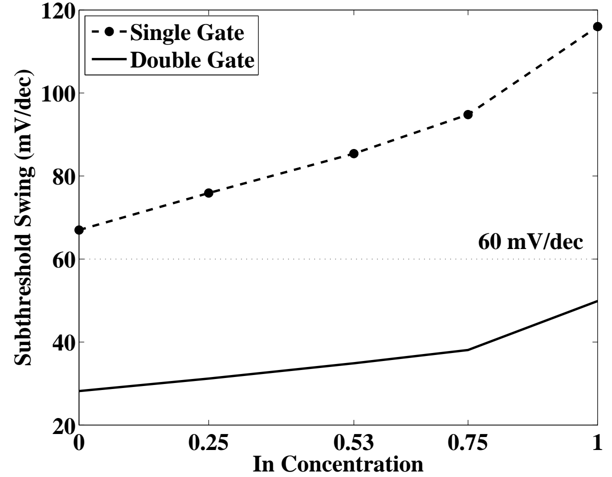

Fig. 5. Subthreshold swing SS of single- (dashed line with symbols) and double-gate (solid line) $In_xGa_{1-x}As$ TFETs with an indium concentration ranging from x=0 to x=1 and L_g=20nm.

irrespective of the indium concentration in the channel.

The poor SS of SG TFETs is mainly due to source-to-drain tunneling (STDT) leakage through the gate potential barrier as indicated in Fig. 7. This effect is almost suppressed by a better electrostatic control in DG TFETs that makes the source-to-drain barrier effectively longer than in SG TFETs. It results SS values ranging from 28 mV/dec for GaAs to 50 mV/dec for InAs as compared to 65 mV/dec and 115 mV/dec in SG devices.

The larger ON-current of DG TFETs is also a consequence of the better electrostatic control provided by two gates instead of a single one. The electric field at the $p-i$ interface becomes larger in DG structures so that the width of the tunneling barrier decreases and electrons can more efficiently flow from the valence band of the source to the conduction band of the drain as shown in Fig. 7.

The channels with a smaller indium concentration suffer less from STDT leakage and have steeper SS because of their higher band gap and larger tunneling effective mass, but they are characterized by lower ON-currents for the same two reasons. Since a high ON-current is desired, InAs-based devices should be promoted. They can reach ON-currents in the order of 130 and 210 $\mu A/\mu m$ for SG and DG, respectively. Note that such ON-current values can only be achieved if the gate voltage swing from the OFF to the ON transistor state amounts to about 0.4 V while the supply voltage V_{DD} and the drain-to-source voltage V_{ds} are set to 0.2 V. Increasing V_{ds} to 0.4 V is not an appropriate solution since V_{bi}+V_{ds} the built-in potential of the $p-i-n$ diode plus the drain-to-source voltage becomes larger than $2{\cdot}E_g$ (2 times the band gap of the channel), which causes large OFF-current and strongly increases the ambipolar behavior of the TFETs [6]. Simultaneously reducing the doping of the n-doped drain and increasing V_{ds} appears more promising.

Also, to avoid the fabrication complexity of DG structures

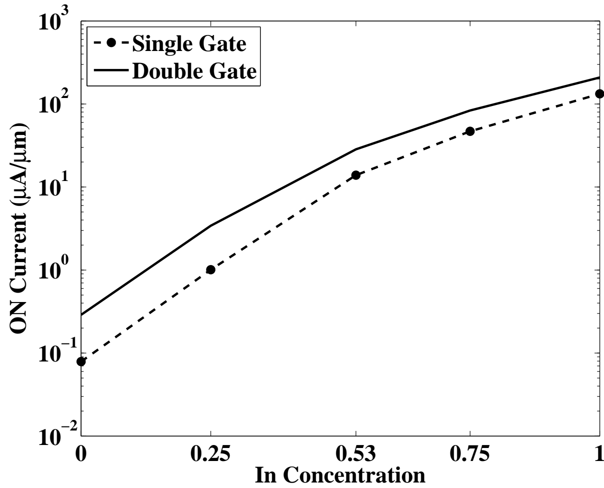

Fig. 6. ON-current (I_d at V_{gs}=0.6 V and V_{ds}=0.2 V) of single- and double-gate (solid line) $In_xGa_{1-x}As$ TFETs. Same label conventions as in Fig. 5.

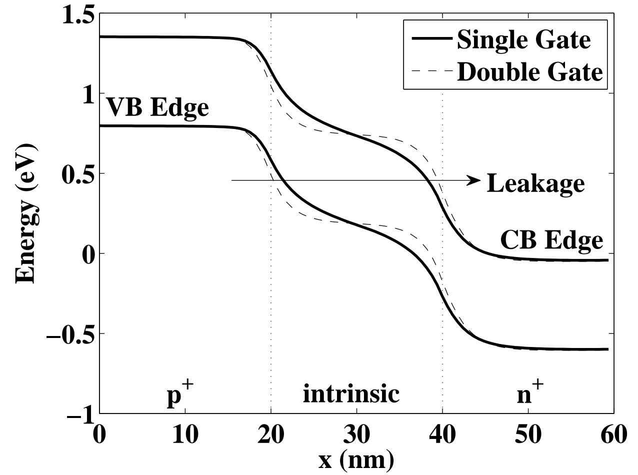

Fig. 7. Conduction and valence band edges of a single- (solid lines) and double-gate (dashed lines) InAs TFET along its transport direction at V_{ds}=0.2 V and V_{gs}=-0.3 V. The leakage path of the tunneling current through the gate potential barrier is indicated.

while minimizing SS the gate length of single-gate InAs devices can be extended to 40nm. At this size STDT completely disappears as SS becomes independent of the gate length as shown in Fig. 8. However, increasing the gate length of devices that might play a role in 2 to 5 years goes in the opposite direction of the ITRS requirement.

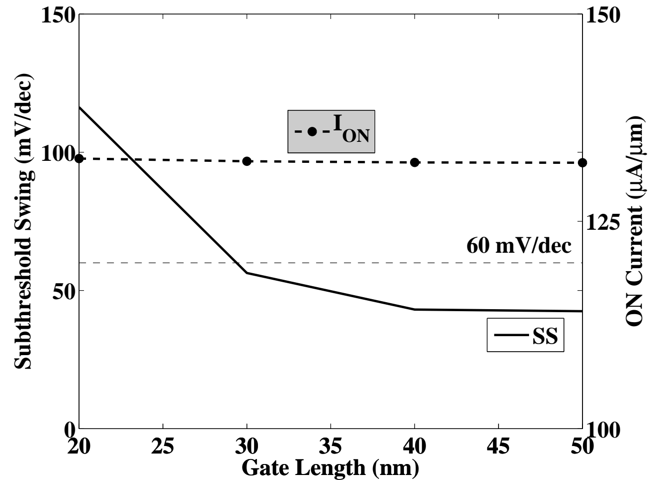

Fig. 8. Subthreshold swing (left axis, solid line) and ON-current (right axis, dashed line with symbols) of single-gate InAs TFETs with gate lengths L_g comprised between 20nm and 50nm.

V. Conclusion

Ultra-thin-body $In_xGa_{1-x}As$ TFETs with single- and double-gate configurations have been modeled with a full atomistic device simulation tool. We have found that (1) DG structures offer higher ON-current and steeper SS, (2) SS improves with decreasing indium concentration in the channel while ON-current follows the opposite trend, and (3) SS can be reduced by increasing the gate length of InAs SG FETs. However, the replacement of conventional Si MOSFETs by III-V TFETs will only be achieved if the TFET ON-current can further be increased by design optimization like the doping of the p, i, and n regions, by introducing gate under- or overlap, or by including heterostructures.

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References

[1] Q. Zhang, W. Zhao and, A. Seabaugh, *IEEE Elec. Dev. Lett.*, 27, p. 297, 2006.
[2] J. Appenzeller, Y.-M. Lin, J. Knoch, and Ph. Avouris, *Phys. Rev. Lett.* 93, 196805, 2004.
[3] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. King Liu, *IEEE Elec. Dev. Lett.*, 28, p. 743, 2007.
[4] Q. Zhang, T. Fang, H. Xing, A. Seabaugh, and D. Jena, *IEEE Elec. Dev. Lett.*, 29, p. 1344, 2008.
[5] K. K. Bhuwalka, J. Schulze, and I. Eisele, *Jpn. J. Appl. Phys.*, 43, p. 4073, 2004.
[6] M. Luisier and G. Klimeck, *IEEE Elec. Dev. Lett.*, 30, p. 602, 2009.
[7] J. Knoch, S. Mantl and J. Appenzeller, *Solid-State Electronics*, 51, p. 572, 2007.
[8] M. Luisier, G. Klimeck, A. Schenk, and W. Fichtner, *Phys. Rev. B*, 74, 205323, 2006.
[9] M. Luisier and G. Klimeck, *Proceedings of the 2008 ACM/IEEE conference on Supercomputing*, article 12, 2008.
[10] T. B. Boykin, G. Klimeck, R. Chris Bowen, and F. Oyafuso, *Phys. Rev. B*, 66, 125207, 2002.
[11] T. B. Boykin, M. Luisier, A. Schenk, N. Kharche, and G. Klimeck, *IEEE Trans. on Nanotechnology*, 6, p. 43, 2007.
[12] http://www.ioffe.rssi.ru/SVA/NSM/Semicond/
[13] T. B. Boykin, private communication, 2008.