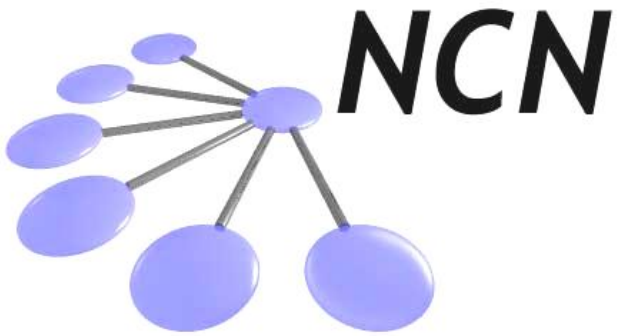
Performance Analysis of SiGe/Si core/shell and Standard Nanowire FETs for High Performance CMOS Application



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Motivation

Shrinking device dimensions. and higher drive current: Moore's Law

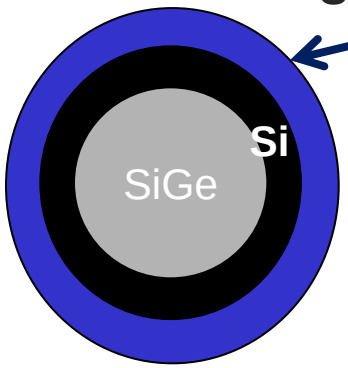
Channel material

Bulk Mobility (cm^2/Vs)[1]	Si	Ge
Electrons	1400	3900
Holes	450	1900

Device structure

Low D_{it} /good interface[2]

SiGe/Si core/shell & SiGe standard NWFETs.



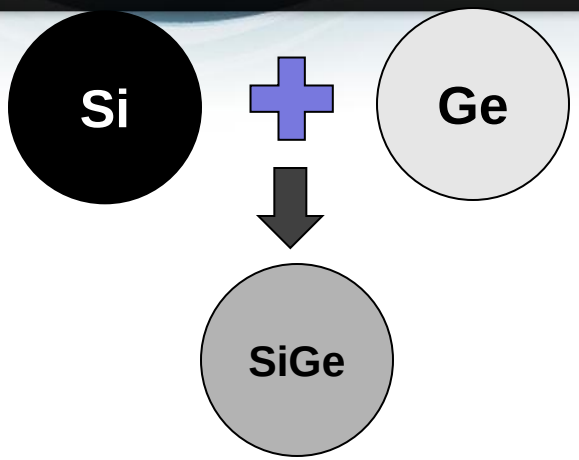
Strong geometrical and potential confinement. Capture bandstructure effects for performance comparison.

[1] http://www.ioffe.rssi.ru/SVA/NSM/Semicond/index.html
[2] Image from http://www.sandia.gov/materials/science/capabilities/materials-character.html

Outline

- Calculation of energy dispersion in SiGe
- Numerical modeling approach.
- Types of nanowire FETs (NWFETs).
- Method for performance comparison in NWFETs.
- Important device metrics and device details.
- Performance comparison for n and p type NWFETs
- Improving p-NWFET performance
- Conclusions.

Bandstructure Calculation in SiGe



"Virtual Atom"

- Change in bond-length.
- Onsite Tight-Binding parameter accounting for internal and external strain
- Coupling parameter accounting for internal and external strain

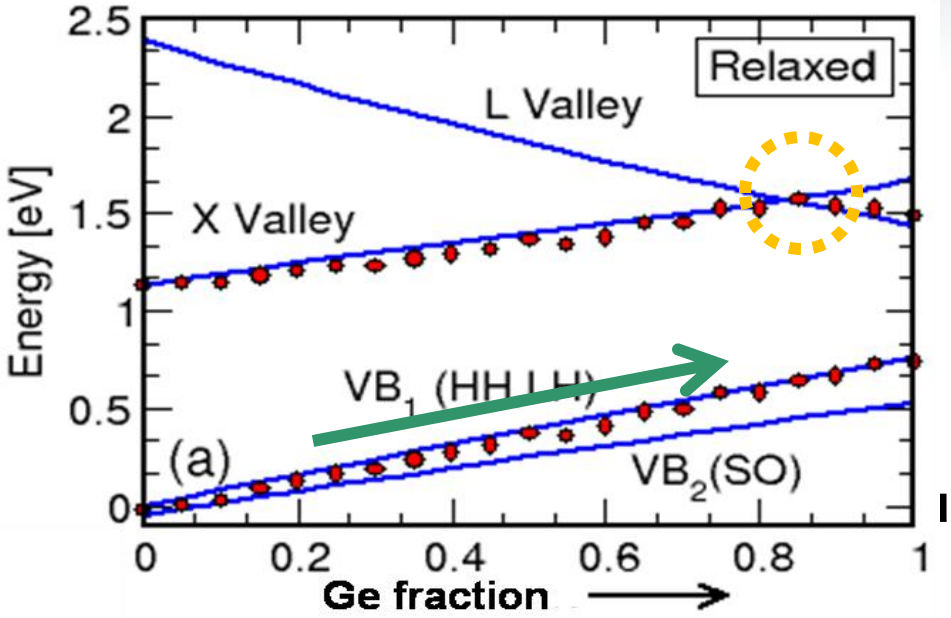
$$a_{SiGe} = x a_{Si} + (1-x) a_{Ge}$$

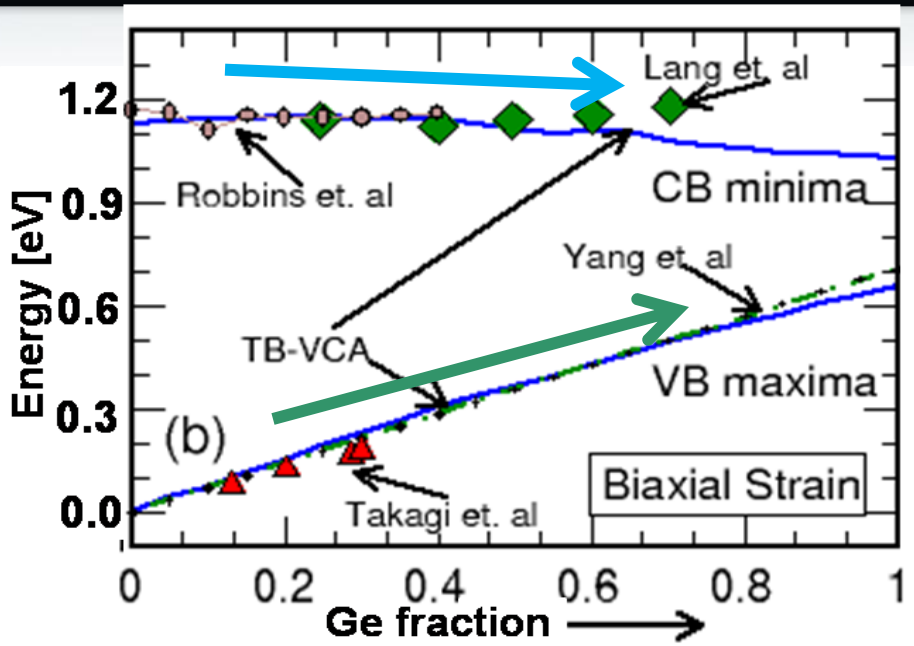
$$E_{A,B}^{strain} = x(E_A + \Delta_A) + (1-x)(E_B + \Delta_B)$$

$$V_{\sigma_1\sigma_2}^{SiGe,strain} = x\left(V^{Si}{}_{\sigma_1\sigma_2}\left[\frac{a_{Si}}{a_{SiGe}}\right]^{\eta_{Si}}\right) + (1-x)\left(V^{Ge}{}_{\sigma_1\sigma_2}\left[\frac{a_{Ge}}{a_{SiGe}}\right]^{\eta_{Ge}}\right)$$

Tight-Binding based Virtual Crystal Approximation → **TB-VCA**

Benchmarking Bulk Band-structure





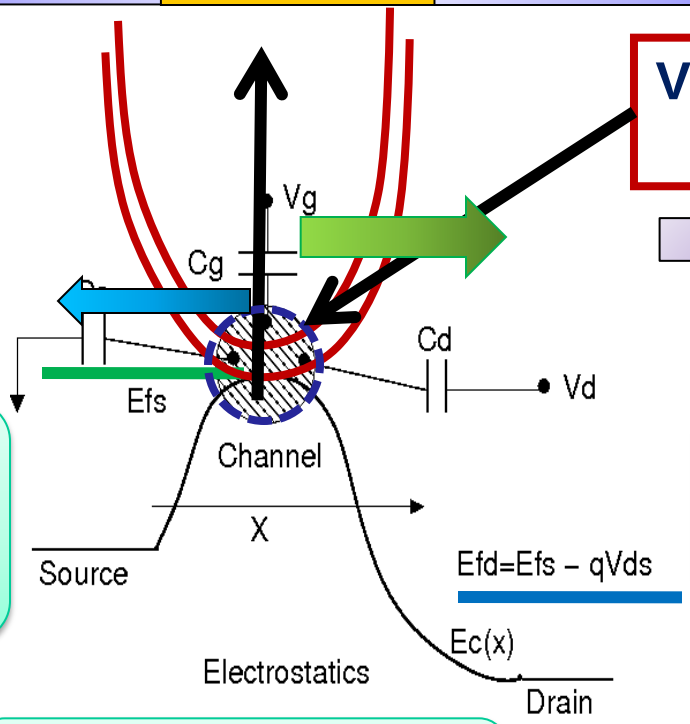
- Captures the band cross-over at 85% Ge for relaxed SiGe CB.
- Valance Band Edge changes by an equal amount in both relaxed and biaxial compressive strained SiGe bulk.
- CB edge is almost constant for all Ge% for strained SiGe Bulk.

Simulated bandstructures in good agreement with experimental data.

Transport Model and Self-consistency

Top of the barrier Ballistic Transport Model

Virtual Source Model



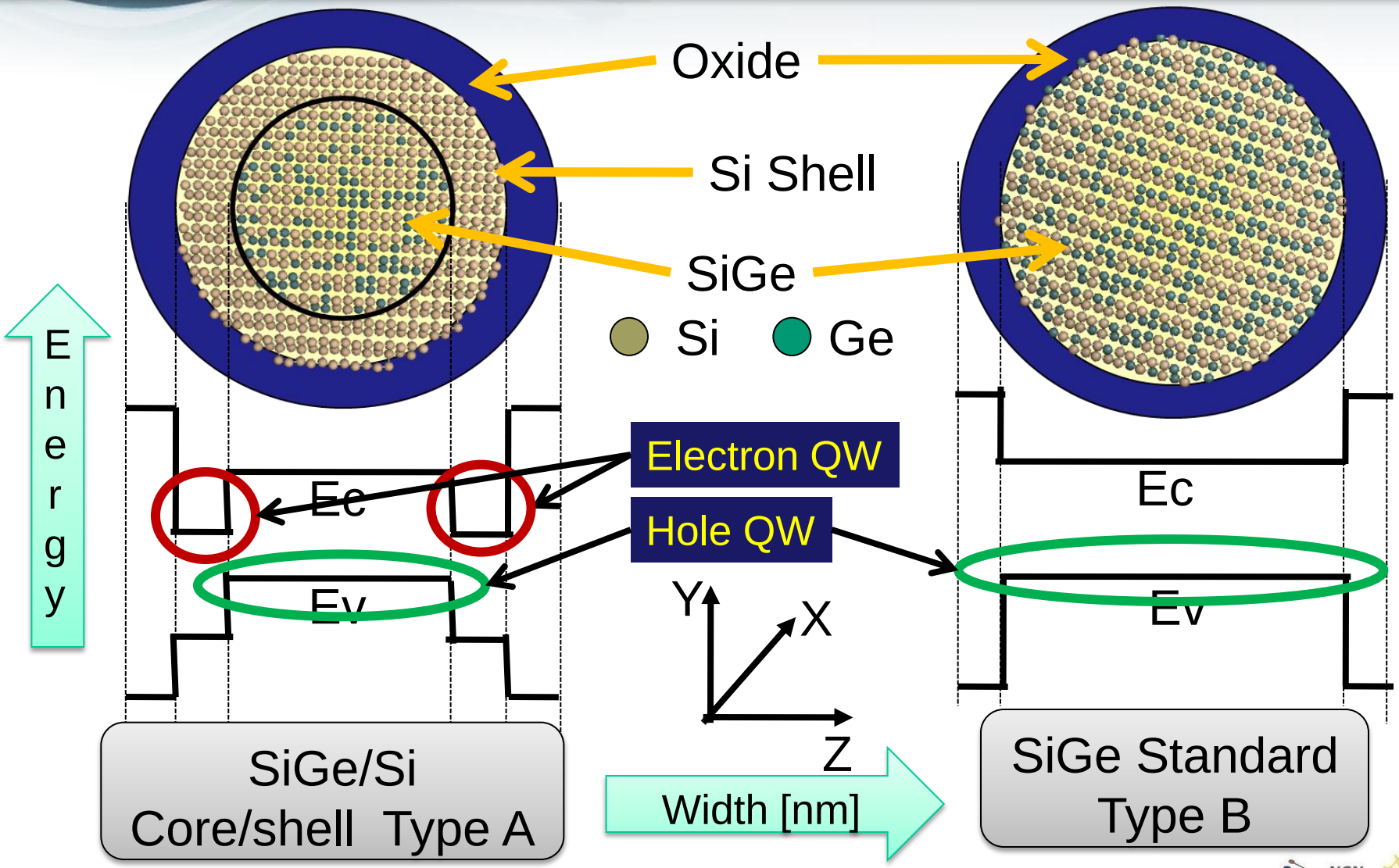
Add potential to onsite hamiltonian. Solve Schrodinger equation.

Fill the EK using the S/D Fermi level to obtain charge.

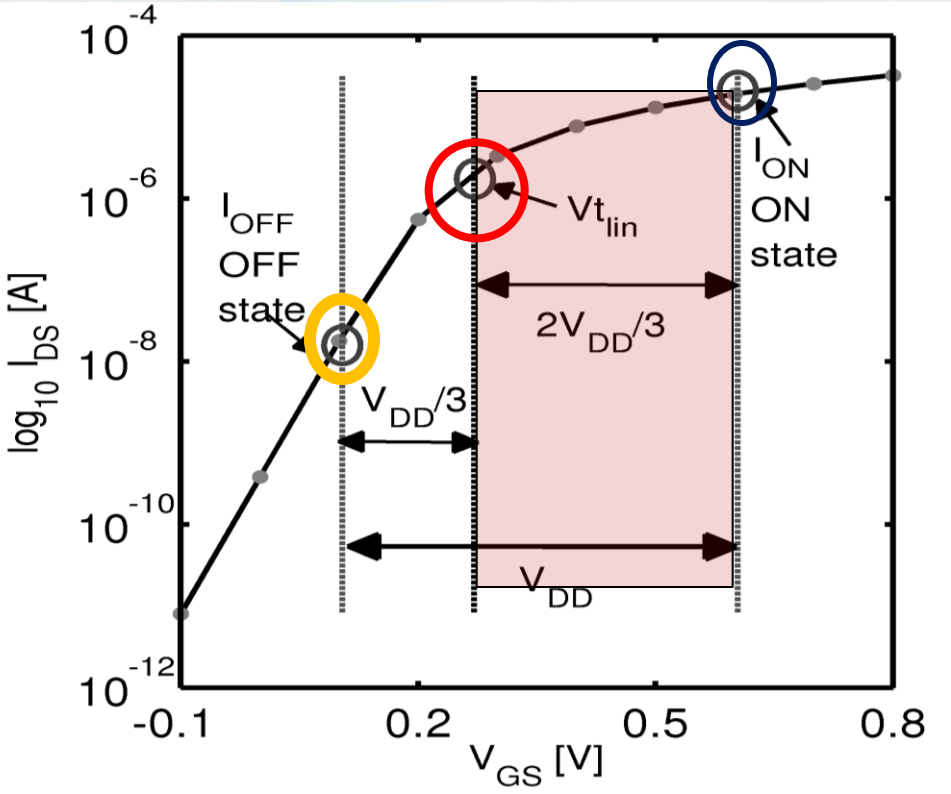
Poisson eqn. Get the Potential.

Self-Consistent Loop.

NWFET Structures



Method of comparing the NWFETs



Steps for comparison of NWFETs :

1. Obtain threshold voltage (V_T)
2. Obtain the ON-state by setting :
   $V_{ON} = V_T + 2V_{DD}/3$
   This sets a ***constant over-drive voltage*** for all the FETs to be compared.
3. **Set the OFF-state by setting:**
   $V_{OFF} = V_T - V_{DD}/3$

Constant Overdrive method [1] is used for the comparison of NWFETs

[1] R Chau et. al.,IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 4, NO. 2, MARCH 2005

Metrics for Performance comparison

Important devices metrics for 1D ballistic FETs are :

$$I_{ON} = C_g \bullet (V_G - V_T) \bullet v_{inj} \propto v_{inj}$$

Higher value indicates better driving capability and faster devices.

$$\tau_D = C_g \bullet (V_G - V_T) / (C_{gl} \bullet (V_G - V_T) \bullet v_{inj}) \propto v_{inj}^{-1}$$

Reflects how fast the device switches from OFF to ON state. Faster devices need smaller delay,

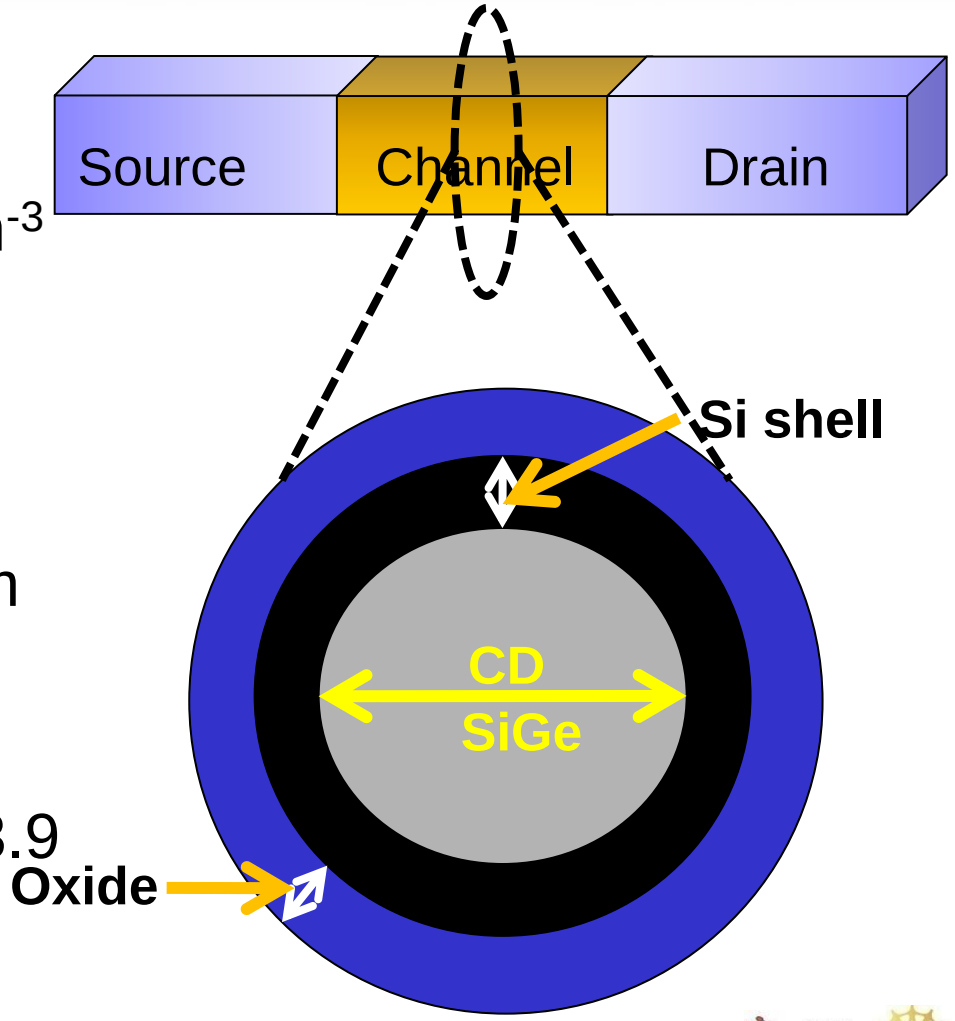
$$V_{inj} = \sum_{n,k} \rho_{n,k} \frac{\partial E_{n,k}}{\partial k} / \sum_{n,k} \rho_{n,k}$$

Reflects the role of bandstructure in deciding the ultimate speed of the carriers in the channel.

I_{ON}, Gate delay and **Virtual source velocity(Vinj)** are 3 imp. metrics.

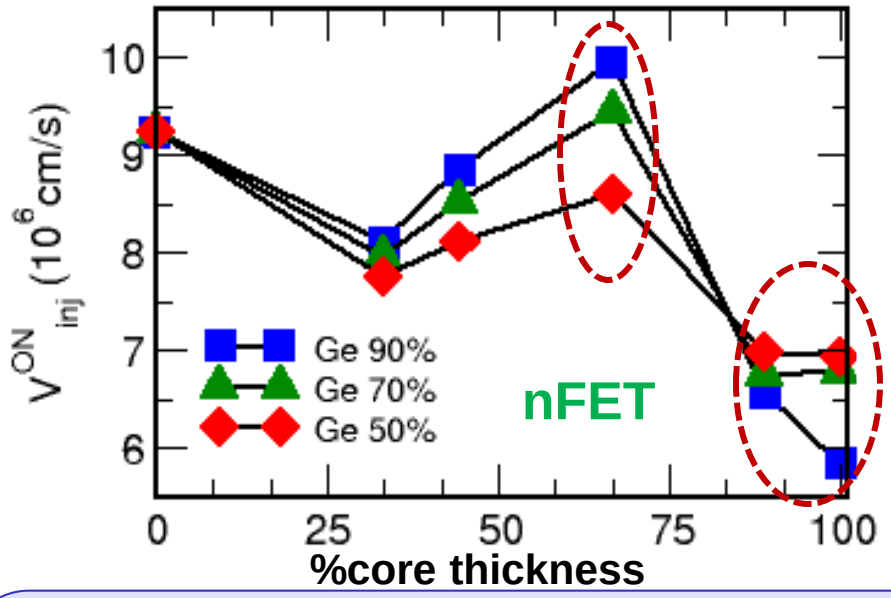
NWFET device details

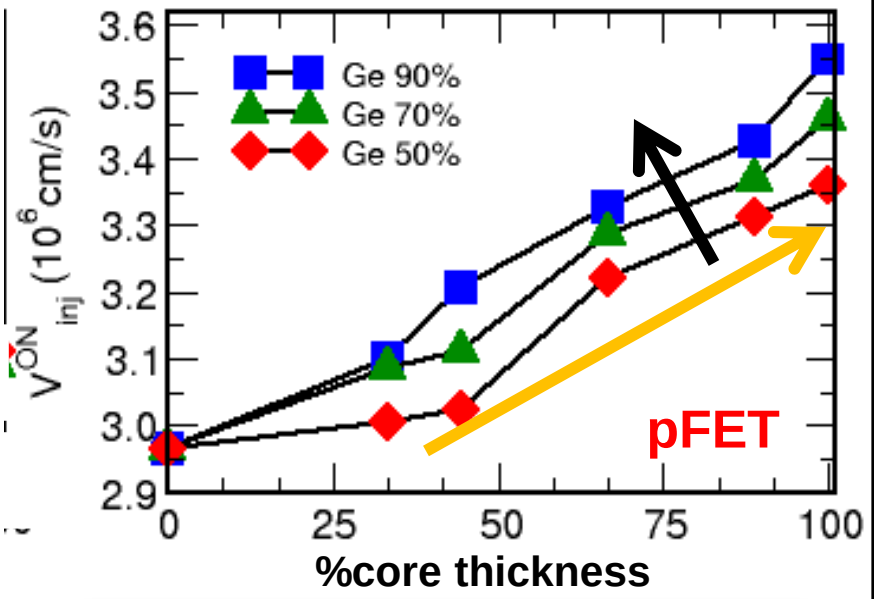
- N and P type SiGe NWFETs.
- Ge% → 90%, 70%, 50%
- Source/Drain doping: 1e20 cm^{-3}
- Channel is intrinsic.
- Metal work function in midgap for all NWFETs.
- Core diameter(CD) varied from
  - 0 (pure Silicon) , 3, 6, 8, 9 nm (no Si shell)
- Oxide thickness = 1.5nm, ε_r =3.9



Virtual Source Velocity (Vinj)

V_{inj} in nFETs ~3X higher than pFETs.



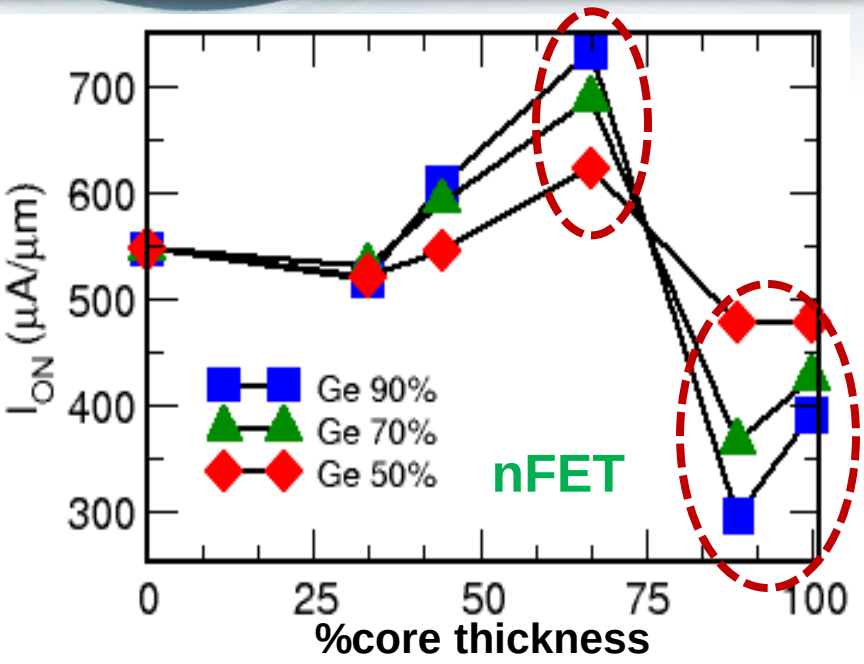


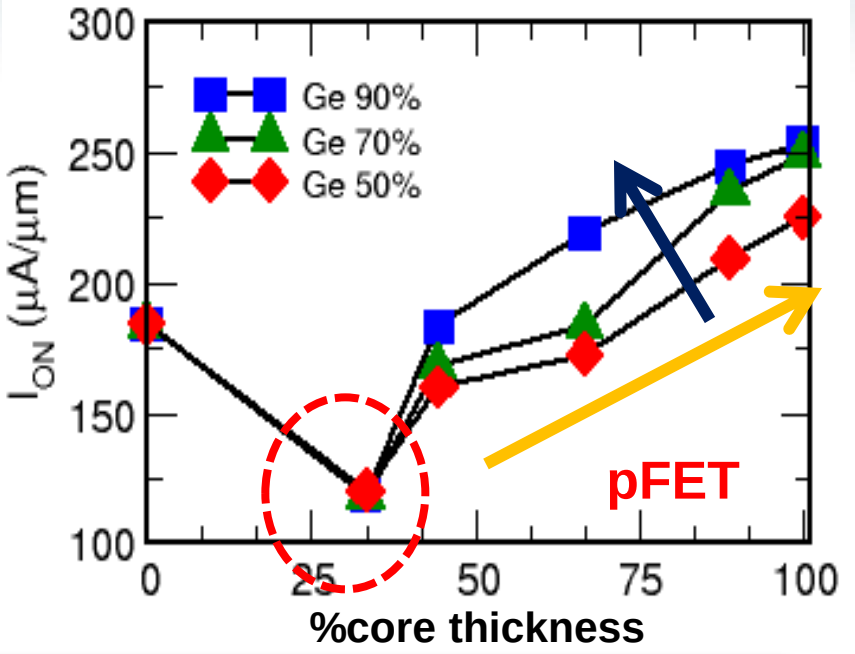
- Maximum Vinj at CD ~ 70% of wire diameter. 90% Ge shows highest Vinj
- For thinner shell Vinj flips. 90% Ge is slowest since <100>n-Ge slower than <100> n-Si for nFETs. [1]

- Vinj increases as Si shell thickness reduces in pFETs.
- 90% Ge content shows highest Vinj for all CD in pFETs.

[1] J. Wang, A. Rahman, G. Klimeck, and M. Lundstrom, doi:10.1109/IEDM.2005.1609399, (2005).

ON state drain current (I_{ON})



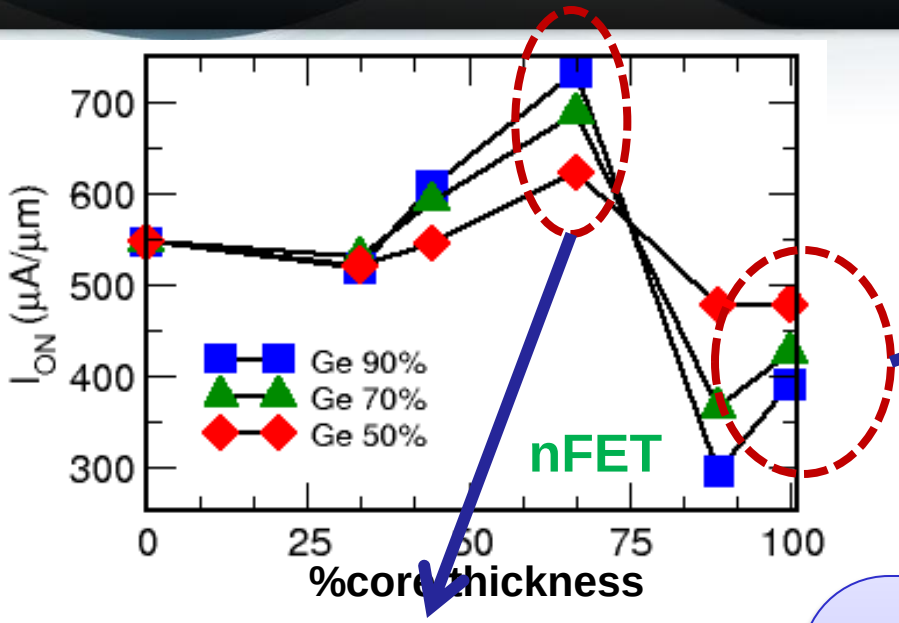


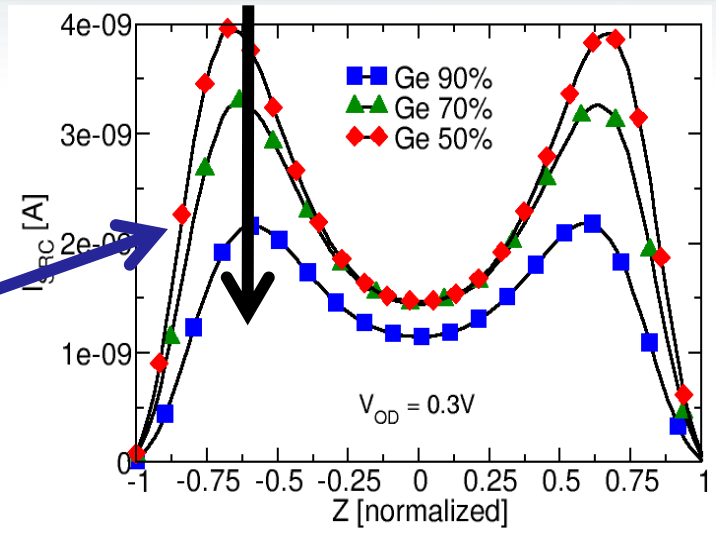
- I_{ON} peaks at CD ~70% wire diameter. Maximum for 90% Ge content.
- I_{ON} trend flips for very thin Si-shell. 90% shows minimum I_{ON}.

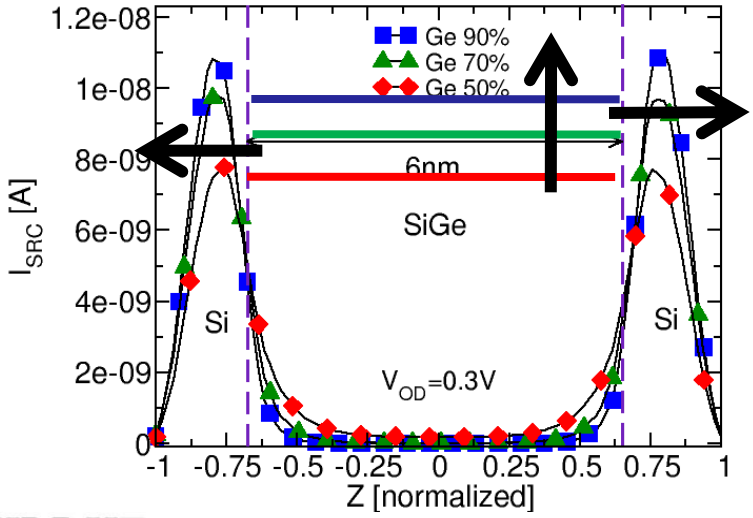
- I_{ON} increases as CD increases.
- For a fixed CD I_{ON} increases with Ge content in the NWFET.
- Dip in I_{ON} observed at very small CD due to very small charge content.

I_{ON} in nFETs ~3X higher than pFETs.

Explanation for I_{ON} in nFETs

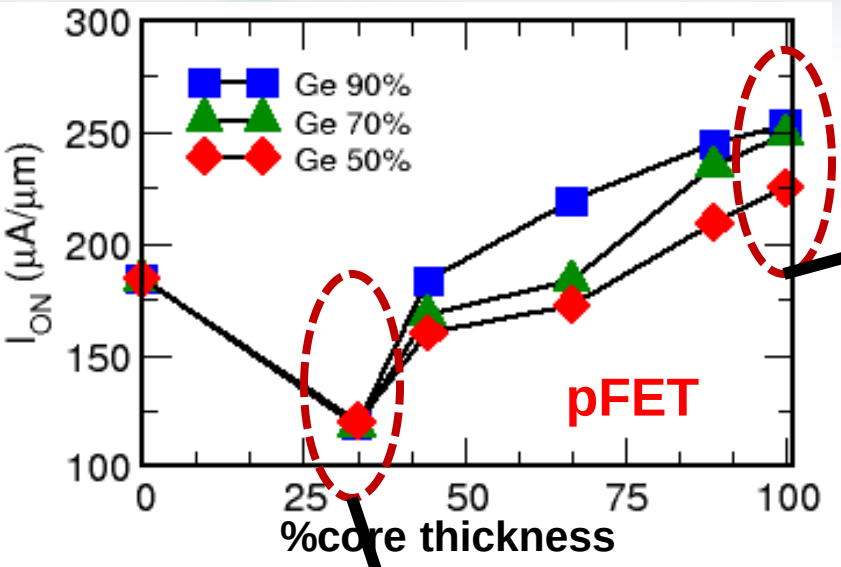


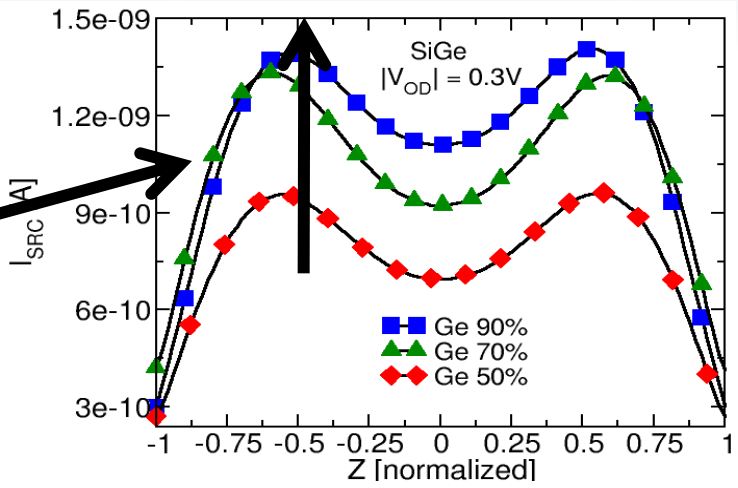


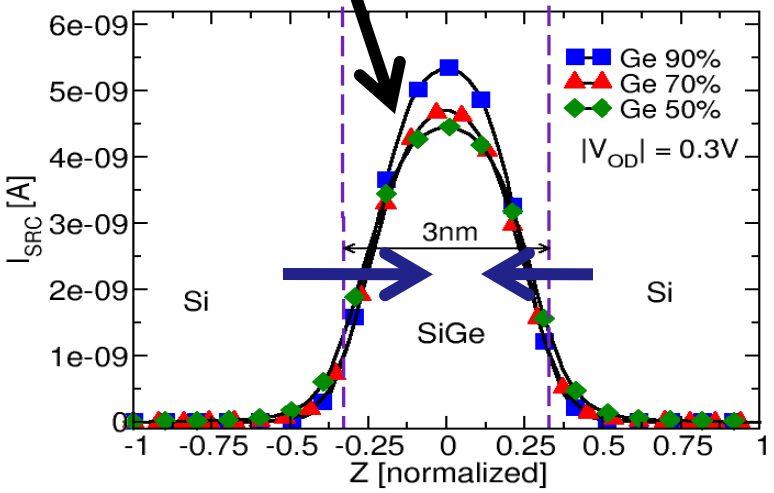


- Higher Ge content increases Ec.
  - Current pushed more in Si shell. 90% Ge with CD~6nm is optimal for maximizing I_{ON}.
- For very thin or no Si-shell. I_{ON} goes down with inc. Ge % . Vinj for <100> n-Ge smaller compared to <100> n-Si

Explanation for I_{ON} in pFETs



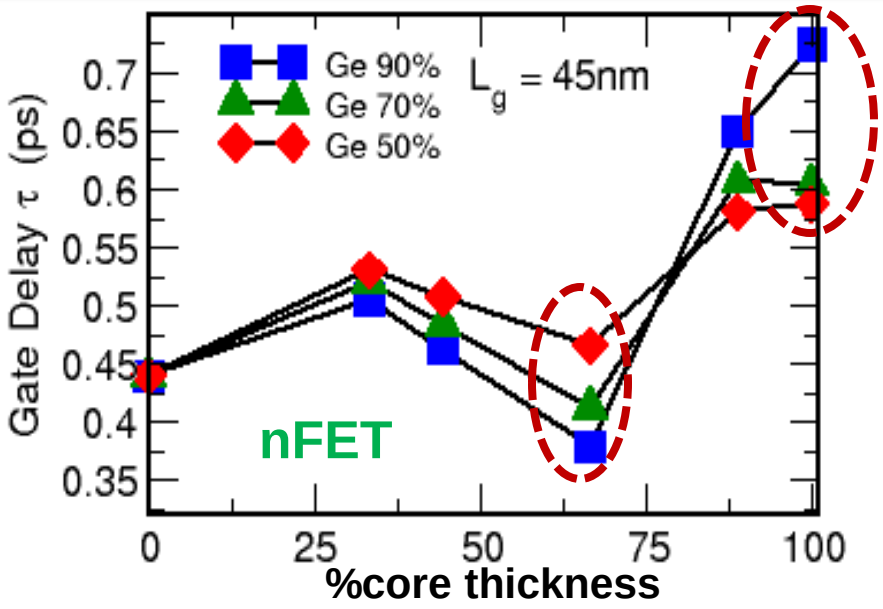


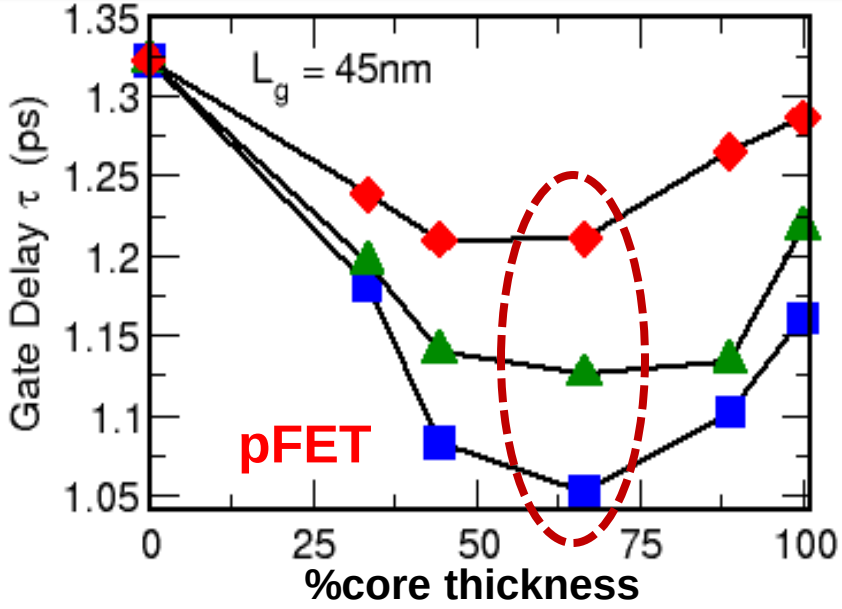


- I_{ON} reduces while moving from Si to SiGe since current is pushed into the narrow SiGe core.
- Higher Ge concentration in the core increases carrier velocity and hence the ON current.

Intrinsic Gate Delay

Gate delay decided by the interplay of charge build-up and velocity in channel





- Fastest device for highest Ge%. and optimal Si-shell thickness.
- Slow device for higher Ge % and no Si-shell.
- Vinj plays key role.

- Fastest device for highest Ge% for any core thickness.
- Cg and Vinj both imp. To decide delay in pFETs.

nFETs ~3X faster than pFETs.

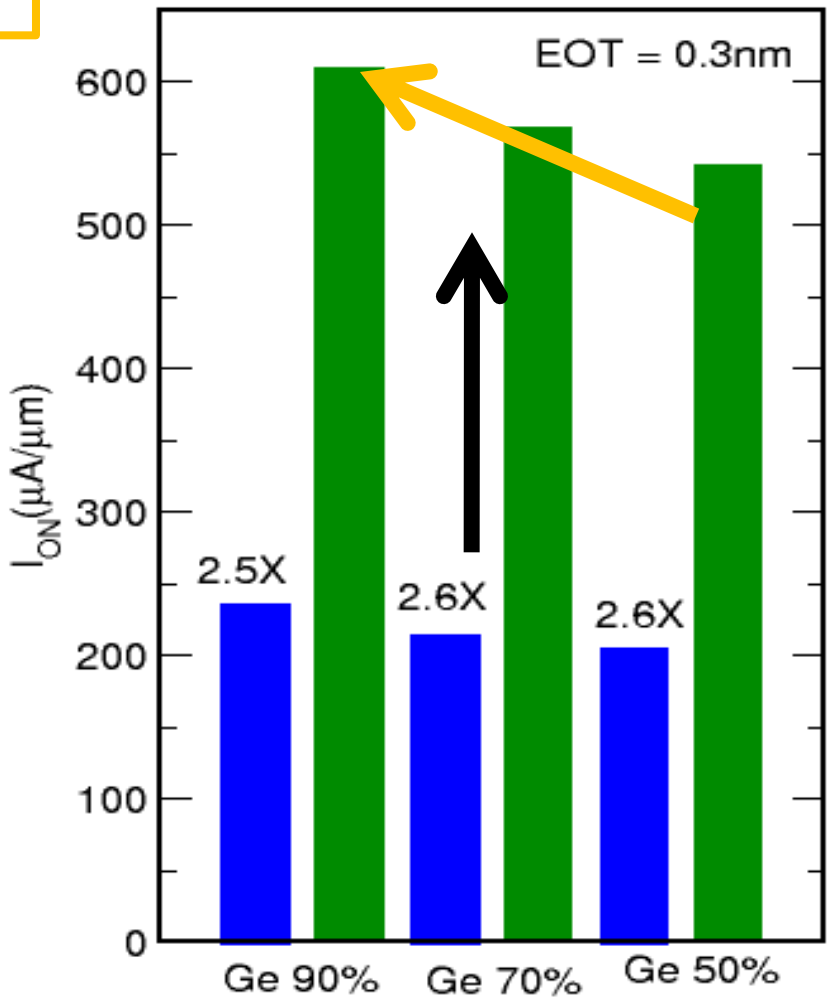
Improvement in pFET performance

I_{ON} in nFETs ~3X higher than pFETs.

Replace SiO_2 → High-K , e = 21.
EOT = 0.3nm.
pFETs with diameter = 9nm. No Si-shell.

- I_{ON} improves for all pFETs.
  ~2.5X improvement compared to SiO_2
- Maximum increase obtained for 90% Ge core.

High-K gate dielectric with almost negligible si-shell improve pFET performance.



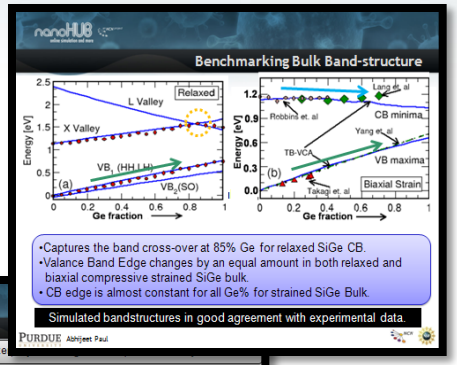
Summary of performance and optimization

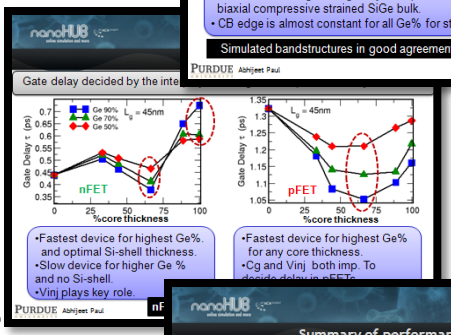
Device Performance	n-NWFETs	p-NWFETs
Vinj improvement	High Ge %, optimal Si-shell	High Ge%, thin Si-shell
I_{ON} improvement	High Ge %, optimal Si-shell	High Ge %, thin Si-shell
Gate delay reduction	~1.2X faster than Si ↑	~1.25X faster than Si ↑
Channel type/gate control	Surface channel/ good gate control. ↑	Buried channel/Bad gate control. ↓
Optimization	Optimally thin Si-shell/high Ge%	High-K, thin Si-shell
Process complexity	Fits in standard CMOS. ↑	More process-steps, High-K integration. ↓

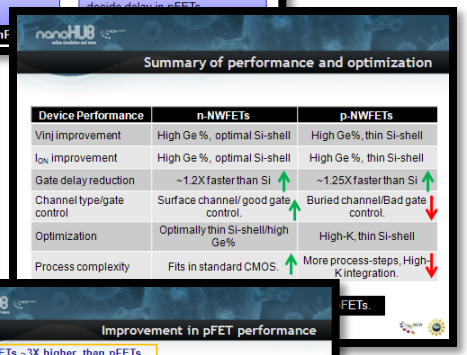
nFETs fit better into CMOS flow compared to pFETs.

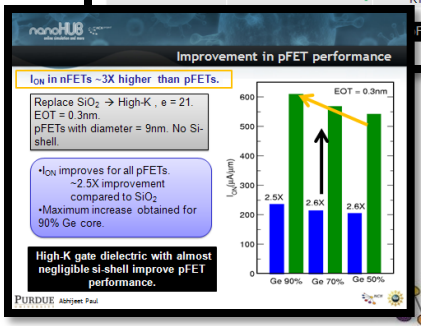
Conclusions

- Developed TB based VCA method for EK calculation.
  - Results in good agreement with experiments
- SiGe nFETs faster than pFETs
- SiGe improves both nFETs and pFETs
  - 1.2X improvement in I_{ON} compared to Si counterpart
- pFETs improvement achieved by high-K gate dielectric and no Si-shell.









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Relaxed SiGe Bulk EK:

CB data: [1] J. F. Morar, P. E. Batson, and J. Tersoff, PRB, 47, 7, 4107-4110, (1993).

VB data: [2] L. Yang, J. R. Watling, R. C. W. Wilkins, M. Borici, J. R. Barker, A. Asenov, and S. Roy, Semi. Sci. and Tech., 19, 10, 1174-1182, (2004).

Strained SiGe Bulk EK:

[1] D. J. Robbins, L. T. Canham, S. J. Barnett, A. D. Pitt, and P. Calcott, JAP, 71, 3, 1407-1414, (1992).

[2] D. V. Lang, R. People, J. C. Bean, and A. M. Sergent, “APL, 47, 12, 1333-1335, (1985).

[3] S. Takagi, J. Hoyt, K. Rim, J. Welser, and J. Gibbons, TED, 45, 2, 494-501, (1998).

[4] L. Yang, J. R. Watling, R. C. W. Wilkins, M. Borici, J. R. Barker, A. Asenov, and S. Roy, Semi. Sci. and Tech., 19, 10, 1174-1182, (2004).

Thank You !!!

Any Questions ?