

Transport in vertically stacked hetero-structures from 2D materials

Fan Chen, Hesameddin Ilatikhameneh, Gerhard Klimeck and Rajib Rahman

The Network for Computational Nanotechnology (NCN), Purdue University, West Lafayette, IN 47906, USA

The fast growth of information technology has been sustained by continuous scaling of silicon-based MOSFETs. The scaling of transistors face two major challenges nowadays: the degradation of gate control (device electrostatics) and fundamental thermionic limitation of the steepness of sub-threshold swing (SS). 2D materials have emerged as promising candidates to replace silicon, as they can maintain excellent device electrostatics at much reduced channel length and thickness [1]. Tunnel field effect transistors (TFETs) based on band to band tunneling has been demonstrated to break the thermionic limitation of SS [1]. However, planar TFETs with Transition Metal Dichalcogenide (TMD) as channel material suffer from low current levels. To increase the tunneling current, a double gated TFET based on vertically stacked 2D TMD materials (as shown in Fig1. a) has been proposed [3]. Yet, a fully systematic device design guideline is still needed.

In this work, we investigate this device structure by the means of atomistic quantum transport simulations based on Non-Equilibrium Green's Function (NEGF) [3]. Self consistent solution of 3D Poisson and NEGF equations within tight binding description has been obtained through our NEMO5 tool [3]. The results show that the subthreshold slope below the thermionic limit can be achieved (Fig. 1b). The atomically thin vertical PN heterojunction can be electrostatically modulated from a type II heterojunction in the OFF-state of the device to a broken bandgap alignment in the ON-state. A systematic study is performed on the impact of device design parameters such as doping, channel length, gate underlap to provide a comprehensive understanding of the device physics and design guideline.

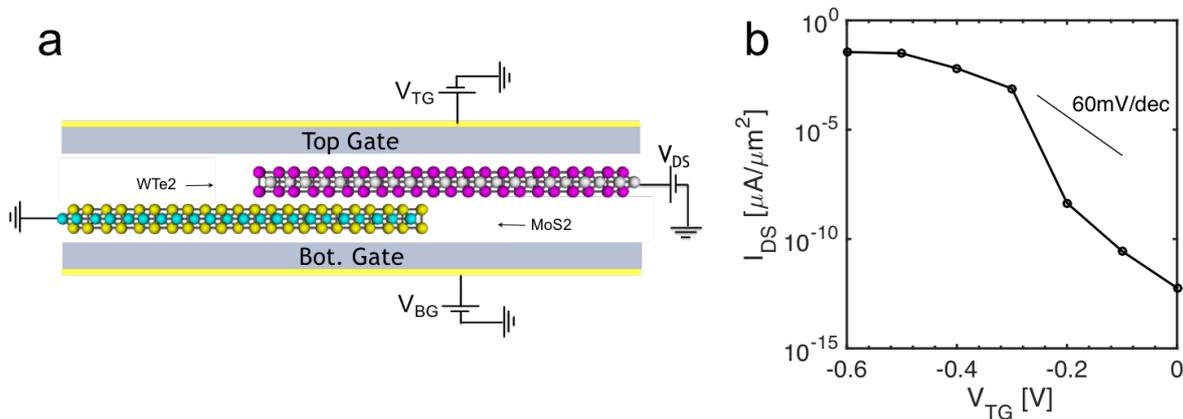


Fig. 1. a) Device Structure. b) Transfer characteristics

References

- [1] Ilatikhameneh, Hesameddin, et al. Exploratory Solid-State Computational Devices and Circuits, IEEE Journal on 1 (2015): 12-18.
- [2] Sarkar, Deblina, et al. Nature 526.7571 (2015): 91-95.
- [3] Fonseca, J. E, et al. Journal of Computational Electronics 2013, 12, (4), 592-600.