Transport characteristics of Nitride TFETs: Ballistic versus scattering

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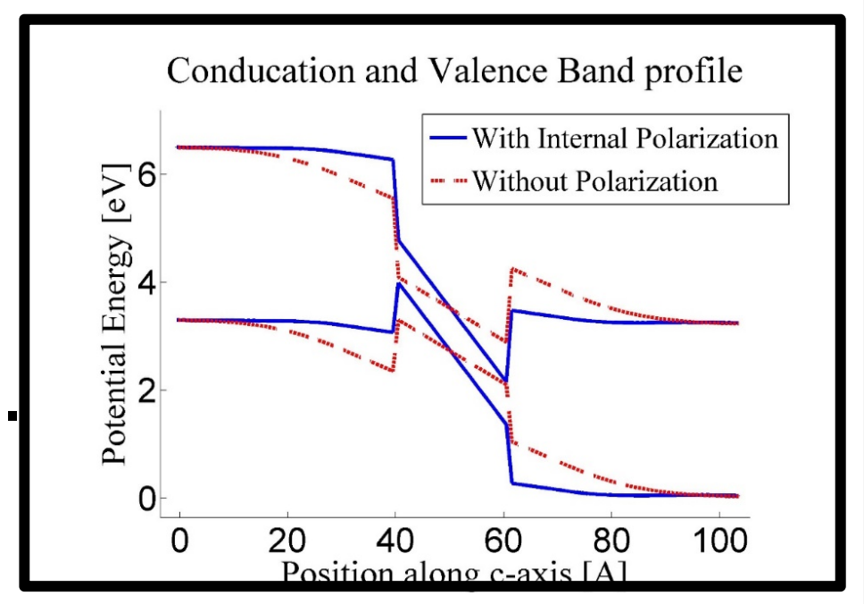
III-Nitride as a prospective TFET

Advantage		Drawback
Possibility of subthreshold swing<60 mV/decade → Lower power consumption	TFET	Tunneling based drive current → low I_{ON}



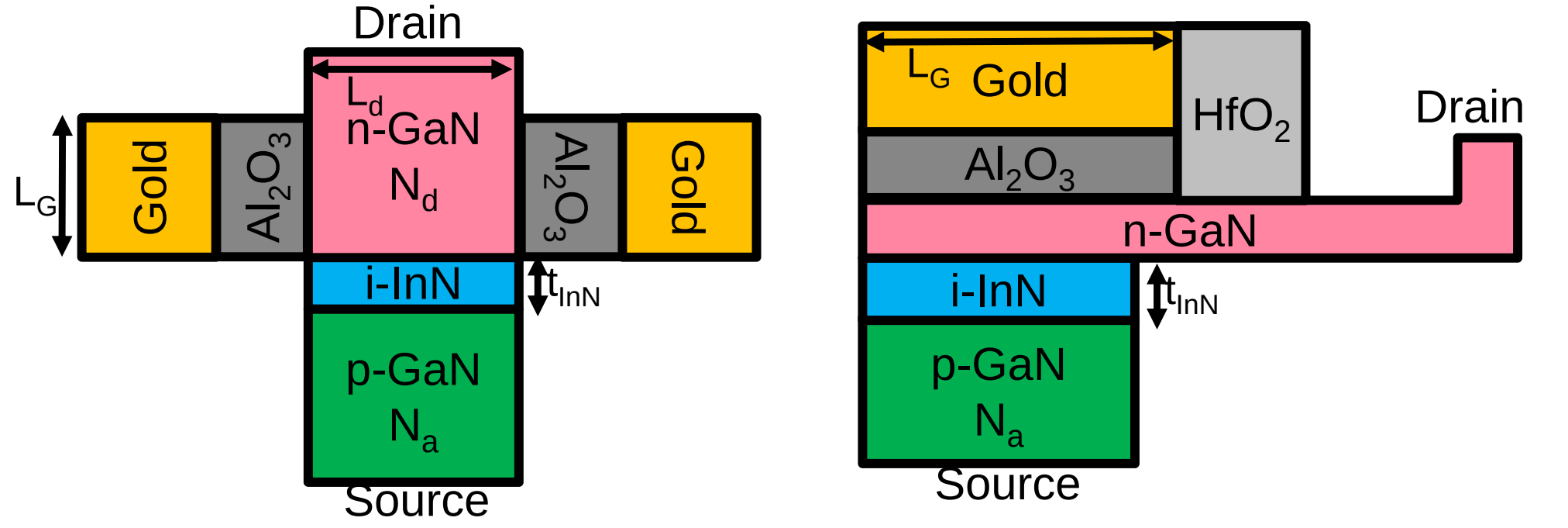
Tunneling rate increase in III-Nitride TFETs

- Large polarization field → small tunneling length.
- Small effective mass (e.g., bulk InN~0.20m_o)
- Tunneling through low bandgap material → efficient tunneling

Open design issues

- Geometry for best gate control:

Sidewall gate structure vs In-line geometry



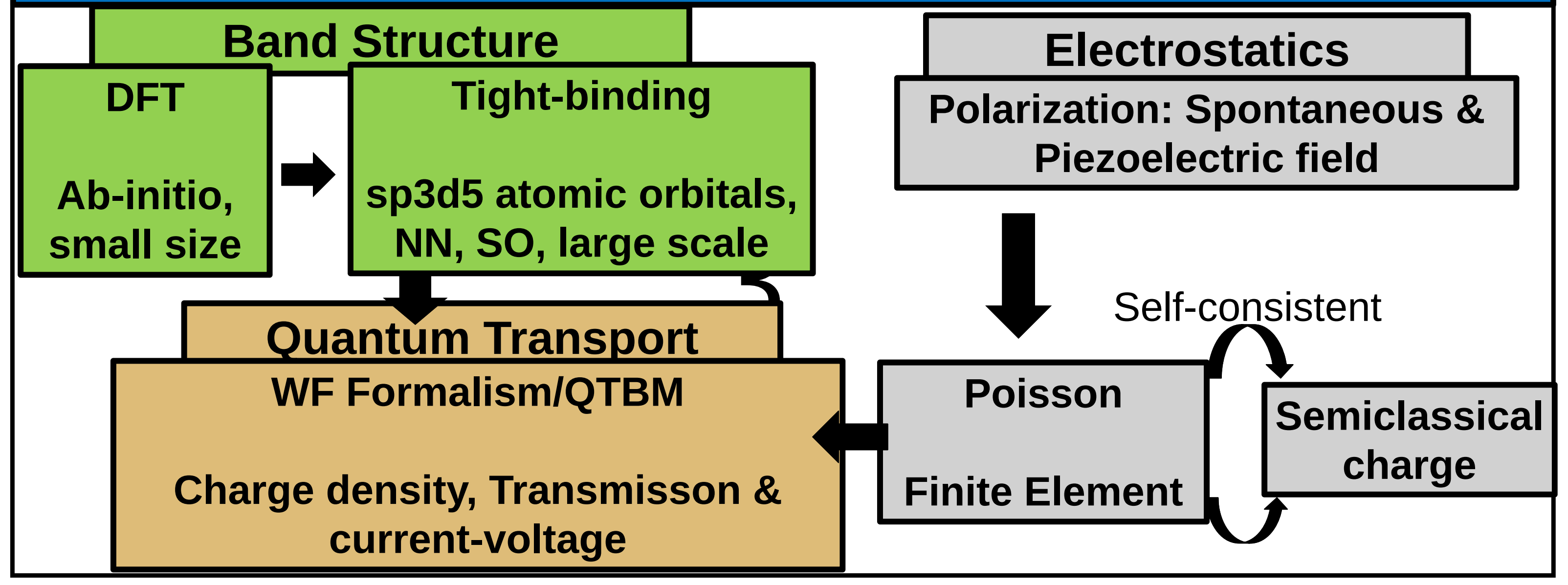
Proposal & Experiments: Jena, Fay, Seabaugh (Notre Dame)

N_d	$1X10^{17}$ cm^{-3}
N_a	$3X10^{19}$cm^{-3}
t_{InN}	1.7 nm
EOT	0.43 nm
L_G	15 nm
L_D	12 nm

- Impact of scattering:

Ballistic vs Non-ballistic simulation

Simulation methodology: Ballistic



Band Structure

DFT: Ab-initio, small size → Tight-binding: sp3d5 atomic orbitals, NN, SO, large scale

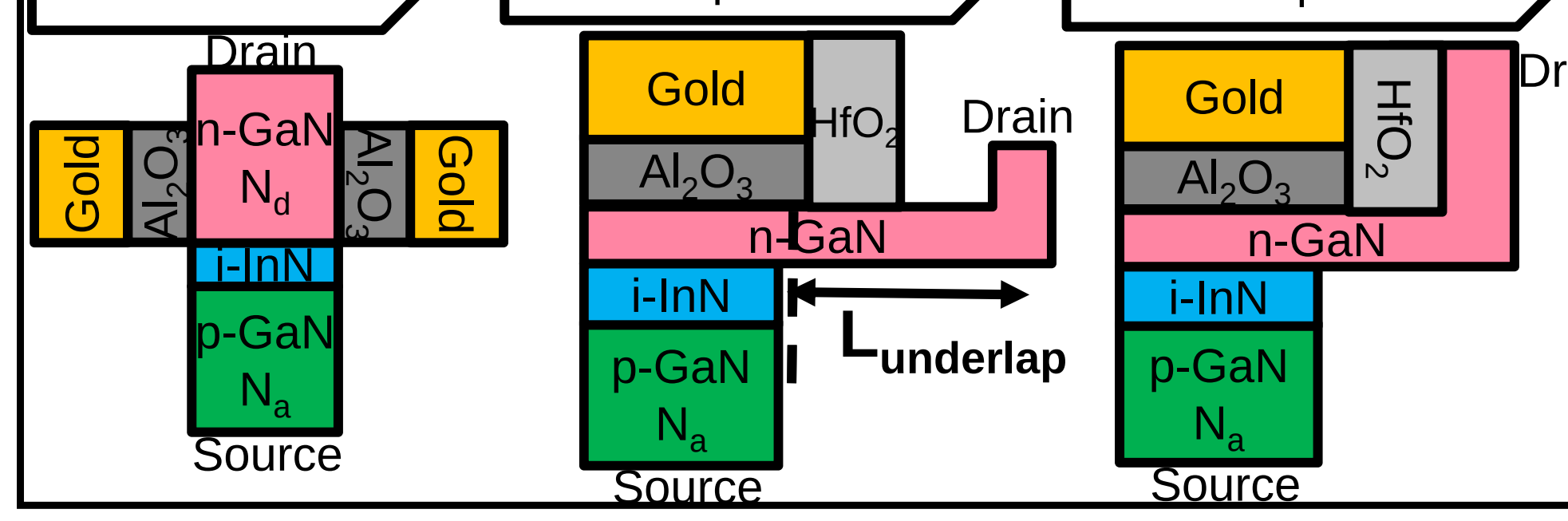
Electrostatics: Polarization: Spontaneous & Piezoelectric field

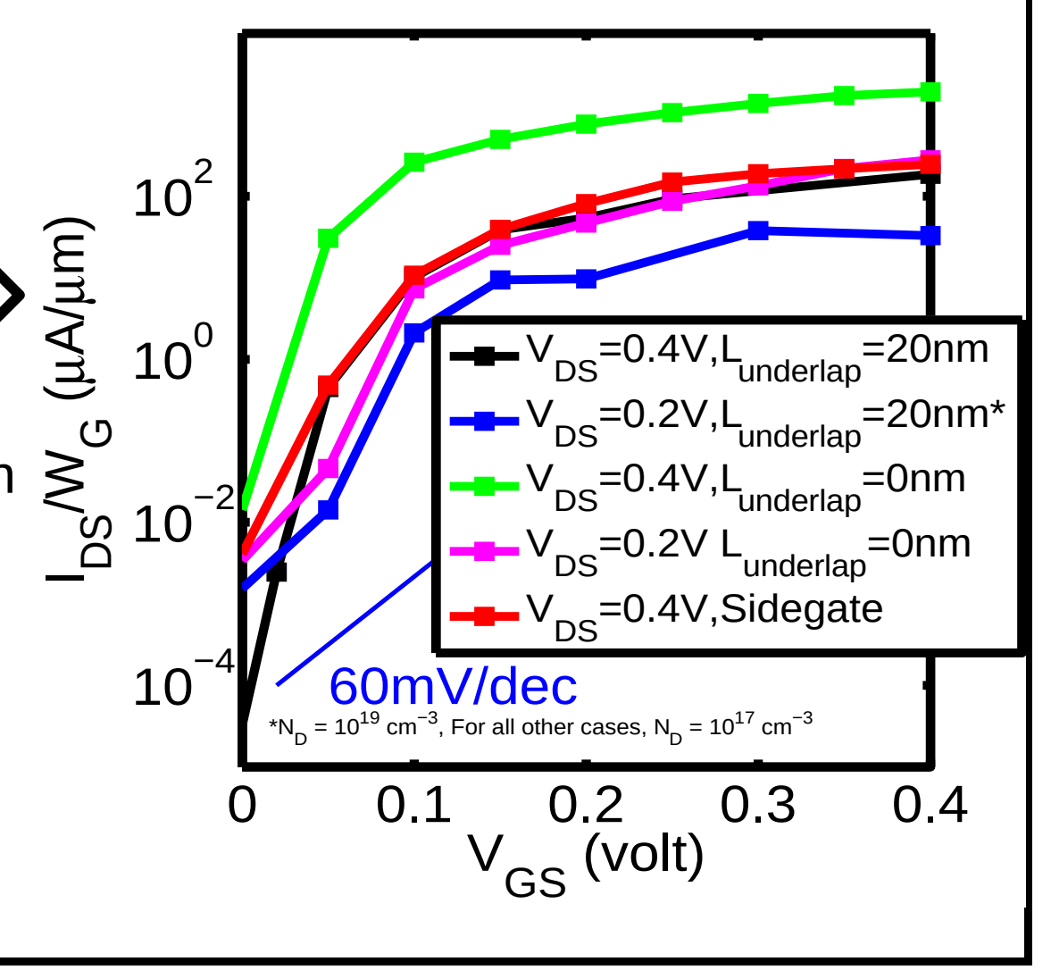
Quantum Transport: WF Formalism/QTBM — Charge density, Transmission & current-voltage

Self-consistent: Poisson (Finite Element) ↔ Semiclassical charge

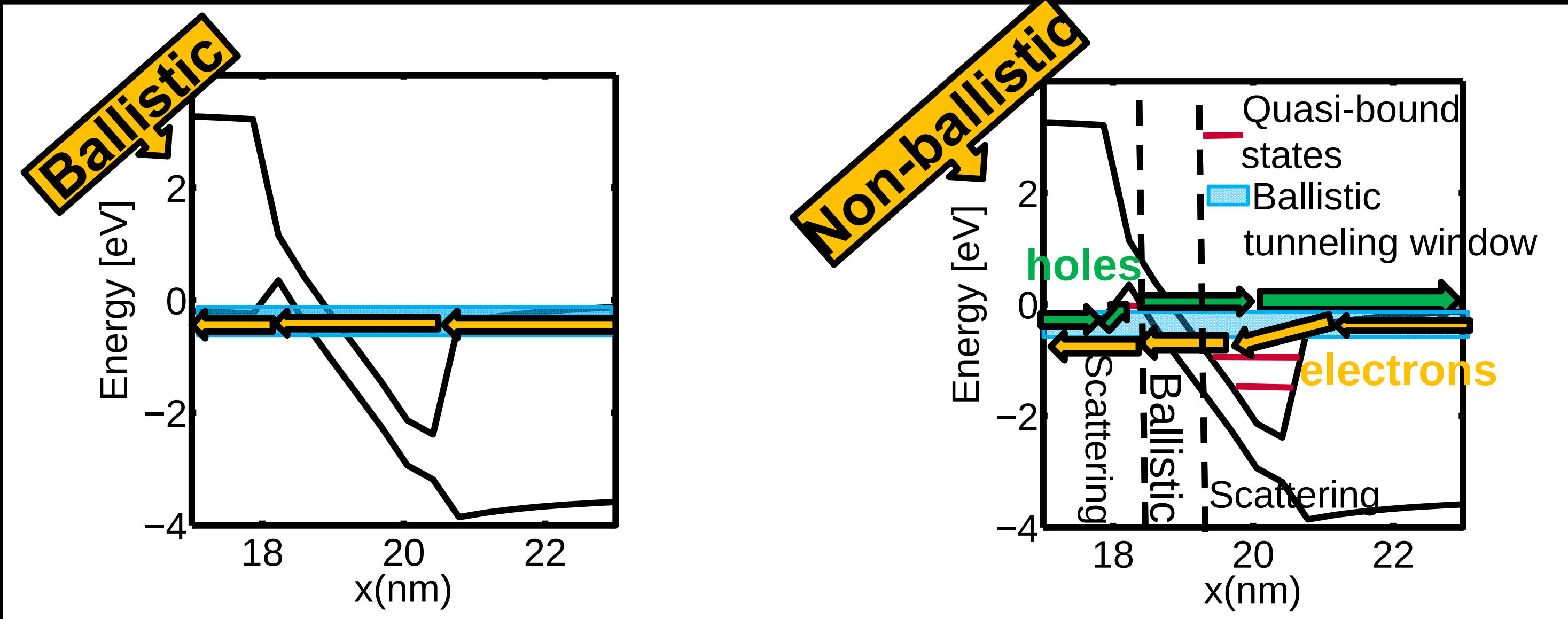
Ballistic current: Sidegate vs In-line

SS: 25mV/dec I_{ON}: 247μA/μm	SS: 12mV/dec I_{ON}: 187μA/μm	SS: 15mV/dec I_{ON}: 1911μA/μm
Sidewall-gate geometry	In-line geometry $L_{underlap}$ = 20nm	In-line geometry $L_{underlap}$ = 0nm





Ballistic vs Non-ballistic simulation



Simulation methodology (Non-ballistic)

Step 1: Divide the device into 3 regions

Scattering region 1 (Left contact)	Ballistic region	Scattering region 2 (Right contact)

Step 2: Solve NEGF with additional broadening term in scattering region.

$E-H-\Sigma(E)-i\eta(E)$	$E-H-\Sigma(E)$	$E-H-\Sigma(E)-i\eta(E)$

$\eta = 6.6meV \Rightarrow \tau = 0.05ps$ is used.

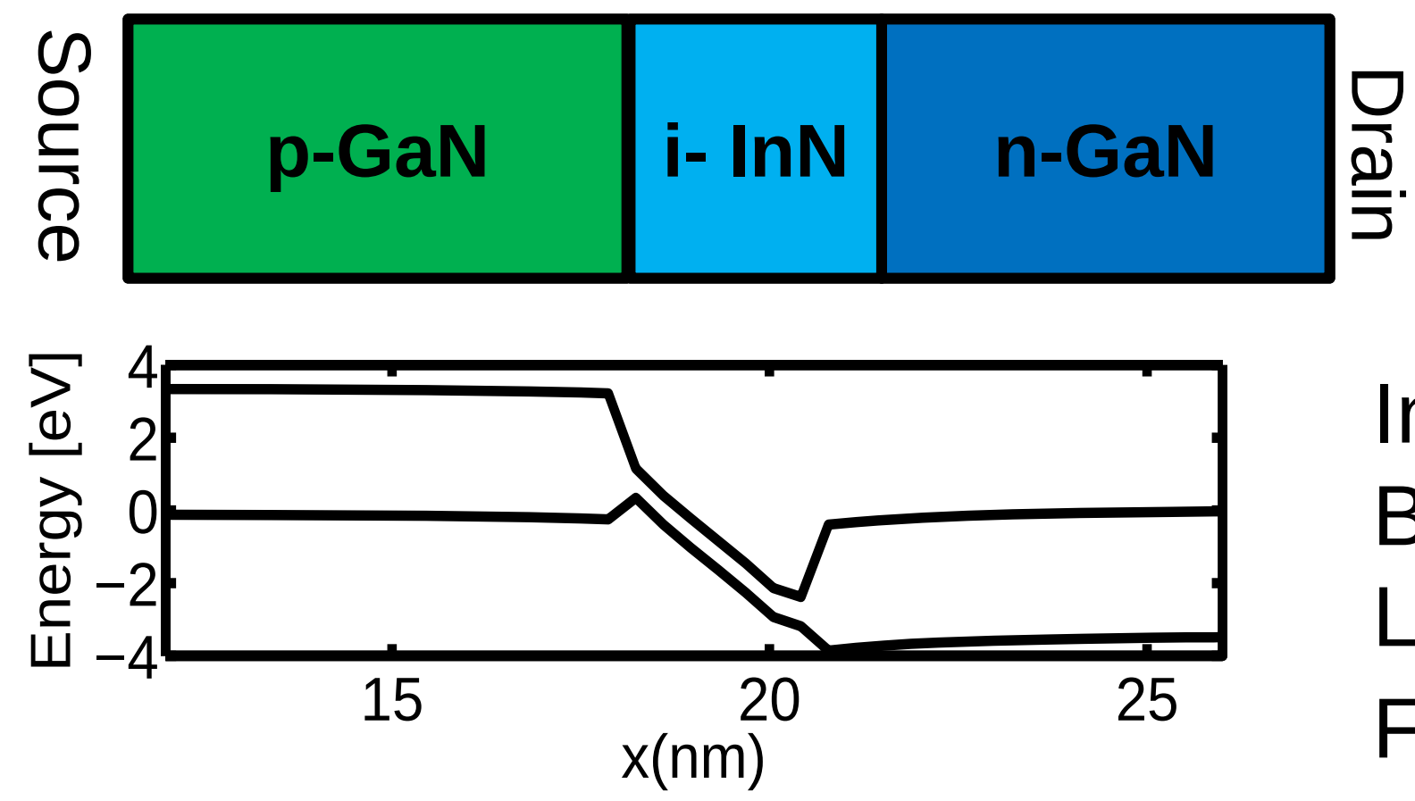
Ref: G. Klimeck, et. al.,Appl. Phys. Lett., 67 (2539), 1995

Σ = Self-energy

$\eta(E)$ = Broadening of state E $=\frac{\hbar}{2\tau}$

τ = Relaxation time of carriers

Open question

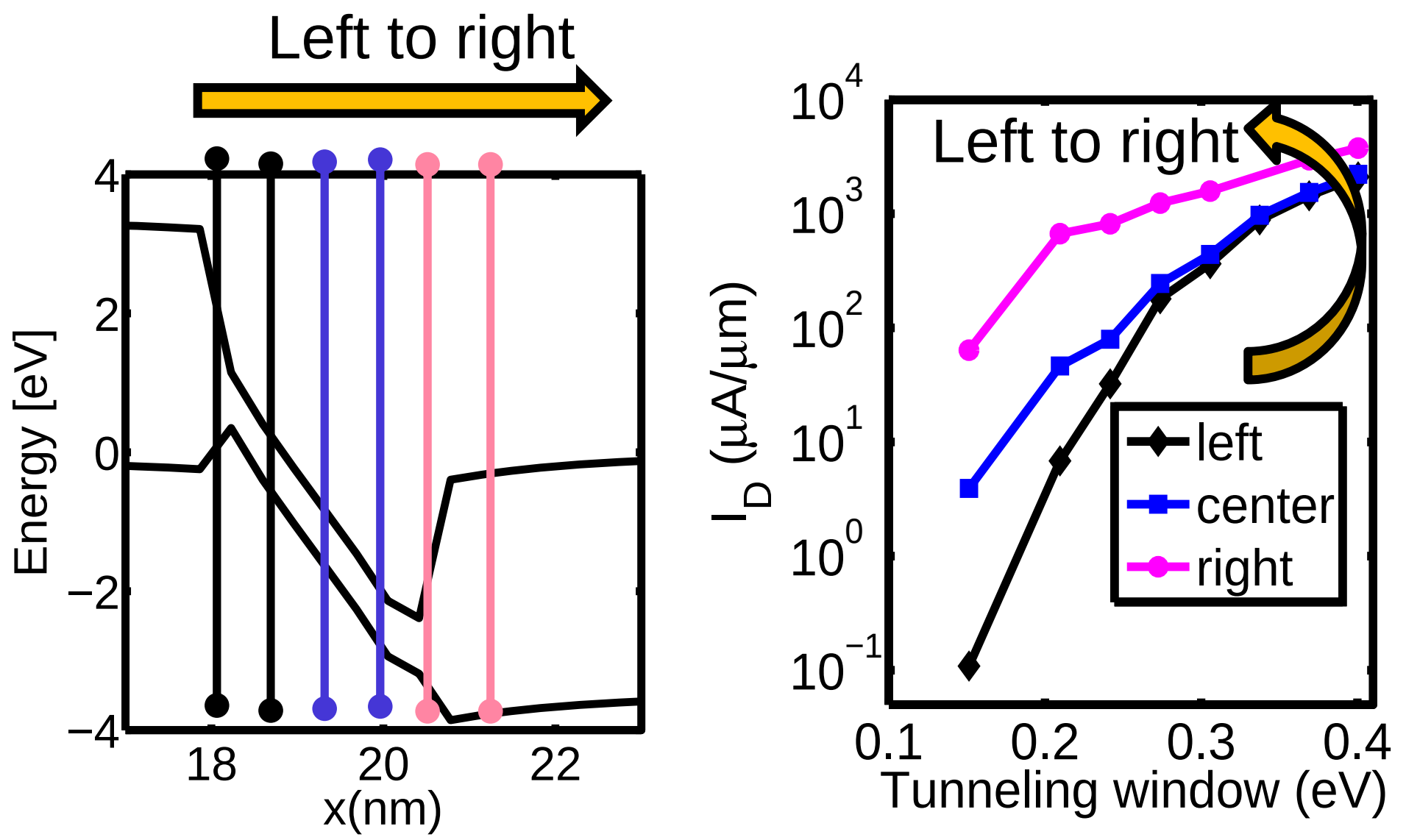


Study the effect of
- Position of the ballistic region
- Width of the ballistic region

In conventional FETs, Ballistic channel length, $L \sim 2\lambda_p \sim 2 * \tau * v_{th}$

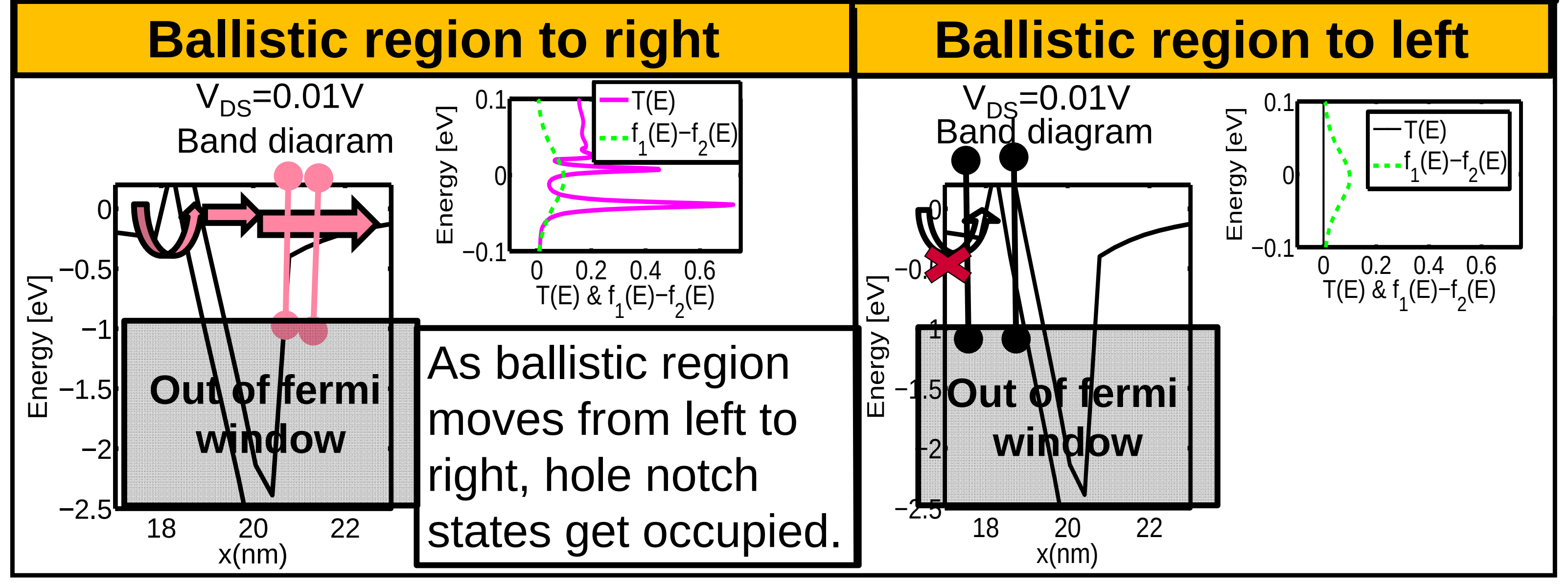
For $\tau = 0.05ps$ and $v_{th} = 10^7 cms^{-1}$, L ~ 10nm

I-V: Variable position of ballistic region



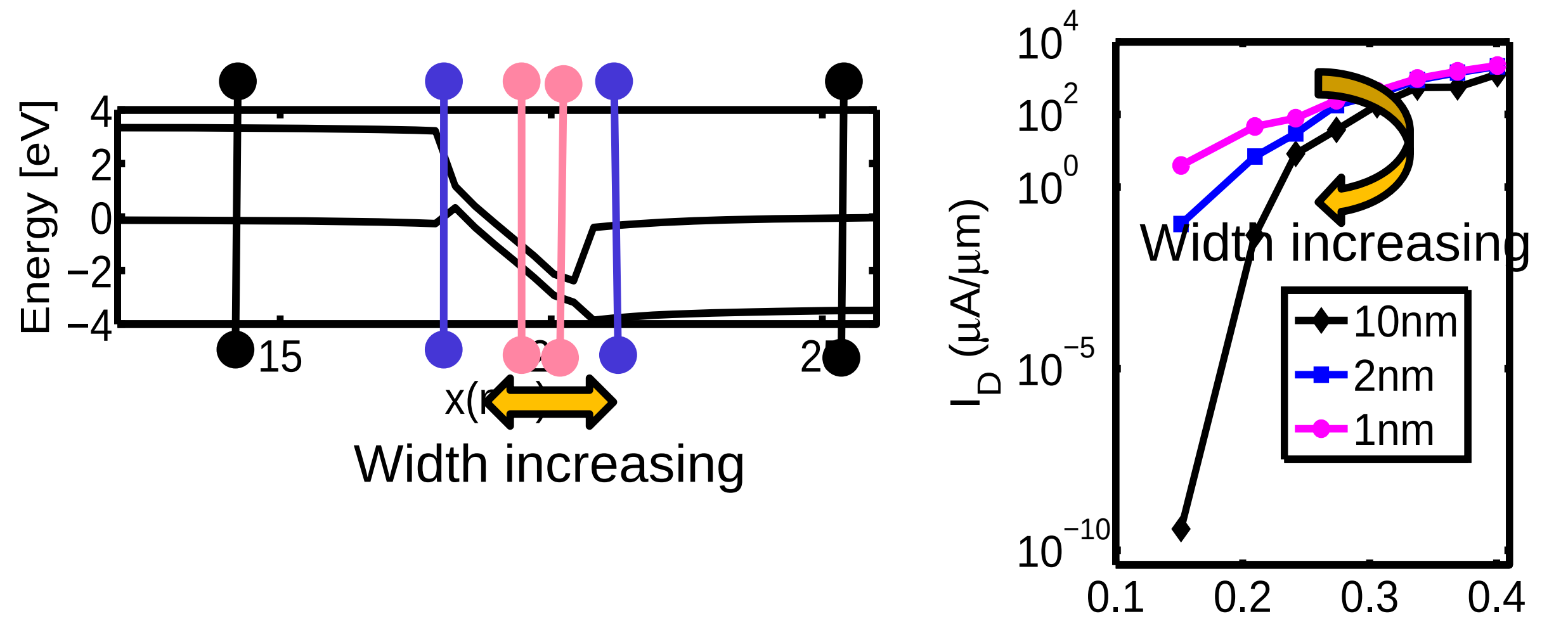
As ballistic region moves towards right, current density increases

Variable position of ballistic region (contd.)



As ballistic region moves from left to right, hole notch states get occupied.

I-V: Variable width of ballistic region



Ballistic width smaller →Notch states more occupied →More current at low tunneling window

Key result statements

- ☐ Ballistic simulation: In-line TFETs show better performance compared to Sidegate TFETs in terms of subthreshold swing and ON current.

Publication:" Polarization-Engineered III-Nitride Heterojunction Tunnel Field-Effect Transistors", Li W. , Sharmin S., Ilatikhameneh H., Rahman R., Lu Y., Wang J., Yan X., Seabaugh A., Klimeck G., Jena D., Fay P., IEEE JExSSCDC, Vol. 1,Jul 2015.

- ☐ Non-ballistic simulation: Filling up of quasi-bound states degrades device performance in subthreshold regime.

Next steps

- ☐ Non-ballistic simulation: Explore graded junction device to overcome the degrading effects of quasi-bound states.

p-GaN	$In_{0.x}Ga_{1-0.x}N$ x = 0 to 1	i-InN	$In_{0.x}Ga_{1-0.x}N$ x = 1 to 0	n-GaN

Graded junction device

- ☐ Investigate the impact of atomistic strain on the transport characteristics of Nitride TFETs

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Theme 2383.002: Quantum Engineered Steep Transistor
Task D.2.4 : Atomistic Carrier Transport Modeling for Steep Devices