Atomistic Simulation on Gate-recessed InAs/GaSb TFETs and Performance Benchmark

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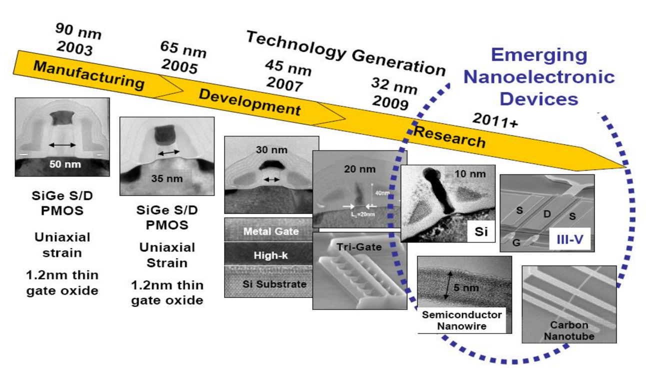
MOTIVATION

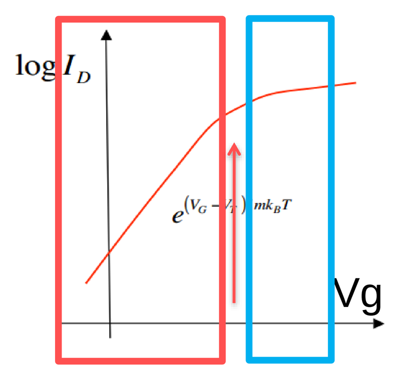
Faster & Power Efficient Switch

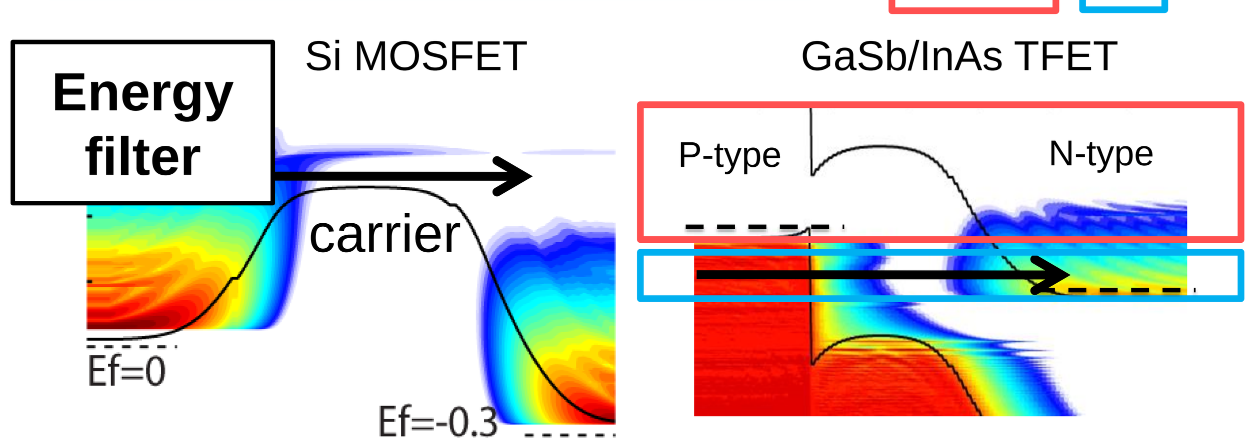


Power density has flattened performance, while transistor count increased: Result clock has stalled or goes backward

MOSFET: Carrier injection from thermal tail of Boltzmann Distribution

TFET: Bandgap blocks "hot" electrons, current due to tunneling

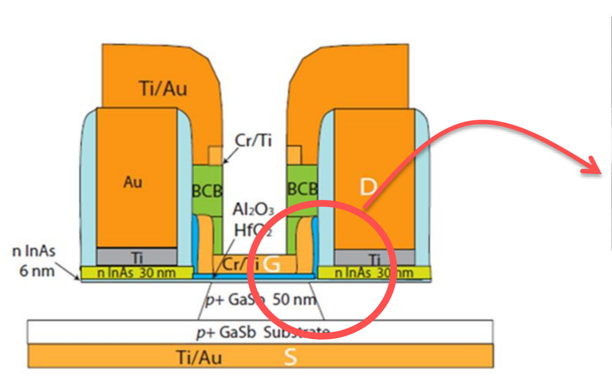




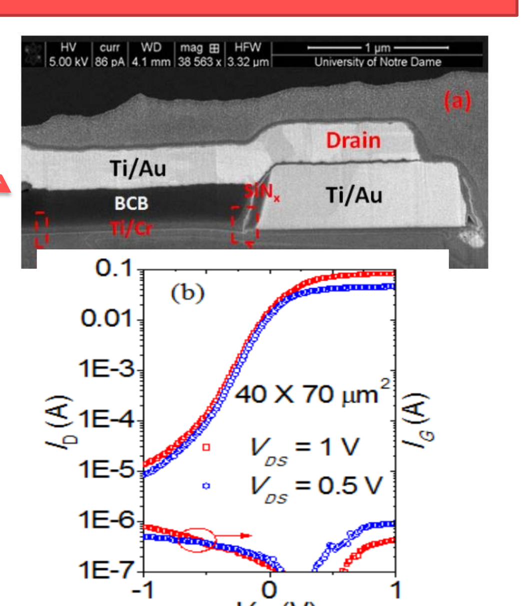
Tunneling current depends on bandgap at tunneling junction.

- Power consumption prevents performance improvement by increasing clock frequency.
- TFETs outperform MOSFET in power efficiency.

Record High I_{on} in Gate-recessed TFETs



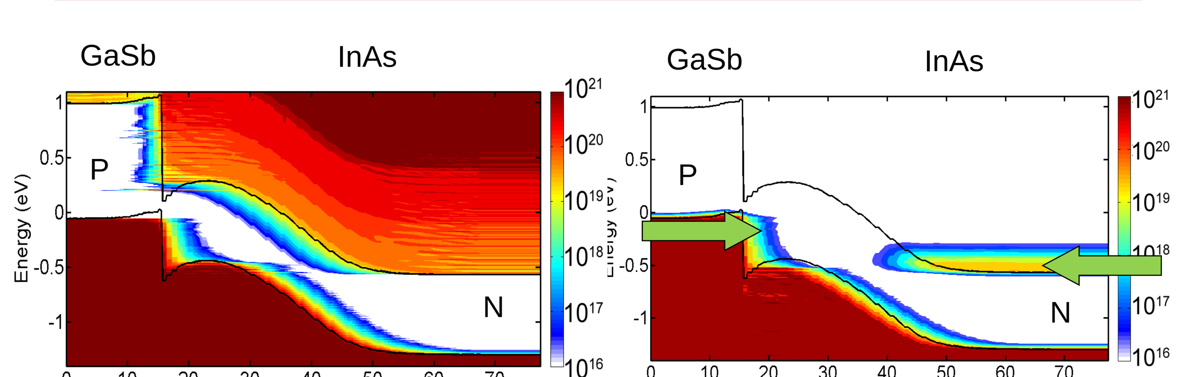
record high I_{ON} of 180 µA/µm achieved at V_{DS} = 0.5 V



Features:

- ✓ Broken-gap GaSb/InAs heterojunction
- ✓ Tunneling direction in-line with gate field
- ✓ Low drain contact and access resistances due to gate-recess process

TFET Electrostatics



Local density of states — Electron density

Electrostatics in TFET:

- Bandgap blocks electron injection from source contact
- Channel is in equilibrium with drain contact → channel follows drain Fermi distribution
- Low charge density in channel → low capacitance

Electrostatics for TFET is much simpler than MOSFET Channel is in ***quasi-equilibrium*** for most biases

METHODS

Two Common Methods for Simulation

Drift Diffusion (DD) + Wentzel–Kramers–Brillouin (WKB)

- ☺Fast convergence
- ☺Available for big structure
- ☺Easy implementation
- ☹Fitting parameter for tunneling coefficient
- ☹No confinement effects

Atomistic tight-binding based NEGF

- ☺Include complex bandstructure effects
- ☺Suitable for nano-scale device
- ☹heavy computational burden

Combine two methods, improve efficiency!

Hybrid Solver: Drift-diffusion + NEGF

Method:

- Semi-classical density with quasi-Fermi level to get potential
- NEGF transport on top of semi-classical potential

1) DD: Band edges for carrier injection

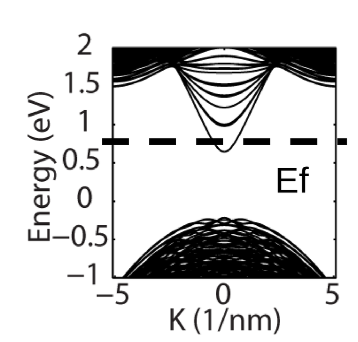
Band edges are extracted from the lead unit cell, which depends on structure and material.

2) DD: Fermi level in the leads

Self-consistent calculations determine differences between band edges and Fermi levels

3) DD: Density of states (DOS)

3D DOS with parabolic band is assumed in the drift diffusion: Effective DOS matching the same Fermi level and density as calculated



3-dimentional DOS for DD simulation

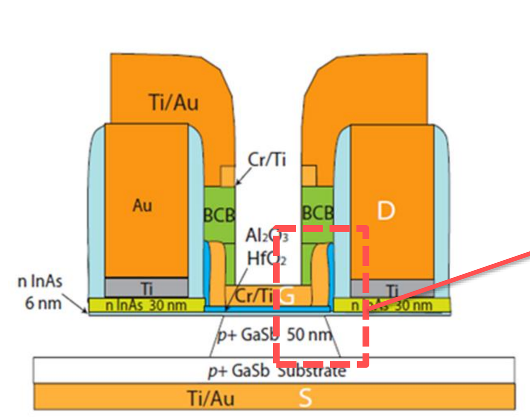
4) Self-consistent DD calculation for electrostatic potential

$$n = N_C \frac{2}{\sqrt{\pi}} F_{1/2}(\eta_C)$$

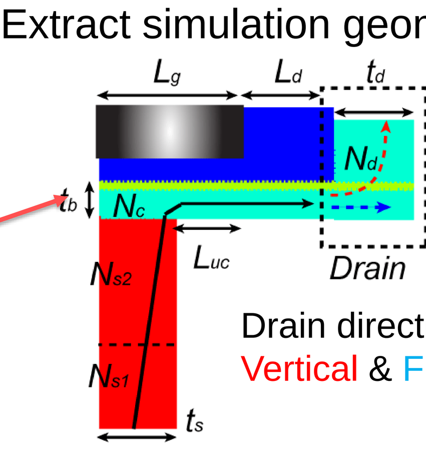
Resulting electrostatic potential from DD is used as the final potential for the NEGF calculation

RESULTS

Gate-recessed TFETs

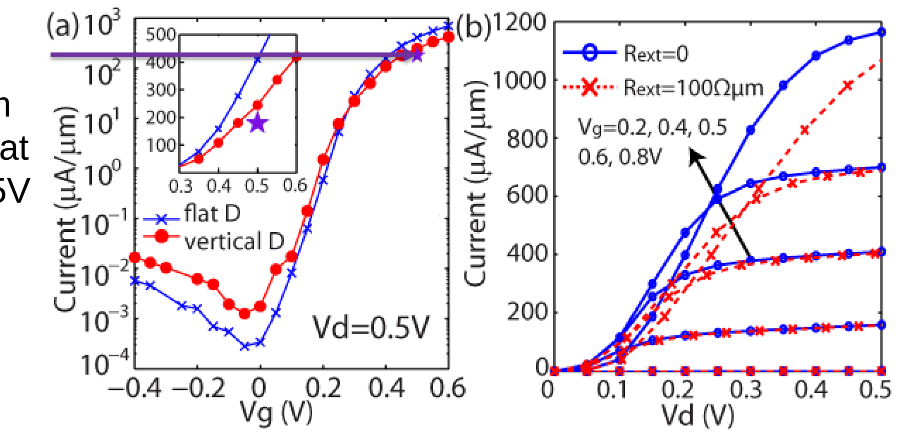


Extract simulation geometry



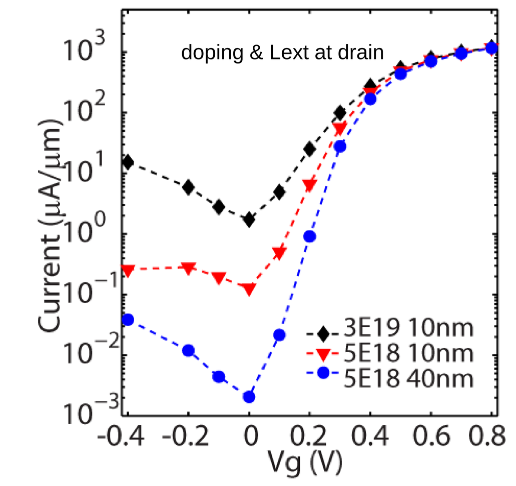
Drain directions: Vertical & Flat

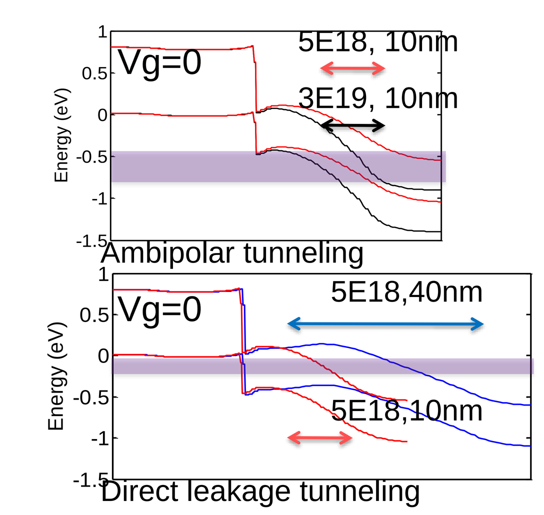
Ion = 180µA/µm measured at Vg=Vd=0.5V



- Vertical drain will introduce additional resistance.
- Low contact resistance due to recessed gate process shows small effects when gate Vg=Vd=0.5V.
- Overall performance improved.

Effects of Drain Extension & Doping



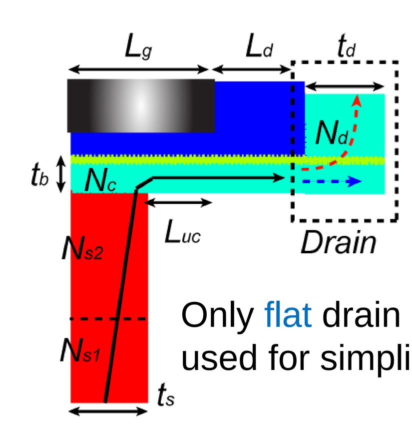


Results:

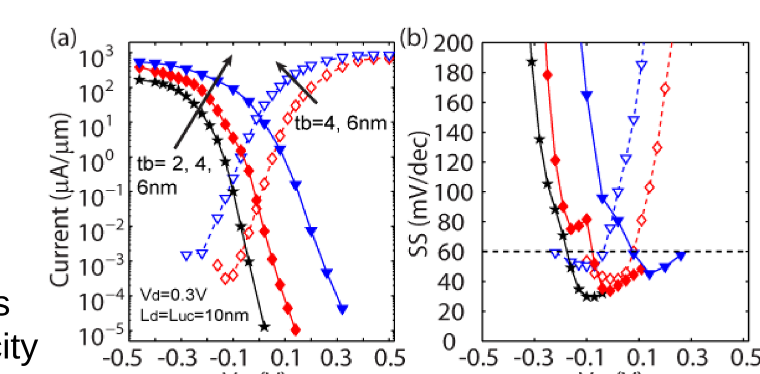
- 6nm InAs drain: 1) small band overlap → high ON current 2) small InAs bandgap → high leakage current
- Moderate doping improves SS → bandgap blocks ambipolar tunneling
- Long drain extension blocks direct leakage tunneling and improves SS

Comparison with Other Architectures

Top-gated TFET

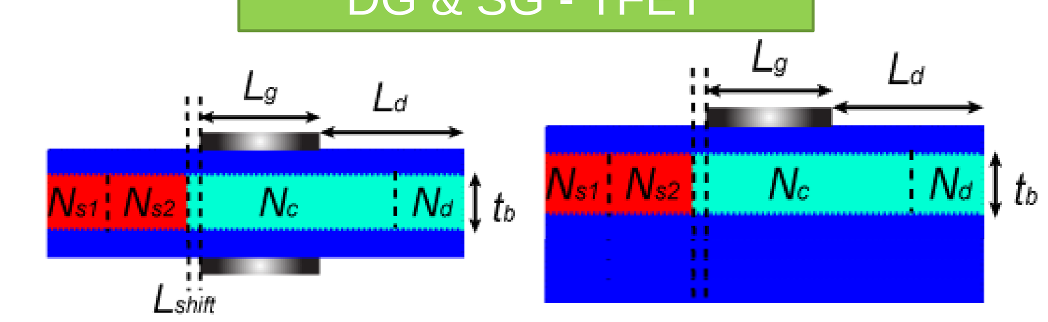


Only flat drain is used for simplicity

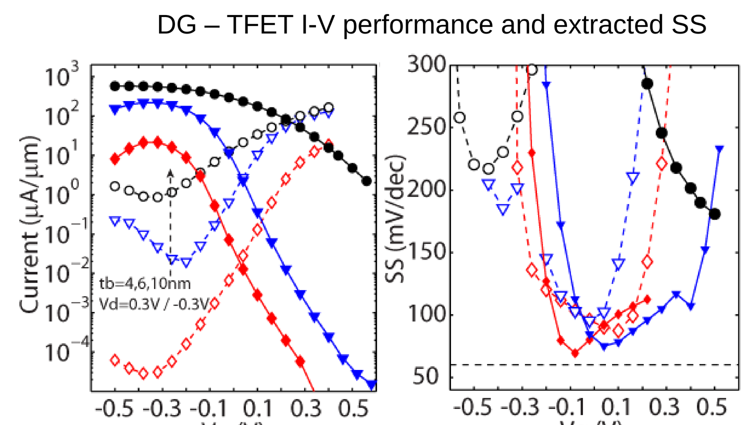


SS < 60mV/dec achieved in both N- and P-type. P-type shows better SS due to small ambipolar current.

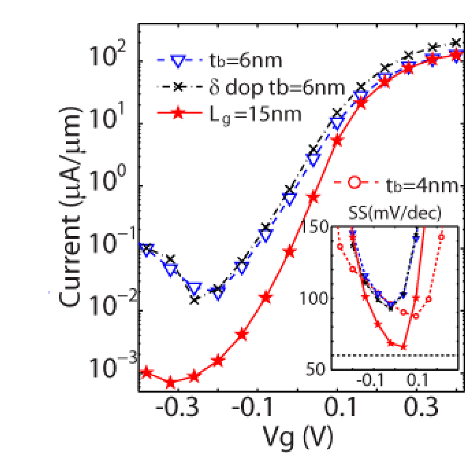
DG & SG - TFET

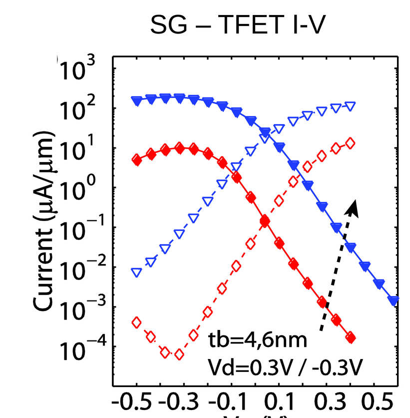


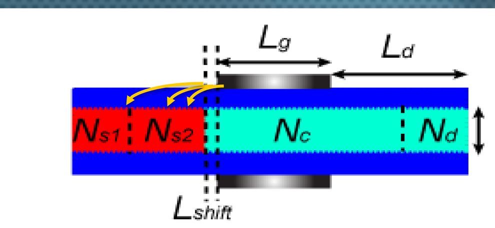
DG – TFET I-V performance and extracted SS — SG – TFET I-V



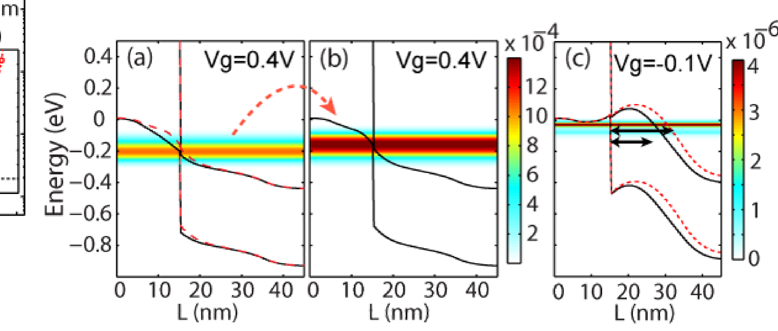
SS > 60mV/dec for all biases. Electrostatic control improved by double-gate structure.







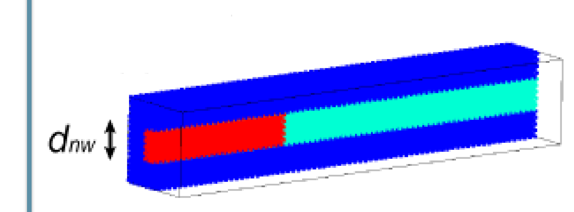
Through oxide, fringing field will couple gate and source and increase tunneling barrier.



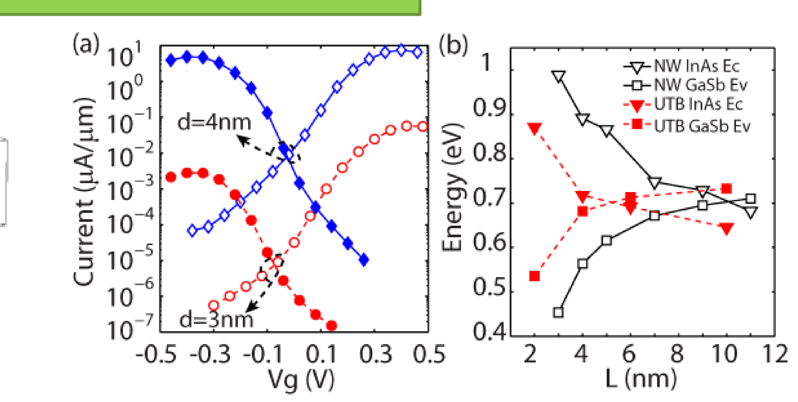
(a-b) Add delta doping layer before tunneling junction. (c) Increase gate length or shift gate position by L_{shift}

By improving doping and geometry, leakage current could be minimized and SS for UTB could be optimized.

NW-TFETs



Nanowire TFET



NW-TFET shows better SS then UTB due to better electrostatic control, but current level is small. Optimized diameter is critical for better current vs. gate control.

Summary

Objectives

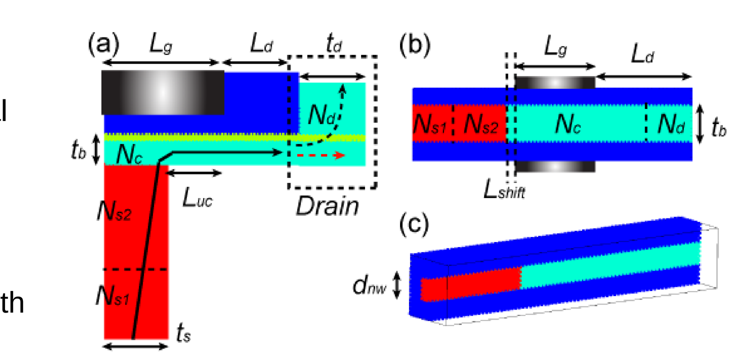
- Comparison of device performances for L-shaped vertical TFETs, UTB TFETs and nanowire TFETs

Methods

- NEGF + Drift Diffusion potential with corrected parameters

Results

- L-shaped TFETs show best performance among III-V TFETs
- Scaling of L-shaped TFETs limited by undercut lengths
- Current of UTB TFETs affected by source-gate coupling
- NW TFETs suffer from small current due to strong confinement



TFETs Device Geometries

	t_b	SS_{min}	I_{on}/I_{max}	I_{off}	L_g	I_{on}/I_{off}
L-nTFET	4	41.5	137.8/693	1e-3	20	1.3e5
L-pTFET	2	29.6	105.7/174	1e-3	20	1.0e5
n-UTB	4	87.4	1.4/18.3	1e-3	10	1.4e3
P-UTB	4	69.4	4.1/21.4	1e-3	10	4.1e3
n-NW*	3	79.5	0.025/0.057	3.2e-5	10	7.8e2
p-NW*	4	61.1	1.28/4.89	1.9e-4	10	6.7e3

CONCLUSIONS

- An efficient hybrid simulation flow is developed to simulation TFET with high accuracy
- Evaluate effects of geometry and doping variations
- Identify leakage source for off current in gate-recessed TFETs
- ➢ Device benchmark: Top-gated TFETs offer best performance, but other architectures could also be further improved.