Extremely thin-body ballistic n-MOSFET designs involving transport in mixed Γ-L valleys

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***Abstract*—Transistor designs based on using mixed Γ-L valleys for electron transport are proposed to overcome the DOS bottleneck while maintaining high injection velocities. Using a self consistent top-of-the-barrier transport model, improved current density over Si is demonstrated in GaAs/AlAsSb, GaSb/AlAsSb and Ge-on-insulator (Ge-OI) based single-gate (SG) thin-body n-channel metal-oxide-semiconductor field-effect transistors (n-MOSFETs). All the proposed designs successively begin to outperform strained-Si-on-insulator (sSi-OI) and InAs-on-insulator (InAs-OI) in terms of ON state currents as the effective oxide thickness (EOT) is reduced below 0.7 nm. InAs-OI still exhibits the lowest intrinsic delay (τ) due to its single Γ valley.**

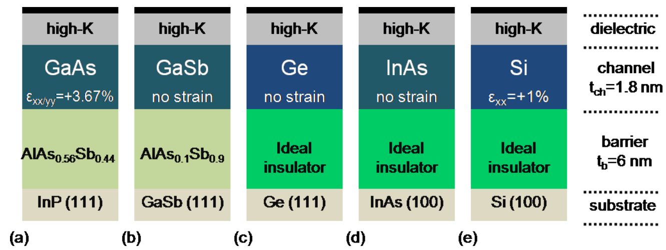

Fig. 1. SG-ETB MOSFET designs (channel/barrier/substrate) involving Γ-L valleys - (a) $GaAs/AlAs_{0.56}Sb_{0.44}/InP$ (b) $GaSb/AlAs_{0.1}Sb_{0.9}/GaSb$ and (c) Ge-OI along with (d) InAs-OI and (e) tensile strained Si-OI.

I. Introduction

HIGH mobility III-V's are projected to be a material of choice for post-Si complementary metal-oxide-semiconductor (CMOS) logic [1]. These III-V materials exhibit high bulk electron mobility because of the light Γ valley that forms its conduction band edge (E_C). A light effective mass also leads to low density of states (DOS), and consequently III-V channel materials provide diminishing benefit over Si as the effective oxide thickness (EOT) is scaled below 0.6 nm [2]. This loss of DOS can be compensated, under (111) confinement, by using several eigenstates of the highly anisotropic L(111) band edge states, or by aligning the Γ and lowest-energy L(111) band edge states (Table I) [3], [4]. Previous work contributing towards this idea utilized idealized interfaces [4]. Another work considered channel thickness (t_{ch}) large enough that renders it unsuitable for a well-behaved SG-MOSFET at sub-10 nm channel lengths [5]. To maintain gate control as channel (L_g) is scaled to sub-10 nm lengths, t_{ch}<3 nm is needed in SG-MOSFETs [6]. In this letter, SG extremely-thin-body (ETB)-MOSFET designs on (111) (Fig. 1(a-c)) are studied and the results are compared against InAs-OI (Fig. 1(d)) and 1% tensile strained Si-OI (Fig. 1(e)) in the ballistic regime at a channel thickness of t_{ch}=1.8 nm.

II. Device Structure

A realistic approach towards designing a (111) SG-ETB-MOSFET requires a careful choice of the channel material, along with a suitable barrier material to confine the carriers and a suitable substrate for fabrication (Fig. 1). The idea behind (111) SG-ETB-MOSFETs is to quantize the anisotropic bulk

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TABLE I
BULK Γ AND L VALLEY BAND-EDGES AND BAND-EDGE MASSES [7]. THE BARRIER HEIGHT (E_b) DIFFERENCE AND VALLEY TYPE UNDER CONFINEMENT (TYPE) IS ALSO SHOWN (* USING $sp^3d^5s^*$ TB MODEL [8])

(111) designs	E_L-E_Γ	E_b-E_Γ	$m^*/m_0(L)$	$m^*/m_0(\Gamma)$	Type
GaAs*/ AlAsSb/InP	385meV	620meV	$m_t = 0.09$ $m_l = 1.73$	$m = 0.046$	Γ-L
GaSb/ AlAsSb/GaSb	63meV	458meV	$m_t = 0.10$ $m_l = 1.3$	$m = 0.04$	L
Ge-OI	-	-	$m_t = 0.08$ $m_l = 1.58$	-	L

L-valley, leading to the formation of multiple L(111) sub-bands with light in-plane transport mass [3]. This necessitates either a channnel material which in bulk has its L-valley either below (e.g. Ge) or only slightly above that of the Γ valley (e.g. GaSb), such that in the thin, quantized channel the L(111) eigenstates are the lowest in energy. A low transport mass with increased DOS can also be obtained by aligning in energy the quantized Γ and L(111) sub-bands in materials having a moderate (0.1-0.4 eV) $\Gamma - L$ separation in the bulk (e.g. GaAs, InAs).

Although we have considered and analyzed many channel designs, we here report in detail only those cases showing high performance [9]. Tensile-strained $GaAs/AlAs_{0.56}Sb_{0.44}$/InP (111) (Fig. 1(a)) was chosen as it is the only case providing $\Gamma - L$ alignment among any composition of strained $In_xGa_{1-x}As/AlAs_{0.56}Sb_{0.44}$/InP (111) for the device structure considered here [10]. Another possible candidate, lattice-matched $GaAs_{0.5}Sb_{0.5}/AlAs_{0.56}Sb_{0.44}$/InP (111) is not discussed here as the confinement of the L-valley bound state is poor, making $\Gamma - L$ alignment difficult. Electron mobility in $GaAs_{0.5}Sb_{0.5}$ is also expected to be poor due to alloy scattering [11]. The strained $In_xGa_{1-x}Sb$ cases were not considered because of the lack of available tight-binding (TB) parameters at the time of the study. For all the cases considered, a channel body thickness of t_{ch}=1.8 nm and a

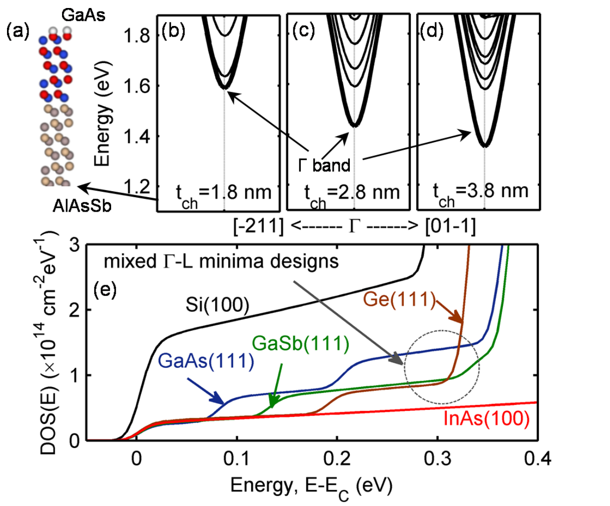

Fig. 2. (a) Atomistic representation of the GaAs/AlAsSb/InP (111) device structure (Fig. 1(a)). Calculated band structure of GaAs/AlAsSb/InP (111) with GaAs thickness (t_{ch}) as (b) 1.8 nm, (c) 2.8 nm and (d) 3.8 nm. The Γ sub-band is highlighted in bold. (e) Calculated DOS(E) vs energy for the different cases considered in Fig. 1.

barrier thickness, t_b=6 nm were used (Fig. 1). Note that at t_{ch}=1.8 nm, the $\Gamma - \mathrm{L}$ valley separation is < 100 meV for the $\mathrm{GaAs/AlAs_{0.56}Sb_{0.44}/InP(111)}$ design (Fig. 2(b)). The III-V (111) $\Gamma - \mathrm{L}$ channel designs are compared to L-valley transport in (111) Ge-OI (Fig. 1(c)) , Γ-valley transport in InAs-OI (Fig. 1(d)) and to uniaxial tensile strained (100) Si-OI (Fig. 1(e)) on (100).

III. Simulation Approach

I_{DS}-V_{GS} characteristics are simulated using a semi-classical top-of-the-barrier transport model by solving the 3-D atomistic Schrödinger (based on $sp^3d^5s^*$ TB model) and 1-D Poisson equation in a self-consistent fashion [12], [13]. The barrier materials are included in the Schrödinger domain for GaAs (Fig. 1(a)) and GaSb (Fig. 1(b)). Because the wavefunctions extend into the barriers, the energy minima and $E-k$ dispersion of the bound states depend signficantly upon the properties of the barrier materials, and we find here different valley energy alignments than if these barriers are neglected [10]. The barriers are sufficiently thick for the wave-functions of the populated bound states to decay to negligible values at the barriers' bottom surfaces; making the simulations insensitive to the substrate parameters. The substrate material is therefore not included in simulations. Lattice mismatch, hence material strain, is of course included in the simulations, i.e. 3.67% in-plane tensile biaxial strain in GaAs (Fig. 1(a)) and 1% uniaxial tensile strain in Si (Fig. 1(e)) [8]. For the cases in Fig 1 (c)-(e), the bottom barrier was treated as an ideal insulator with zero wavefunction penetration. In all cases considered, the gate dielectric is treated as an ideal insulator with zero wavefunction penetration. A zero-electric field boundary condition is applied at the bottom of the barrier to mimic the continuity of the potential profile. The transport direction for all the cases is taken to be <110> except InAs-OI, for which the transport direction is <100>. The ON-state is defined at V_{DS}=V_{GS}=0.6 V, with the threshold voltage set such that off state current is $I_{\mathrm{DS}}^{\mathrm{OFF}}$=0.1 $\mu A/\mu m$. To capture the effect of the increasing dielectric capacitance, the simulations were performed for EOT values ranging from 0.1 nm to 0.7 nm and subsequently ON state characteristics were extracted.

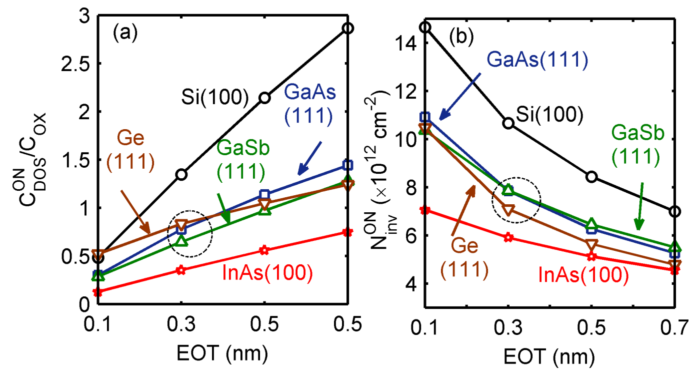

Fig. 3. Calculated ON state (a) C_{DOS}^{ON}/C_{OX} and (b) inversion charge, N_{inv}^{ON} as a function of EOT. The "Γ-L minima designs" are identified by a circle.

IV. Results

The nearly 4:1 difference in DOS between Si and InAs can be readily noted in Fig 2(e). The low DOS is improved by populating two L(111) valley sub-bands for GaSb and Ge (Fig. 2(e)), while the Γ and first two sub-bands of L(111) are populated for GaAs(111). We will refer to the (111) GaSb, Ge, and GaAs cases (Fig. 1(a-c)) as "mixed $\Gamma - \mathrm{L}$ minima designs". The DOS bottleneck occurs when the density of states capacitance (C_{DOS}=$q^2\frac{dN_{\mathrm{inv}}}{dE_{\mathrm{fs}}}$) begins to dominate over the dielectric capacitance, C_{OX} i.e. $\frac{C_{\mathrm{DOS}}}{C_{\mathrm{OX}}}$ $<$1, nullifying the expected gains as EOT is scaled to smaller values. From Fig 3(a), it can be seen that InAs (100) suffers from DOS bottleneck at all the values of EOT$<$0.7 nm. It should also be noticed that as the EOT is scaled, first $\Gamma - \mathrm{L}$ minima designs at EOT$\simeq$0.4 nm and Si (100) at EOT$\simeq$0.2 nm also begin to be C_{DOS}-limited. Consequently, as shown in Fig. 3(b), Si (100) exhibits the highest ON state carrier density while InAs (100) has the lowest ON state carrier density. It should also be noted that as the EOT is scaled from 0.7 nm to 0.1 nm, InAs-OI shows $\sim$ 1.5X increment in ON state inversion carrier density, while both Si (100) and "mixed Γ-L minima designs" exhibit $\sim$ 2X increment in ON state inversion carrier density. This highlights the relative advantage of higher DOS as dielectrics are thinned.

Fig. 4(a) shows the ON state currents for the different ETB MOSFET cases. Note that even for 0.1 nm EOT, InAs (100) shows larger $I_{\mathrm{DS}}^{\mathrm{ON}}$ than Si (100). This conclusion differs from that of [2] because of the thin 1.8 nm channel considered here. Given the strongly nonparabolic InAs Γ valley, the E_C edge mass increases from its bulk value of 0.023 m_0 to 0.08 m_0 for a 1.8 nm thin quantum well [3], [8]. At the same time, the proposed Γ-L minima designs begin to outperform InAs (100) as EOT is scaled. In terms of the ON state current, GaSb outperforms InAs at EOT=0.7 nm, GaAs outperforms InAs at EOT=0.5 nm and Ge outperforms InAs at EOT=0.3 nm At the

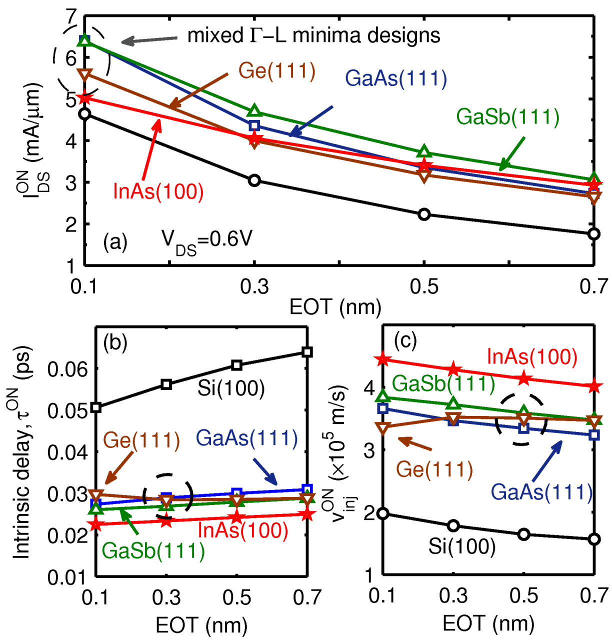

Fig. 4. Calculated ON state (a) drain current and (b) the intrinsic transit delay, τ^{ON} (assuming L_g=10 nm) and (c) injection velocity, $v_{\mathrm{inj}}^{\mathrm{ON}}$ for the different ETB-MOSFET cases as a function of EOT.

extreme limit of EOT=0.1 nm, GaAs and GaSb deliver ∼27% more current than InAs and ∼36% more current than Si [14]. The calculated transit delay τ^{ON} (=L_g/v_{inj}^{ON}) at the ON state is shown in Fig 4(b). InAs exhibits the lowest delay because of higher injection velocity (v_{inj}) as shown in Fig. 4(c).

V. Conclusion

In this letter SG-ETB designs, that include GaAs/AlAsSb/InP (111), GaSb/AlAsSb/GaSb (111) and Ge-OI (111), that provide both high charge density and high carrier velocity in highly scaled MOSFETs are presented. The performance of the proposed Γ-L minima designs have been compared against InAs-OI (100) and tensile strained Si-OI (100) MOSFETs at the same channel body thickness of 1.8 nm in the ballistic limit. All designs provide larger on current than InAs-OI (100) for EOT<0.3 nm. The proposed transistor designs allow a scope for MOSFET performance improvements even at the extreme EOT scaling limits. These results also suggest that for double gate FinFET designs with (111) side walls, the proposed channel materials would outperform InAs FinFET with (100) sidewalls at EOT<0.6 nm. Future work would include quantum transport simulations including carrier scattering and source-drain tunneling, that becomes more relevant as L_g is scaled to sub-10 nm.

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