Design of high-current L-valley $GaAs/AlAs_{0.56}Sb_{0.44}/InP$ (111) ultra-thin-body nMOSFETs

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***Abstract*— We propose and analyze a high-current III-V transistor design using electron transport in the Γ- and L-valleys of (111) GaAs. Using $sp^3d^5s^*$ empirical tight-binding model for band-structure calculations and the top-of-the-barrier transport model, improved drive current is demonstrated using L-valley transport in a strained GaAs channel grown on an (111) InP substrate. At a body thickness of 2 nm the (111)GaAs/InP MOSFET design outperforms both (100) Si and (100) GaAs/InP for all EOTs larger than 0.3nm.**

I. Introduction

III-V nMOSFETs have small transport effective mass that provides high electron velocities and high on-state currents. However, small effective mass also leads to a small semiconductor density of states, and consequently III-V channels provide no benefit over Si for EOT < 0.6 nm [1]. This loss of state density can be compensated by using the highly anisotropic L-valley for electron transport [2]. Confining the channel along the (111) direction leads the L-valley to have a large confinement mass and much smaller in-plane transport mass. At some channel thickness, the Γ- and L-valleys are aligned in energy, increasing the state density and on-current [3]. Simulations in [3] ignored interactions of the channel wavefunction with gate dielectric and the well bottom barrier: here we report practical L-valley GaAs channel designs incorporating $AlAs_{0.56}Sb_{0.44}$ barriers to set the boundary conditions for Γ-L alignment.

II. Device structure

Interaction of the channel wavefunction with the amorphous gate dielectric is difficult to compute, hence ideal hydrogen-terminated semiconductor interfaces are often assumed in simulations. To prevent this interaction from changing the Γ-L energy alignment and dispersion, the designs here reported use thin $AlAs_{0.56}Sb_{0.44}$ cladding layers to strongly attenuate the channel wavefunction at the dielectric-semiconductor interface. Fig. 1 shows device geometries. A single-gate (SG) MOSFET consists of a biaxially strained (3.67% mismatch with InP) GaAs channel grown on a 5nm $AlAs_{0.56}Sb_{0.44}$ barrier layer, lattice matched to InP. Two monolayers of $AlAs_{0.56}Sb_{0.44}$ serve as a cap-layer. Similarly, for a double-gate (DG) MOSFET a biaxial strained GaAs with $AlAs_{0.56}Sb_{0.44}$ cap layer on top and bottom are assumed. Similar designs are used for GaAs/InP (100) and Si (100) (no cap layer) for comparison of device performance.

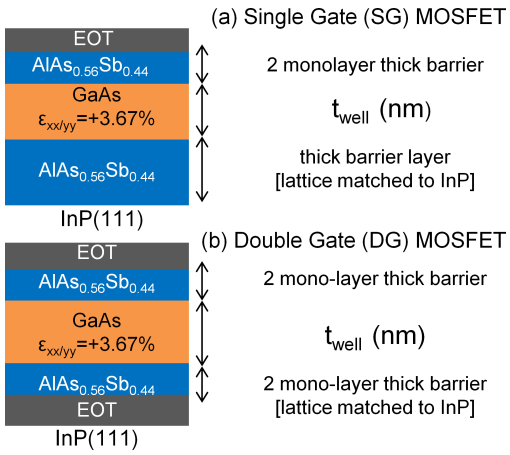

Fig. 1. $GaAs/AlAs_{0.56}Sb_{0.44}/InP$ (111) MOSFETs based on (a) a single gate with strained GaAs channel and $AlAs_{0.56}Sb_{0.44}$ as a capping and barrier layer (b) a double gate structure with strained GaAs channel $AlAs_{0.56}Sb_{0.44}$ capping layer.

III. Simulation Methodology

Band structure calculations of the DG structure (Fig. 1(b)) are performed using an $sp^3d^5s^*$ empirical tight-binding model including spin-orbit coupling [4]. Both the channel material, GaAs and the capping layer $AlAs_{0.56}Sb_{0.44}$ are included. Fig. 2 explicitly shows the effect of including a barrier layer on the band structure calculations. For a 2 nm thick and GaAs thin body structure grown on InP(111) with idealized hydrogen-terminated interfaces, the conduction band minima is formed

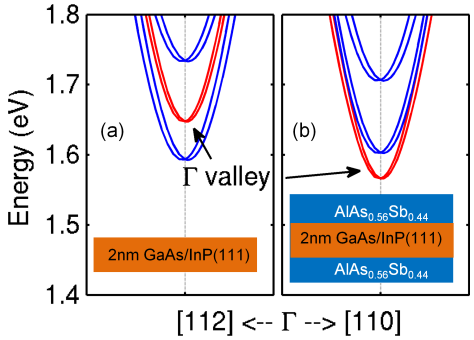

Fig. 2. Bandstructure calculations for 2 nm thick and biaxialy strained (a) GaAs/InP(111) and (b)GaAs/InP(111) with 5 nm thick $AlAs_{0.56}Sb_{0.44}$ layers.

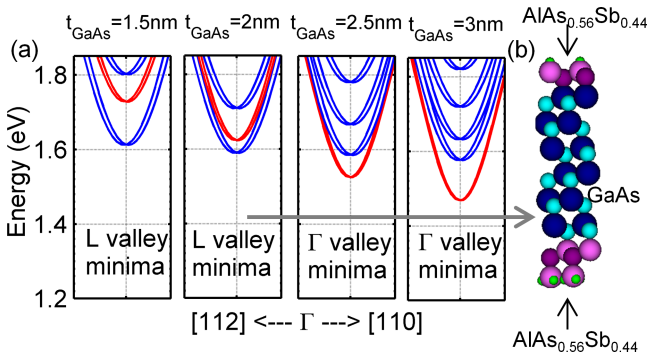

Fig. 3. Tight-binding bandstructure ($sp^3d^5s^*$) calculations for (111) oriented GaAs terminated with 1-2 monolayer $Al_{0.56}As_{0.44}Sb$ lattice matched to InP. The blue lines correspond the L valley states, while the red lines correspond to the Γ valley states.

by the L-valley states. The inclusion of $AlAs_{0.56}Sb_{0.44}$ layers on top and bottom reduces confinement and the Γ valley becomes the lowest-energy band. The density of states and carrier velocity calculated from the band structure are used to calculate I_{on} using the ballistic top-of-barrier transport model implemented in NEMO5 simulation package [5].

IV. Results

From the band structure calculations it is revealed that L-valley minima transistor can be reached by confining GaAs to a 2 nm body thickness (Fig. 3(a)). As a next step, ON state currents are calculated for 2 nm body structures with the channel material as GaAs/InP(111), which is the L-valley minima case, GaAs/InP (100) and Si (100). The on-state current is defined as the current at V_{ds}=V_{gs}=0.5V, with V_{th} set so that $I_{off} = 0.1\mu A/\mu m$. The on-state currents are calculated for different EOT values ranging from 0.3nm to 1.1nm. The degrading effect of the $AlAs_{0.56}Sb_{0.44}$ cap layer on the capacitive coupling of the GaAs channel to the gate is considered by increasing the EOT per gate by 0.1nm.

Fig. 4 compares state density and carrier velocity, and Fig. 5 computed I_{on}. GaAs/InP(111) exhibits a higher density of states than GaAs/InP(100) because of the contribution of higher-energy subbands. Yet, GaAs/InP(111) retains the advantage of a high carrier velocity resulting from the light in-plane transport mass. GaAs/InP(111) has a smaller density of states than Si (100), hence loses its advantage over Si at ultra thin EOT values. For SG and DG MOSFET designs, Si(100) surpasses GaAs/InP(100) in $I_{on} \simeq 1.0$ nm and $\simeq 0.6$ nm EOT, respectively. GaAs/InP(111) exhibits the highest on-current; only at $\simeq 0.3$ nm EOT is Si comparable. At EOT=0.5 nm, considered feasible for MOSFETs at L_g=5nm, the GaAs/InP(111) design delivers 8.5% higher I_{on} than Si(100) DG MOSFETs and 18% higher than Si(100) SG MOSFETs confirming the efficacy of the Γ-L channel designs (see [6]).

V. Acknowledgment

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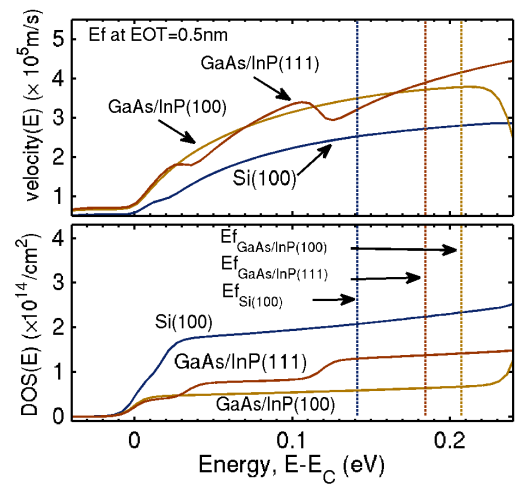

Fig. 4. Density of states and carrier velocity for 2 nm thick GaAs/InP(111), GaAs/InP(100) and Si(100) structures. Fermi level E_f position in the on state for DG MOSFET and EOT=0.5 nm is also shown.

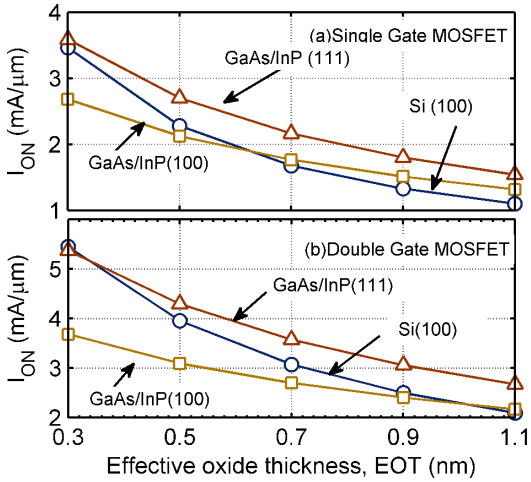

Fig. 5. ON state currents calculated for different EOT values for (a) single gate and (b) double gate structures.

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