Task 6.1: MOSFETs near end of the roadmap

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Sub-8 nm channel lengths predicted by ~ 2020

Device scaling to 8 nm and below...

Will S-D tunneling limit device scaling?

The tunneling phenomenon

Source-drain tunneling a serious challenge below 8 nm...

The tunneling probability

Source-drain tunneling probability can be controlled by transport mass, m*

Toward the nanoscale MOSFETs

- Scaling of the transistors:
  - New device architectures
  - Improve gate control

- Gate-all-around MOSFET
  - Increasing the number of gates offers a better control of the potential

Bandstructure in <100> Si nanowire

Bandstructure in <110> Si nanowire

Device geometry for L_{gate}=3nm MOSFETs

Si / InAs nanowires: orientation/strain effects

Source-Drain tunneling at OFF state

Subthreshold characteristics at L<8nm

ON state performance at L<8nm

Conclusions & Future work

- Device scaling will reach sub 8 nm channel lengths by 2020.
- Moving into S-D tunneling limited regime.
- Tunneling engineering can be used to obtain different transport masses.
- Moving to a heavier transport mass can be advantageous, by limiting source-drain tunneling and improving performance at L<8nm.

FUTURE WORK

- Explore PMOS designs options below L=8 nm.
- Explore the effects of scattering with a heavier mass.