Atomistic Modeling of a Tunable Single-Electron Quantum Dot in Silicon using NEMO3D-peta

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INTRODUCTION

Silicon based quantum computing (QC) structures have been extensively studied due to inherently long spin decoherence time [1]. In particular, the gate controlled metal-oxide-semiconductor quantum dot structure in silicon (Si MOS QD) is of interest since it utilizes state-of-the-art silicon fabrication technology. Recent efforts by Lim et al. revealed that it is possible to control the electron filling in the dot down to a single electron despite the six-fold valley degeneracy of silicon and oxide interface charge [2]. Inherently, the QC operation in Si MOS QD is severely limited by the valley degeneracy. Therefore, large valley splitting (VS) – the energy split between the lowest two energy states – at the single electron regime becomes an important measure of the qubit operability [3]. The QD is electrostatically defined in a cryogenic environment. An understanding of the behavior of VS in Si MOS QD requires an approximate self-consistent methodology to extract VS characteristics in low temperatures and determine the variability of VS as a function of applied bias and gate size.

METHODOLOGY

The Si MOS QD of interested is shown in Fig. 1a and b. Its operation is controlled by five independent gates. L1 and L2 control source and drain, respectively, which provides or extracts electrons in and out of the quantum dot. B1 and B2 gates create depletion region in the channel, which serves as barriers for tunnelling electrons. The plunger gate P over on the top controls electron filling in the middle dot region by raising or lowering the energy level in the dot. Simulation of this device is handled by NEMO3D-peta, a massively parallelized nano-electronic modelling tool that is built to handle large-scale modelling tasks atomistically [4 5]. The simulation domain only includes the center QD region of the MOS structure, controlled by three gates B1, B2 and P. It is assumed that Fermi-level inside the dot

region is maintained and fixed by the source and drain, since the entire device structure is large enough compared to the QD. The SiO_2 thickness is roughly 10nm and the oxide aluminum surrounding each metal gate is ignored in the domain. To investigate gate geometric effects on the VS, the width of the plunger gate is adjusted to four different values (W_C = 30, 40, 50 and 60 nm), while the length is fixed at 30nm. The overall electronic domain is fixed to 60x90x40 and contains about 8 million atoms. The electronic structure of Si substrate is atomistically represented by $sp^3d^5s^*$ tight-binding (TB) Hamiltonian, which automatically includes the six-fold valley degeneracy of Si and has successfully matched experimental VS results in a SiGe-Si-SiGe miscut quantum well [6].
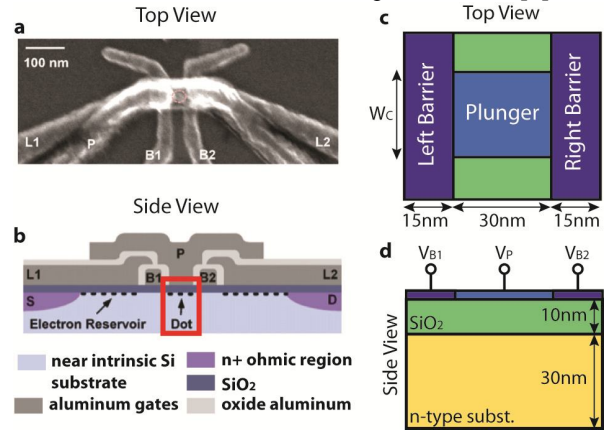

Fig 1. a, b Physical structure of Si MOS QD. Five top gates marked L1/L2/B1/B2/P are on top of the oxide interface to create electron reservoir (L1/L2), barrier between QD and the reservoir (B1/B2) and QD (P). Image taken from Ref.[1] with permission. c, d Simulation domain used in NEMO3D-peta for self-consistent simulation. Central region of the device (solid red box in (b)) is taken and it includes the plunger gate (P) and part of the barrier gates (B1/B2). The total simulation domain size is 60x90x40 (nm^3) (8 million atoms).

A standard Schrödinger-Poisson self-consistent simulation scheme is used in solving for the confined potential profile inside the quantum dot. Typically,

self-consistent simulation in an 8-million-atom structure would be computationally intractable, however, the 3D spatial parallelization scheme of NEMO3D-peta can handle large structures such as this in manageable time. At low temperature, the Fermi function acts like a heaviside function. As a result, in order to ensure a single electron in the QD, the ground state of QD must align perfectly with the Fermi level. Therefore, after each self-consistent iteration, the plunger gate bias V_p is adjusted to align the ground energy state with the Fermi level. Under low temperature, even a small change in potential can result in a large fluctuation in the convergence pattern. Therefore, the convergence criteria must be closely monitored and adjusted when necessary. Once the potential profile converges, the VS is extracted as the difference between the lowest two eigenstates.

SIMULATION RESULTS

NEMO3D-peta has exceptional scaling abilities, as shown in the almost ideal scaling graph in Fig. 2. The efficient 3D spatial parallelization scheme has allowed the eigenstate calculation of 8-million atom structure to be performed in the range of hours.

Simulations are performed over various bias combination and gate width. The VS ranges from 100~500µeV, which is comparable to the experimental result of 100 µeV [2]. Fig. 3a shows that the plunger gate bias V_P and barrier gate bias V_B must change in opposite ways in order to preserve a single electron in the dot. For QD with smaller gate size, a large gate bias is required to obtain the same number of electron. Plots of VS dependence in Fig. 3b show that VS increases with potential confinement strength and electric field, which is in agreement with other modelling work [7].

CONCLUSION

The quantum dot region in Si MOS structure has been successfully modelled with NEMO3D-peta. The electronic structure of Si substrate is represented by an atomistic sp3d5s* tight-binding Hamiltonian. NEMO3D-peta utilized an efficient 3D spatial parallelization scheme that allowed self-consistent simulation of 8-million-atom substrate within realistic time limit. The calculated VS value is comparable to known experimental results. The effect of gate size on VS as well as VS dependence on electric field has also been explored and results showed reasonable trend.

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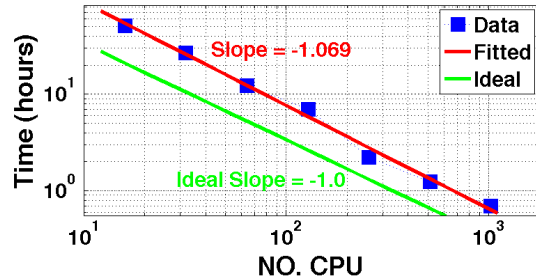
Fig 2. Electronic structure calculation time as a function of the number of processors for a 60x90x40nm³ domain containing 8 million atoms.
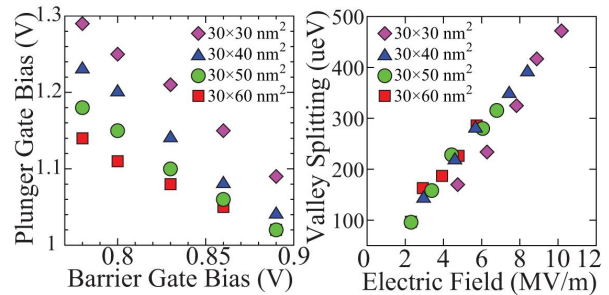

Fig 3. a. Combination of gate biases that satisfies single electron regime QD. Plunger gate bias V_P and barrier gate bias V_B must change in opposite ways in order to preserve single electron in the dot. For QD with smaller gate size, a large gate bias is required to obtain same number of electron. b. The electric field dependence of VS for different QD sizes. The electric field is related to the confinement along the substrate direction and smaller VS is expected for weaker electric fields.