Contact Modeling and Analysis of InAs HEMT Transistors

Seung Hyun Park, *Student Member, IEEE*, Hong-Hyun Park, Mehdi Salmani-Jelodar, *Student Member, IEEE*, Sebastian Steiger, Michael Povolotsky, Tillmann Kubis, *Member, IEEE*, and Gerhard Klimeck, *Senior Member, IEEE*

***Abstract*— Novel device concepts and better channel materials than Si are required to improve the performance of conventional metal-oxide-semiconductor field-effect transistors (MOSFETs). The exploration of III-V semiconductors is mainly driven by the extremely high electron mobility of the materials. Recently, several researches have demonstrated that III-V high electron mobility transistors (HEMTs) can achieve high-speed operation at low supply voltage for applications beyond Si-CMOS technology. While the intrinsic device performance looks promising, current prototypes are dramatically influenced by high contact resistances. From a modeling point of view the understanding of the intrinsic device performance is now quite advanced, while the understanding of the contacts remains quite limited. Hence, a precise theoretical approach is required to model the contact characteristics. This work investigates the contact resistance physics of InAs HEMT transistors. The Nano-Electronic Modeling Tool (NEMO5) is used to solve the non-equilibrium Green's function (NEGF) formalism which embeds Schrödinger and Poisson equations self-consistently. For this study a real-space effective mass approximation with a simple phonon scattering is utilized.**

I. Background

The exponential miniaturization of Si CMOS technology has been a key to the electronics revolution [1]. Meanwhile, the continuous downscaling of the gate length is the biggest challenge. Both industry and academia have been studying new device architectures and materials to solve this issue. The usage of III-V materials turned out to be one of the promising candidates for a post Si era due to extremely high electron mobility. For instance, it was shown recently that III-V HEMTs can achieve high-speed operation at low supply voltage for future logic applications [2-10].

However, the contact resistance of such HEMTs has not been fully understood, yet it is clear that the contacts dominate the overall performance of these nano-scale transistors. Therefore, a precise contact modeling is required to optimize the extrinsic part of the device for performance improvement [11].

This paper is composed of 4 sections. Section II describes details of device modeling in a InAs HEMT. Also, applied simulation approach is introduced. Section III shows results of the intrinsic and extrinsic domain simulations of InAs HEMT. Finally, Section IV summarizes the contents in the previous sections, and the conclusion and the outlook are presented.

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Seung Hyun Park and Mehdi Salmani-Jelodar are currently working toward the Ph D degree in the school of Electrical and Computer Engineering at Purdue University, West Lafayette, IN 47907 USA (e-mail: park43@purdue.edu / msalmani@purdue.edu).

Hong-Hyun Park is a post doctoral fellow at Purdue University, West Lafayette, IN 47907 USA. (e-mail: park310@purdue.edu).

Sebastian Steiger, Michael Povolotsky, and Tillmann Kubis are post doctoral fellows at Purdue University, West Lafayette, IN 47907 USA.

Gerhard Klimeck is currently a director in the Network for Computational Nanotechnology and a Professor of electrical and computer engineering at Purdue University, West Lafayette, IN 47907 USA. (e-mail: gekco@purdue.edu).

II. Device Details And Simulation Approach

A. Device Details

The device schematic is shown in Fig. 1 (a). In this study, InAs HEMT structure splits into the source / drain contact and the channel as shown in Fig. 1, and a two-step modeling approach is adopted. Such splitting of the simulation domain allows us to study more details about the contact part.

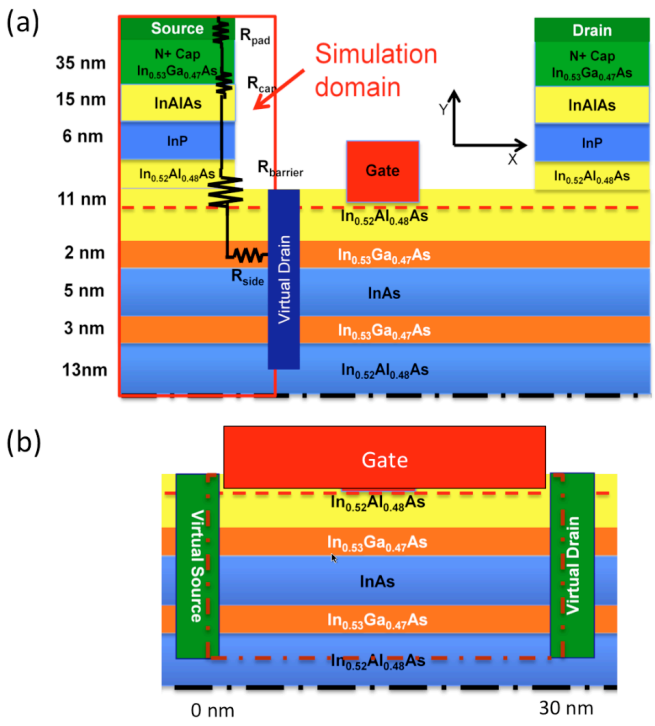

Figure 1. (a) Schematic of the HEMT structure, and the L-shaped hetrostructure simulation domain with a virtual drain. The width of the

source region is 25nm in the simulation. (b) The intrinsic model simulation domain with a gate length of 30nm.

First, the simulation domain of an InAs HEMT structure is the L-shaped contact region to extract series resistance ($R_{S/D}$). Second, we solve the only intrinsic simulation domain as shown in Fig. 1 (b) in the ballistic transport regime. Then, the source (R_S) and drain (R_D) series resistances taken from the first step are added to the intrinsic *I-V* characteristics in a post-processing step. This method is applied in the previous works, and it showed great agreement with experimental data [13-15].

This HEMT device is composed of highly doped $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ n+ cap, InP etch stopper, $In_{0.52}Al_{0.48}As$ barrier, delta-doped layer, $In_{0.53}Ga_{0.47}As$ / InAs channel, and $In_{0.52}Al_{0.48}As$ substrate. The $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ n+ cap layer is n-doped with a donor concentration N_D=2×10^{19} cm^{-2}. A delta-doped layer is n-doped with a donor concentration N_D=5×10^{19} cm^{-2} with 0.5nm thickness, and it is placed below gate contact to induce the channel conduction electrons. These specific set of data such as thickness of each materials and doping concentration are obtained from the previous work and the MIT group [2-4]. To reduce computational cost, the L-shaped simulation domain is chosen from the HEMT structure and the width of the source region is set to 25nm instead of 1-2μm of the real device.

B. Simulation Approach

The 2-D real-space quantum transport simulator capabilities of NEMO5 are used to solve the NEGF Schrödinger and Poisson equations self-consistently [12]. The used effective masses for device materials such as InAs and In0.53Ga0.47As are extracted from tight-binding band structure (sp3d5s*) calculations. To treat electron-phonon scattering the scattering self-energy is calculated self-consistently assuming bulk phonon parameters based on deformation potential theory [13]. For typical parallel processing computation time require about 20 hours on 960 cores on two 2.1 GHz 12-core AMD 6172 processor [14].

III. Results And Discussion

In this study, the series resistance of the source / drain regions of InAs HEMT structure is modeled into L-shaped simulation domain. First, the contact resistance between the channel and the cap is investigated to extract the series resistance ($R_{S/D}$) [4, 15]. This contact resistance is associated with various factors such as the hetero-barrier layers, contact pad, and electron-phonon scattering. The InAs HEMT device schematic is shown in Fig. 1. The scattering self-energy implementation is documented elsewhere [13].

Fig. 2 shows the electron density profile: The heavily n-doped cap has the highest electron density and lowers the $In_{0.52}Al_{0.48}As$ and InP barriers. Electrons are strongly confined within the $In_{0.53}Ga_{0.47}As$ / InAs quantum well.

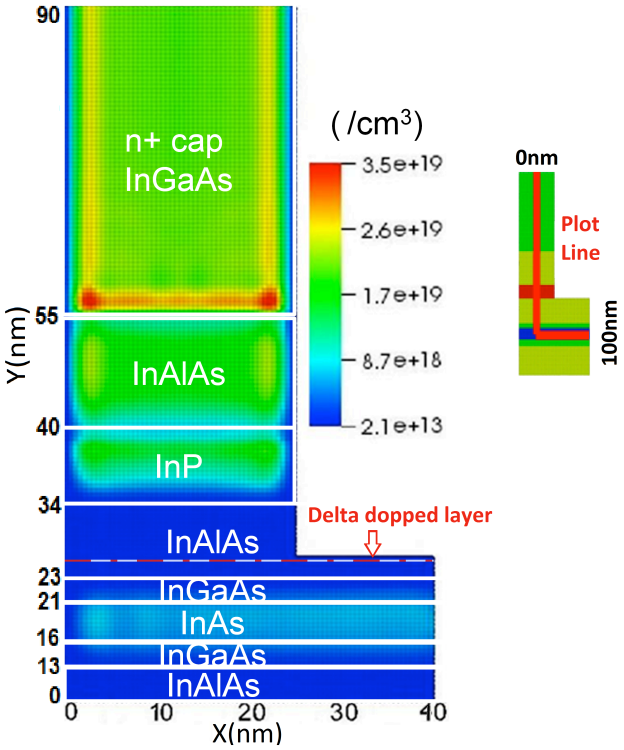

Figure 2. Electron density profile on the contact region is shown in the left figure. The plot line which is used for drawing Fig 3 is depicted in the right side.

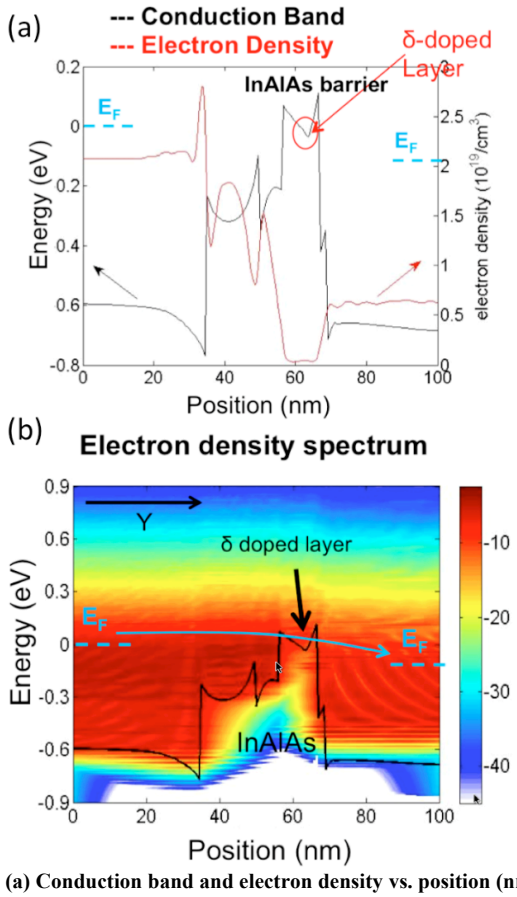

Figure 3. (a) Conduction band and electron density vs. position (nm) (b) Electron density spectrum and conduction band along the polt line depicted in Fig. 2.

The electron density spectrum and conduction band edge shown in Fig. 3 (a) and (b) demonstrate that electrons are well-thermalized at the contact regions due to electron-phonon interactions. When the bias is increased, electrons start flowing over the thick $In_{0.52}Al_{0.48}As$ barrier.

The obtained $R_{S/D}$ is measured at V_{DS}=0.0~0.15V due to a voltage drop in the contact region, and the measured data for each V_{DS} is shown in Fig. 4 (a). Since effects of Schottky barrier, impurity scattering, band non-parabolicity, and inter-valley phonon scattering are not yet included, the most resistance of the contact region is from hetero-barrier layers and phonon scattering in the current contact resistance model. The measured resistance is quite close to the experimentally measured resistance [2, 4]. The simulation results indicate that the $In_{0.52}Al_{0.48}As$ barrier between n-doped cap and $In_{0.53}Ga_{0.47}As$ / InAs quantum well plays an important role in the series resistance.

As mentioned earlier, the attained ballistic I_D-V_{GS} characteristics requires a post-processing step to add series resistance where $V^*_{GS} = V_{GS} - I_{ON}R_S$ accounts for the correction. As shown in Fig. 4 (b) the series resistance significantly reduces the drain current in the ON-state. It shows that the contacts resistance dominate the overall performance of these nano-scale transistors.

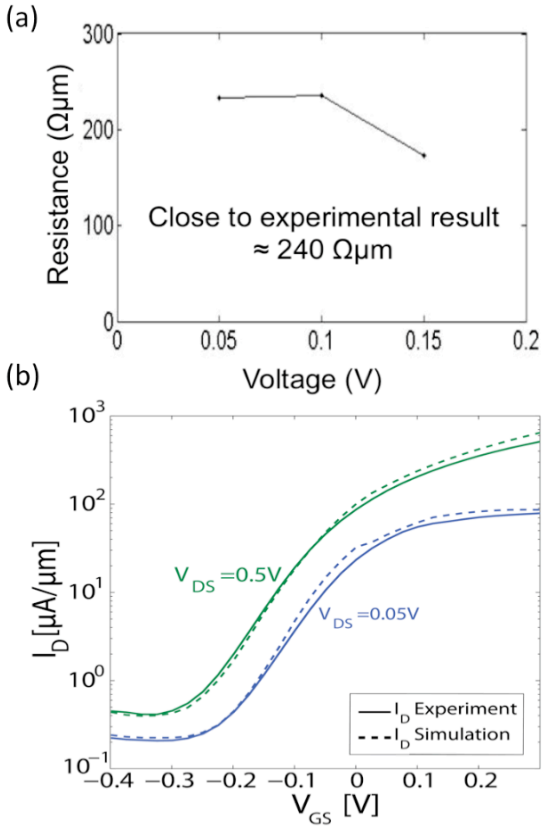

Figure 4. (a) Resistance vs. biased voltages for the L-shaped contact simulation domain. (b) Simulated I_D-V_{GS} characteristics for 30nm channel length InAs HEMT device with measured series resistance ($R_{S/D}$) from Fig. 4 (a) for two given drain voltage V_{DS} = 0.05 V and V_{DS} = 0.5 V with different gate voltages V_{GS} from 0.0 to 0.3 V.

The achieved results indicate a good match with experimental I_D-V_{GS} data for the 30nm InAs HEMT. There is still discrepancy of ON-currents between simulated and experimental results, and the obtained simulation result underestimates the series resistance ($R_{S/D}$). We expect that the discrepancy might be from effects of Schottky barrier, band non-parabolicity, and inter-valley phonon scattering. Also, the deformation potential phonon model is in further need of improvement.

IV. Conclusion and Outlook

The understanding of the origin of the contact resistance remains limited, even though the effects of contact series resistance on the nano-scale transistors are quite important. In this paper, we have investigated the contact-to-channel resistance of the InAs HEMT, and extracted the series resistance ($R_{S/D}$) from the contact simulation domain. The contact-to-channel area is explored to find various series resistance factors such as the hetero-barrier layers, contact pad, and electron-phonon scattering.

The simulation results indicate that the $In_{0.52}Al_{0.48}As$ barrier plays an important role in the series resistance, and the obtained resistance is close to the experimentally measured results. We compared with experimental data from 30nm gate length of InAs HEMT with simulation results by applying the obtained series resistance in the post-processing step. The results prove that of III-V FETs optimization process of the extrinsic part of III-V FETs is essential to improve the performance. There are on-going works to further study the various contact resistance factors.

Acknowledgement

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