Validation

Detection latency → Recovery time → Repair ends

Assumption of no concurrent error
⇒ In this time window, no additional error happens

Detection coverage
- Accuracy (or recall)
- Precision

S: Success  F: Failure

Ground truth:

F  S  F  F  F  F  S  S  S  S  S  S

Detection algorithm says:

S  S  F  F  F  S  F  F  F  S  S

Accuracy = Out of the denominator, how many did the detection algo catch

\[ \frac{\text{Total \# real failures}}{\text{Total \# real failures}} \]

Precision = Out of the denominator, how many are actual failures

\[ \frac{\text{Total \# failures flagged by the detection algo}}{\text{Total \# failures flagged by the detection algo}} \]
Here, \[ \text{Accuracy} = \frac{3}{4} = 75\% \]

\[ \text{Precision} = \frac{3}{5} = 60\% \]

**Hardware gate level faults**

1. **Stuck-at fault**

2. **Inverted fault**

<table>
<thead>
<tr>
<th>Fault at transistor level</th>
<th>Fault at gate level</th>
<th>Fault in software</th>
</tr>
</thead>
<tbody>
<tr>
<td>one-to-one</td>
<td></td>
<td></td>
</tr>
<tr>
<td>one-to-many</td>
<td></td>
<td></td>
</tr>
<tr>
<td>many-to-one</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>many-to-many</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: The table indicates that there is a one-to-one correspondence between faults at the transistor level and faults at the gate level, with a checkmark for the one-to-one correspondence. However, there is no direct correspondence indicated for faults at the gate level or software level.