The Devices:
MOS Transistors

References:
Semiconductor Device Fundamentals, R. F. Pierret, Addison-Wesley
Prentice Hall
NMOS Transistor

CROSS-SECTION of NMOS Transistor

Gate Oxide

Source

Polysilicon

Drain

n+

n+

p-substrate

Field Oxide

(SiO₂)

p+ stopper

Bulk Contact

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@ Purdue Univ.
Cross-Section of CMOS Technology
At $x$, the gate to channel voltage equals $V_{GS} - V(x)$
Transistor in Linear Region

- Assume that the voltage exceeds \( V_T \) all along the channel
- Induced charge/area at point \( x \)
  \[ Q_i(x) = -C_{ox}[V_{GS} - V(x) - V_T] \]
- Current
  \[ I_D = -v_n(x).Q_i(x).W \]
  \[ v_n(x) : \text{drift velocity} \quad v_n = -\mu_n E(x) = \mu_n \frac{dV}{dx} \]

\[ \therefore I_ddx = \mu_n.C_{ox}.W(V_{GS} - V - V_T)dV \]

- Integrating over the length of the channel \( L \)
  \[ I_D = K'_n \frac{W}{L}((V_{GS} - V_T).V_{DS} - \frac{V_{DS}^2}{2}) \]
  \[ K'_n = \mu_n C_{ox} = \mu_n \frac{C_{ox}}{T_{ox}} \]
Transistor In Saturation

V_{GS} \quad G \quad V_{DS} > V_{GS} - V_{T}

S \quad n+ \quad V_{GS} - V_{T} \quad + \quad n+
Transistor in Saturation

- If drain-source voltage increases, the assumption that the channel voltage is larger than $V_T$ all along the channel ceases to hold.

- When $V_{GS} - V(x) < V_T$ pinch-off occurs

- Pinch-off condition

$$V_{GS} - V_{DS} \leq V_T$$
Saturation Current

• The voltage difference over the induced channel (from pinch-off to the source) remains fixed at $V_{GS} - V_T$ and hence, the current remains constant.

• Replacing $V_{DS}$ by $V_{GS} - V_T$ in equation for $I_D$ yields

$$I_D = \frac{K'}{2} \frac{W}{L} (V_{GS} - V_T)^2$$

• Effective length of the conductive channel is modulated by applied $V_{DS}$ - Channel Length Modulation
Current-Voltage Relations

Cut-off: \( V_{GS} \leq V_T, \ I_{DS} \approx 0 \)

Linear Region: \( V_{DS} < V_{GS} - V_T \)

\[
I_D = k'_n \frac{W}{L} \left( (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)
\]

\[
k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} \text{ Process Transconductance Parameter}
\]

Saturation Mode: \( V_{DS} \geq V_{GS} - V_T \)

\[
I_D = \frac{k'_n W}{2L} \left( V_{GS} - V_T \right)^2 \left( 1 + \lambda V_{DS} \right)
\]

Channel Length Modulation

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I-V Relations

Linear: $V_{DS} < V_{GS} - V_T$

(a) $I_D$ as a function of $V_{DS}$

(b) $\sqrt{I_D}$ as a function of $V_{GS}$ (for $V_{DS} = 5V$)

NMOS Enhancement Transistor: $W = 100 \mu m$, $L = 20 \mu m$
Threshold Voltage: Concept

\[ V_T = V_{FB} + V_B + V_{ox} \]

\[ V_B = 2\phi_F \]
Energy band diagram

$E_{\text{vac}}$

**Vacuum Level**

$q\phi_m = 4.1\ eV$

$E_f$

Metal (aluminum)

$E_v$

Silicon Dioxide

$E_c$

0.95 eV

8 - 9 eV

$q\chi = 4.05\ eV$

$q\phi_s = q\chi + E_g/2 + q\phi_B$

$E_f$

$E_v$

P-type silicon

$E_c$

$E_g = 1.12\ eV$

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Here, $\phi_m = \phi_s$

Flat band condition

$\phi_s$ can be changed with doping

Bands will not be flat if $\phi_m \neq \phi_s$ -- apply a negative voltage ($\phi_m - \phi_s$) with respect to Si substrate
The electric field causes band bending
- Electric field at any point is the slope of $E_c$ or $E_v$ at that point
- The electrostatic potential ($\psi$) at any point is the net band bending at that point

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MOS-cap: Depletion

Positive gate voltage

Surface potential ($\psi_s$) > 0

For a small positive gate bias:
- Bands bend downwards at the surface i.e. $E_v$ moves away from $E_f$
- Majority carriers (holes) are depleted at the surface

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Surface potential \((\psi_s) > 0\)

\[ \psi_s \text{ (inv)} = 2 \cdot \psi_B = 2 \cdot \frac{k_B T}{q} \cdot \ln \left( \frac{N_a}{n_i} \right) \]

Where,
- \(N_a\) = Doping density in the bulk (cm\(^{-3}\))
- \(n_i\) = Intrinsic carrier concentration \(\sim 10^{10}\) (cm\(^{-3}\))

Inversion layer at the surface

Channel at the surface is inverted when \((\psi_s = 2\psi_B)\)
Threshold Adjustment by Ion Implantation

- Implant a relatively small, precisely controlled number of either boron or phosphorus ions into the near-surface region of semiconductor.
- Implantation of boron causes a positive shift in threshold voltage.
- Implantation of phosphorus causes a negative shift.
- Like placing additional “fixed” charges.

\[
\Delta V = - \frac{Q_I}{C_{ox}} \quad Q_I = \pm qN_I
\]

\((+) :\) donor \( (-) :\) acceptor
Back Biasing or Body Effect

- $V_{SB}$ is normally positive for n-channel devices, negative for p-channel devices.
- Always increases the magnitude of the ideal device threshold voltage.
- Inversion occurs at $\phi_S = (2\phi_F + V_{SB})$.
- Increases the charges stored in depletion region:

$$Q_B = \sqrt{2qN_A \varepsilon_{si} (2\phi_F + V_{SB})}$$
Threshold voltage

\[ V_T = V_{FB} + V_B + V_{ox} \]

\[ V_T = \left( \Phi_{ms} - \frac{Q_I}{C_{ox}} \right) - 2\Phi_F - \frac{Q_B}{C_{ox}} \]
Dynamic Behavior of MOS Transistor

Source of Cap. - Basic MOS structure
- channel charge
- depletion region of resource bias p-n junctions

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The Gate Capacitance

(a) Top view

(b) Cross-section

\[ C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL \]

Can be decomposed into a number of elements each with a different behavior

Source: Intel
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Parasitic capacitance between gate and source (drain) called **Overlap Capacitance** (linear)

\[ C_{gsO} = C_{gdO} = C_{ox} \cdot x_d \cdot W = C_o \cdot W \]

**Channel Capacitance**: \( C_{gs}, C_{gd}, \) and \( C_{gb} \)

**Cut-Off**: no channel, total capacitance = \( C_{ox} \cdot W_{L_{eff}} \) appears between gate and bulk

**Triode Region**: Inversion layer - acts as conductor \( \therefore C_{gb} = 0 \)

Symmetry dictates \( C_{gs} \approx C_{gd} \approx \frac{C_{ox} \cdot W_{L_{eff}}}{2} \)

**Saturation**: Pinch off, \( \therefore C_{gd} \approx 0, C_{gb} = 0 \)

\( C_{gs} \) averages \( (2/3)C_{ox} \cdot W_{L_{eff}} \)
Reverse biased source-bulk and drain-bulk pn junctions
Diffusion Capacitance (Junction Capacitance)

- **Bottom plate**

\[ C_{\text{bottom}} = C_j W L_s, \]

- **Side-wall junctions**

- formed by source \((N_D)\) and \(P^+\) channel stop \((N_{A^+})\)

- graded junction \((m=1/3)\)

\[ C_{\text{sw}} = C'_{\text{jsw}} x_j (w + 2L_s) \]

\[ = C_{\text{jsw}} (W + 2L_s) \]

\[ C_{\text{jsw}} = C'_{\text{jsw}} x_j , \quad x_j = \text{junction depth} \]

- **\(C_{\text{diff}}\)**

\[ C_{\text{diff}} = C_{\text{bottom}} + C_{\text{sw}} \]

\[ = C_j * \text{Area} + C_{\text{jsw}} \times \text{Perimeter} \]

\[ = C_j L_s W + C_{\text{jsw}} (2L_s + W) \]
Junction Capacitance

\[ C_j = \frac{C_{j0}}{(1 - V_D / \phi_0)^m} \]
The Sub-Micron MOS Transistor

- Threshold Variations (Manufacturing tech., $V_{SB}$)
- Parasitic Resistances
- Velocity Saturation and Mobility Degradation
- Subthreshold Conduction
- Latchup
Threshold Variations

- In derivation of $V_T$ the following assumptions were made:
  - Charge beneath the gate originates from MOS field effects
  - Ignores depletion region at the source and drain junctions (reverse biased)
- A part of the region below the gate is already depleted (by source & drain fields), a smaller $V_T$ suffices to cause strong inversion
- $V_T$ decreases with $L$
- Similar effect can be obtained by increasing $V_{DS}$ or $V_{DB}$ as it increases drain-junction depletion region
Threshold Variations

• $V_T$ can also drift over time (Hot-carrier effect)
  – Decreased device dimensions
  – Increase in electrical field
  – Increasing velocity of electrons, can leave Si surface and enter gate oxide
  – Electrons trapped in gate oxide change $V_T$ (increases in NMOS, decreases in PMOS)

• For a electron to be hot, electric field of $10^4 \text{ V/cm}$ is necessary
  – Condition easily met for sub-micron devices
Parasitic Resistances

\[ R_S = \frac{L}{W} R_{\parallel} + R_C \]

Solutions: cover the diffusion regions with low-resistivity material such as titanium or tungsten, or make the transistor wider.
Velocity Saturation (1)

short channel devices

(a) Velocity saturation

\[ \nu_{sat} = 10^7 \text{ cm/sec} \]

Constant mobility (slope = \( \mu \))

\[ E_{sat} = 1.5 \]

(b) Mobility degradation

\[ \mu_n \]

\[ \mu_{n0} \]

\[ 700 \]

\[ 250 \]

\[ E_t (V/\mu m) \]

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Velocity Saturation (2)

\[ I_{DSAT} = v_{SAT} C_{ox} W (V_{GS} - V_{DSAT} - V_T) \]

Linear Dependence on \( V_{GS} \)

independent on \( L \) \( \text{current drive cannot be improved by decreasing } L \)
Sub-threshold Conduction

\[ I_D = K \cdot e^{(V_{gs}-V_t)q/nkT} (1 - e^{V_{ds}q/kT}) \]

SOI has better sub-threshold leakage

(Inverse) Rate of decrease of current: \( \left( \frac{d}{dV_{gs}} \ln(I_D) \right)^{-1} = \frac{KT}{q} \ln 10(1+\alpha) \)

60mV/decade At T= 300°C
Latch-up

(a) Origin of latch-up

(b) Equivalent circuit
Latch-up

- Parasitic circuit effect
- Shorting of $V_{\text{DD}}$ and $V_{\text{SS}}$ lines resulting in chip self-destruction or system failure with requirements to power down
- To understand latchup consider: Silicon Controlled Rectifiers (SCRs)

![Diagram of SCR with current labels](image-url)
Latch-up

If \( I_g \uparrow \Rightarrow I_{c2} \uparrow \)

\( I_{c2} \) is the base current \( I_{b1} \) of the p-n-p transistor

\[ \therefore I_g \uparrow \Rightarrow I_{b1} \uparrow \Rightarrow I_{c1} \uparrow \Rightarrow I_{b2} \uparrow \]

(magnitude of current increases)

If the gain of the transistor are \( \beta_1 \) and \( \beta_2 \)

Then if \( \beta_1 \beta_2 \geq 1 \), the feedback action will turn device ON permanently and current will self destruct device.
Latch-up Triggering

- Parasitic n-p-n & pin-p has to be triggered and holding state to be maintained
- Can be triggered by transient currents
  - Voltages during power-up
  - Radiation pulses
  - Voltages or current beyond operating range

\[
I_{n\text{trigger}} \approx \frac{V_{\text{pnp-on}}}{\alpha_{\text{nnp}}R_{\text{well}}}
\]

\[\alpha_{\text{nnp}}: \text{Common base gain of n-p-n transistor}\]

Similarly, vertical triggering → due to the voltage drop across \( R_{\text{substrate}} \) as current is injected into the emitter
Latch-up Triggering

- Triggering occurs due to (mainly) I/O circuits where internal voltages meet external world and large currents can flow
  - When NMOS experiences undershoot by more than 0.7V, the drain is forward biased, which initiates latchup
  - When PMOS experiences overshoot by more than 0.7V, the drain is forward biased, which initiates latchup
Latch-up Prevention

Analysis of the circuit shows that for latchup to occur the following inequality has to be true

\[ \beta_{n_p n} \beta_{p n p} > 1 + \frac{(\beta_{n_p n} + 1)(I_{Rsub} + I_{Rwell} \cdot \beta_{p n p})}{I_{DD} - I_{Rsub}} \]

where

\[ I_{Rsub} = \frac{V_{benpn}}{R_{sub}} \]

\[ I_{Rwell} = \frac{V_{bepnp}}{R_{well}} \]

\[ I_{DD} = \text{total supply current} \]

The feedback current flowing into n-p-n base is collector current offset by \( I_{Rsub} \). To cause the feedback, this current must be greater than initial n-p-n base current, \( I_b \).
Prevention of latch-up

- Reduce the resistor values (substrate & well) and reduce the gain of parasitic transistors
- Latch-up resistant CMOS process
- Layout techniques
Spice Models

- Level 1: Long Channel Equations - Very Simple
- Level 2: Physical Model - Includes Velocity Saturation and Threshold Variations
- Level 3: Semi-Emperical - Based on curve fitting to measured devices
- Level 4 (BSIM): Emperical-Simple and Popular
# Main MOS Spice Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
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### SPICE Parameters for Parasitics

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### SPICE Transistor Parameters

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## Technology Evolution

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