Systematic PCB Verification Approach:

1. **Parts Completion Check:**
   a. All major components included?
      - Microcontroller/FPGA/SoC/Microprocessor/CPLD?
      - Power supply? Regulation? Battery Management?
      - Sensors?
      - User interface elements? (LCDs, buttons, switches, etc.)
      - Actuator drivers and control? (Motor control? LED driver circuitry? Audio filters and amplifiers? Etc. etc. etc.)
   b. All support components included?
      - Microcontroller system guidelines and/or minimum connection requirements followed?
      - Application circuits and/or relevant app notes for all major components followed?
      - Support components proper package as well as value? (Power circuit support components designed to handle necessary voltages and currents?)
   c. Other components included?
      - Programming header?
      - Reset circuit?
      - Power connector(s)?
      - Mounting holes?
      - Power indicator(s)?
      - Heartbeat LED?
      - Oscillator/clocking circuitry?
      - Debugging LEDs or interfaces?
2. **PCB Footprint Verification Check:**
   a. All parts fit on 1:1 scale printout of PCB
3. **Parts Placement Check:**
   a. Oscillator close to microcontroller?
   b. Decoupling caps close to/under related ICs?
   c. Connectors on board edges?
   d. Parts grouped by system and/or in reasonable way that minimizes routing?
4. **Mechanical/Space Conflict Check:**
   a. Has x- and y- footprint space around electrical pins and pads of all parts been accounted for?
   b. Has z-height of all parts been accounted for?
   c. Has clearance been provided for the bolt heads of all mounting holes?
   d. Have connectors been placed on the outer edges of boards where appropriate? Are they overhanging edges of boards where appropriate? Are they oriented in the correct direction?
   e. Are all mounting and mechanical support holes free of traces and other electrical items?
5. **Routing Completion Check:**
   a. All traces routed? (In Eagle, the ratsnest command will say “nothing to do”)
   b. Oscillator traces clear of interfering signals?
   c. Traces of appropriate widths to handle current being passed? (Including power traces)
   d. Traces entering pads at 90-degree angles (or 45 degree angles, where appropriate)?
6. **Routing Minimization Check:**
   a. Trace lengths have been minimized where possible?
   b. Octagonal (45-degree constrained) layout mode has been utilized, where possible?
   c. Right angles have been removed, except where necessary?
   d. Acute angles have been eliminated from all board routing?

7. **Via Minimization Check:**
    a. Vias have been eliminated to extent reasonable?
    b. Signal planes on opposite sides of boards are connected by vias at reasonable intervals?
8. **Signal Plane Check:**
    a. Signal planes have been included, where reasonable?
    b. Analog ground (AGND), has been separated from the main ground net in accordance with microcontroller datasheets?
    c. Isolation on all signal planes has been set to at least 12 mils?
9. **Silkscreen check**
    a. Silkscreen labels have been provided for all component IDs and connector signal names?
    b. Silkscreen labels have been appropriately placed near components, but not on top of pads or pins?
    c. Pin 1 of all ICs and other polarity-sensitive components (such as diodes) is clearly marked?
    d. Board silkscreen layer includes course and team number (ECE477 Group <x>)?
    e. Board silkscreen layer includes names of all team members, if possible?
    f. Board silkscreen layer includes a descriptive name to identify the board?
    g. Board silkscreen layer includes a revision number and/or last modified date?
10. **Gerber Check**
    a. Gerber files have been inspected by a gerber viewer program (e.g. gerbv) to check for any last-minute software CAM-processing defects