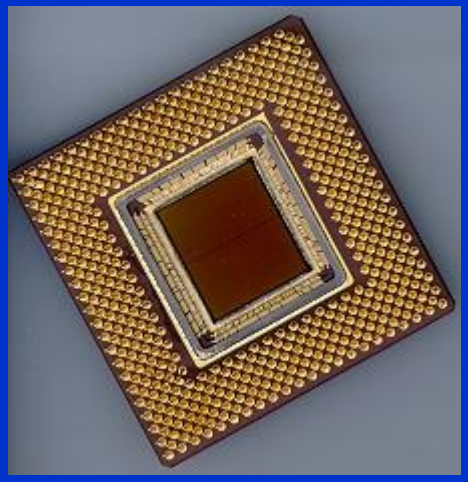
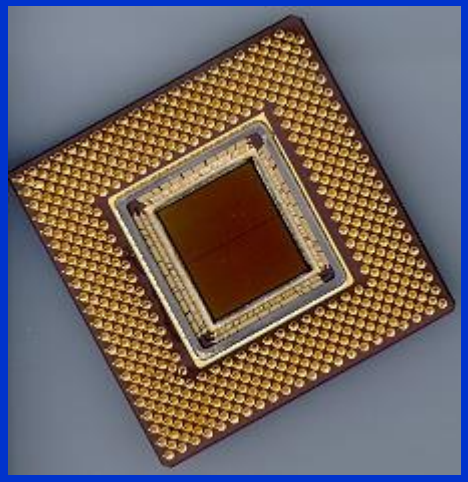


ECE 477 Digital Systems Senior Design Project

Module 2

Digital System Hardware Design Considerations



ECE 477 Digital Systems Senior Design Project

Module 2-A

Logic Levels and Noise Margins

Reading Assignment:

DDPP 4th Ed., pp. 96-103

Learning Objectives:

- **Identify key information contained in a logic device data sheet**
- **Calculate the DC noise immunity margin of a logic circuit and describe the consequences of an insufficient margin**
- **Describe the consequences of a "non-ideal" voltage applied to a logic gate input**
- **Describe how unused ("spare") CMOS inputs should be terminated**

Outline

- Overview
- Data sheets
- Noise
- Logic levels and noise margins
- Non-ideal inputs
- Unused (“spare”) inputs
- Electrostatic discharge

Overview

- **Objective:** To be able to design ***real*** circuits using CMOS or other logic families
  - need to ensure that the "***digital abstraction***" is valid for a given circuit
  - need to provide adequate engineering ***design margins*** to ensure that a circuit will work properly under a variety of conditions
  - need to be able to read and understand data sheets and specifications, in order to create reliable and robust real-world circuits and systems

Data Sheet for a Typical CMOS Device

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE
The following conditions apply unless otherwise specified:
Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

Sym.	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	μA
I_{IL}	Input LOW current	V_{CC} = Max., $V_I = 0$ V		—	—	−1	μA
V_{IK}	Clamp diode voltage	V_{CC} = Min., $I_N = -18$ mA		—	−0.7	−1.2	V
I_{IOS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	−35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	$I_{OH} = -20$ μA	4.4	4.499	—	V
			$I_{OH} = -4$ mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	$I_{OL} = 20$ μA	—	.001	0.1	V
			$I_{OL} = 4$ mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, $I_O = 0$		—	2	10	μA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, $C_L = 50$ pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	$V_{IN} = 0$ V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

NOTES:

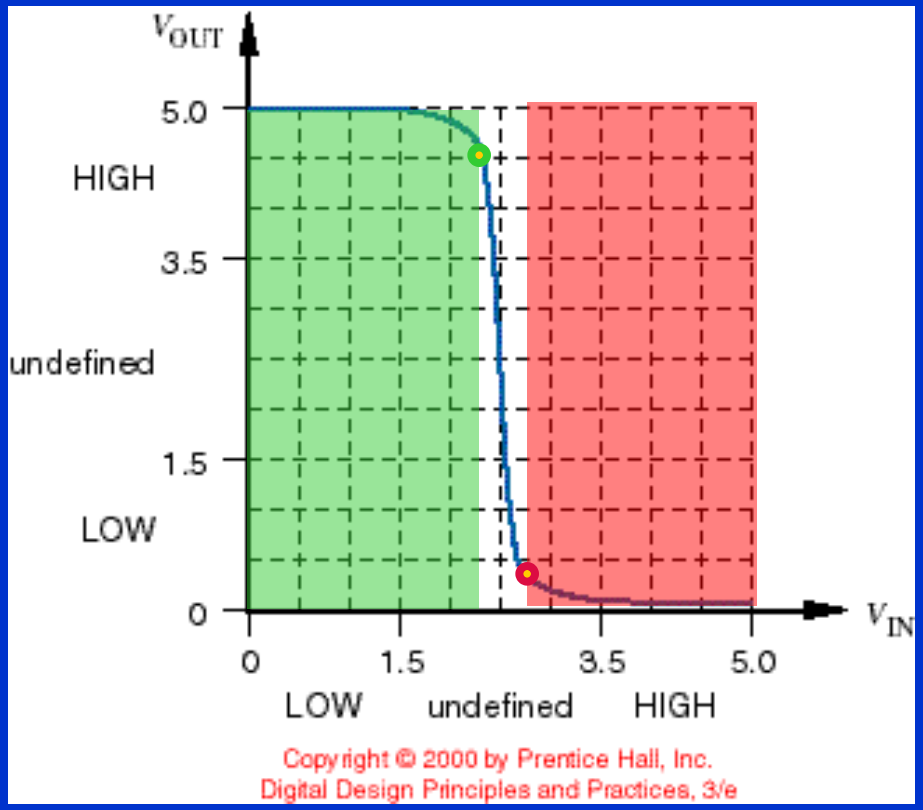
1. *For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.*
2. *Typical values are at $V_{CC} = 5.0$ V, +25°C ambient.*
3. *Not more than one output should be shorted at a time. Duration of short-circuit test should not exceed one second.*
4. *This parameter is guaranteed but not tested.*

Noise

- The main reason for providing engineering design margins is to ensure proper operation in the presence of ***noise***
- Examples of noise sources:
  - cosmic rays
  - magnetic fields generated by machinery
  - power supply disturbances
  - the "***switching action***" of the logic circuits themselves

Logic Levels and Noise Margins

- **Typical input-output transfer characteristic of a CMOS inverter**



<u>Problem</u>:
Typical*, NOT *guaranteed!

Logic Levels and Noise Margins

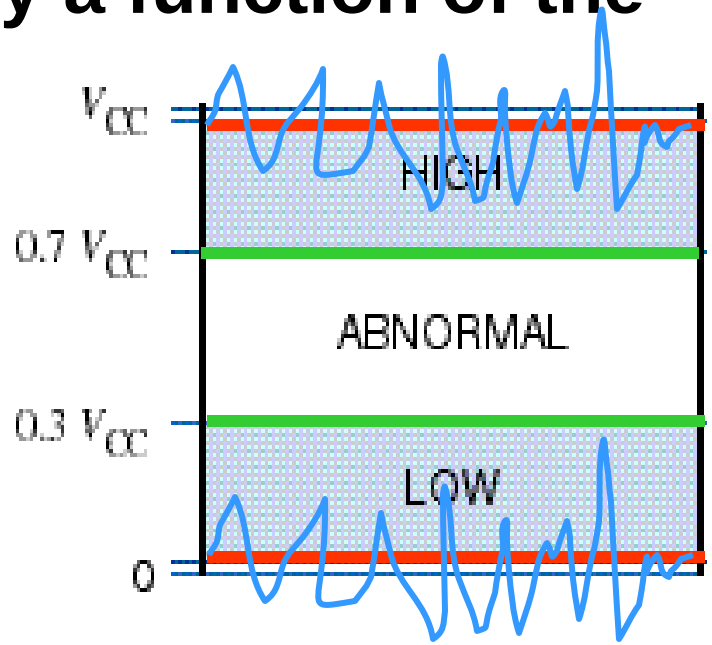
- **Factors that cause the transfer characteristic to vary**
  - **power supply voltage**
  - **temperature**
  - **output loading**
  - **conditions under which a device was fabricated**
- **Sound engineering practice dictates that we use more "*conservative*" specifications for LOW and HIGH**

Logic Levels and Noise Margins

- **Definitions:**
  - $V_{OH_{min}}$ - the minimum **output** voltage in the **HIGH** state
  - $V_{IH_{min}}$ - the minimum **input** voltage guaranteed to be recognized as a **HIGH**
  - $V_{IL_{max}}$ - the maximum **input** voltage guaranteed to be recognized as a **LOW**
  - $V_{OL_{max}}$ - the maximum **output** voltage in the **LOW** state

Logic Levels and Noise Margins

- **CMOS levels are typically a function of the power supply "rails"**
  - **$V_{OH_{min}}$ Vcc – 0.1v**
  - **$V_{IH_{min}}$ 70% of Vcc**
  - **$V_{IL_{max}}$ 30% of Vcc**
  - **$V_{OL_{max}}$ GND + 0.1v**



DC noise margin is a measure of how much noise it takes to *corrupt* a worst-case output voltage into a value that may not be recognized properly by an input

Data Sheet for a Typical CMOS Device

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE
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V_{IK}	Clamp diode voltage	V_{CC} = Min., I_N = −18 mA		—	−0.7	−1.2	V
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			I_{OL} = 4 mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, I_O = 0		—	2	10	μA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, C_L = 50 pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	V_{IN} = 0 V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

Logic Levels and Noise Margins

- Calculation of DC noise margin (or the "noise immunity margin")

$$DCNM = \min (V_{OH_{min}} - V_{IH_{min}}, V_{IL_{max}} - V_{OL_{max}})$$

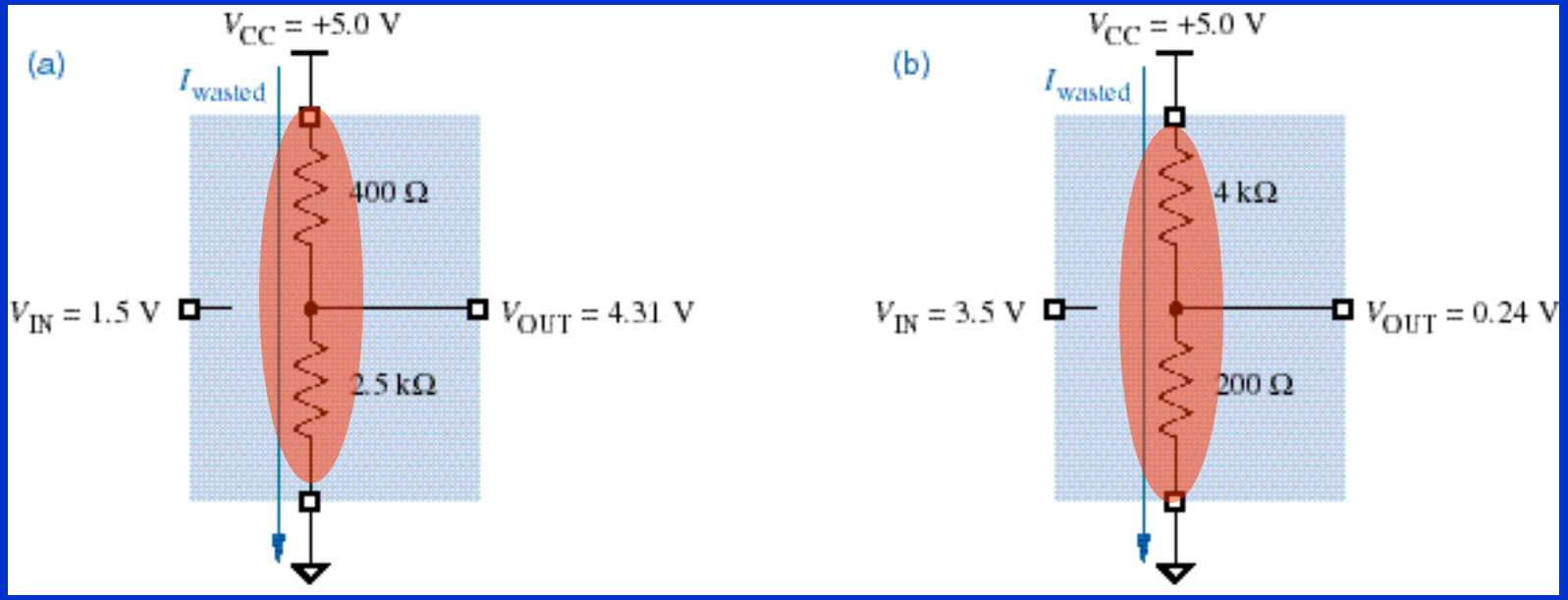
- Example: HC-series CMOS

$$DCNM = \min (4.4 - 3.15, 1.35 - 0.1)$$

$$= 1.25 \text{ v}$$

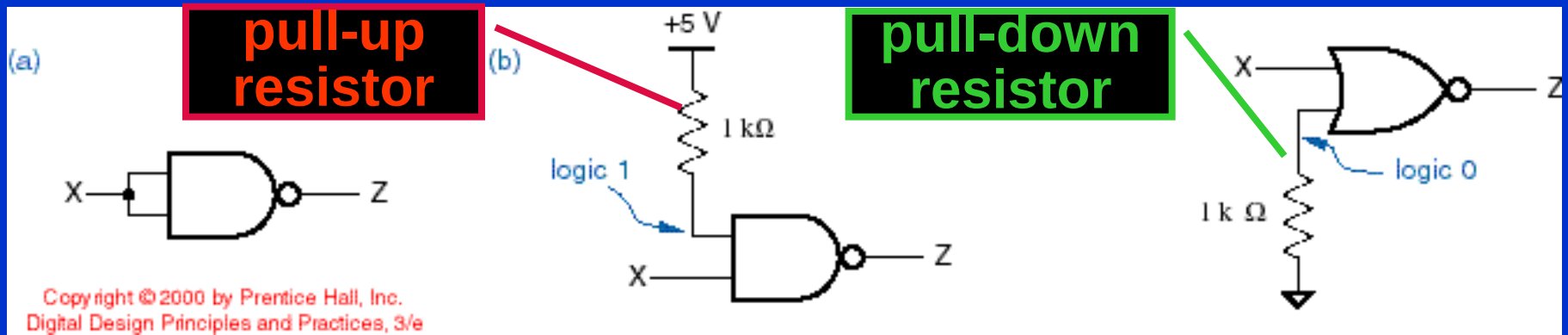
Non-ideal Inputs

- **If the inputs to a CMOS circuit are not close to the Vcc / GND rails, the "on" transistor may not be *fully on* and the "off" transistor may not be *fully off* – causing power dissipation of the device to *increase***



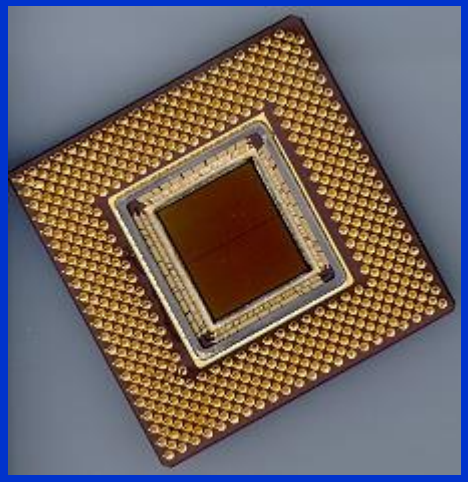
Unused ("Spare") Inputs

- Unused ("spare") CMOS inputs should *never* be left unconnected **("floating")**
- A small amount of circuit noise can temporarily make a floating input look HIGH
- Instead, unused inputs should be:
  - tied to another input of the same gate
  - tied HIGH (for AND and NAND gates)
  - tied LOW (for OR and NOR gates)
  - ***note: most microcontrollers have programmable "pull" devices on input ports***



Electrostatic Discharge

- **CMOS device inputs are subject to damage from electrostatic discharge (ESD)**
- **Apply these precautions in lab:**
  - **before handling a CMOS device, touch a source of *earth ground***
  - **transport CMOS devices in *conductive* bags, foam, or tubes**
  - **handle circuit boards containing CMOS devices by the *edges*; touch a ground terminal on the board to earth ground before "poking around with it"**
  - **use anti-static mats and wrist bands *(be sure to connect to earth ground)***



ECE 477 Digital Systems Senior Design Project

Module 2-B

Current Sourcing and Sinking

Reading Assignment:

DDPP 4th Ed., pp. 103-114

Learning Objectives:

- **Identify key information contained in a logic device data sheet**
- **Describe the relationship between logic gate output voltage swing and current sourcing/sinking capability**
- **Describe the difference between "DC loads" and "CMOS loads"**
- **Calculate V_{OL} and V_{OH} of a logic gate based on the "on" resistance of the active device and the amount of current sourced (I_{OH}) or sunk (I_{OL}) by the gate output**
- **Calculate logic gate fan-out and identify a practical lower limit**
- **Calculate the value of current limiting resistor needed for driving an LED**
- **Describe the deleterious effects associates with loading a gate output beyond its rated specifications**

Outline

- Sourcing and sinking current
- CMOS and DC loads
- Fan-out
- Driving LEDs
- Effects of excessive loading

Sourcing and Sinking Current

- **CMOS gate inputs have a very high impedance and consume very little current from the circuits that drive them**
  - **I_{IL} the maximum current that flows into the input in the LOW state**
  - **I_{IH} the maximum current that flows into the input in the HIGH state**

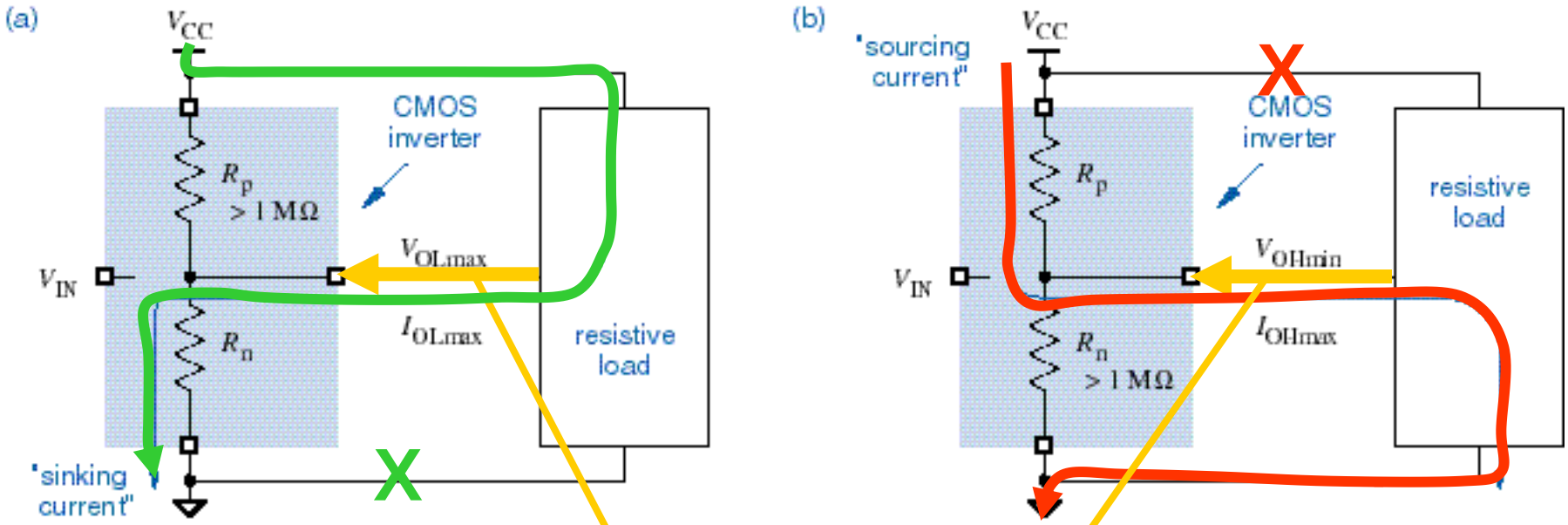
For CMOS logic, the input current is *very small* (about one microamp) – it takes very little power to maintain a CMOS input in either the HIGH or LOW state

Sourcing and Sinking Current

- IC manufacturers specify a maximum load for the output in each state (HIGH or LOW) and guarantee a worst-case output voltage for that load
  - $I_{OL_{max}}$ - the maximum current that the output can "sink" in the LOW state while still maintaining an output voltage *no greater than* $V_{OL_{max}}$
  - $I_{OH_{max}}$ - the maximum current that the output can "source" in the HIGH state while still maintaining an output voltage *no less than* $V_{OH_{min}}$

Sourcing and Sinking Current

- **Circuit definitions of $I_{OL_{max}}$ and $I_{OH_{max}}$**



sinking current (positive)

current arrow

NOTE: Convention is for the input/output current arrows to point "in"

sourcing current (negative)

Sourcing and Sinking Current

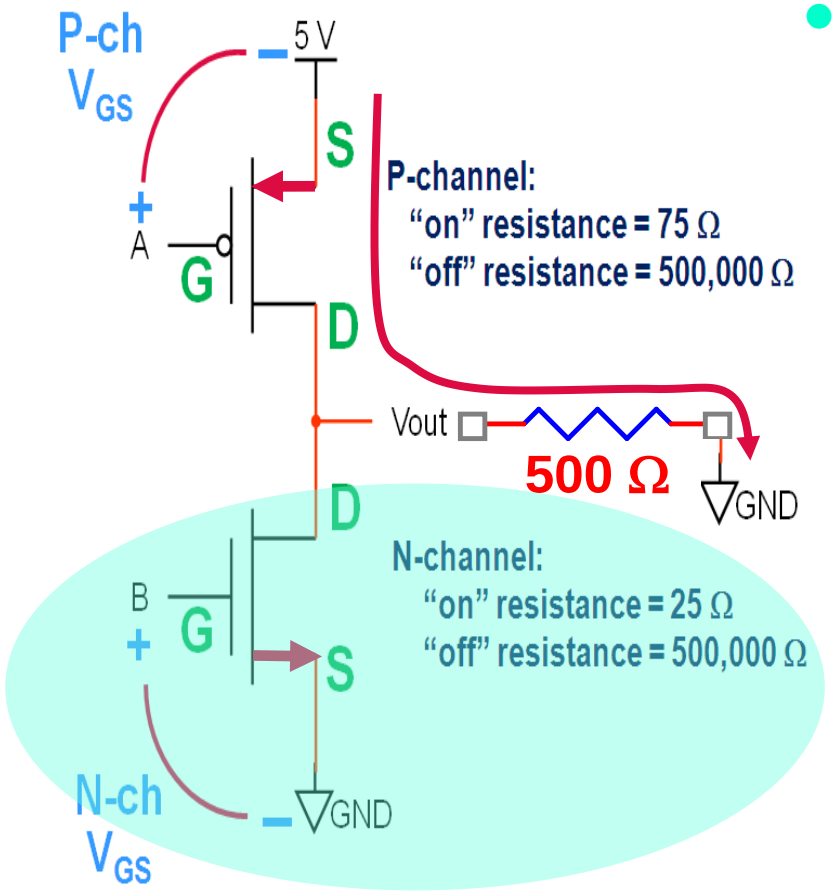
- **Often times gate outputs need to drive devices that require a non-trivial amount of current to operate – called a *resistive* load or *DC* load**
- **When driving a resistive load, the output of a CMOS circuit is not nearly as *ideal* as described previously**
- **In either output state, the CMOS output transistor that is "on" has a non-zero resistance, and a load connected to its output terminal will cause a voltage drop across this resistance**

CMOS and DC Loads

- **Consequently, most CMOS devices have two sets of loading specifications:**
  - **"CMOS loads" – device output connected to other CMOS inputs, which require *very little current* to recognize a "high" input or "low" input**
  - **"DC loads" – device output connected to resistive loads (devices that consume significant current, typically several milliamps)**

Note: With "DC loads" the output voltage swing of a CMOS circuit may significantly *degrade*

Example: Inverter - Current Sourcing



- **Calculate V_{OH} and I_{OH} for A=B=0V**

Current SOURCING configuration

DC Load is 500 Ω resistor between V_{out} and GND

P-ch device is "on" (R_{DS} = 75 Ω)

N-ch device is "off" (R_{DS} = 500,000 Ω)

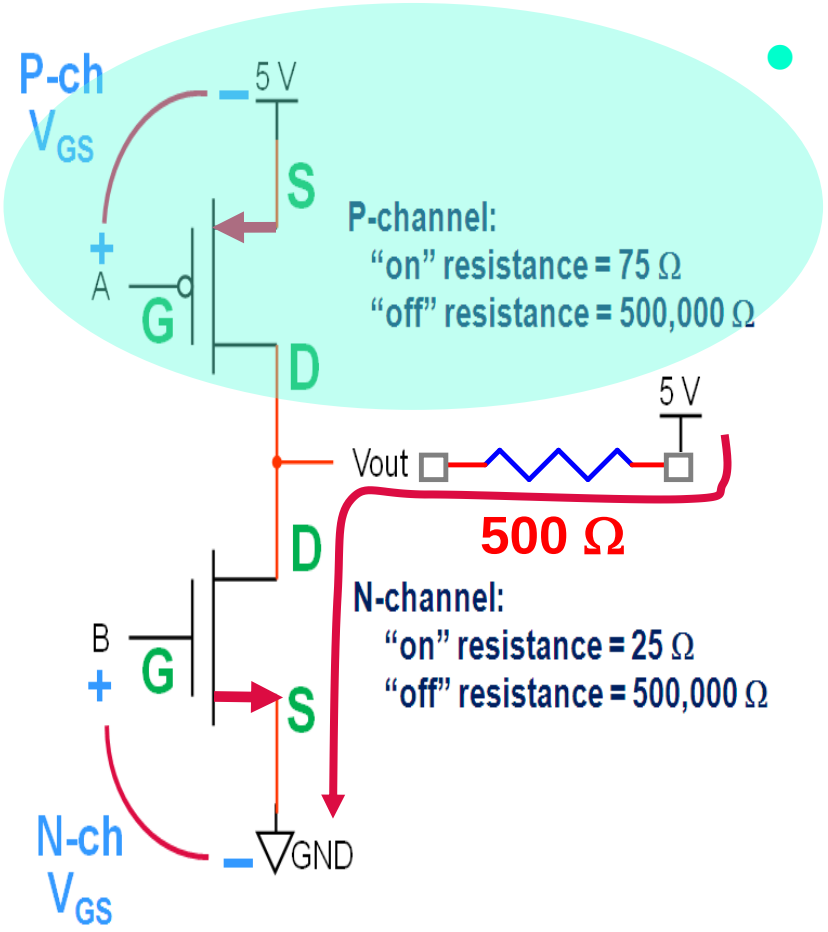
Load impedance is 500,000 Ω in parallel with 500 Ω ≈ 500 Ω

V_{OH} ≈ 5 x (500 / 575) ≈ 4.35 V

I_{OH} ≈ 5 / (75 + 500) ≈ 0.0087 A (8.7 mA)

Note: In the current SOURCING configuration, the inverter output is active high ("asserted high"); the N-channel pull-down virtually "disappears"

Example: Inverter - Current Sinking



- **Calculate V_{OL} and I_{OL} for A=B=5V**

Current SINKING configuration

DC Load is 500 Ω resistor between 5 V supply and V_{out}

P-ch device is "off" (R_{DS} = 500,000 Ω)

N-ch device is "on" (R_{DS} = 25 Ω)

Load impedance is 500,000 Ω in parallel with 500 Ω ≈ 500 Ω

V_{OL} ≈ 5 x (25 / 525) ≈ 0.24 V

I_{OL} ≈ 5 / (25 + 500) ≈ 0.0095 A (9.5 mA)

<u>Note</u>: In the current SINKING configuration, the inverter output is active low ("asserted low"); the P-channel pull-up virtually "disappears"

Fan-out

- Definition: The number of gate inputs that a gate output can drive ***without exceeding*** its worst-case loading specifications
  - depends on characteristics of both the output device and the inputs being driven
  - must be examined for both the "sourcing" and "sinking" cases
  - limitations due to capacitive loading (impact on rise/fall times may be more of a limiting factor than fan-out or DCNM)

$$\text{Fan-out} = \min\left(I_{OH_{max}} / I_{IH},\ I_{OL_{max}} / I_{IL} \right)$$

Data Sheet for a Typical CMOS Device

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:

Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

Sym.	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	μA
I_{IL}	Input LOW current	V_{CC} = Max., V_I = 0 V		—	—	−1	μA
V_{IK}	Clamp diode voltage	V_{CC} = Min., I_N = −18 mA		—	−0.7	−1.2	V
I_{OS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	−35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	I_{OH} = −20 μA	4.4	4.499	—	V
			I_{OH} = −4 mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	I_{OL} = 20 μA	—	.001	0.1	V
			I_{OL} = 4 mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, I_O = 0		—	2	10	μA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, C_L = 50 pF

Sym.	Parameter[4]	Test Conditions	Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y	—	9	19	ns
C_I	Input capacitance	V_{IN} = 0 V	—	3	10	pF
C_{pd}	Power dissipation capacitance per gate	No load	—	22	—	pF

Fan-out Calculation

- **Example: HC-series CMOS**

$$\text{Fan-out} = \min\left(I_{OH_{max}} / I_{IH},\ I_{OL_{max}} / I_{IL} \right)$$

$$= \min(0.02\ \text{mA} / 0.001\ \text{mA},\ -0.02\ \text{mA} / -0.001\ \text{mA})$$

$$= 20$$

Note: DC fan-out is considerably greater in this case if the output voltage swing is degraded … *but* DCNM is lower and signal transitions times are longer, causing speed degradation

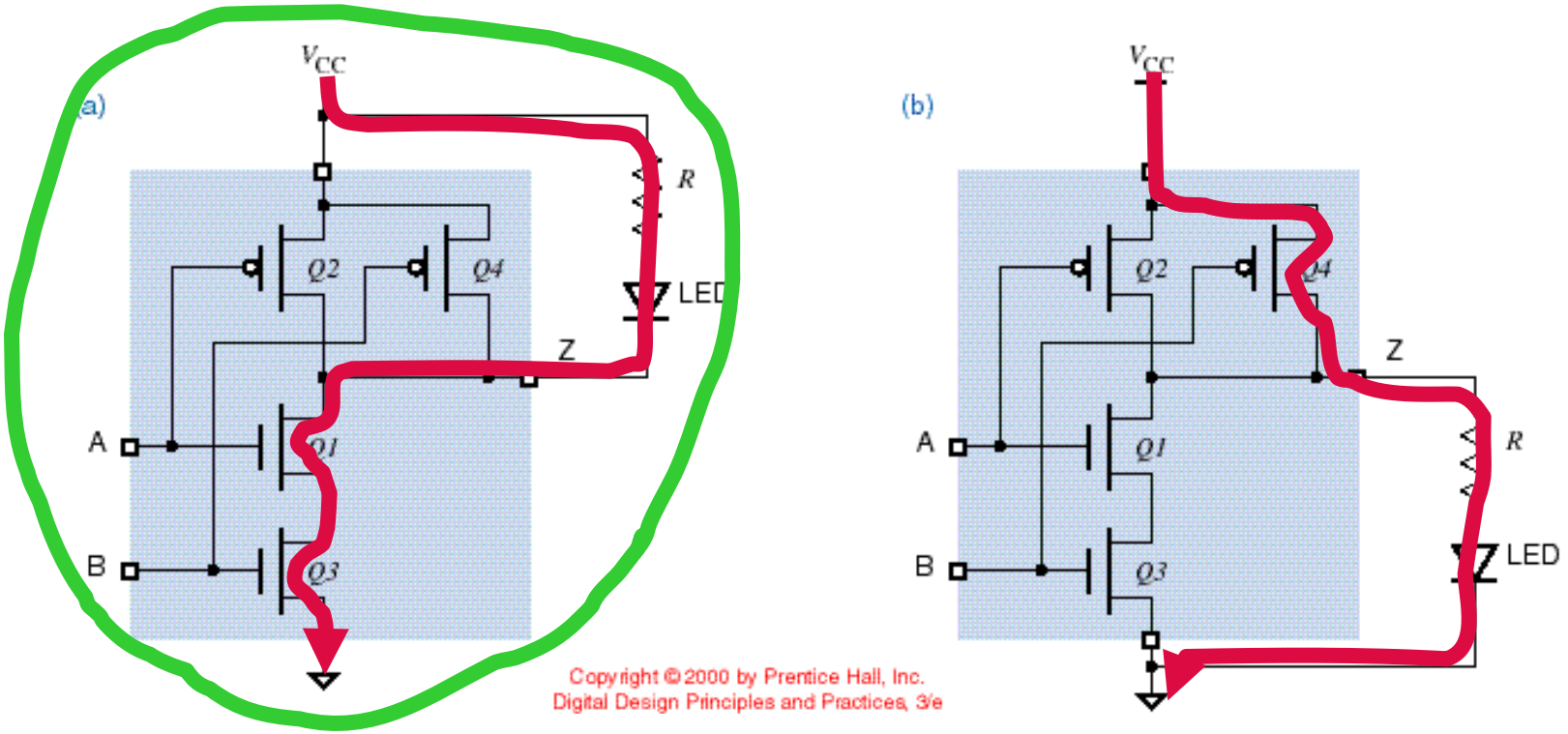
Practical Fan-out

- In a practical application, a gate output may drive a "mixture" of loads
- **HIGH-state fan-out** – The sum of the I_{IHmax} values of all the driven inputs must be *less than or equal* to the I_{OHmax} of the driving output
- **LOW-state fan-out** – The sum of the I_{ILmax} values of all the driven inputs must be *less than or equal* to the I_{OLmax} of the driving output

The "practical" fan-out is the *minimum* of the HIGH- and LOW-state fan-outs

Driving LEDs

- **LEDS represent "DC loads" and can be interfaced to a CMOS gate output either by sinking current (LOW output) or sourcing current (HIGH output)**



Question: Which method is generally preferred?

Example: **Based on the data provided in Table 3-3 of the course text, calculate the value of the LED current limiting resistor for the worst case *current sinking* configuration. Also calculate the amount of power dissipated by the current limiting resistor.**

Assume V_{LED} is 1.9 volts.

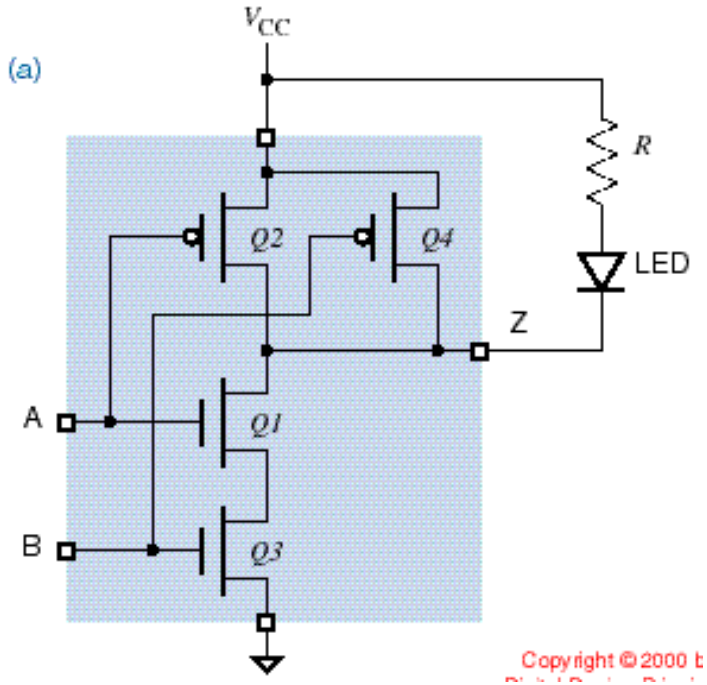


Table 3.3 from *DDPP*

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V_{IK}	Clamp diode voltage	V_{CC} = Min., I_N = −18 mA		—	−0.7	−1.2	V
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SWITCHING CHARACTERISTICS OVER OPERATING RANGE, C_L = 50 pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
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C_I	Input capacitance	V_{IN} = 0 V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

NOTES:

1. *For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.*
2. *Typical values are at V_{CC} = 5.0 V, +25°C ambient.*
3. *Not more than one output should be shorted at a time. Duration of short-circuit test should not exceed one second.*
4. *This parameter is guaranteed but not tested.*

SOLUTION:

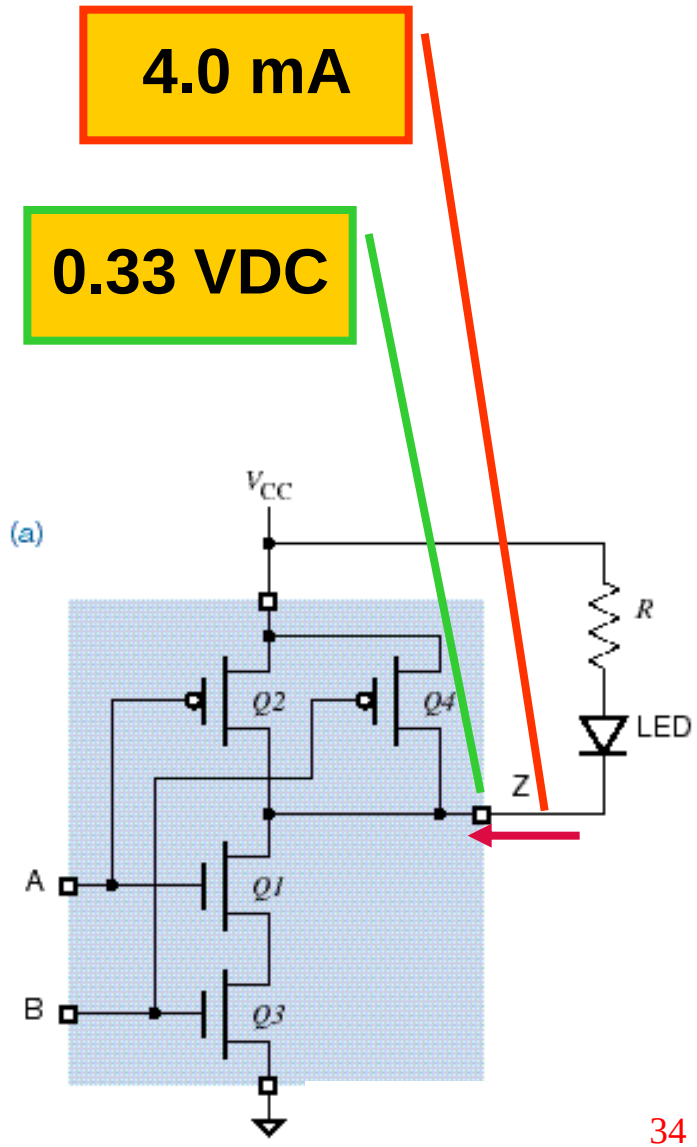
$V_R = 5.0 - V_{LED} - V_{OL} = 5.0 - 1.9 - 0.33 = 2.77$ V

NOTE: Here, use "Max" value indicated for V_{OL} of 0.33 V

$R = V_R / I_{OL} = 2.77/0.004 = 693\ \Omega$

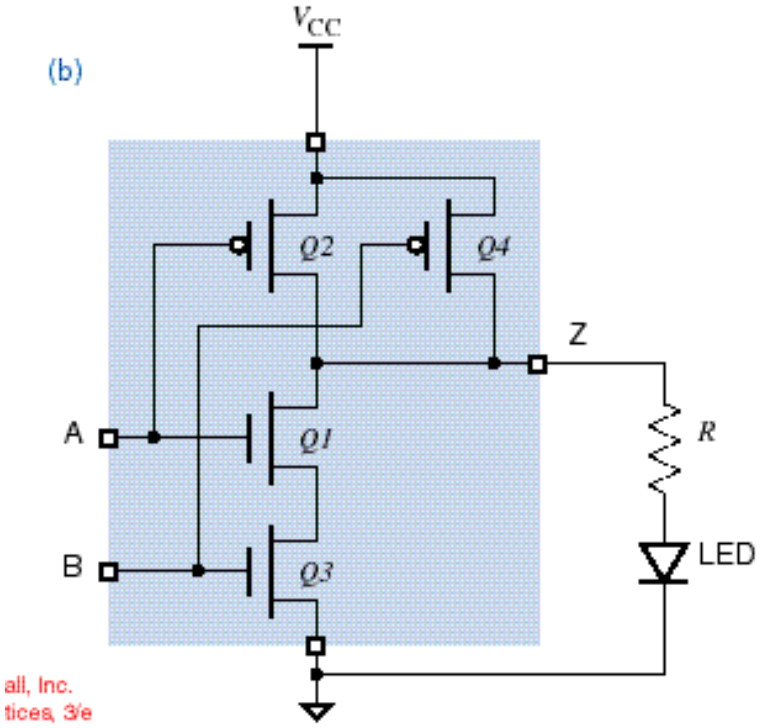
$P_R = R \times I_{OL}^2 = 693 \times (0.004)^2 = 11.1$ milliwatts

NOTE: Can also calculate power dissipation of resistor using $V_R \times I_{OL}$ or $(V_R^2)/R$



Example: Based on the data provided in Table 3-3 of the course text, calculate the value of the LED current limiting resistor for the worst case *current sourcing* configuration. Also calculate the amount of power dissipated by the current limiting resistor.

Assume V_{LED} is 1.9 volts.



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I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	μA
I_{IL}	Input LOW current	V_{CC} = Max., $V_I = 0$ V		—	—	−1	μA
V_{IK}	Clamp diode voltage	V_{CC} = Min., $I_N = -18$ mA		—	−0.7	−1.2	V
I_{OS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	−35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	$I_{OH} = -20$ μA	4.4	4.499	—	V
			$I_{OH} = -4$ mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	$I_{OL} = 20$ μA	—	.001	0.1	V
			$I_{OL} = 4$ mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, $I_O = 0$		—	2	10	μA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, $C_L = 50$ pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	$V_{IN} = 0$ V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

NOTES:

1. *For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.*
2. *Typical values are at $V_{CC} = 5.0$ V, +25°C ambient.*
3. *Not more than one output should be shorted at a time. Duration of short-circuit test should not exceed one second.*
4. *This parameter is guaranteed but not tested.*

SOLUTION:

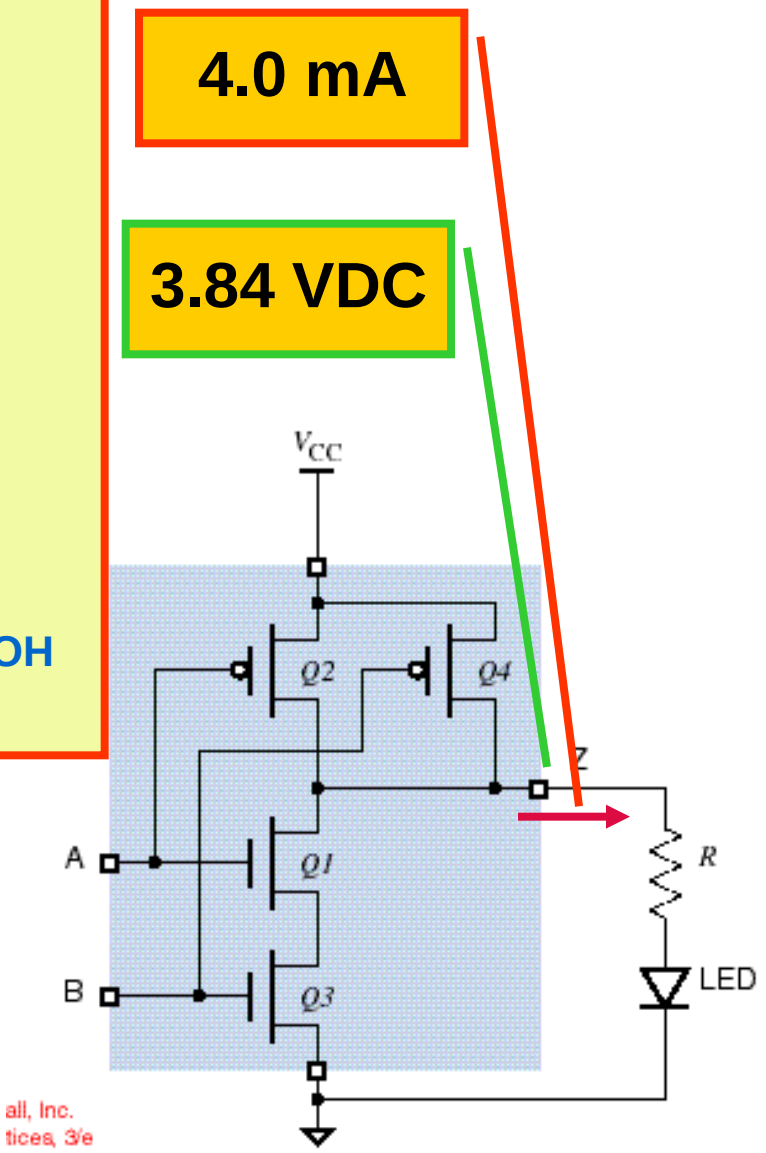
$V_R = V_{OH} - V_{LED} = 3.84 - 1.9 = 1.94$ V

NOTE: Here, use "Min" value indicated for V_{OH} of 3.84 V

$R = V_R / I_{OH} = 1.94/0.004 = 485\ \Omega$

$P_R = R \times I_{OH}^2 = 485 \times (0.004)^2 = 7.8$ milliwatts

NOTE: Can also calculate power dissipation of resistor using $V_R \times I_{OH}$ or $(V_R^2)/R$



Effects of Excessive Loading

- **Loading a gate output beyond its rated fan-out can have several deleterious effects:**
  - **in the LOW state, the output voltage (V_{OL}) may increase beyond $V_{OL_{max}}$**
  - **in the HIGH state, the output voltage (V_{OH}) may fall below $V_{OH_{min}}$**
  - **output rise and fall times may increase beyond their specifications**
  - **the operating temperature of the device may increase, thereby *reducing* the *reliability* of the device and eventually causing device *failure***

Example – DCNM, Family A → Family B

Family "A"

V_{CC} = 5 V	V_{OH} = 4.4 V	V_{OL} = 0.40 V	V_{IH} = 3.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -4 mA	I_{OL} = 4 mA	I_{IH} = 0.4 μA	I_{IL} = -0.4 μA

Family "B"

V_{CC} = 5 V	V_{OH} = 3.3 V	V_{OL} = 0.30 V	V_{IH} = 2.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -400 μA	I_{OL} = 8 mA	I_{IH} = 40 μA	I_{IL} = -0.4 mA

$$DCNM_{A \rightarrow B} = \min(4.4-2.6,\ 1.6-0.4) = 1.2V$$

Question: Is this a "good" DCNM (for 5 V CMOS logic)?

Example – DCNM, Family B → Family A

Family "A"

V_{CC} = 5 V	V_{OH} = 4.4 V	V_{OL} = 0.40 V	V_{IH} = 3.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -4 mA	I_{OL} = 4 mA	I_{IH} = 0.4 μA	I_{IL} = -0.4 μA

Family "B"

V_{CC} = 5 V	V_{OH} = 3.3 V	V_{OL} = 0.30 V	V_{IH} = 2.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -400 μA	I_{OL} = 8 mA	I_{IH} = 40 μA	I_{IL} = -0.4 mA

$$DCNM_{B \rightarrow A} = \min(3.3-3.6,\ 1.6-0.3) = -0.3V$$

Question: What is the consequence of a negative DCNM?

What is the minimum DCNM required? DCNM > 0

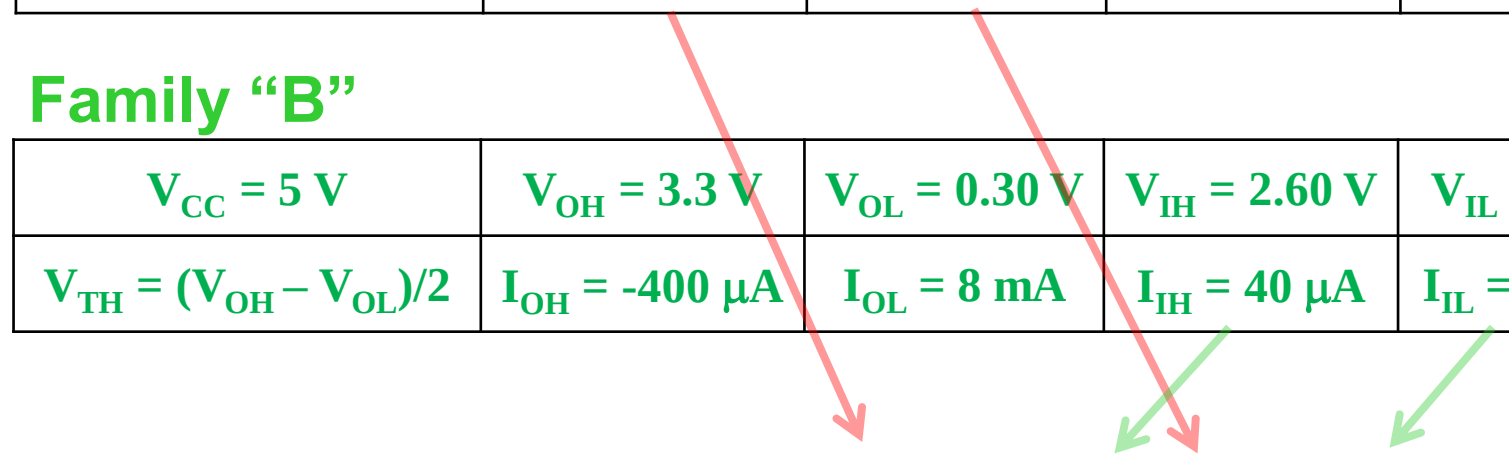
Example – Fan-out, Family A → Family B

Family "A"

V_{CC} = 5 V	V_{OH} = 4.4 V	V_{OL} = 0.40 V	V_{IH} = 3.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -4 mA	I_{OL} = 4 mA	I_{IH} = 0.4 μA	I_{IL} = -0.4 μA

Family "B"

V_{CC} = 5 V	V_{OH} = 3.3 V	V_{OL} = 0.30 V	V_{IH} = 2.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -400 μA	I_{OL} = 8 mA	I_{IH} = 40 μA	I_{IL} = -0.4 mA



$$\text{Fanout}_{A \to B} = \min(4 / 0.04, 4 / 0.4) = 10$$

Note: Current arrows for I_O and I_I point in *opposite directions*

Question: Is it possible for the fan-out to be negative? NO!

Example – Fan-out, Family B → Family A

Family "A"

V_{CC} = 5 V	V_{OH} = 4.4 V	V_{OL} = 0.40 V	V_{IH} = 3.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -4 mA	I_{OL} = 4 mA	I_{IH} = 0.4 μA	I_{IL} = -0.4 μA

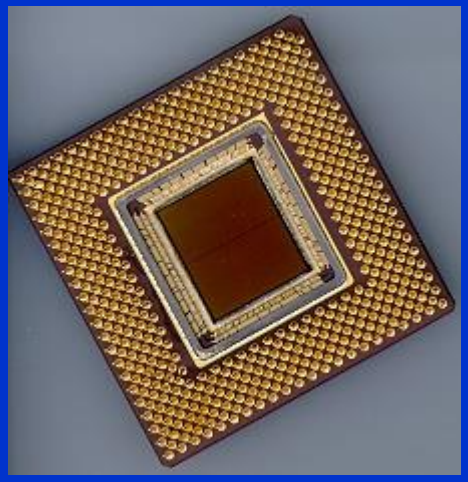
Family "B"

V_{CC} = 5 V	V_{OH} = 3.3 V	V_{OL} = 0.30 V	V_{IH} = 2.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -400 μA	I_{OL} = 8 mA	I_{IH} = 40 μA	I_{IL} = -0.4 mA

Fanout $_{B \rightarrow A}$ = min(400/0.4, 8/0.0004) = 1000

Question: What is the minimum fan-out required?

Fan-out ≥ 1



ECE 477 Digital Systems Senior Design Project

Module 2-C

Propagation Delay and Transition Time

Reading Assignment:

DDPP 4th Ed., pp. 114-122

Learning Objectives:

- **Define propagation delay and list the factors that contribute to it**
- **Define transition time and list the factors that contribute to it**
- **Estimate the transition time of a CMOS gate output based on the "on" resistance of the active device and the capacitive load**
- **Describe ways in which load capacitance can be minimized**

Outline

- Overview
- Propagation delay
- Transition time
- Equivalent circuit transition time analysis
  - Calculation
  - Estimation
- Load capacitance

Overview

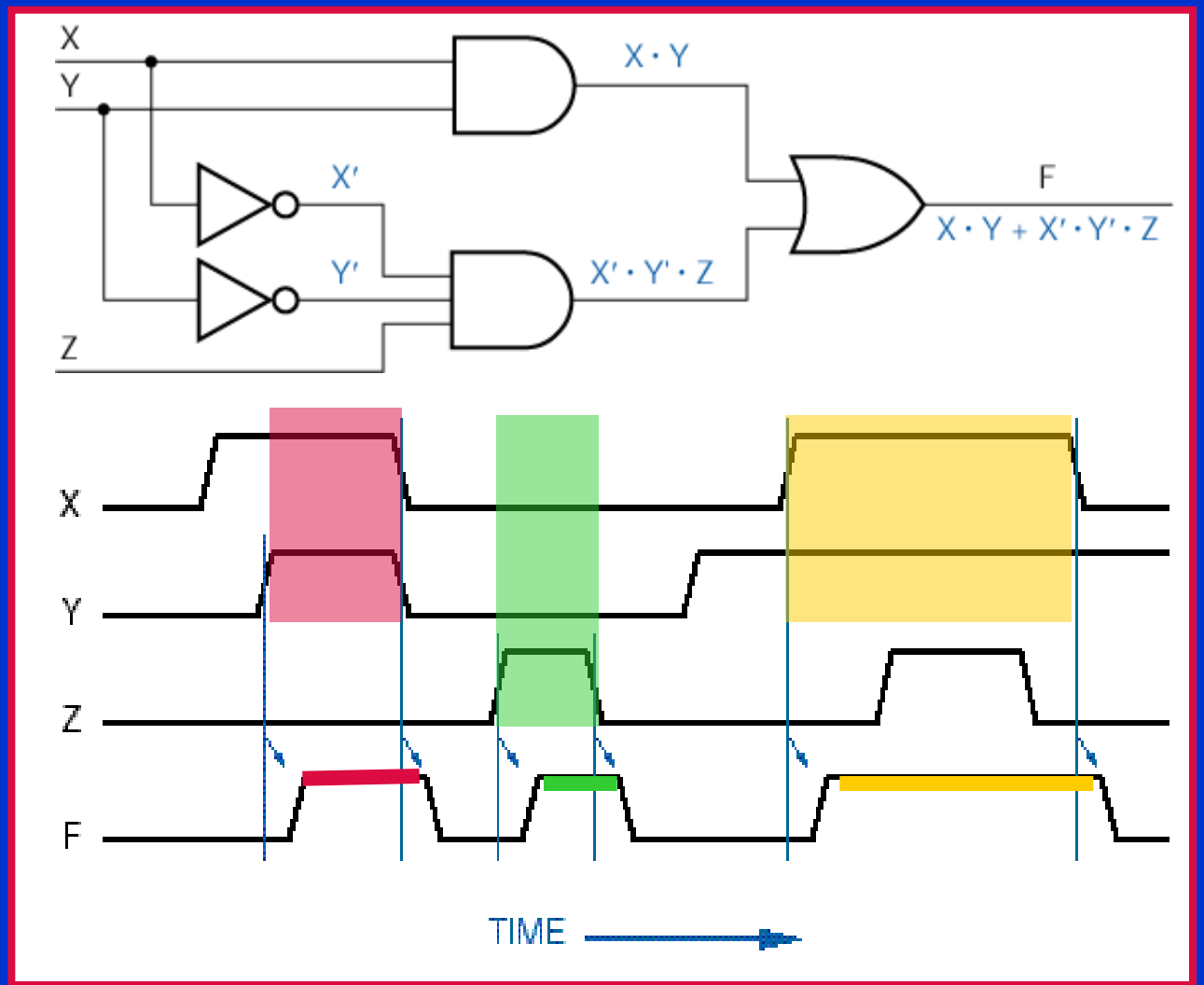
- The ***speed*** and ***power dissipation*** of a CMOS device depend on the dynamic ("AC") characteristics of the device and its load
- Logic designers must carefully examine the effects of output loading and redesign where the loading is too high
- Speed (performance) depends on two characteristics:
  - ***propagation delay***
  - ***transition time***

Time Matters

- Logic gates require a certain amount of "think time" to produce a new output in response to changing inputs – referred to as the ***propagation delay*** of the gate
- Logic gate outputs can not change from a low voltage to a high voltage (or vice-versa) "instantaneously" – referred to as the ***transition time*** of the gate
- A ***timing diagram*** can be used to show how a logic circuit responds to time-varying input signals

Time Matters

- Time response of a combinational circuit

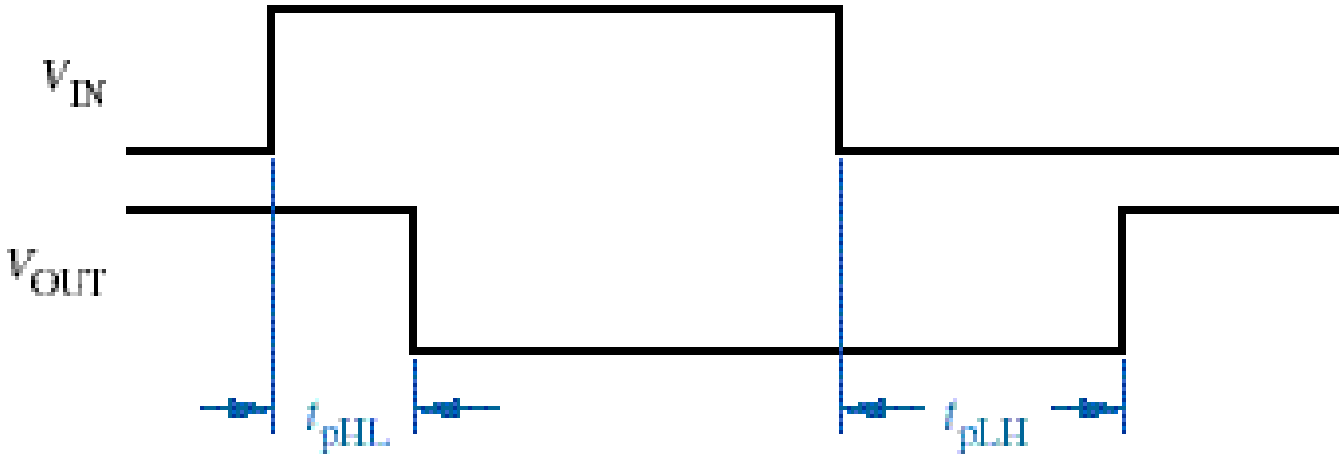


Propagation Delay – Definition

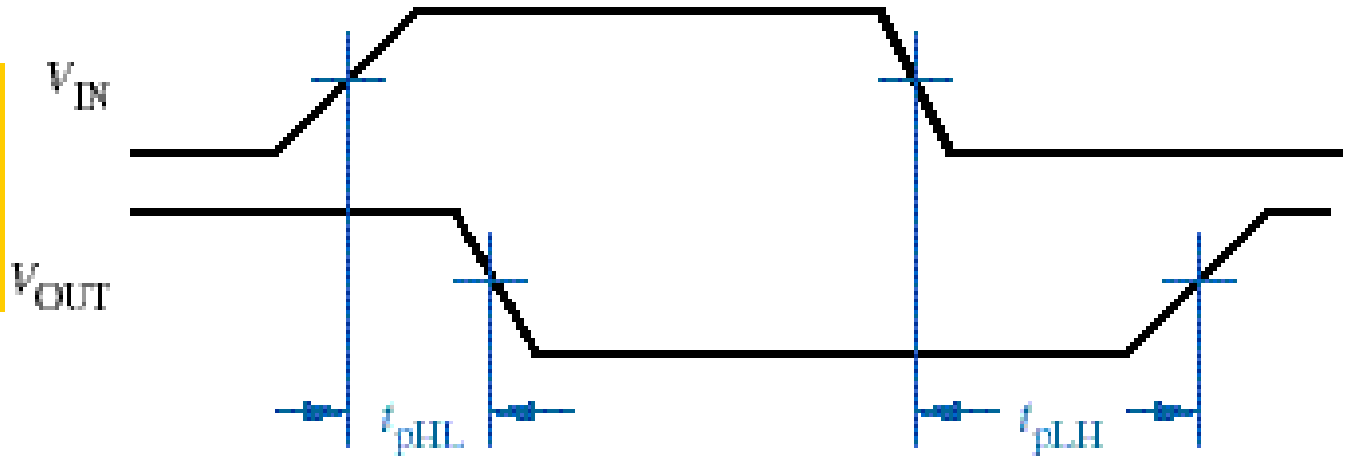
- **Definition: The electrical path from a particular input signal of a logic element to its output signal is called a *signal path***
- **Definition: The amount of time it takes for a change in an input signal to cause a corresponding change in a gate's output signal is called the *propagation delay* (t_p)**
- **The propagation delay for an output signal going from LOW-to-HIGH (t_{PLH}) may be different than the propagation delay of that signal going from HIGH-to-LOW (t_{PHL})**

Propagation Delay – Measurement

Ignoring rise and fall times



Measured at midpoints of transitions

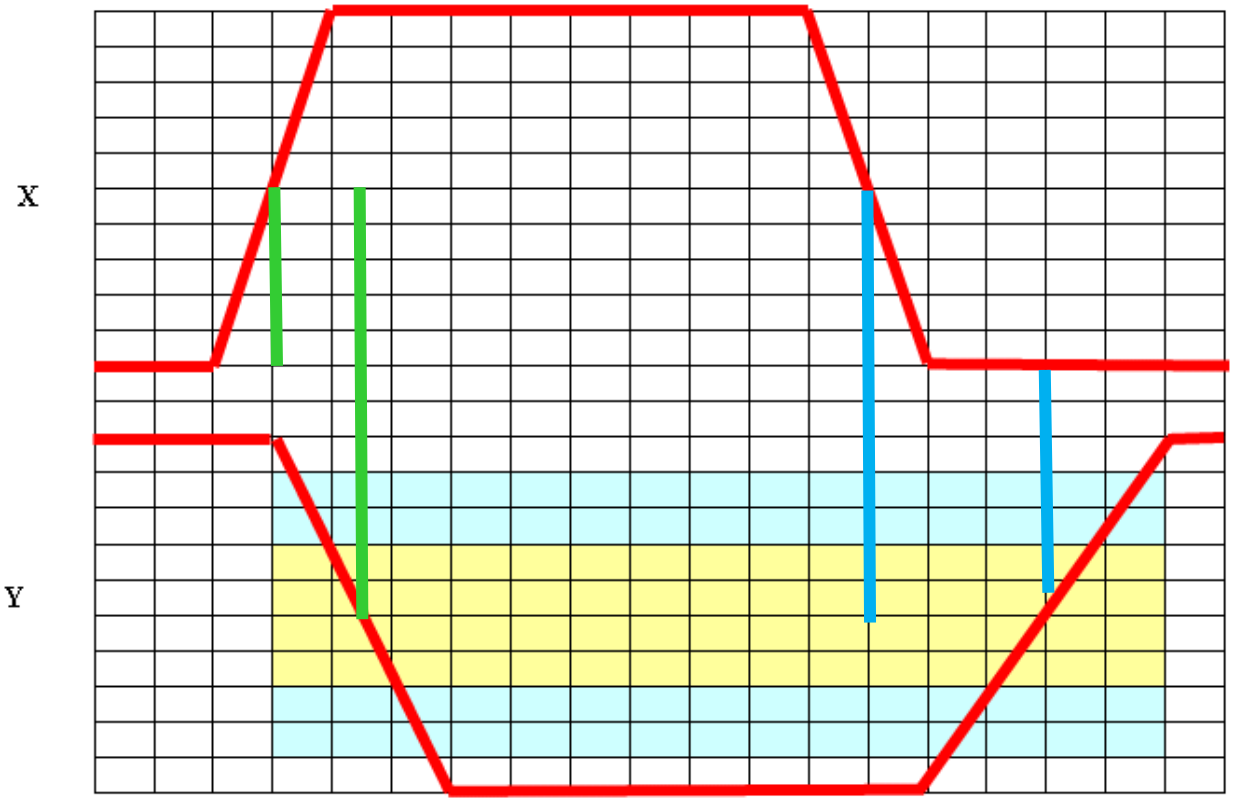


Propagation Delay – Why Non-zero

- **Several factors lead to *non-zero* propagation delays in CMOS circuits:**
  - **the rate at which transistors change state is influenced both by semiconductor physics and the circuit environment (input signal transition time, input capacitance, and output loading)**
  - **multistage devices (e.g., non-inverting gates) may require several internal transistors to change state before the output can change state**

Example – Propagation Delay Measurement

Find each of the following, rounded to the nearest ½ ns (assume each division is 1 ns)



Rise propagation delay (t_{PLH}) = 3 ns

Fall propagation delay (t_{PHL}) = 1.5 ns

Transition Time – Definition

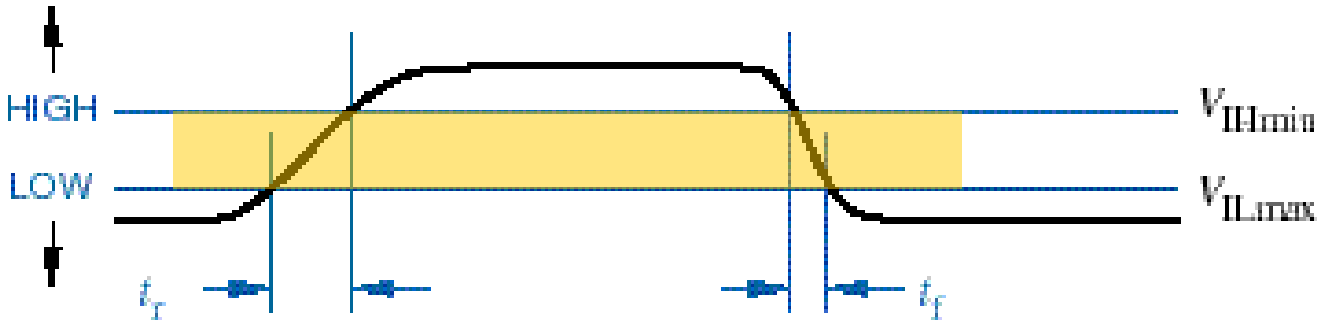
- **Definition**: The amount of time that the output of a logic circuit takes to change from one state to another
  - **rise time** (**tr** or t_{TLH}): the **time** an output signal takes to **transition** from **low**-to-**high**
  - **fall time** (**tf** or t_{THL}): the **time** an output signal takes to **transition** from **high**-to-**low**
- Gate outputs can ***not*** change state ***instantaneously*** (i.e., with a transition time of zero) because they need to ***charge the stray capacitance*** of the wires and other components they drive

Transition Time – Measurement

“ideal”

“less ideal”

“reality”



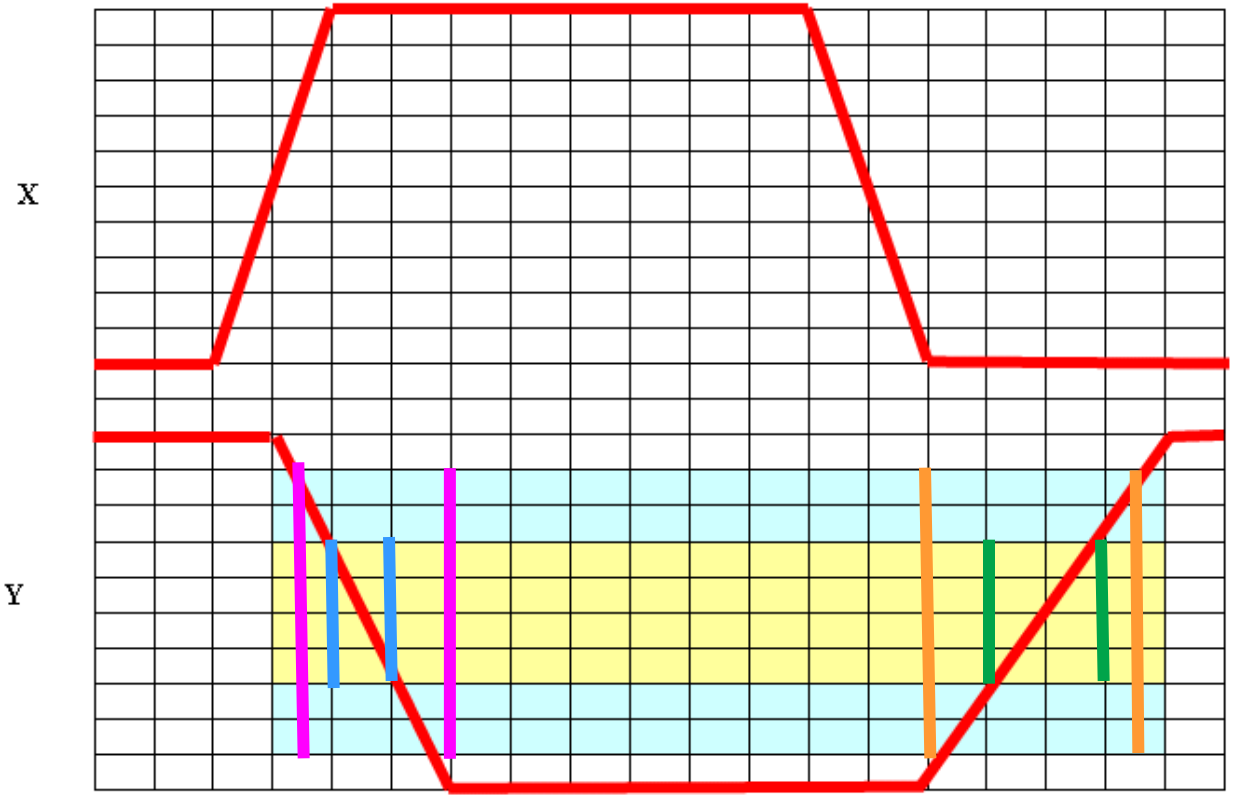
Note: tf is typically *not* equal to tr

Transition Time – Endpoints

- To avoid difficulties in defining the endpoints, transition times are normally measured one of two different ways:
  - at the boundaries of the valid logic levels (i.e., $V_{IH_{min}}$ and $V_{IL_{max}}$)
  - at the 10% and 90% points of the output waveform
- Using the first convention (above), the rise and fall times indicate how long it takes for an output signal to pass through the (undefined) ***indeterminate region*** between **LOW** and **HIGH**

Example – Transition Time Measurement

Find each of the following, rounded to the nearest ½ ns (assume each division is 1 ns)



Rise time (t_{TLH}) based on Wakerly's (30%-70%) definition = 2 ns

Rise time (t_{TLH}) based on standard 10%-90% definition = 3.5 ns

Fall time (t_{THL}) based on Wakerly's (70%-30%) definition = 1 ns

Fall time (t_{THL}) based on standard 90%-10% definition = 2.5 ns

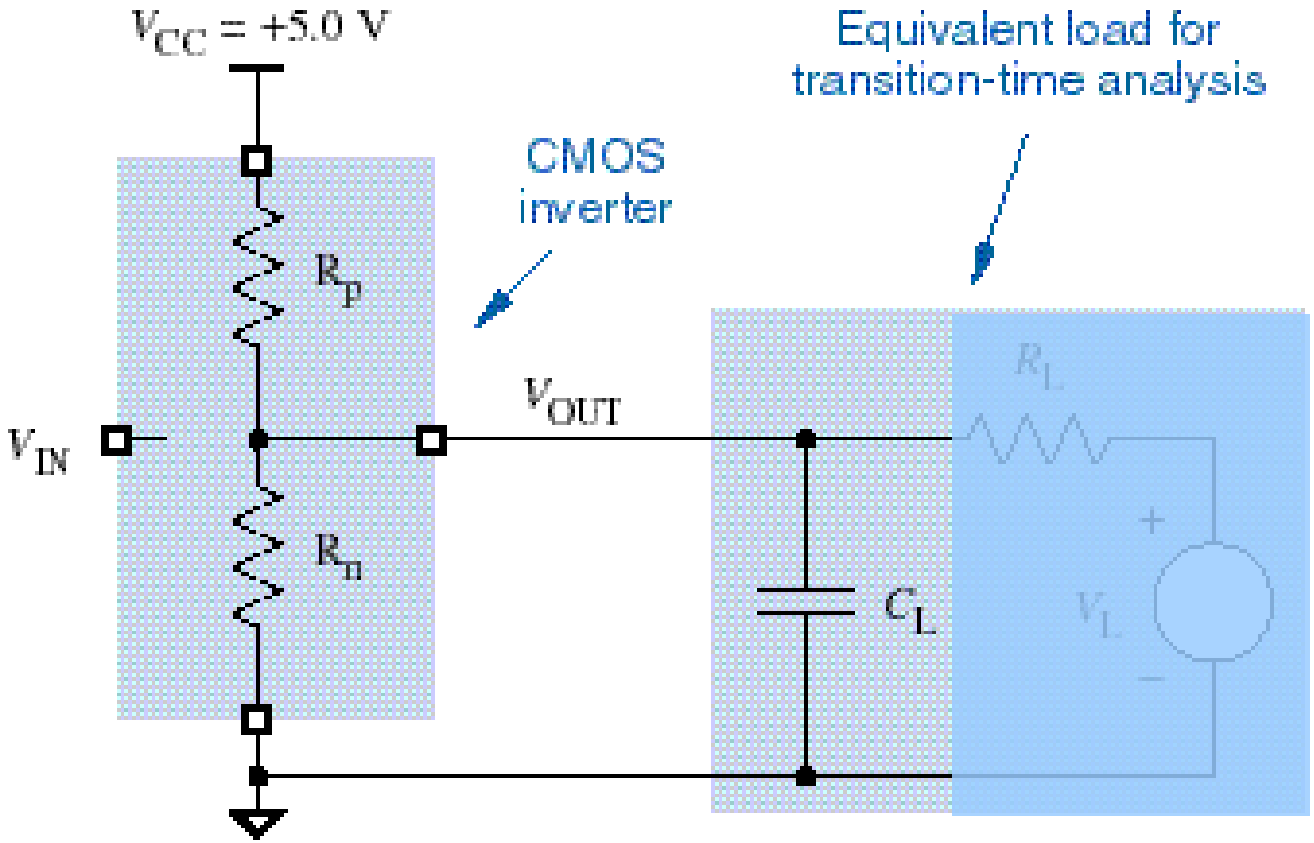
Transition Time – Factors

- **The transition times of a CMOS circuit depend mainly on two factors:**
  - ***the "on" transistor resistance***
  - ***the load capacitance***
- ***Stray capacitance*** **(called an "*AC load*") arises from at least three different sources:**
  - **output circuits – including transistors, internal wiring, and packaging**
  - **wiring that connects a gate output to other gate inputs**
  - **input circuits – including transistors, internal wiring, and packaging**

Transition Time – Equivalent Circuit

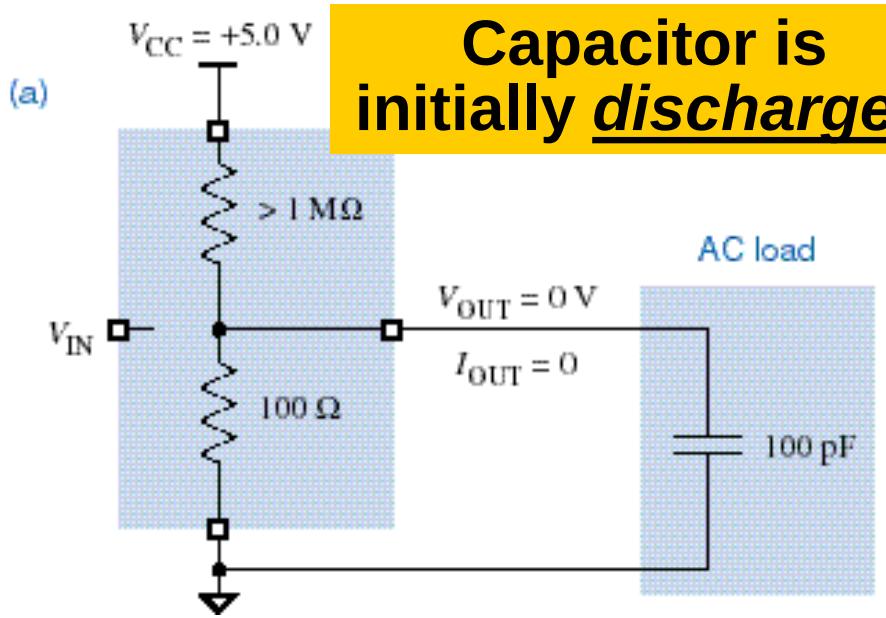
- A gate output's load can be modeled by an equivalent load circuit with 3 components:
  - R_L and V_L represent the DC load – they determine the steady state voltages and currents present and do not have much effect on transition times
  - C_L represents the AC (capacitive) load – it determines the voltages and currents present while the output is changing, as well as how long it takes to change from one state to another

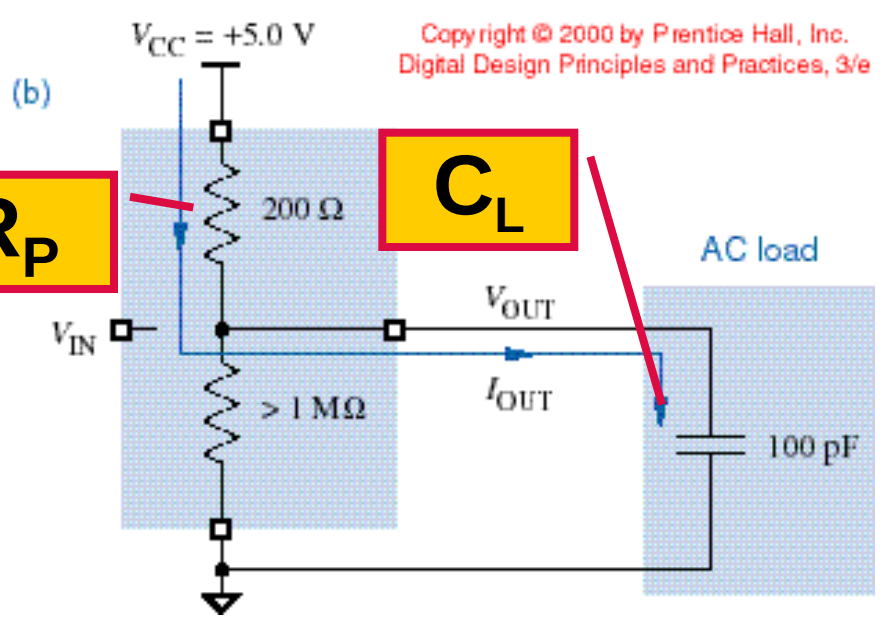
Equivalent Circuit for Transition Time Analysis of a CMOS Output



Model of a CMOS LOW-to-HIGH Transition (with Negligible DC Load)

Capacitor is initially *discharged*

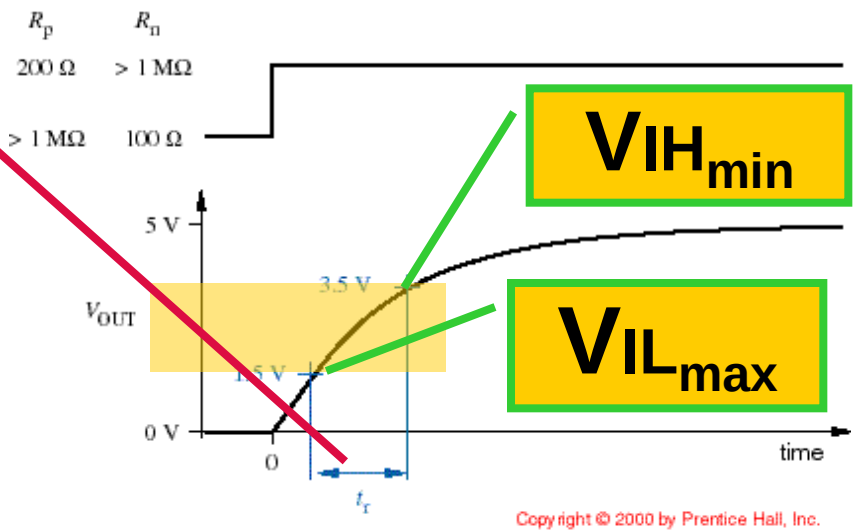




R_P

C_L

rise time

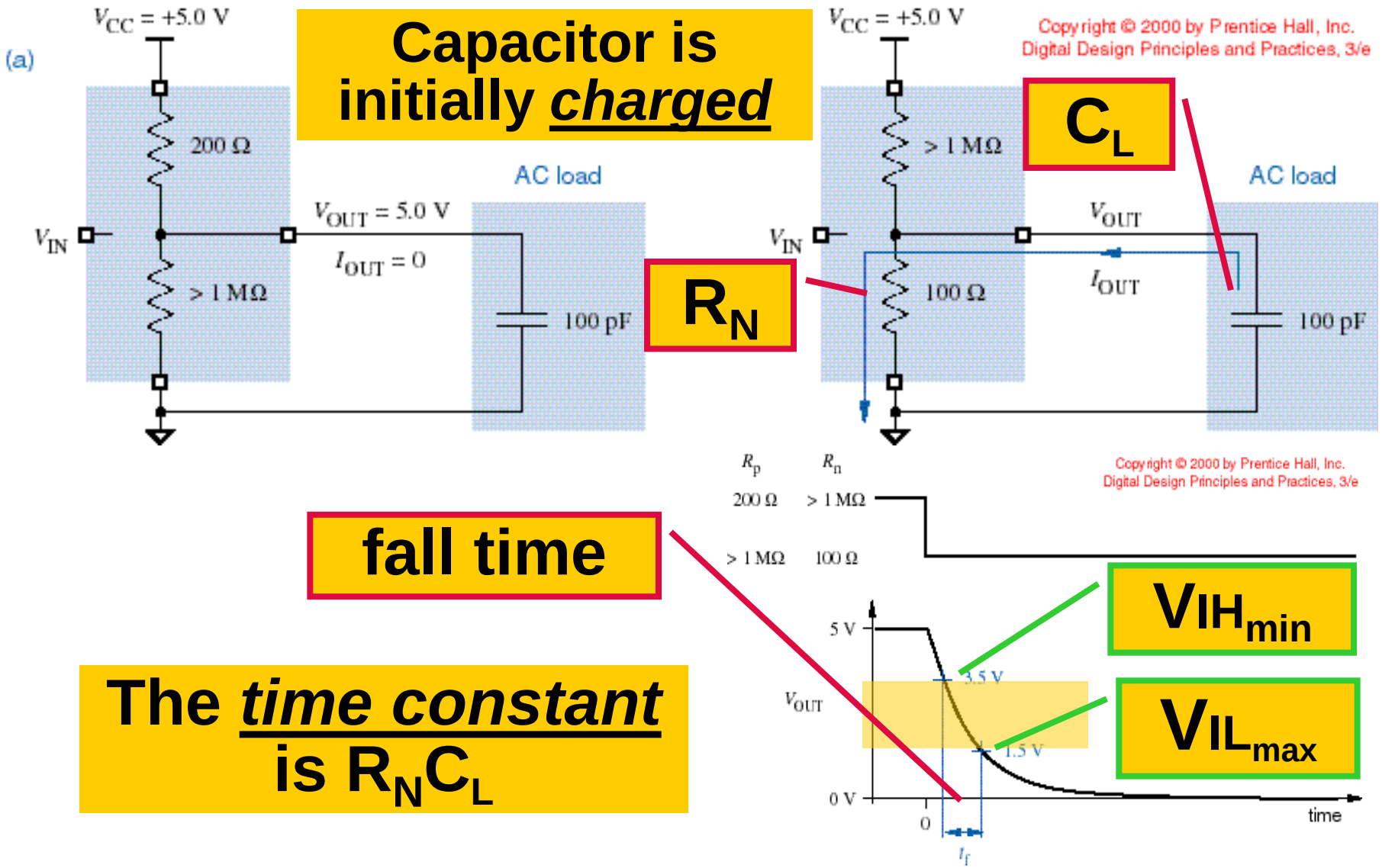


$V_{IH_{min}}$

$V_{IL_{max}}$

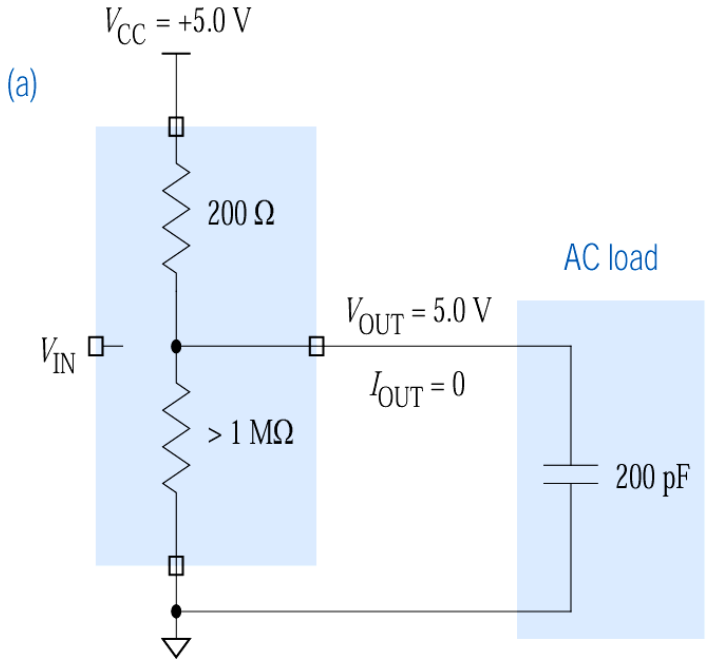
The *time constant* is R_PC_L

Model of a CMOS HIGH-to-LOW Transition (with Negligible DC Load)



Example

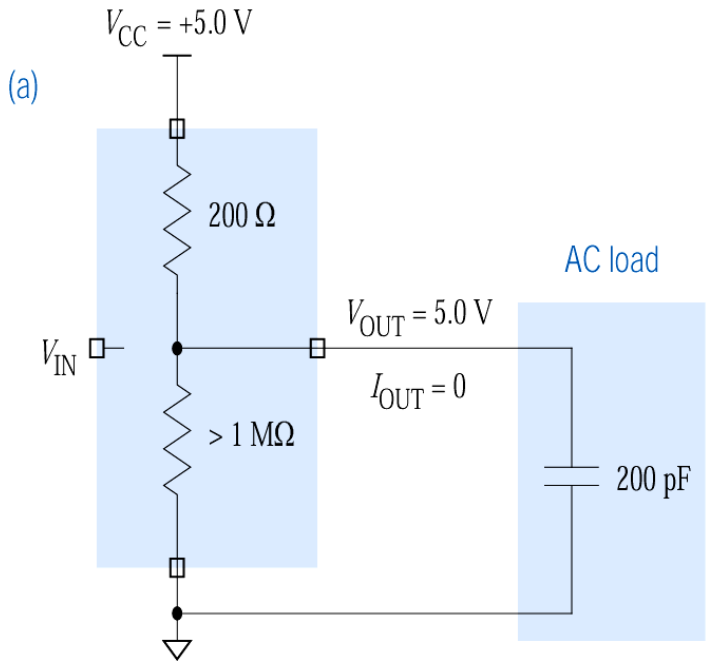
- **Given that a CMOS inverter's P-channel MOSFET has an ON resistance of 200Ω, that its N-channel MOSFET has an ON resistance of 100Ω, and that the capacitive (or AC) load C_L = 200 pF, calculate the fall time**



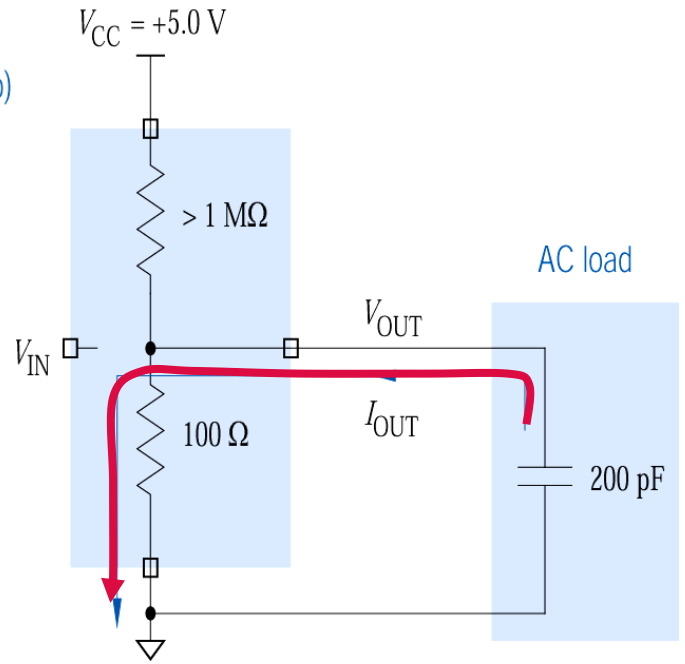
initial conditions

Example – Fall Time Calculation

- **Given that a CMOS inverter's P-channel MOSFET has an ON resistance of 200Ω, that its N-channel MOSFET has an ON resistance of 100Ω, and that the capacitive (or AC) load C_L = 200 pF, calculate the fall time**

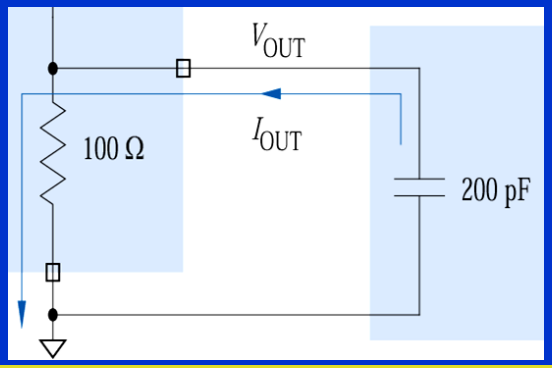


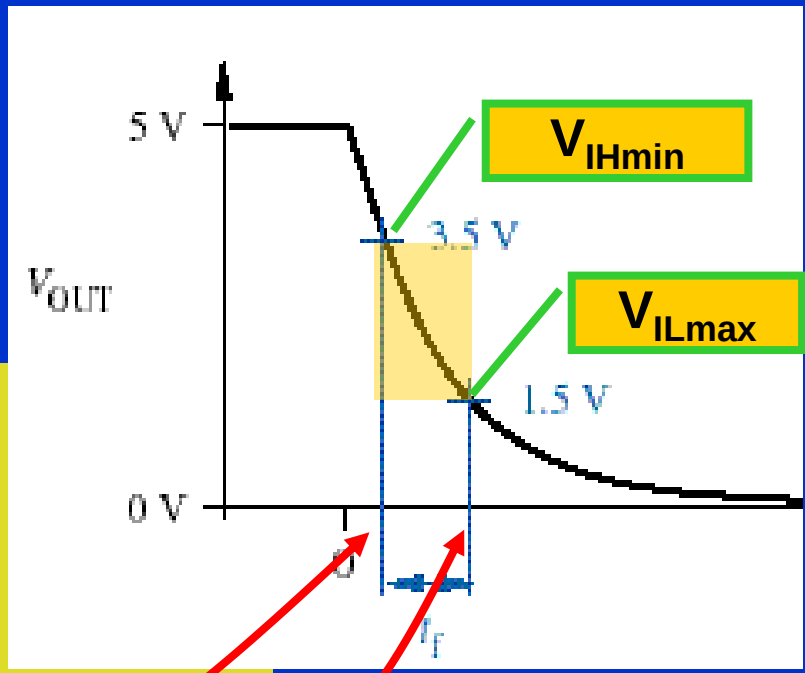
initial conditions



output goes low

Example – Fall Time Calculation





$t = -R_n * C_L * \ln (V_{out}/V_{DD})$

$= -100 * 200 * 10^{-12} * \ln (V_{out} / 5.0)$

$= -20 * 10^{-9} * \ln (V_{out} / 5.0)$

$t_{3.5} = -20 * 10^{-9} * \ln (3.5/5.0) = 7.13$ ns

$t_{1.5} = -20 * 10^{-9} * \ln (1.5/5.0) = 24.08$ ns

$t_{PHL} = t_f$ ***(fall time)*** $= 24.08 - 7.13 = 16.95$ ns

Note: ***Calculated transition times are sensitive to the choice of logic levels (i.e., V_{IHmin} and V_{ILmax})***

Transition Time Estimation

- **Rule of Thumb: In practical circuits, the transition time can be *estimated* using the RC time constant of the charging or discharging circuit**

Example – Transition Time Estimates

- Given that a CMOS inverter's P-channel MOSFET has an ON resistance of 200Ω, that its N-channel MOSFET has an ON resistance of 100Ω, and that the capacitive (or "A.C.") load C_L = 200 pF, ***estimate*** the **fall time** and **rise time**

Fall time estimate:

$R_N \times C_L = 100 \times 200$ pF

$= 1 \times 10^2 \times 2 \times 10^{-10}$

$= 2 \times 10^{-8} = 20 \times 10^{-9}$

= 20 ns

Rise time estimate:

$R_P \times C_L = 200 \times 200$ pF

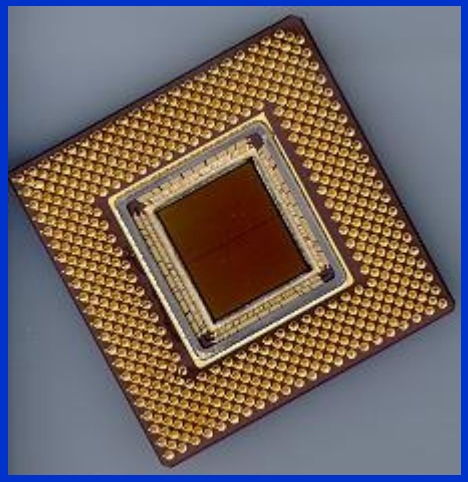
$= 2 \times 10^2 \times 2 \times 10^{-10}$

$= 4 \times 10^{-8} = 40 \times 10^{-9}$

= 40 ns

Load Capacitance

- **Conclusion: An increase in load capacitance causes an increase in the RC time constant and a corresponding increase in the output transition (rise/fall) times**
- **Load capacitance must be *minimized* to obtain high circuit performance – this can be achieved by:**
  - **minimizing the number of inputs driven by a given signal**
  - **creating multiple copies of the signal (using "buffers")**
  - **careful *physical layout* of the circuit**



ECE 477 Digital Systems Senior Design Project

Module 2-D

Power Consumption and Decoupling

Reading Assignment:

DDPP 4th Ed., pp. 122-124

Learning Objectives:

- **Identify sources of dynamic power dissipation**
- **Plot power dissipation of CMOS logic circuits as a function of operating frequency**
- **Plot power dissipation of CMOS logic circuits as a function of power supply voltage**
- **Describe the function and utility of decoupling capacitors**

Outline

- Overview
- Dynamic power dissipation
- Power dissipation as a function of operating frequency
- Power dissipation as a function of supply voltage
- Current spikes and decoupling

Overview

- **Definition: The power dissipation (consumption) of a CMOS circuit whose output is *not changing* is called *static (quiescent) power dissipation***
- **Most CMOS circuits have *very low* static power dissipation**
- **CMOS circuits only dissipate a significant amount of power during *transitions* – this is called *dynamic power dissipation***

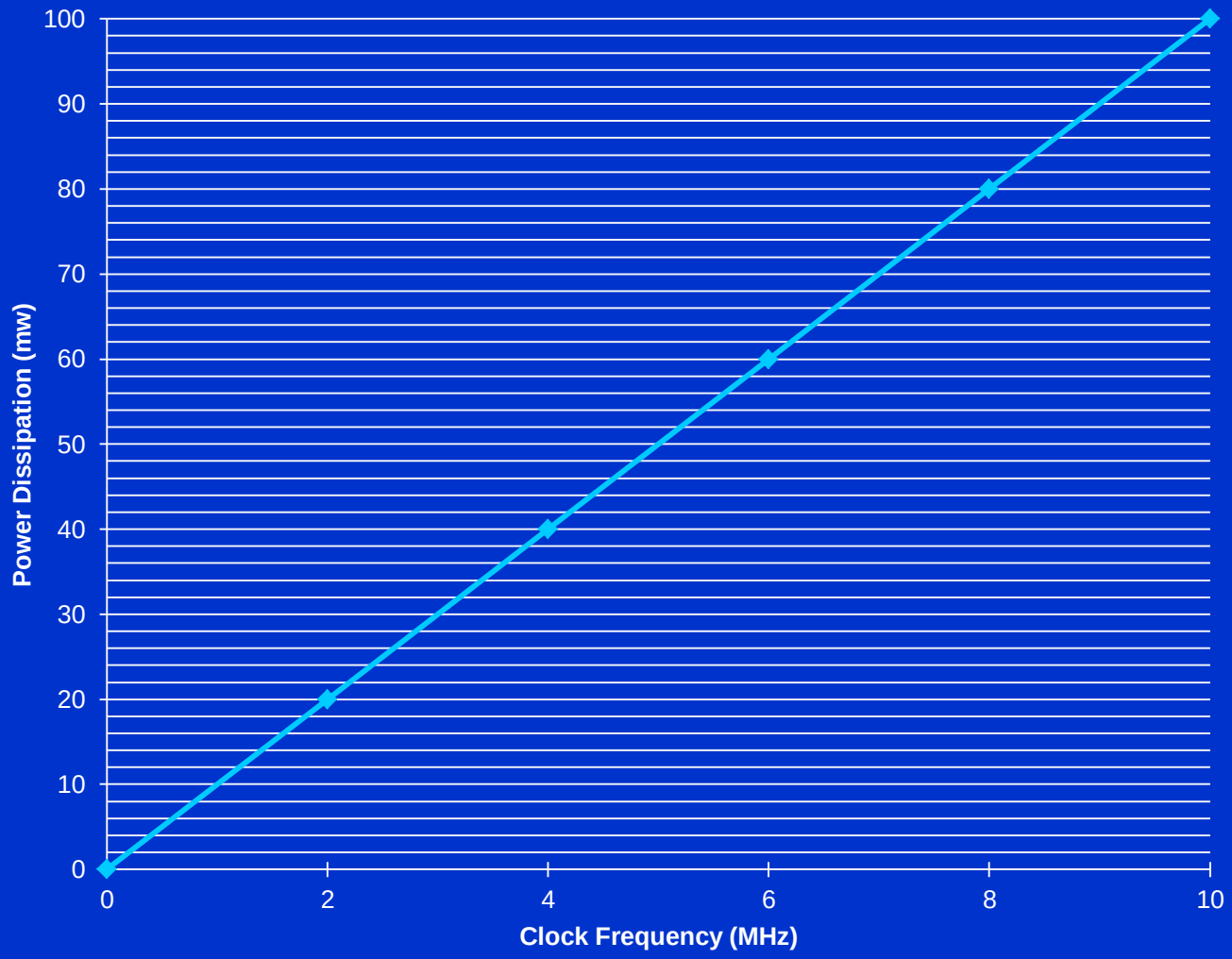
Dynamic Power Dissipation

- Sources of dynamic power dissipation:
  - the partial "short-circuiting" of the CMOS output structure (e.g., when the input voltage is not close to one of the power supply rails) – called "P_T" (power due to output transitions)
  - the capacitive load on the output (power is dissipated in the "on" resistance of the active transistor to charge/discharge the capacitive load) – called "P_L" (power due to charging/discharging load)

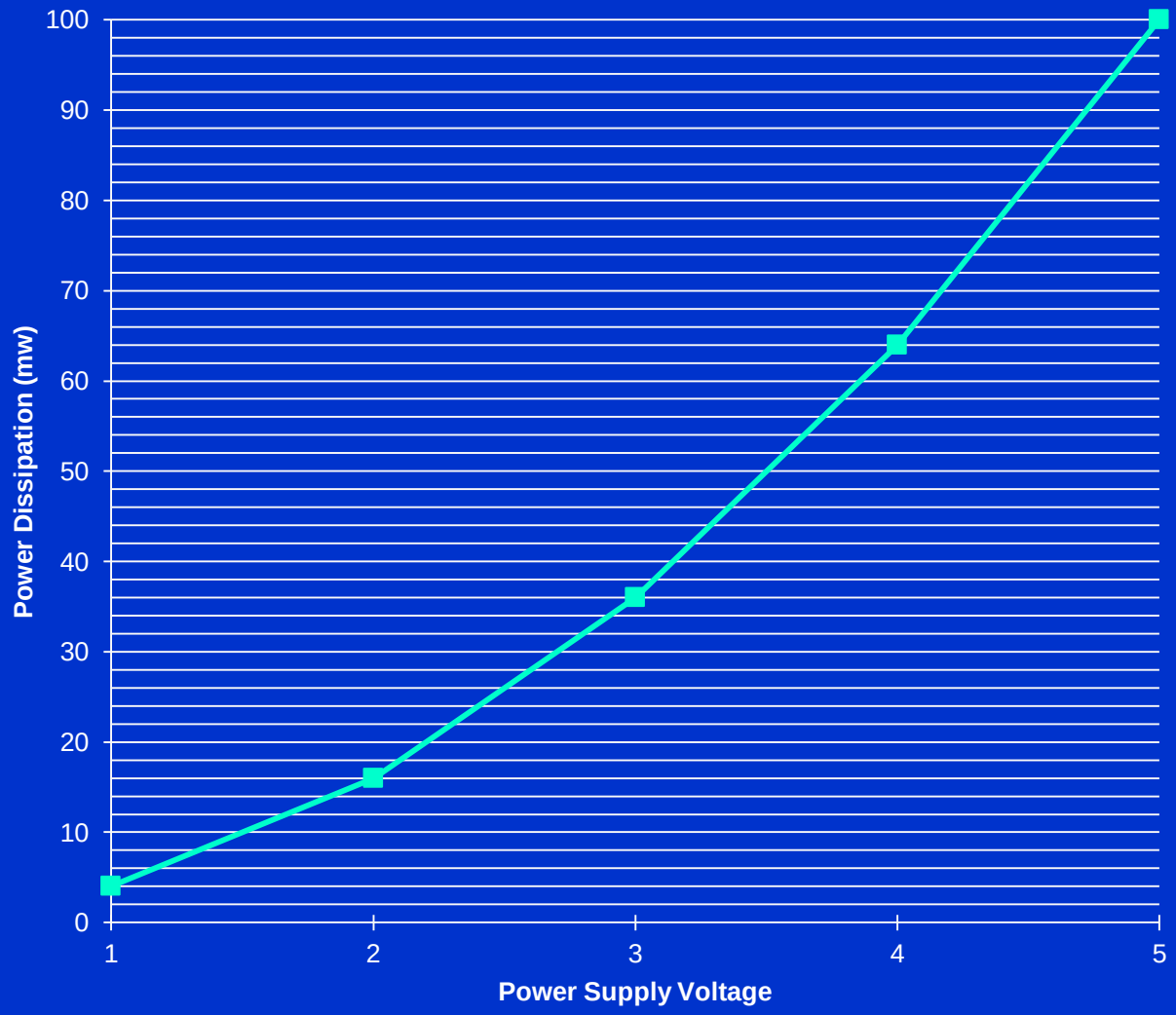
Power Consumption

- Total dynamic power dissipation ($P_T + P_L$) is proportional to the ***square*** of the power supply voltage times the transition frequency
- Conclusions:
  - power dissipation increases ***linearly*** as the frequency of operation increases
  - reducing the power supply voltage results in a ***quadratic*** reduction of the power dissipation

Example - A microcontroller can operate over a frequency range of **0 Hz to 10 MHz**, and dissipates **100 mW** when operated at **10 MHz**; plot its power dissipation over **the specified frequency range**



Example - A microcontroller can operate over a power supply range of **1 to 5 volts,** and dissipates **100 mW** when operated at **5 VDC**; plot its power dissipation over the **specified power supply range**



$100 \times (4/5)^2 = 64$

$100 \times (3/5)^2 = 36$

$100 \times (2/5)^2 = 16$

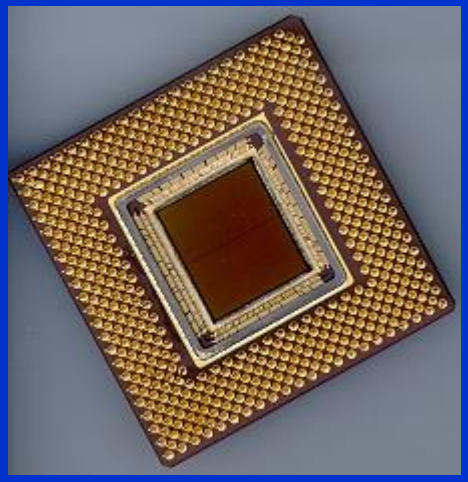
$100 \times (1/5)^2 = 4$

Current Spikes and Decoupling

- **When a CMOS gate output changes state, the P- and N-channel transistors are both partially on simultaneously, causing a *current spike***
- **Current spikes often show up as *noise* on the power supply and ground connections**
- ***Decoupling capacitors* (between Vcc and GND) must be distributed throughout a printed circuit board (PCB) to serve as a source of instantaneous current during output transitions – *this helps mitigate noise and improve signal quality***

Decoupling Capacitors

- **Decoupling capacitors should be located as *physically close* as possible to each IC**
- **Use 0.1 μF decoupling capacitors for system frequencies up to 15 MHz**
- **Above 15 MHz, use 0.01 μF decoupling capacitors**



ECE 477 Digital Systems Senior Design Project

Module 2-E

Three-State and Open-Drain Outputs

Reading Assignment:

DDPP 4th Ed., pp. 132-136, 138-141

Learning Objectives:

- **Define high-impedance state and describe the operation of a tri-state buffer**
- **Define open drain as it applies to a CMOS logic gate output and calculate the value of pull-up resistor needed**
- **Describe how to create "wired logic" functions using open drain logic gates**
- **Calculate the value of pull-up resistor needed for an open drain logic gate**

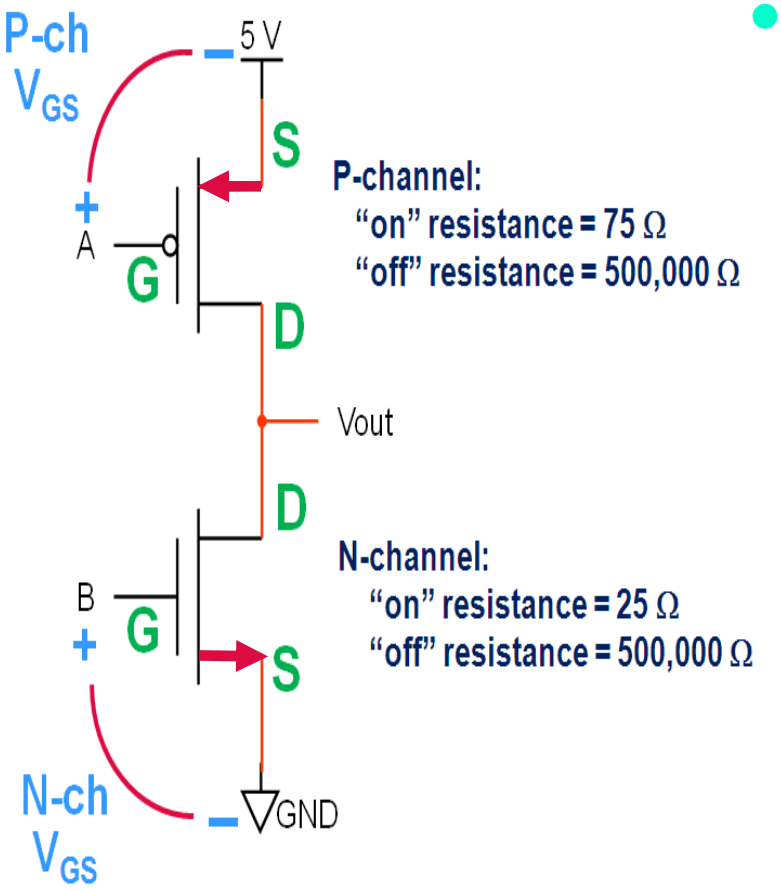
Outline

- Three-state (tri-state) outputs
- CMOS tri-state buffer circuit
- Tri-state buffer application – buses
- Tri-state buffer float delay
- Open drain outputs
- Driving LEDs
- Wired logic
- Pull-up resistor calculations

Three-State (Tri-State) Outputs

- **Definition: A gate output that has a third "electrical state" is called a *three-state output* (or *tri-state output*)**
- **This third electrical state is called the *high impedance*, *Hi-Z*, or *floating* state**
- **In the high impedance state, the gate output effectively appears to be *disconnected* from the rest of the circuit**
- **Three-state devices have an extra input, typically called the *Output Enable* (OE), for enabling data to "flow through" the device (when asserted) or placing the output in the high impedance state (when negated)**

Basic CMOS Logic Circuit Revisited



- **Calculate V_{out} for the case A=5V, B=0**

P-ch device is "off" (R_{DS} = 500,000 Ω)

N-ch device is "off" (R_{DS} = 500,000 Ω)

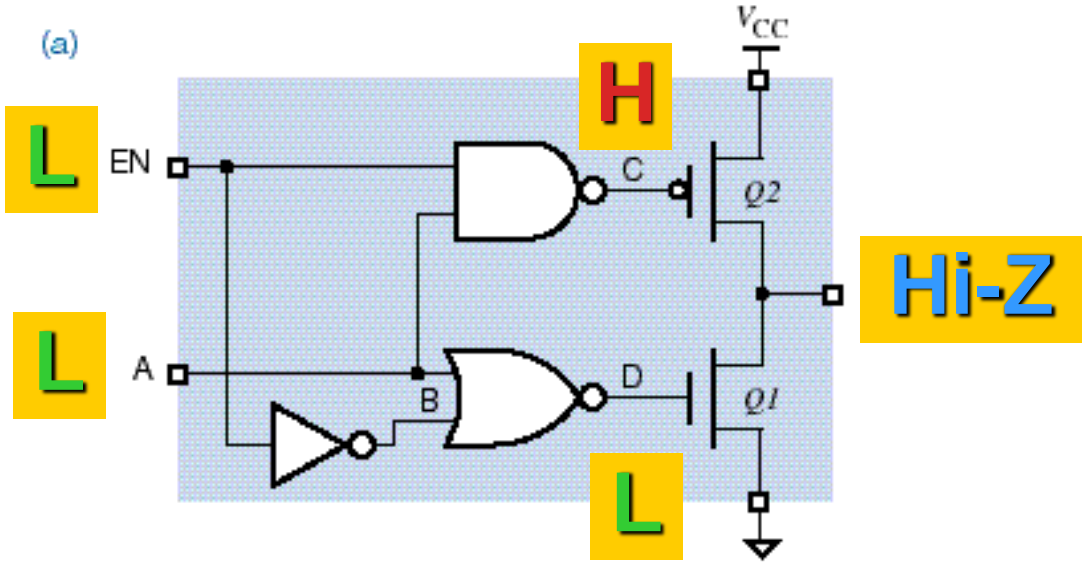
V_{out} = 5 x (500,000 / 1,000,000) = 2.5 V

$P_{dissipation}$ = 5^2 / 1,000,000 = 0.025 mW

Here, Vout is effectively disconnected (in the "Hi-Z state") when A is high and B is low

Use OE (output enable) signal to force A high and B low when OE is negated

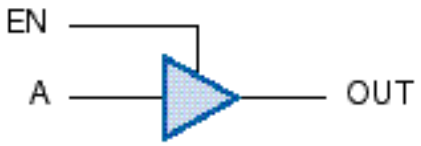
CMOS Tri-State Buffer Circuit

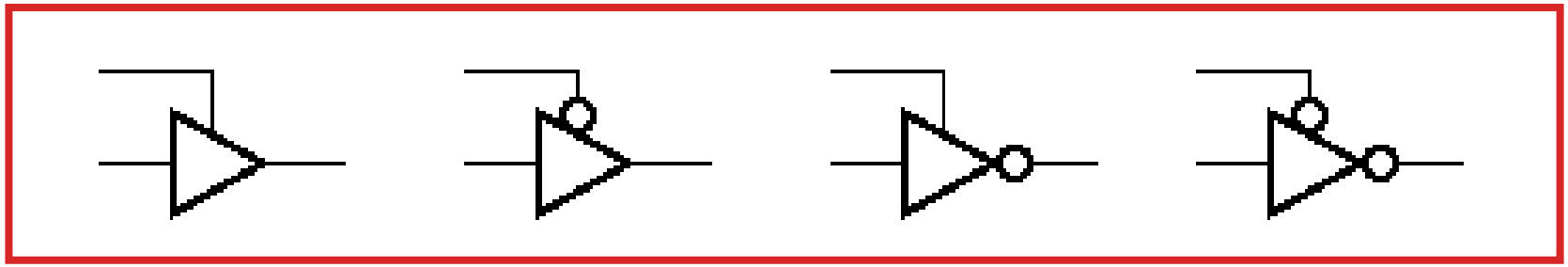


(b)

EN	A	B	C	D	Q1	Q2	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H

(c)

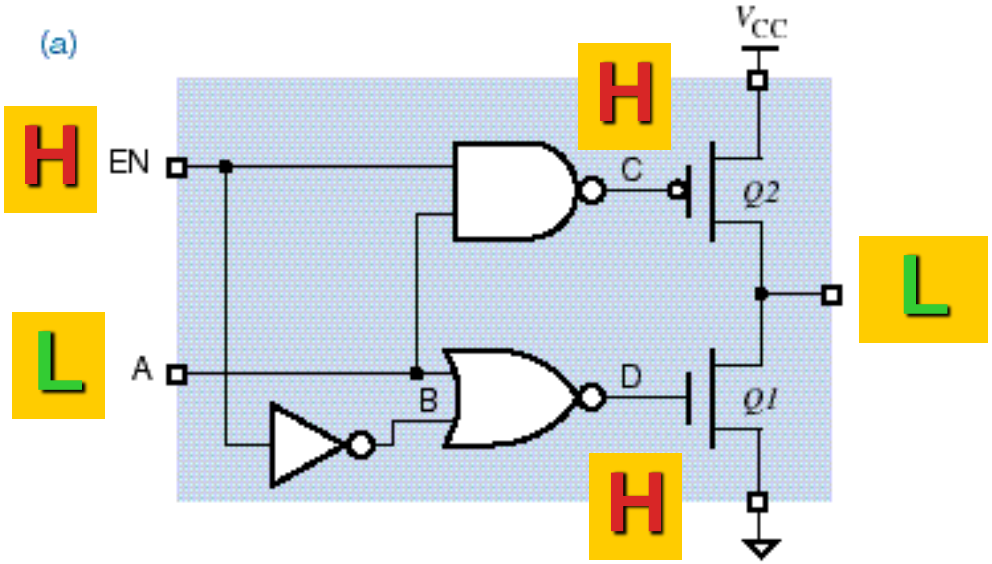




<u>Basic variations</u>: The buffer may be inverting or non-inverting, and the tri-state enable can either be active low or active high

CMOS Tri-State Buffer Circuit

(a)



(b)

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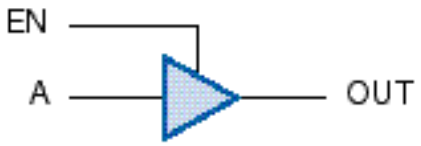
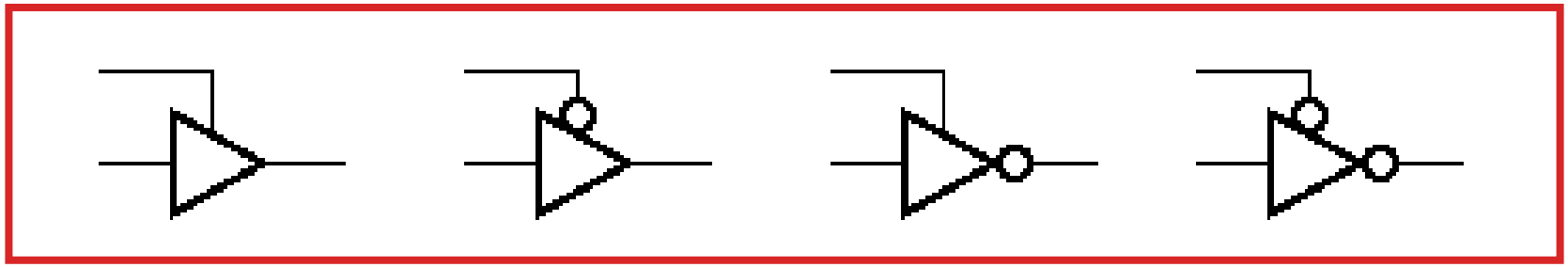
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H

(c)





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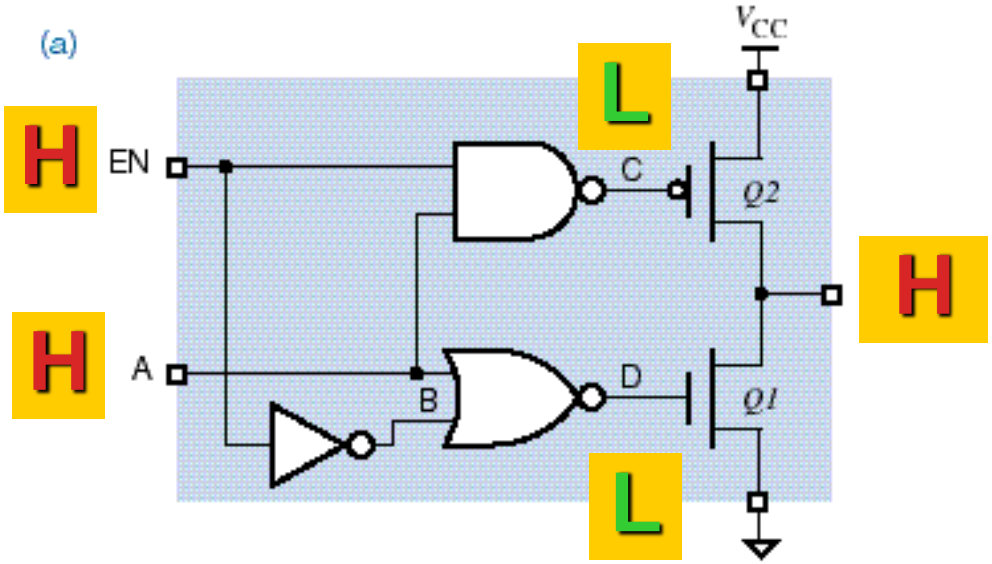

(b)

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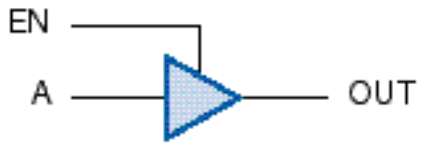
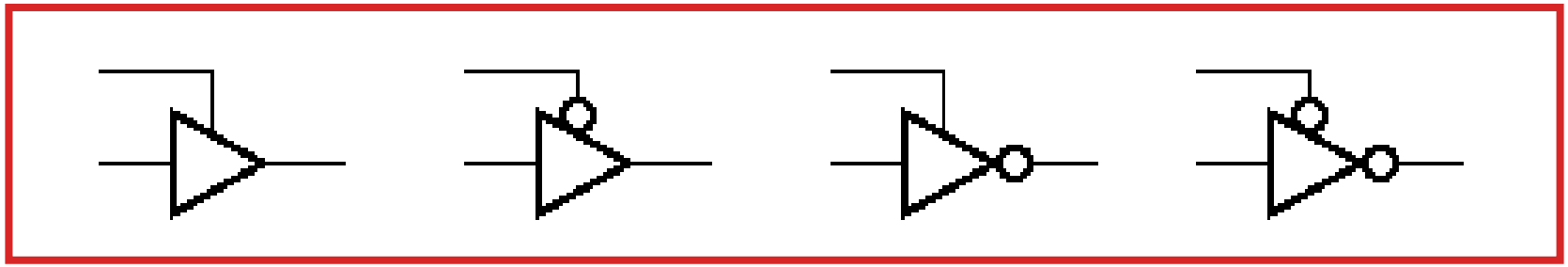
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H

(c)





<u>Basic variations</u>: The buffer may be inverting or non-inverting, and the tri-state enable can either be active low or active high

Tri-State Buffer Application – Buses

- **The most common use of tri-state buffers is to create *data buses* over which digital subsystems can (bi-directionally) send and receive data**
- **Definition: A *bus* is a collection of signals with a "common purpose" (e.g., sending the address of an item in memory, sending the data to be written to memory, etc.)**
- **A *bus transceiver* contains pairs of tri-state buffers connected in opposite directions between each pair of pins, so that data can be transferred in *either direction***

Tri-State Buffer Float Delay

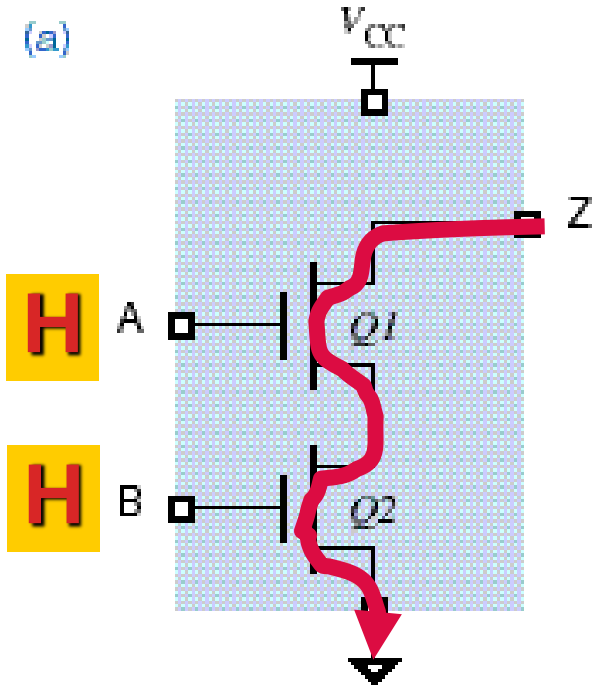
- Tri-state outputs are typically designed so that they ***go into*** the Hi-Z (high impedance) state faster than they ***come out of*** the Hi-Z state (i.e., t_{pLZ} and t_{pHZ} are both less than t_{pZL} and t_{pZH})
- The time it takes to go from a "driven" state (valid logic level) to the Hi-Z "floating" state is called the ***float delay***
- Given this "rule", if one tri-state device is disabled and another tri-state device is enabled simultaneously, then the first device will get ***off*** the bus before the second one gets ***on*** – this helps prevent ***fighting***

Open-Drain Outputs

- **Definition: A CMOS output structure that does not include a P-channel (pull-up) transistor is called an *open-drain output***
- **An open-drain output is in one of two states: LOW or "open" (i.e., disconnected)**
- **An *underscored diamond* (or "O.D.") is used to indicate that an output is open drain**
- **An open-drain output requires an external pull-up resistor to *passively* pull it high in the "open" state (since the output structure does NOT include a P-channel active pull-up)**

Open-Drain CMOS NAND Gate

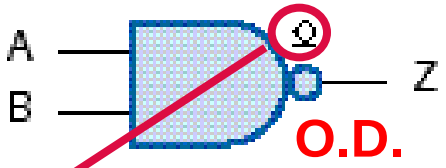
(a)



(b)

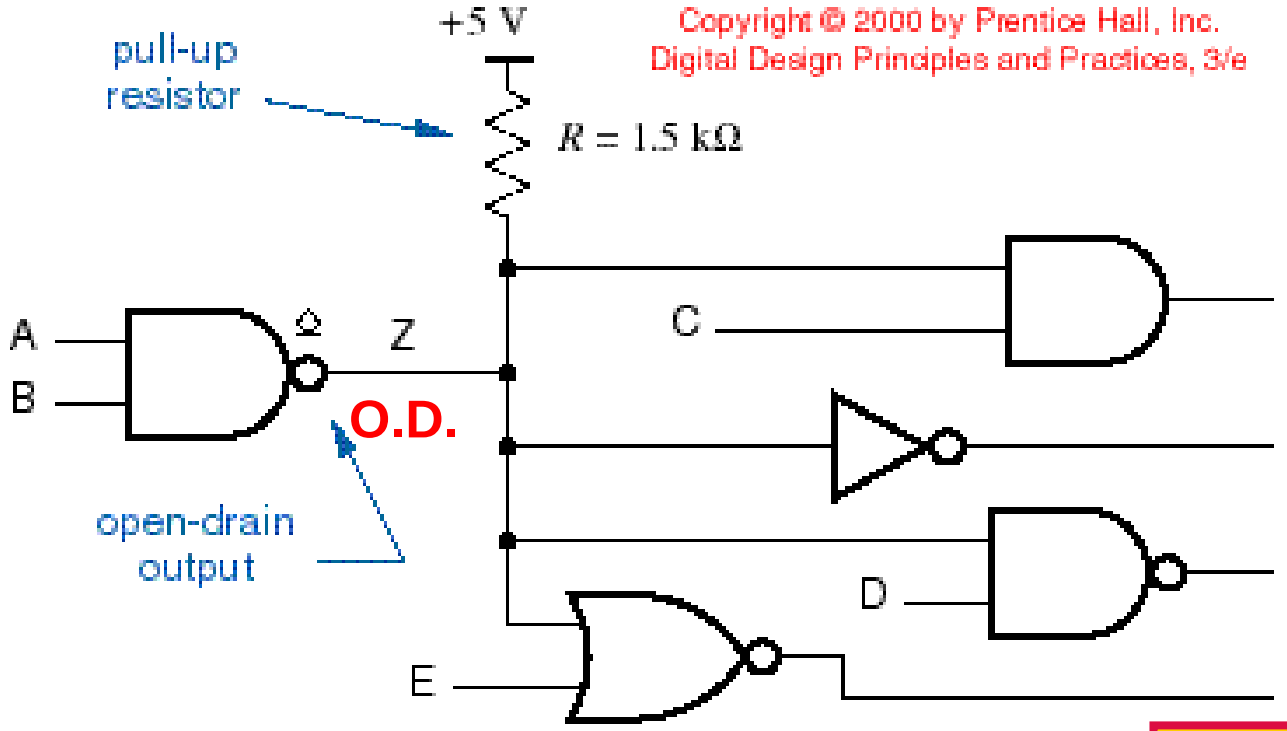
A	B	Q1	Q2	Z
L	L	off	off	open
L	H	off	on	open
H	L	on	off	open
H	H	on	on	L

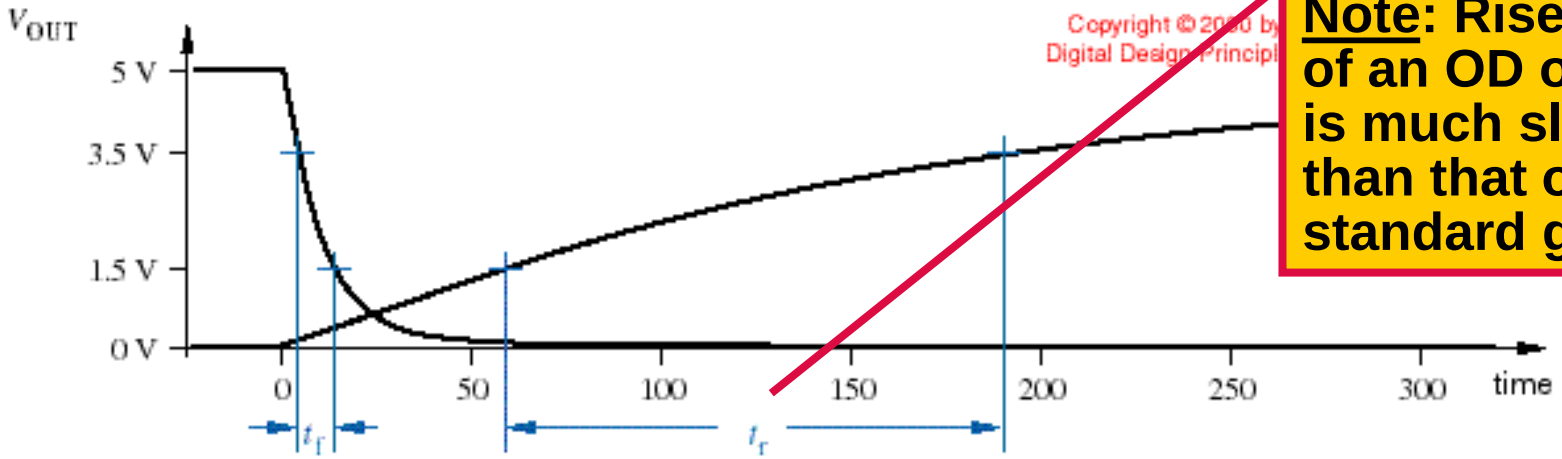
(c)



Symbol that denotes an open-drain output

Open-Drain Gate Driving a Load

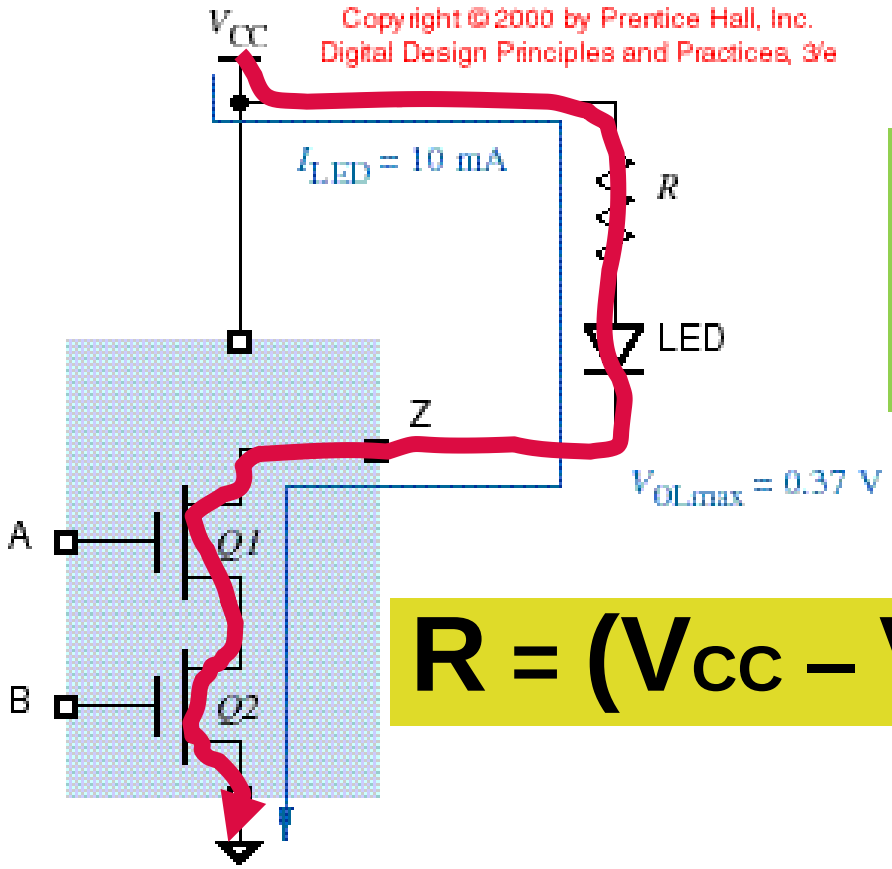




Note: Rise time of an OD output is much slower than that of a standard gate

Driving LEDs

- **One application for open-drain outputs is driving light-emitting diodes (LEDs)**

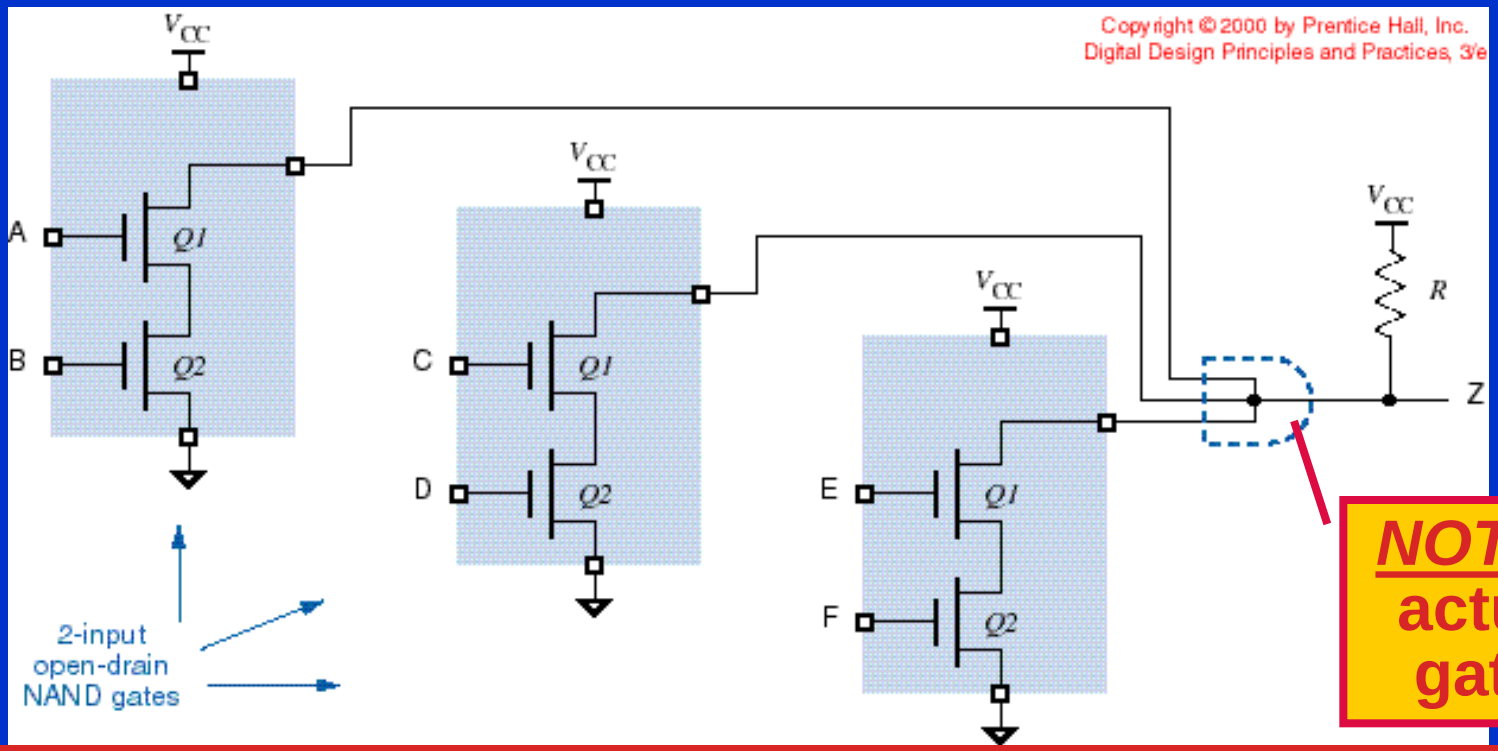


O.D. outputs can typically sink more current than conventional gates

$$R = (V_{CC} - V_{OL} - V_{LED}) / I_{LED}$$

Wired Logic

- **Definition**: ***Wired logic*** **is performed if the outputs of several open-drain gates are tied together with a single pull-up resistor**

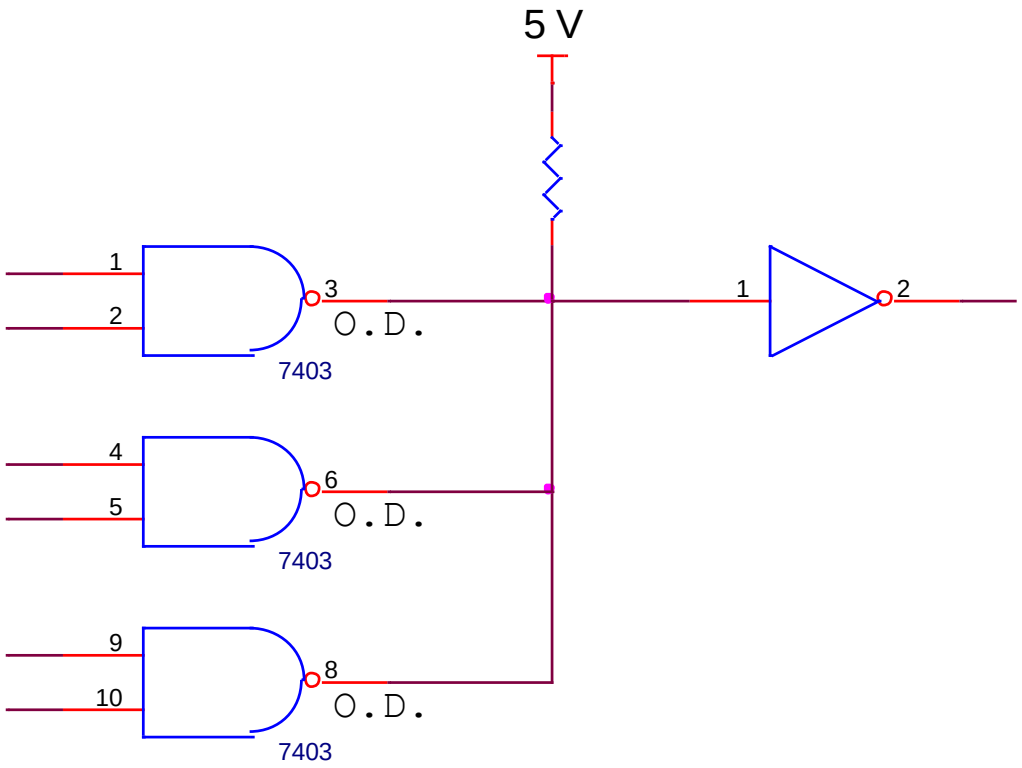


Caution: This ONLY works for open-drain outputs!

Pull-up Resistor Calculations

- In open-drain applications, two calculations bracket the allowable values of the pull-up resistor R:
  - **LOW** The sum of the current through R plus the LOW state input currents of the gate inputs driven ***must not exceed*** the $I_{OL_{max}}$ of the active device
  - **HIGH** The voltage drop across R in the HIGH state ***must not reduce*** the output voltage below the $V_{IH_{min}}$ of the driven gate inputs

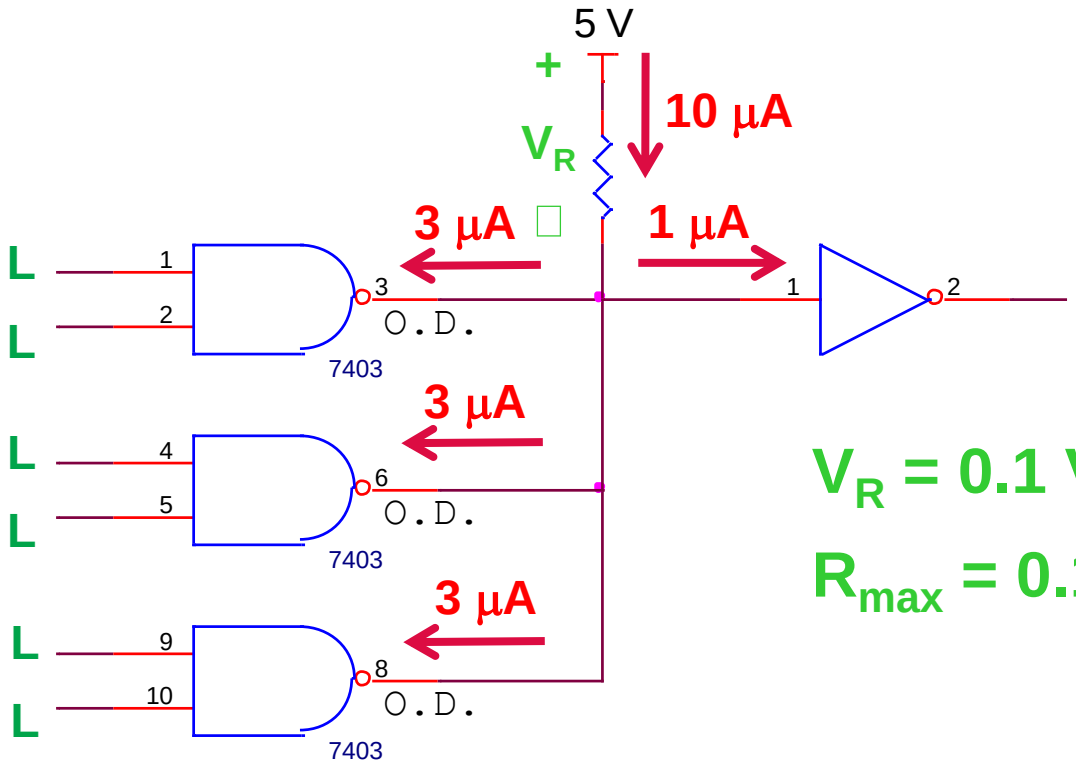
Example - Calculate a suitable value of pull-up resistor to use with the following circuit:



Specifications (hypothetical data):

- Off-state leakage current of O.D. NAND gate output: +3 μA
- I_{IH} and I_{IL} required by inverter input: ±1 μA
- V_{IH} desired for inverter input: 4.9 V
- $I_{OL\ max}$ of O.D. NAND gate output: +10 mA @ V_{OL} = 0.3 V

Solution, maximum R Value – based on V_{IH} desired



V_R = 0.1 V I_R = 10 μA

R_{max} = 0.1/0.00001 = 10,000 Ω

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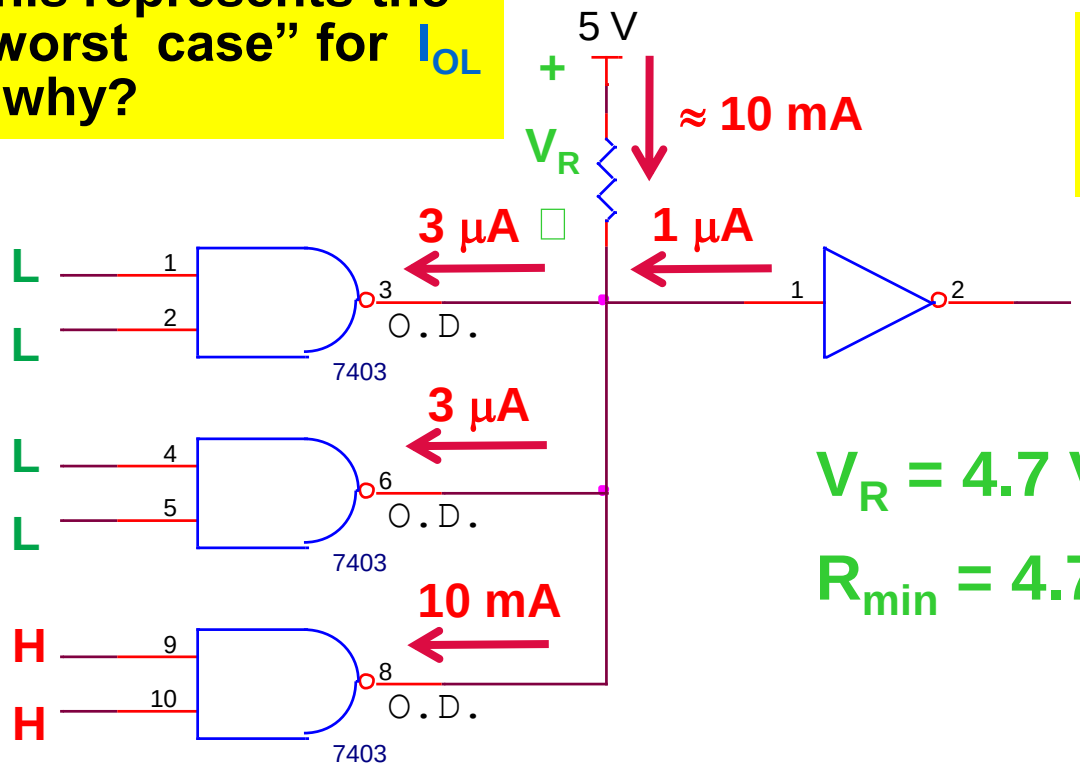
Solution, minimum R Value – based on $I_{OL\ max}$ of one gate

This represents the "worst case" for I_{OL} – why?



Here, can safely ignore leakage and I_{IL} currents – why?

$V_R = 4.7\ V \quad I_R \approx 10\ mA$

$R_{min} = 4.7/0.01 = 470\ \Omega$

Specifications (hypothetical data):

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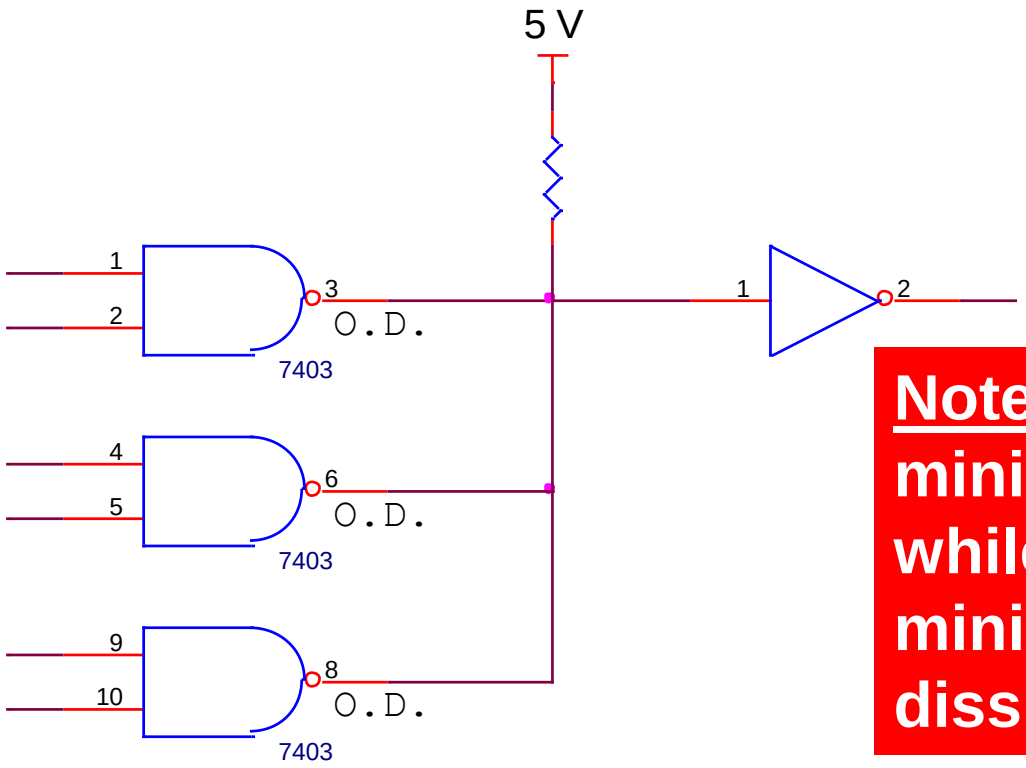
Conclusion – a pull-up resistor ranging from 470 Ω (R_{min}) to 10,000 Ω (R_{max}) will satisfy the specified constraints



Note: Picking R_{min} will minimize the rise time, while picking R_{max} will minimize the power dissipation

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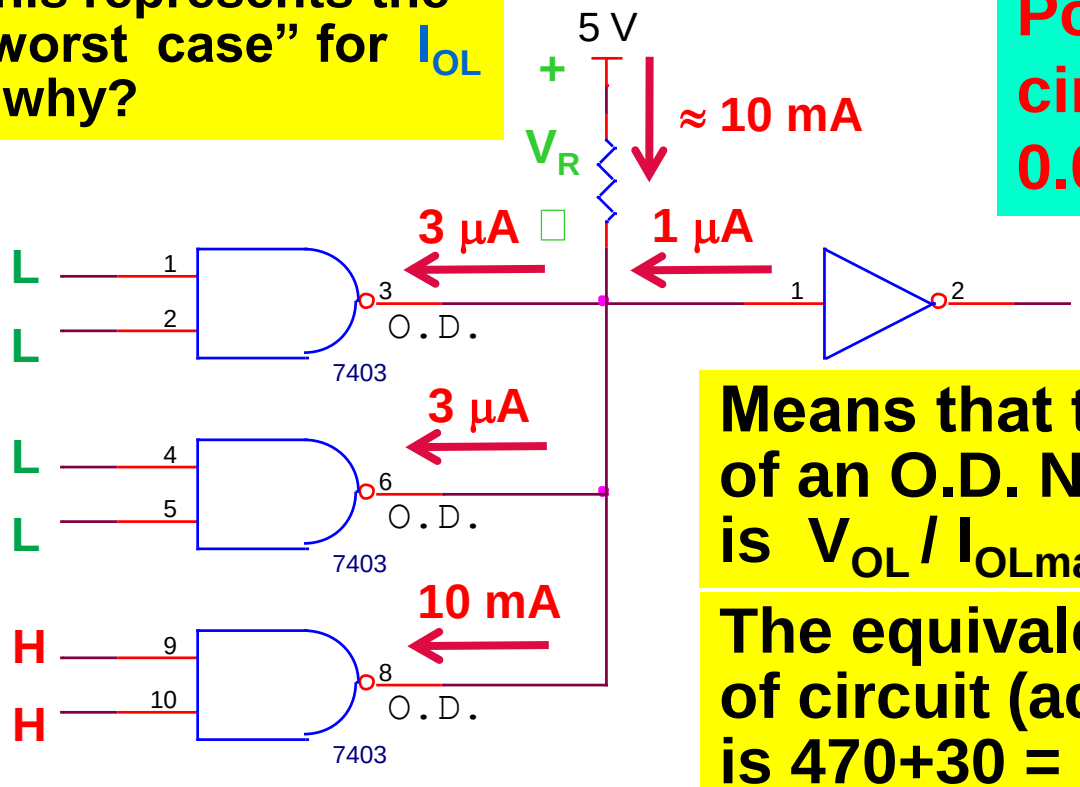
Follow-up – "prove" the "worst case" scenario (R = 470 Ω)

This represents the "worst case" for I_{OL} – why?



Power dissipation of circuit is $I_R^2 \times R_{eq}$ = $0.01^2 \times 500 \approx 50$ mW

Means that the "on" resistance of an O.D. NAND gate used here is V_{OL} / I_{OLmax} = 0.3/0.01 = 30 Ω

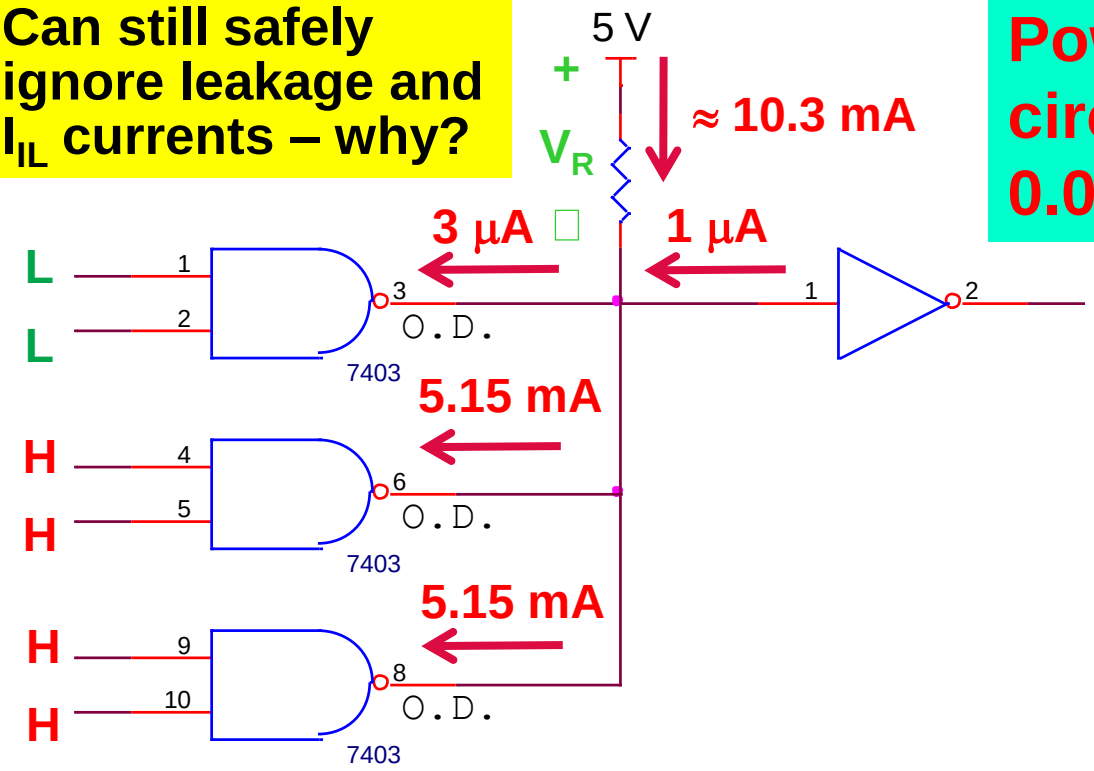
The equivalent load impedance of circuit (across power supply) is 470+30 = 500 Ω

Specifications (hypothetical data):

- Off-state leakage current of O.D. NAND gate output: +3 μA
- I_{IH} and I_{IL} required by inverter input: ±1 μA
- V_{IH} desired for inverter input: 4.9 V
- **$I_{OL\ max}$ of O.D. NAND gate output: +10 mA @ V_{OL} = 0.3 V**

Follow-up – "prove" the "worst case" scenario (R = 470 Ω)

Can still safely ignore leakage and I_{IL} currents – why?



Power dissipation of circuit is I_R^2 x R_{eq} = 0.0103^2 x 485 ≈ 51.5 mW

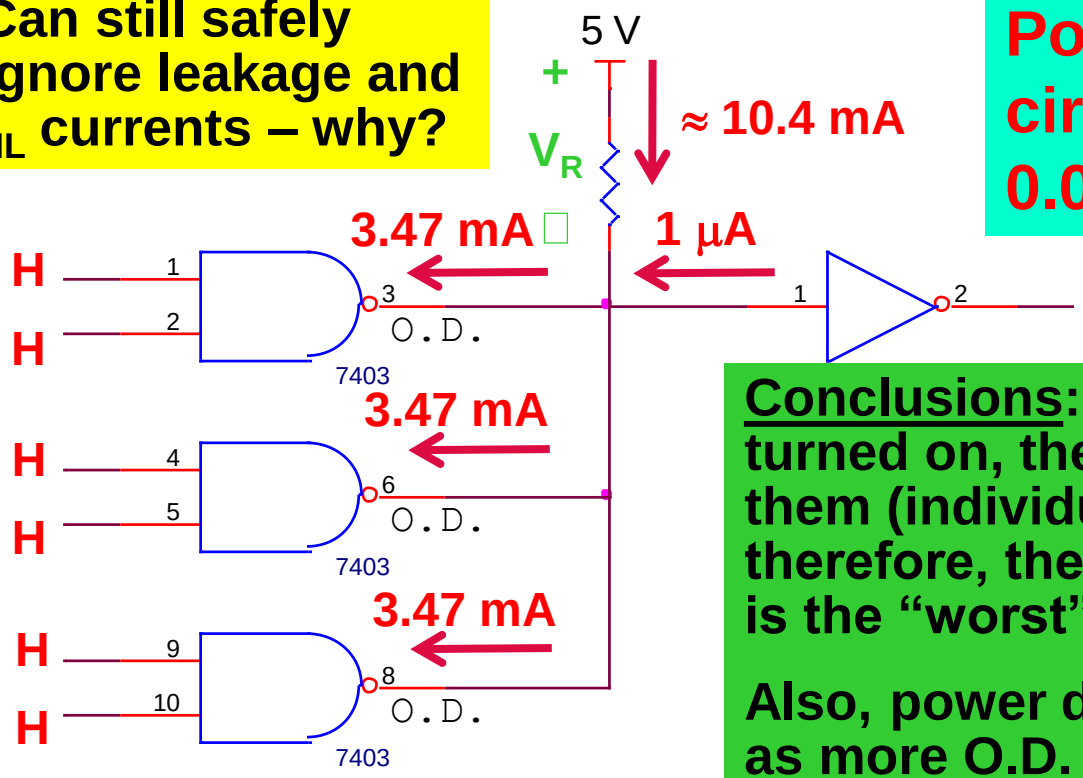
Next, turn on <u>two</u> O.D. gates

The equivalent load impedance of circuit is 470+15 = 485 Ω (because have two 30 Ω "on" resistances in parallel)

I_R is now 5 / 485 = 0.0103 A = 10.3 mA, which is <u>split</u> between the two gates that are "on"

Follow-up – "prove" the "worst case" scenario (R = 470 Ω)

Can still safely ignore leakage and I_{IL} currents – why?



Power dissipation of circuit is I_R^2 x R_{eq} = 0.0104^2 x 480 ≈ 52 mW

Conclusions: As more O.D. gates are turned on, the amount of current each of them (individually) has to sink is reduced; therefore, the first case (single gate "on") is the "worst" one with respect to I_{OL}.

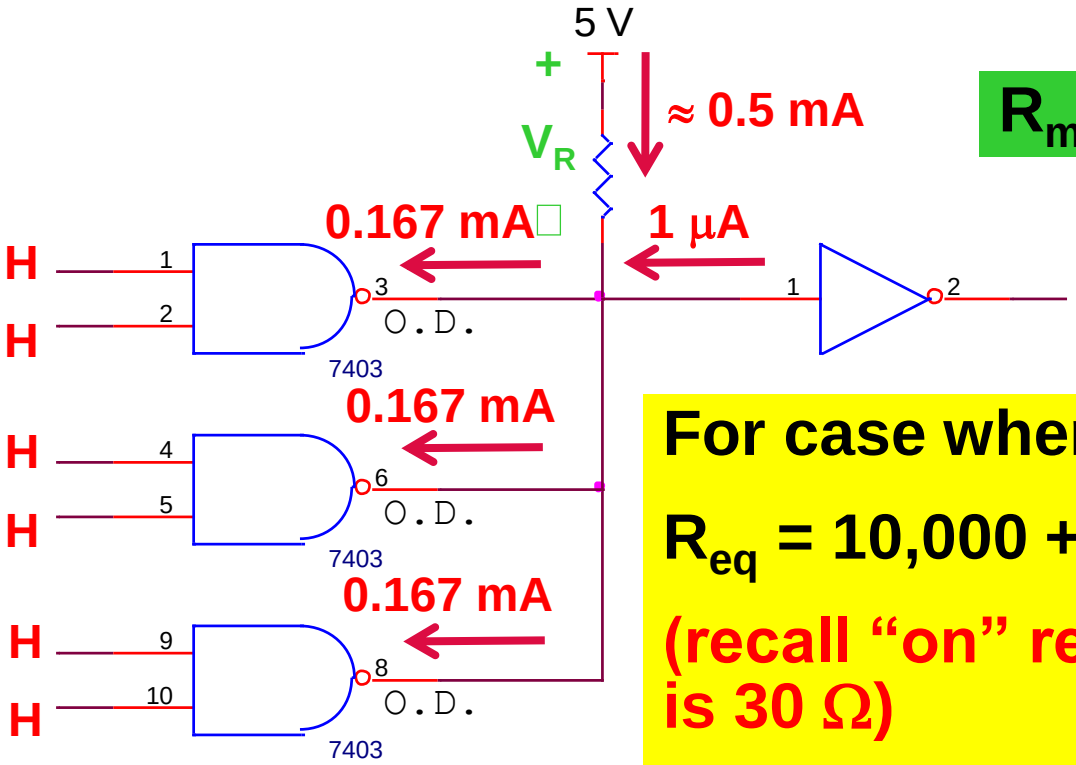
Also, power dissipation increases slightly as more O.D. gates are turned on.

Finally, turn on all three O.D. gates

The equivalent load impedance of circuit is 470+10 = 480 Ω (because have three 30 Ω "on" resistances in parallel)

I_R is now 5 / 480 = 0.0104 A = 10.4 mA, which is split among the three gates that are "on"

Follow-up – compare power dissipation of circuit using R_{min} vs. R_{max} as the pull-up resistor



R_{max} (10,000 Ω)

For case where all gates are <u>on</u>:

R_{eq} = 10,000 + 10 = 10,010 Ω

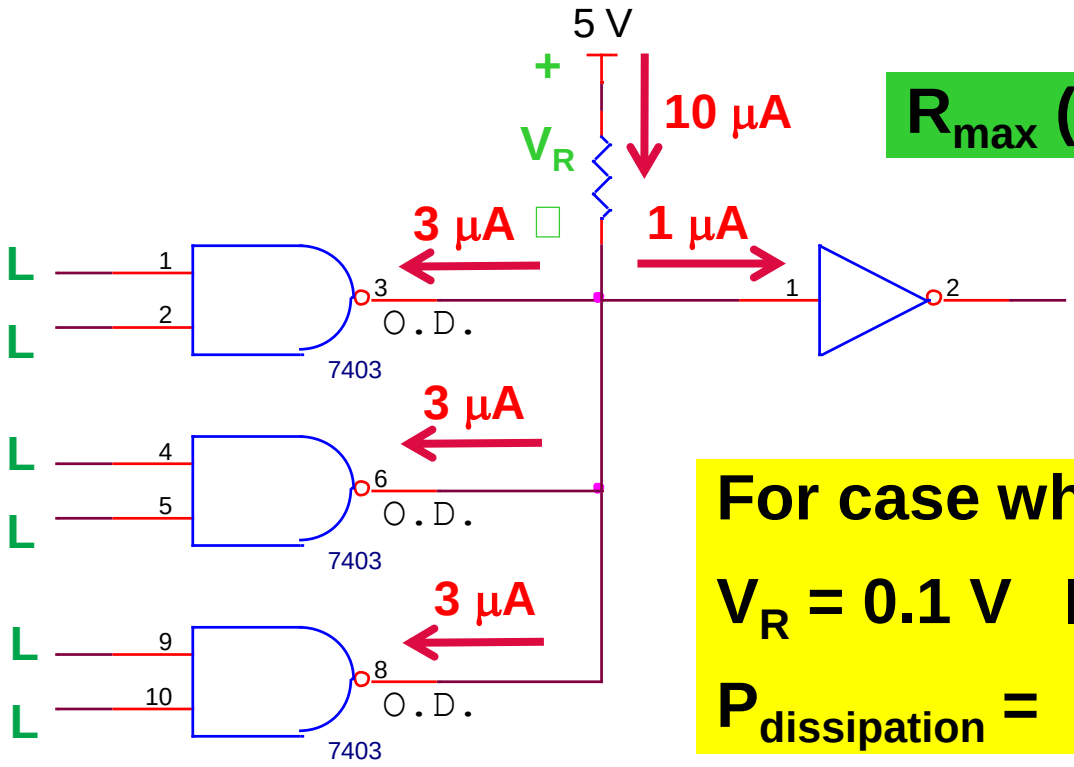
(recall "on" resistance of each gate is 30 Ω)

$I_R \approx 5 / 10{,}010 \approx 0.5$ mA (note - split among three gate outputs)

$P_{dissipation} = I_R^2 \times R_{eq} \approx 2.5$ mW

<u>Note</u>: V_{IL} of inverter is nearly 0 V

Follow-up – compare power dissipation of circuit using R_{min} vs. R_{max} as the pull-up resistor



R_{max} (10,000 Ω)

For case where all gates are <u>off</u>:

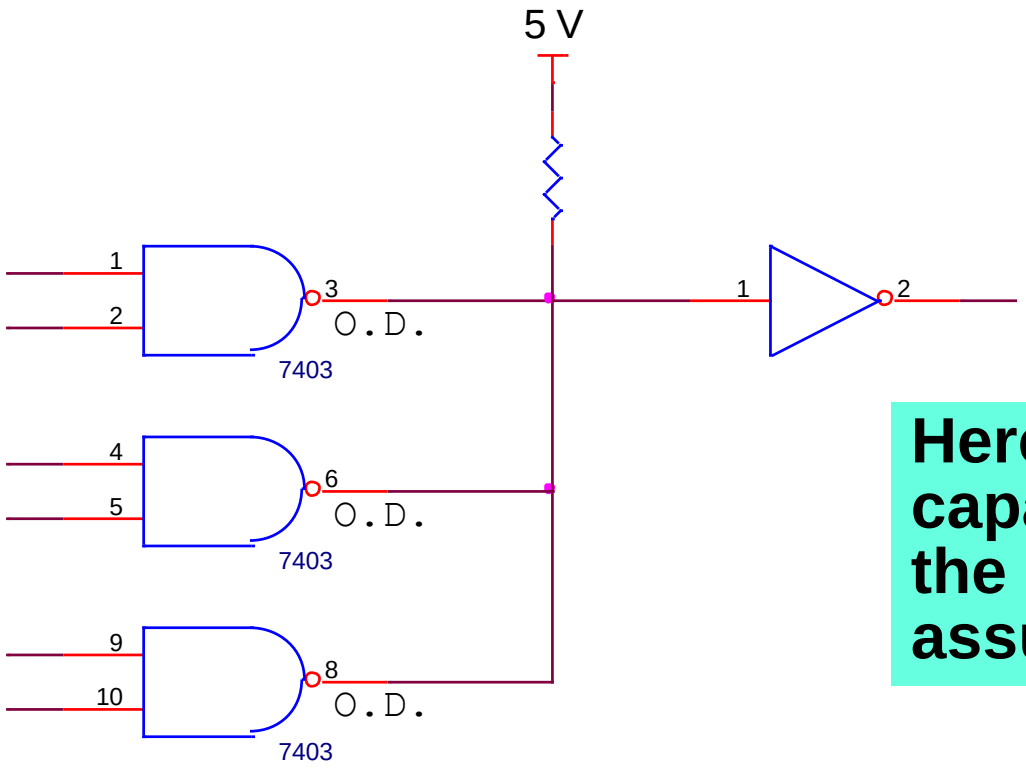
V_R = 0.1 V I_R = 10 μA

$P_{dissipation}$ = I_R^2 x R = 1 μW

<u>Note</u>: V_{IH} of inverter is 4.9 V

<u>Conclusion</u>: Power dissipation when R_{max} is used does not exceed 2.5 mW (vs. 52 mW for R_{min}); therefore, use of R_{max} minimizes the power dissipation

Follow-up – compare rise time estimates of circuit using R_{min} vs. R_{max} as the pull-up resistor

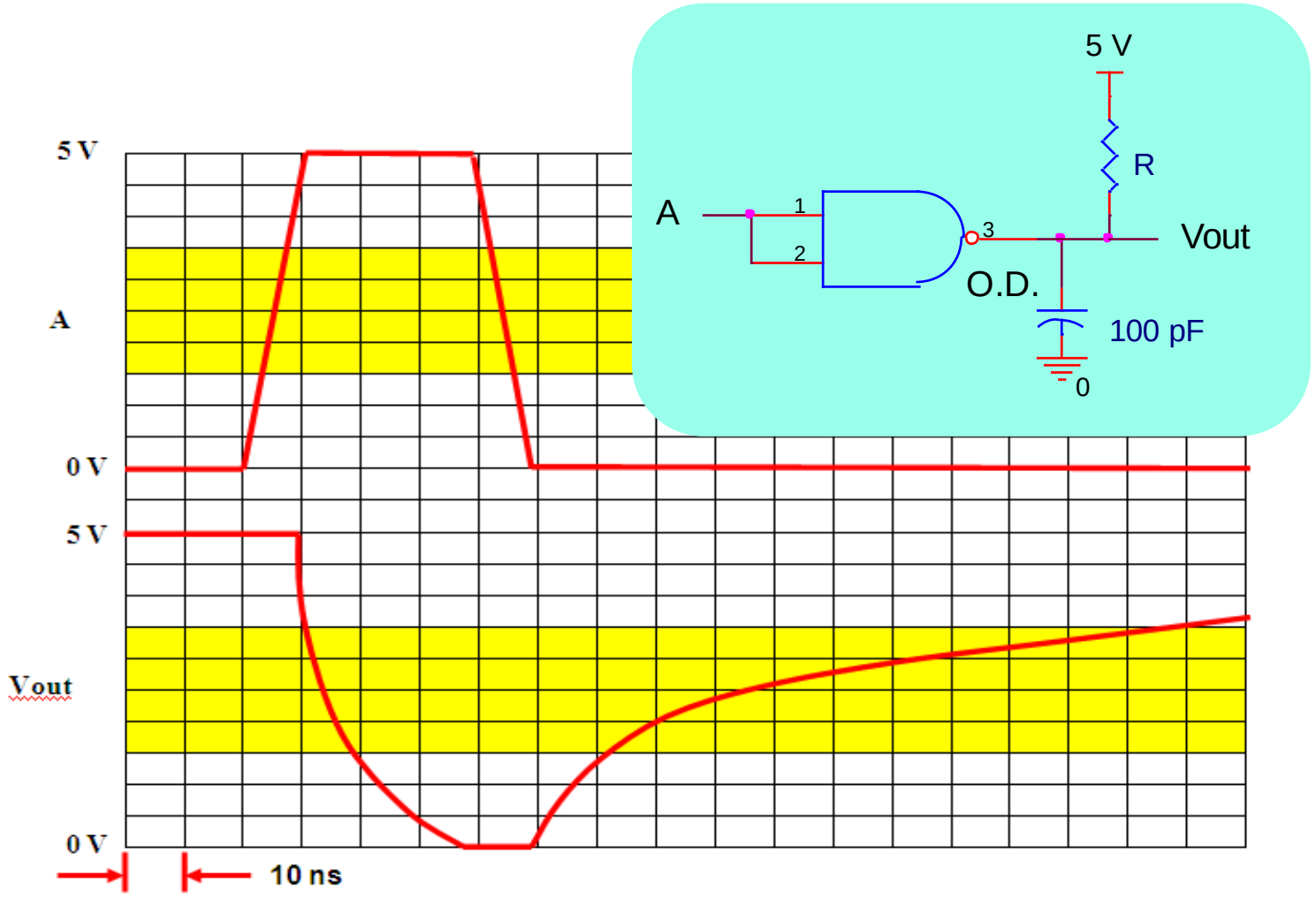


Here, need to know the capacitive load (C_L); for the sake of analysis, assume it is 100 pF

Comparison:

- **For $R_{min,}$ rise time estimate is 470 x 100 x 10^{-12} = 47 ns**
- **For $R_{max,}$ rise time estimate is 10,000 x 100 x 10^{-12} = 1000 ns**
- **Conclusion: rise time for R_{max} case is <u>considerably longer</u>**

Example – Estimate the "on" resistance of an O.D. gate and pull-up resistor value based on rise/fall times



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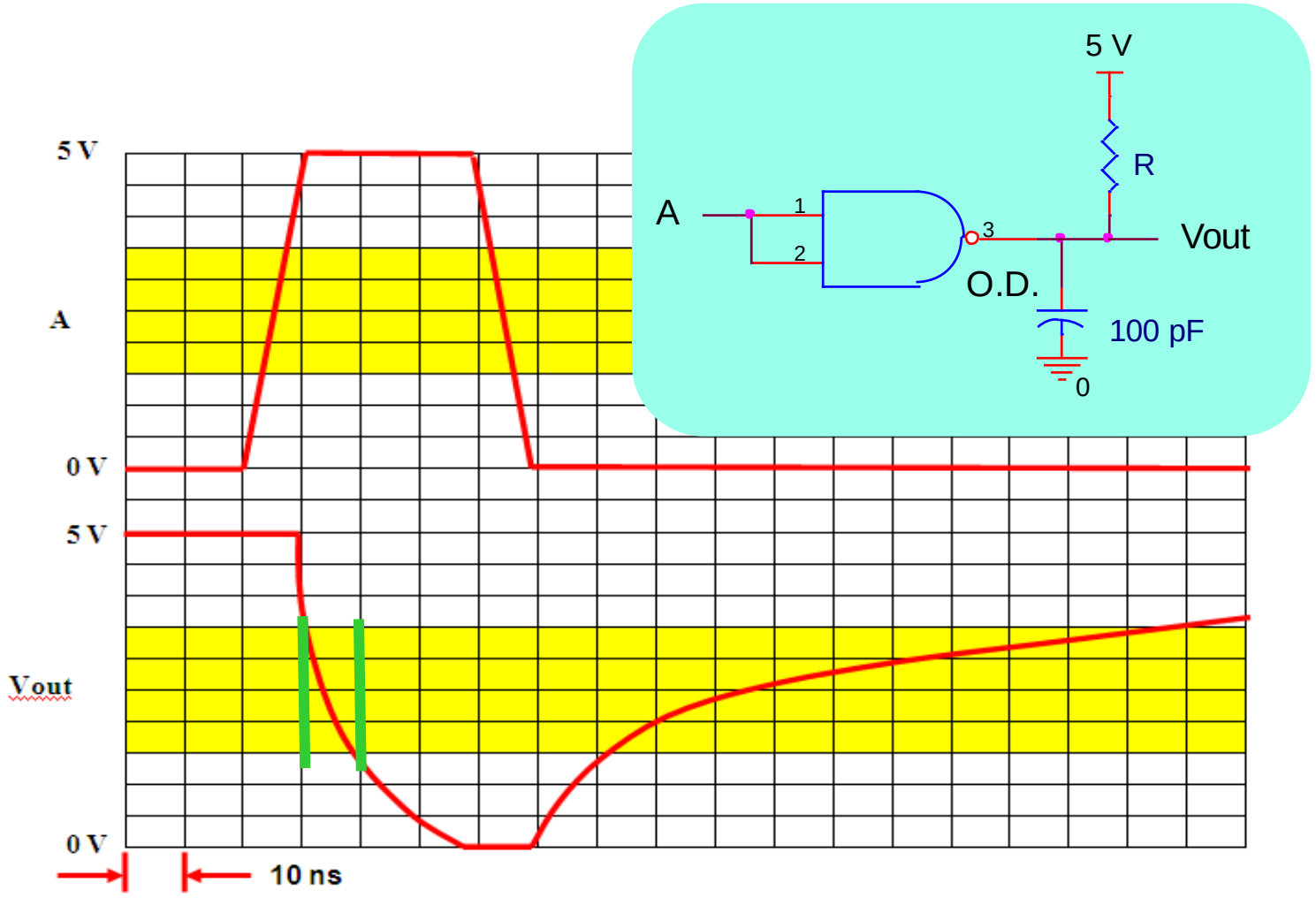
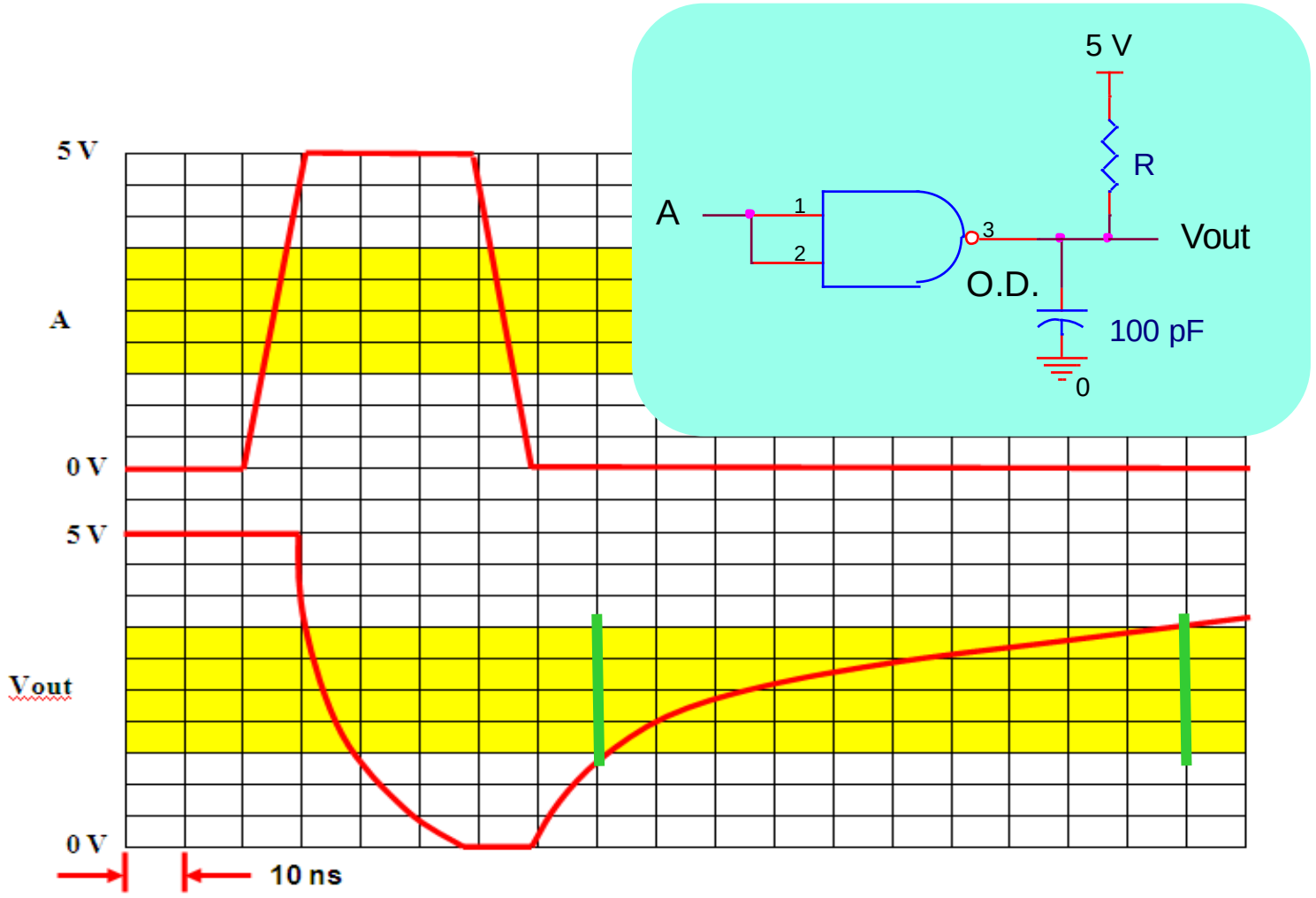


fall time = 10 ns = R_{on} x 100 pF $\rightarrow$ R_{on} = 100Ω

Example – Estimate the "on" resistance of an O.D. gate and pull-up resistor value based on rise/fall times



rise time = 100 ns = $R_{pull\text{-}up}$ x 100 pF → $R_{pull\text{-}up}$ = 1000 Ω